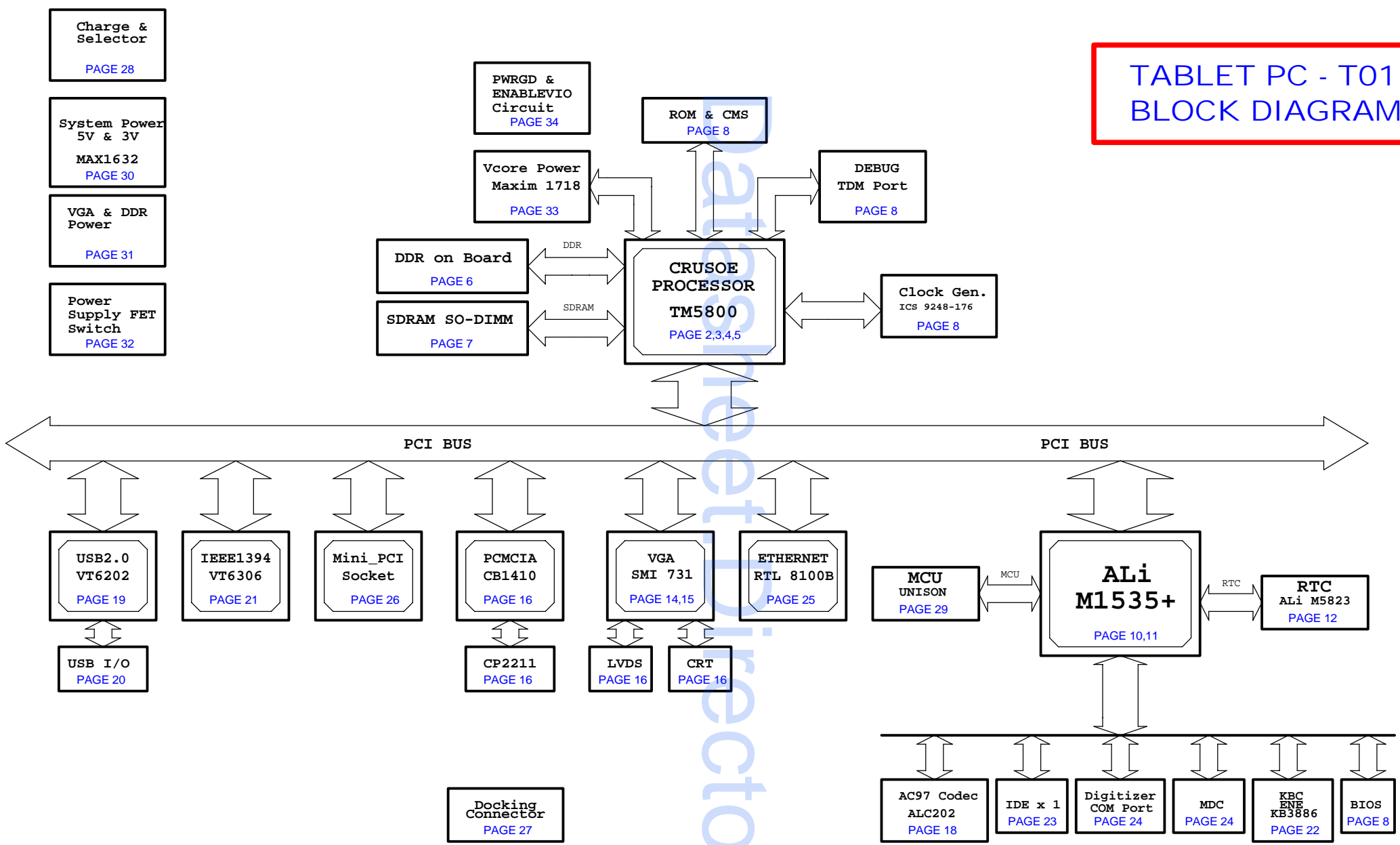
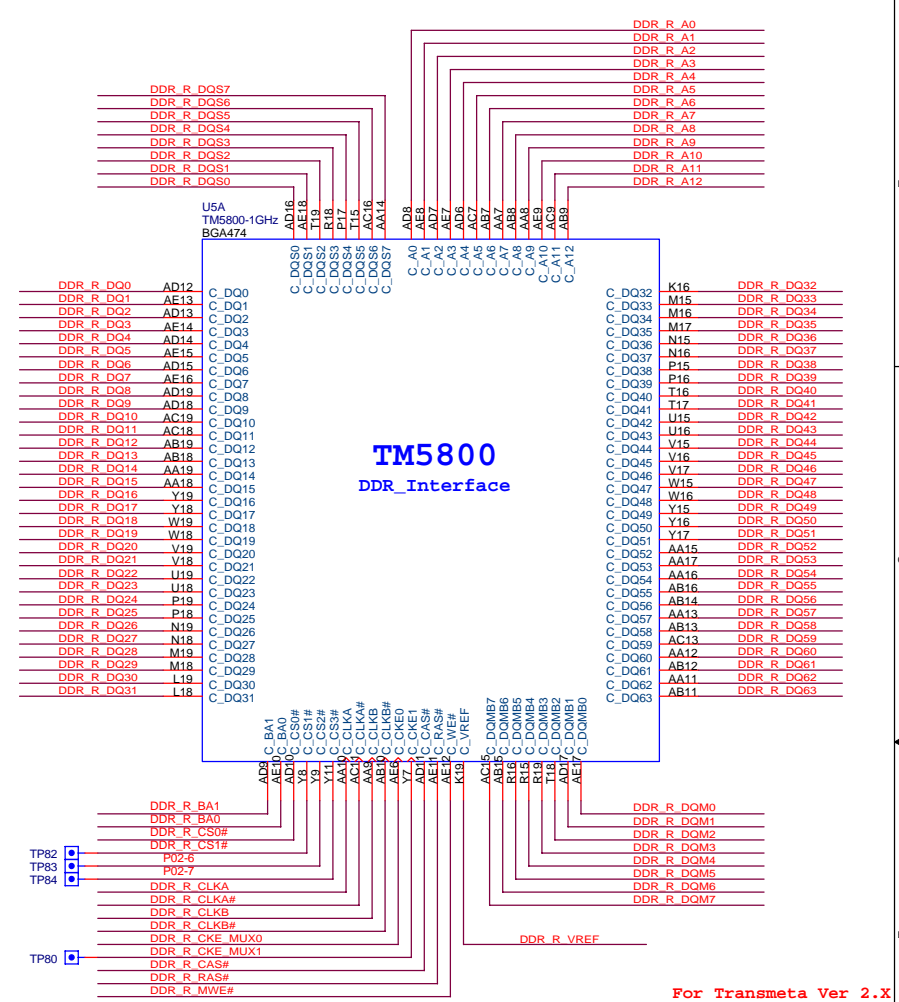
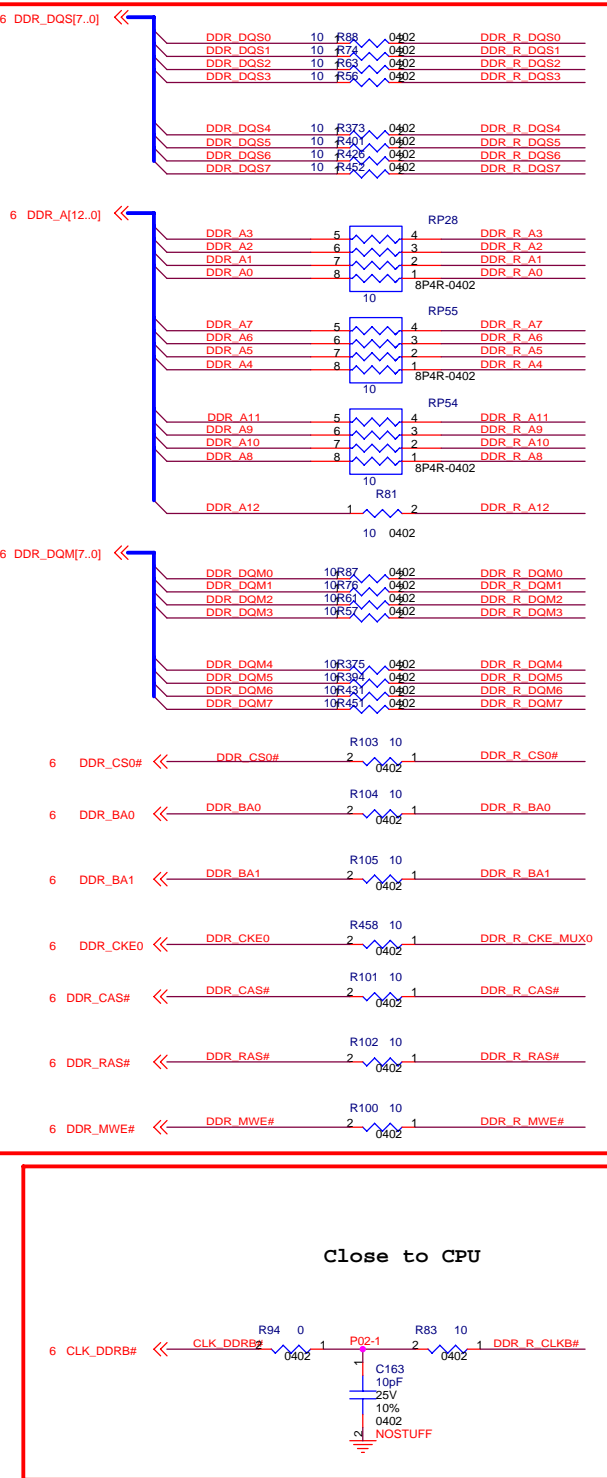
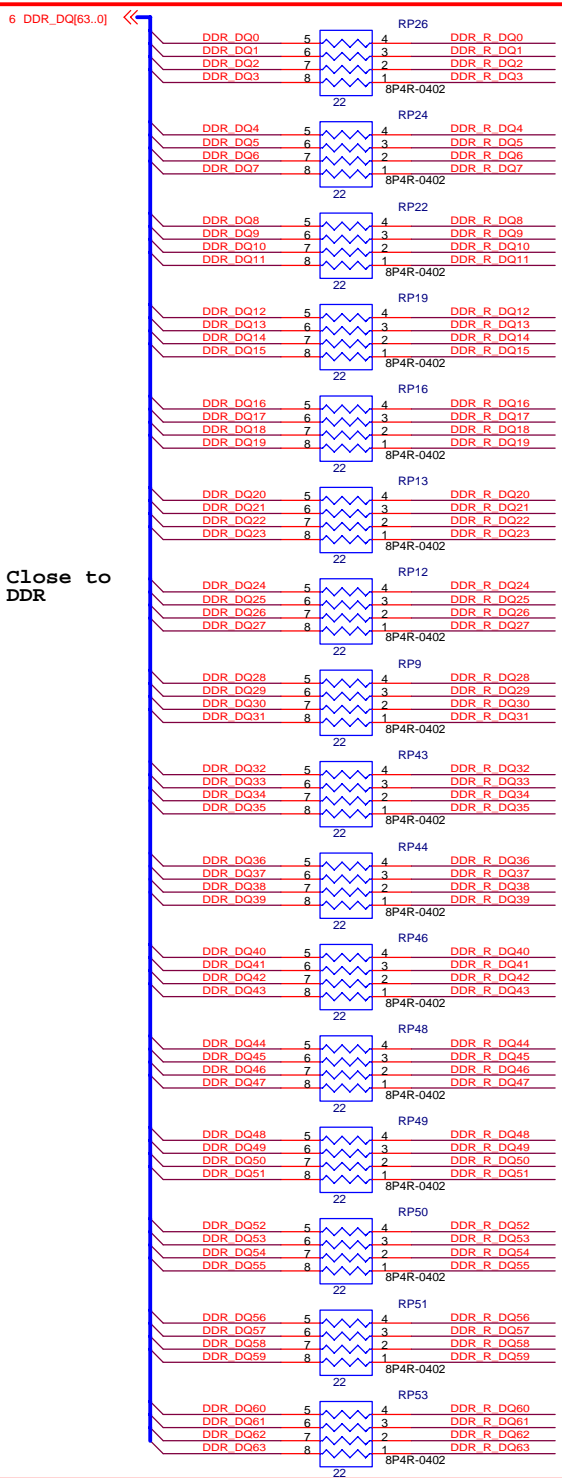


# TABLET PC - T01 BLOCK DIAGRAM

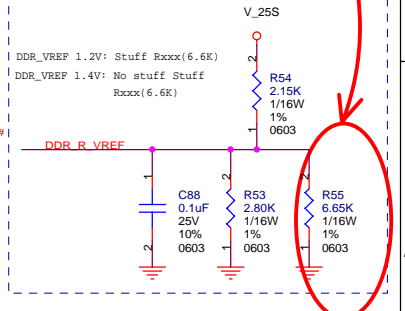




Close to DDR

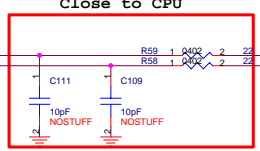
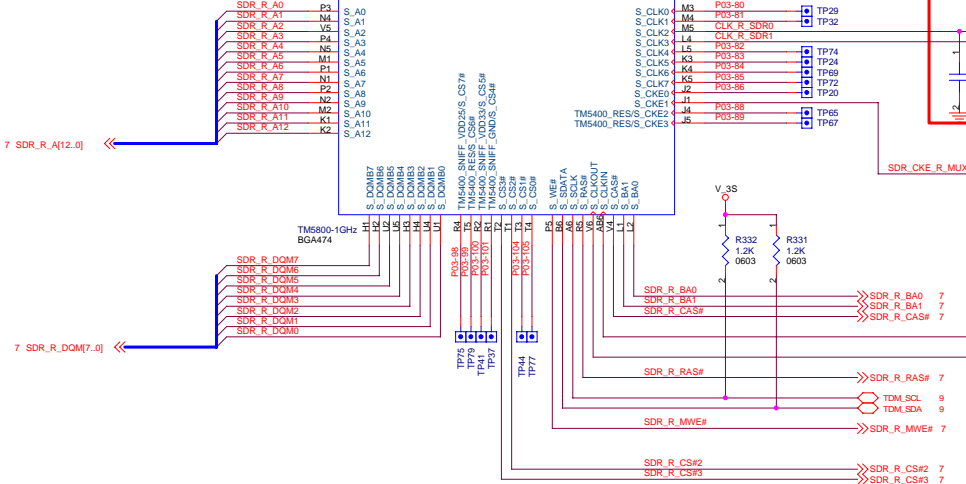
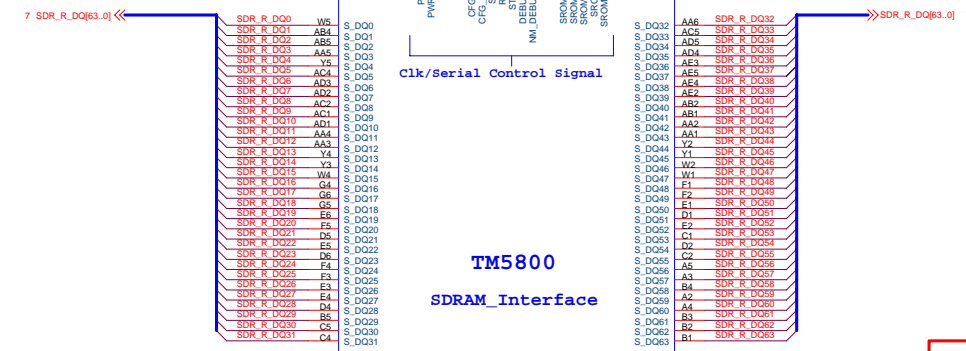
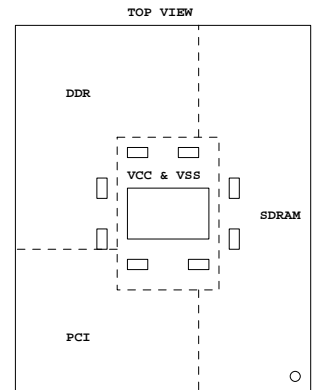
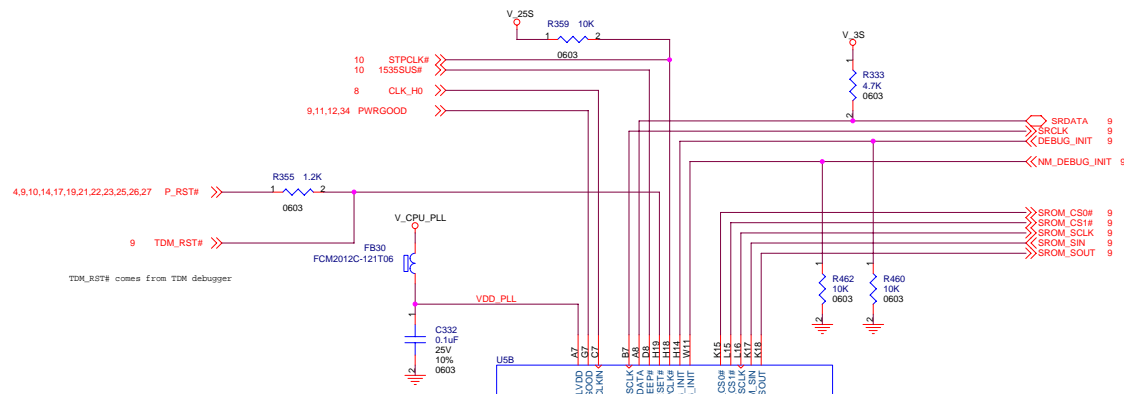
Close to CPU

Close to Transmeta

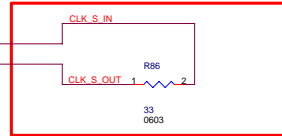


For Transmeta Ver 2.X

<b>AMTEK SYSTEM CO.,LTD</b>			
Title TRANSMETA DDR INTERFACE			
Size B	Document Number TBD	Rev 2.0	
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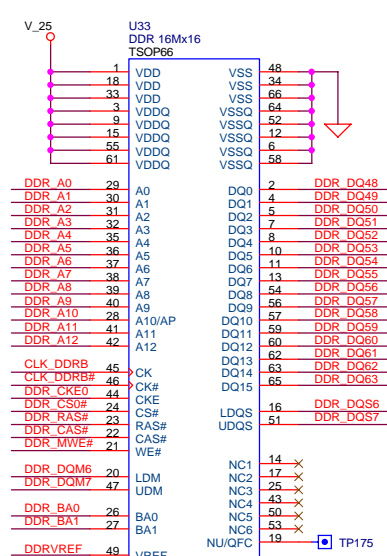
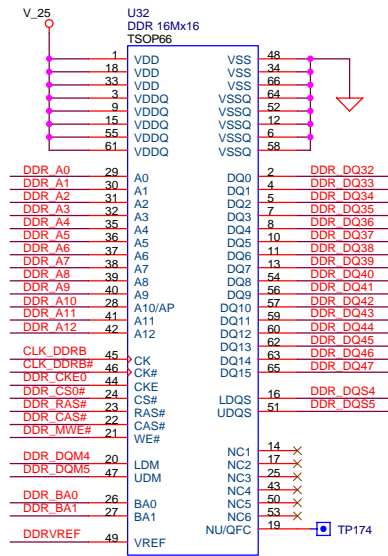
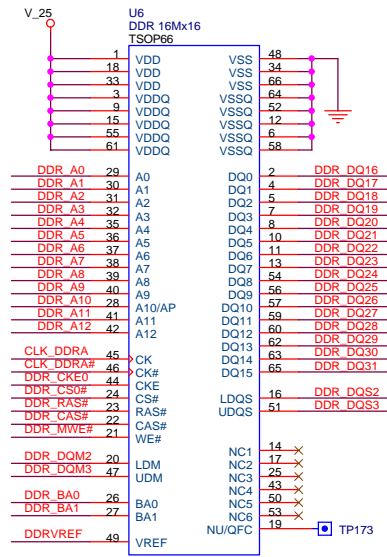
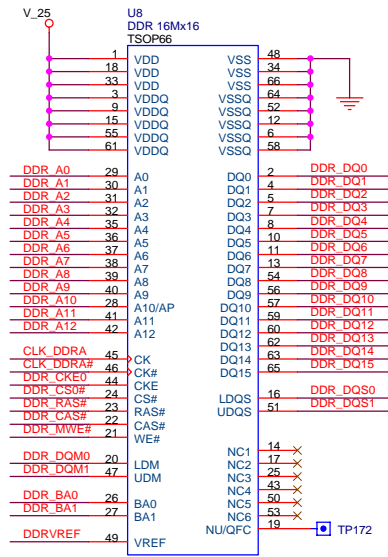


Resistor should go close to processor at S\_CLKOUT. Trace length should be calculated to be equal to the average of all the data line trace lengths.

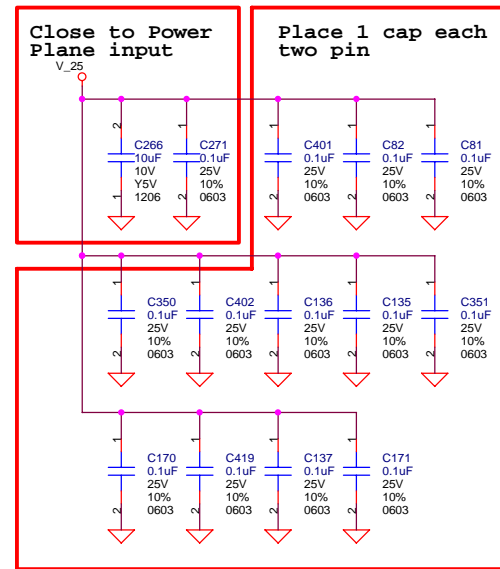








2 DDR\_CKE0 >>> DDR\_CKE0



- 2 DDR\_A[12..0] <<< VSS
- 2 DDR\_DQ[63..0] <<< VSS
- 2 DDR\_DQS[7..0] <<< VSS
- 2 DDR\_DQM[7..0] <<< VSS
- 2 CLK\_DDRA <<< CLK\_DDRA
- 2 CLK\_DDRA# <<< CLK\_DDRA#
- 2 CLK\_DDRB <<< CLK\_DDRB
- 2 CLK\_DDRB# <<< CLK\_DDRB#
- 2 DDR\_CS0# <<< DDR\_CS0#
- 2 DDR\_RAS# <<< DDR\_RAS#
- 2 DDR\_CAS# <<< DDR\_CAS#
- 2 DDR\_MWE# <<< DDR\_MWE#
- 2 DDR\_BA0 <<< DDR\_BA0
- 2 DDR\_BA1 <<< DDR\_BA1

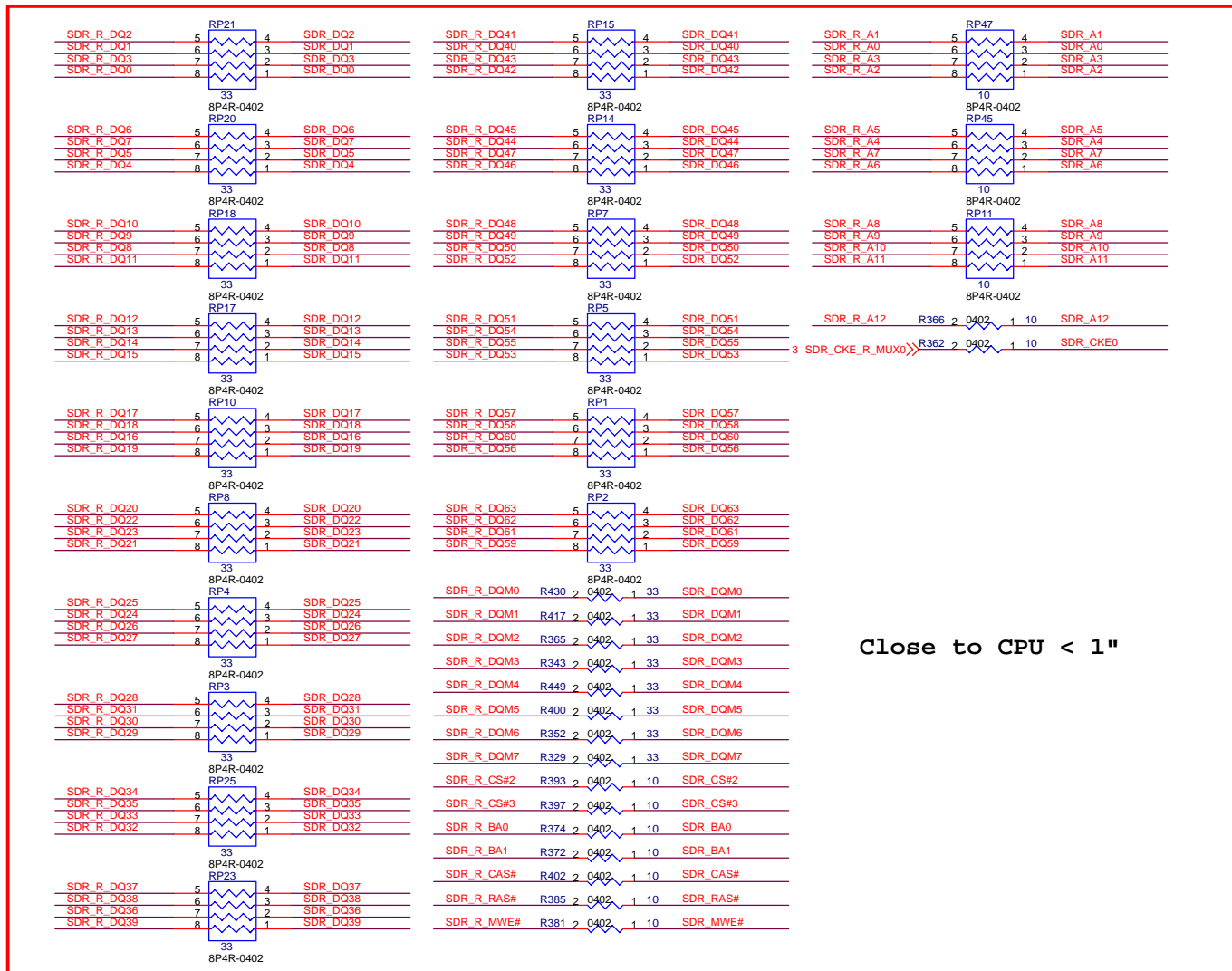
3 SDR\_R\_DQM[7..0] << SDR\_R\_DQM[7..0]

3 SDR\_R\_CS#2 << SDR\_R\_CS#2  
 3 SDR\_R\_CS#3 << SDR\_R\_CS#3  
 3 SDR\_R\_BA0 << SDR\_R\_BA0  
 3 SDR\_R\_BA1 << SDR\_R\_BA1

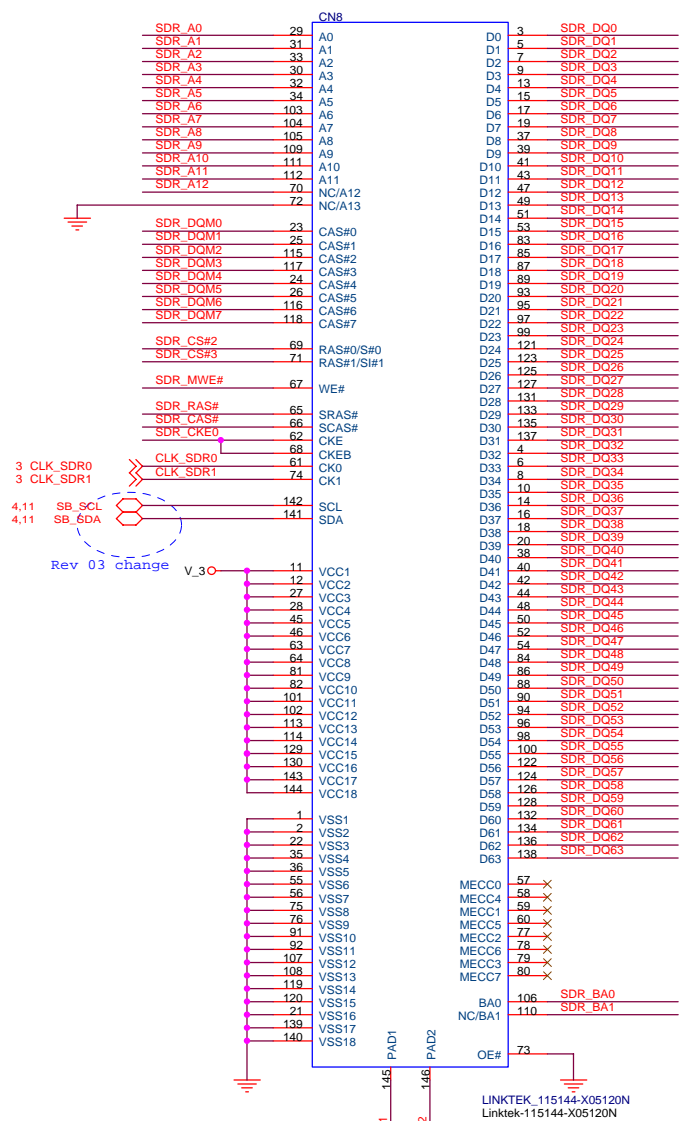
3 SDR\_R\_CAS# << SDR\_R\_CAS#  
 3 SDR\_R\_RAS# << SDR\_R\_RAS#  
 3 SDR\_R\_MWE# << SDR\_R\_MWE#

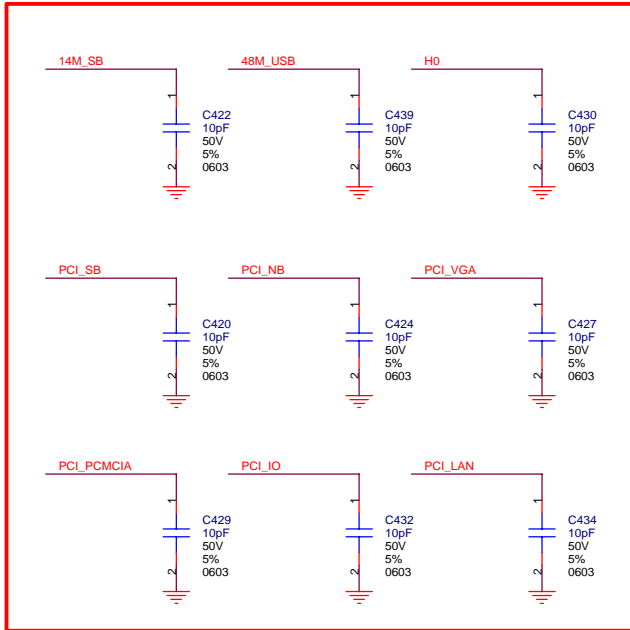
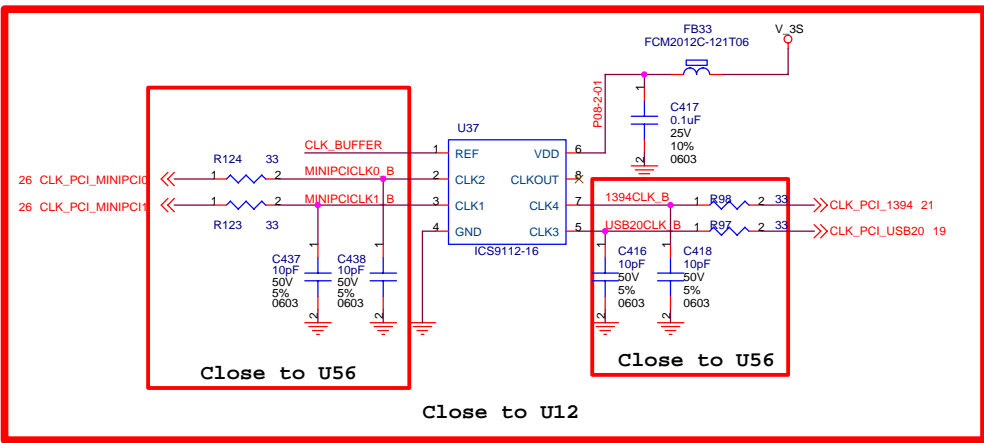
3 SDR\_R\_A[12..0] << SDR\_R\_A[12..0]

3 SDR\_R\_DQ[63..0] << SDR\_R\_DQ[63..0]

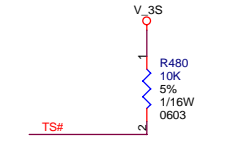


Close to CPU < 1"

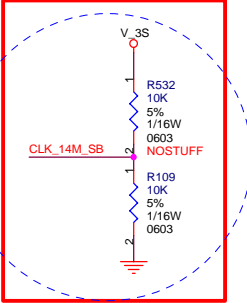




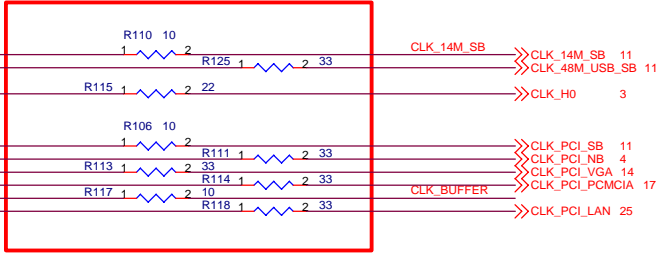
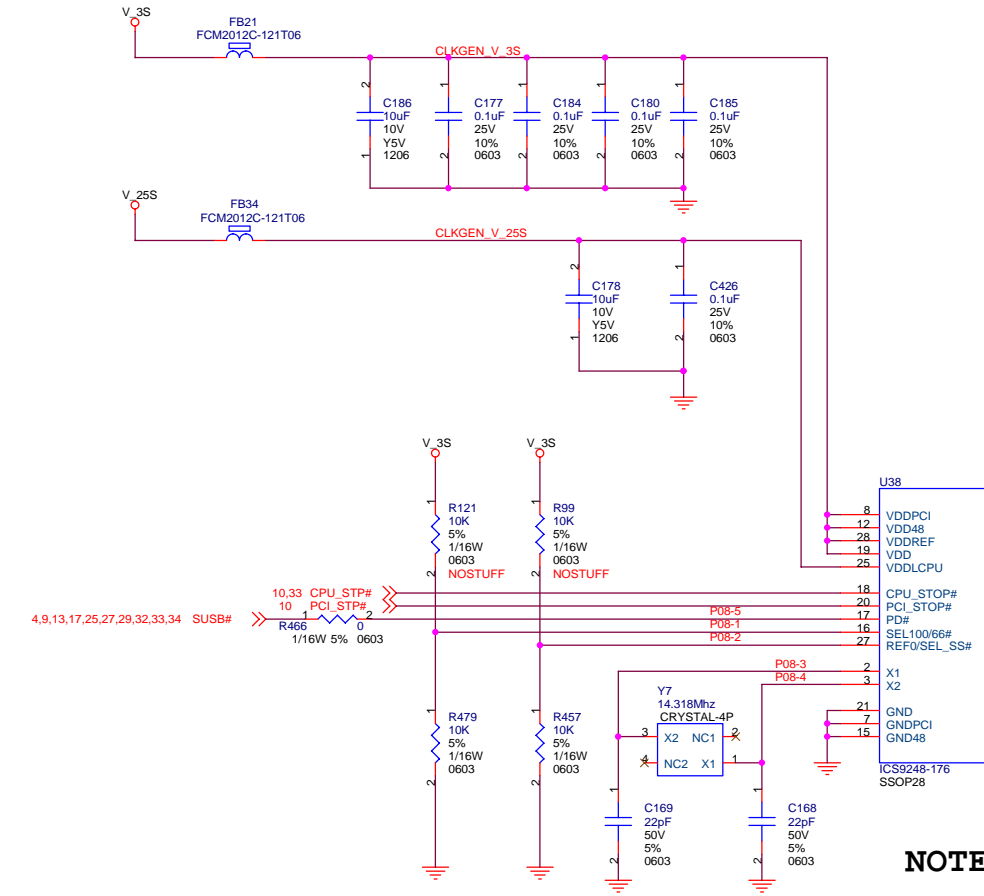
Note : These capacitor placed near clock generator as near as possible



When pull-up,disable spread spectrum. When pull-low,enable spread spectrum. Placed near the M1535



Rev 03 change



Note : These resistor placed near clock generator as near as possible

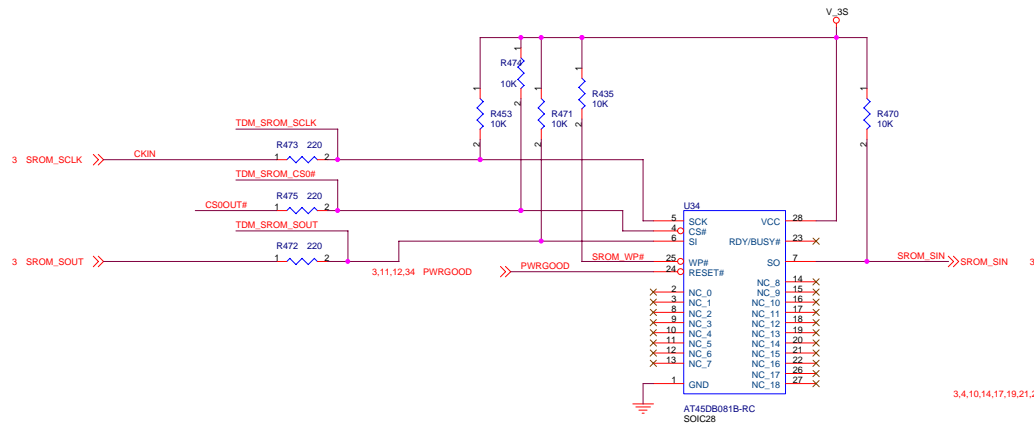
**NOTE : THE CLK GND OVERLAP TO SYSTEM GND BY LAYOUT**

Title		
Clock Generator		
Size	Document Number	Rev
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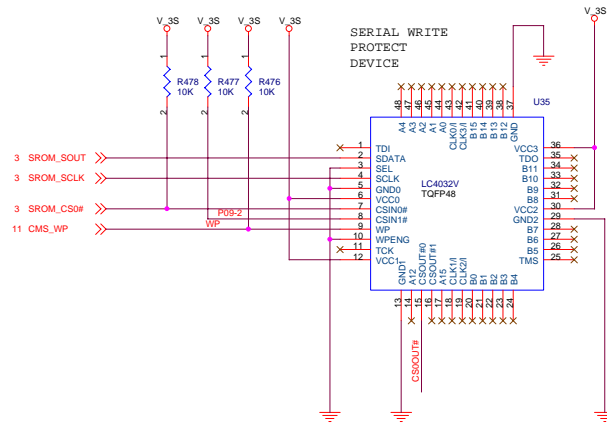


8MBIT SERIAL FLASH ROM For CMS.

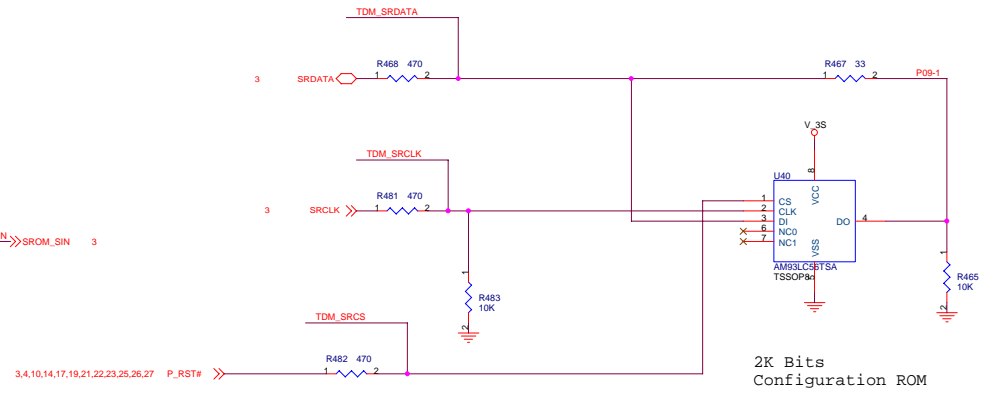
For Flash ROM short issue, we must design 2 different package for source.



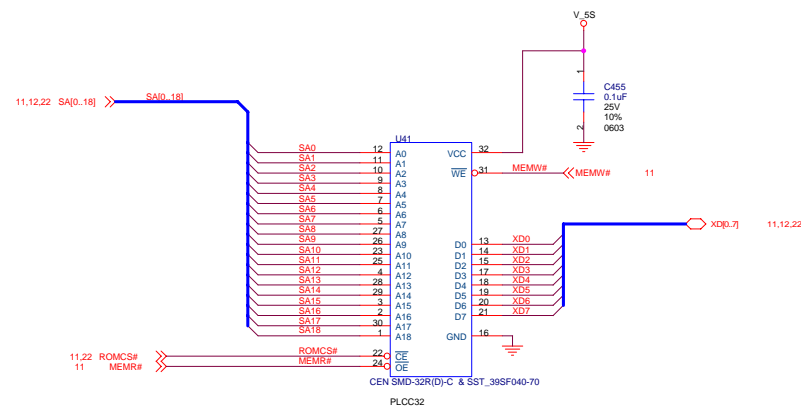
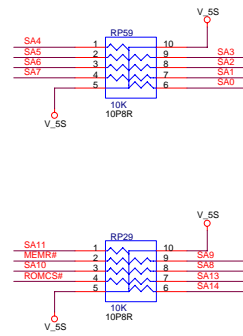
SROM\_WP IS A GPIO, MUST BE 3.3V IO



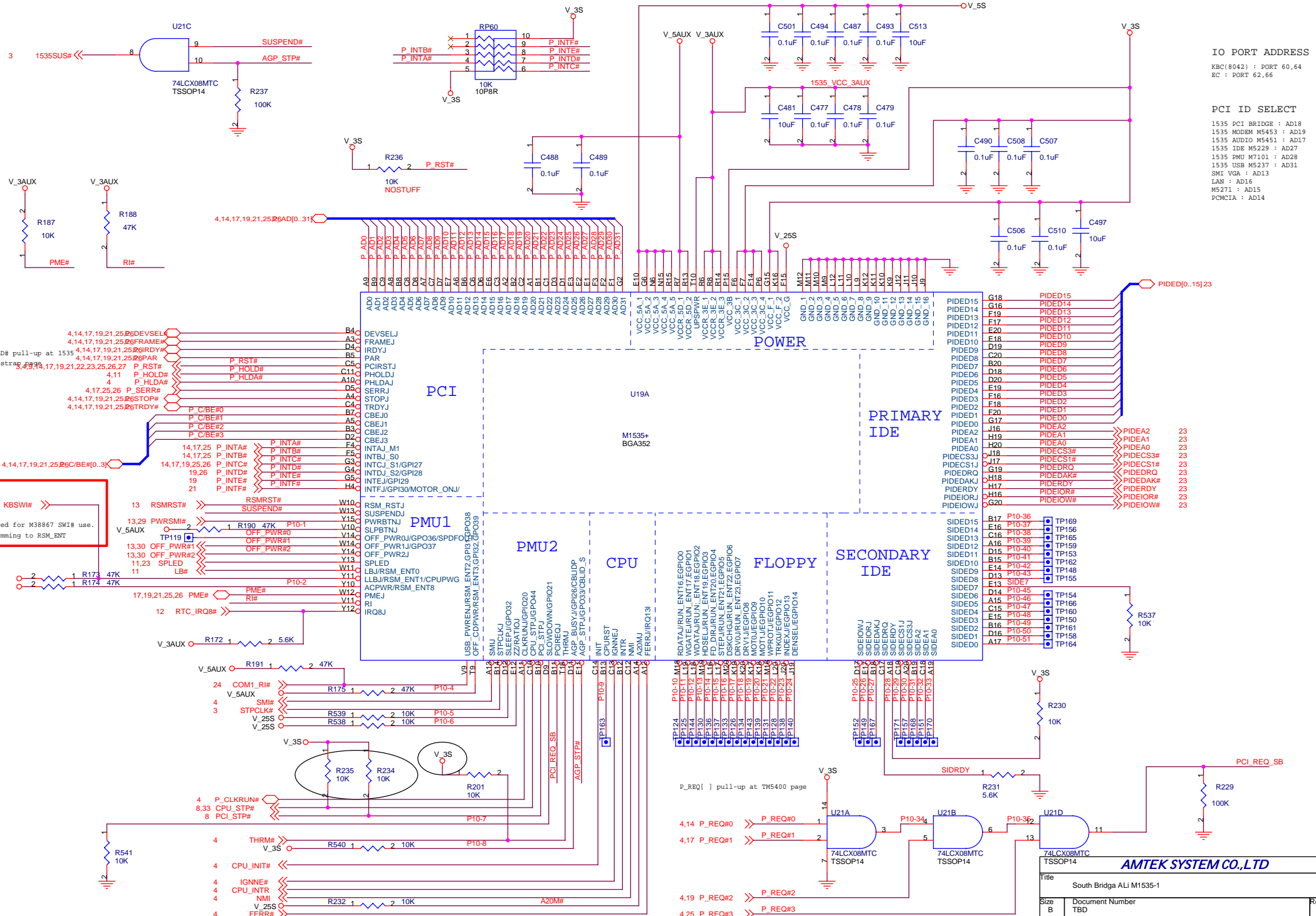
PRIMARY DEBUG CONNECTOR A



2K Bits Configuration ROM



<b>AMTEK SYSTEM CO.,LTD</b>			
File	ROM & Debug Port		
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**IO PORT ADDRESS**  
 KBC(8042) : PORT 60,64  
 EC : PORT 62,66

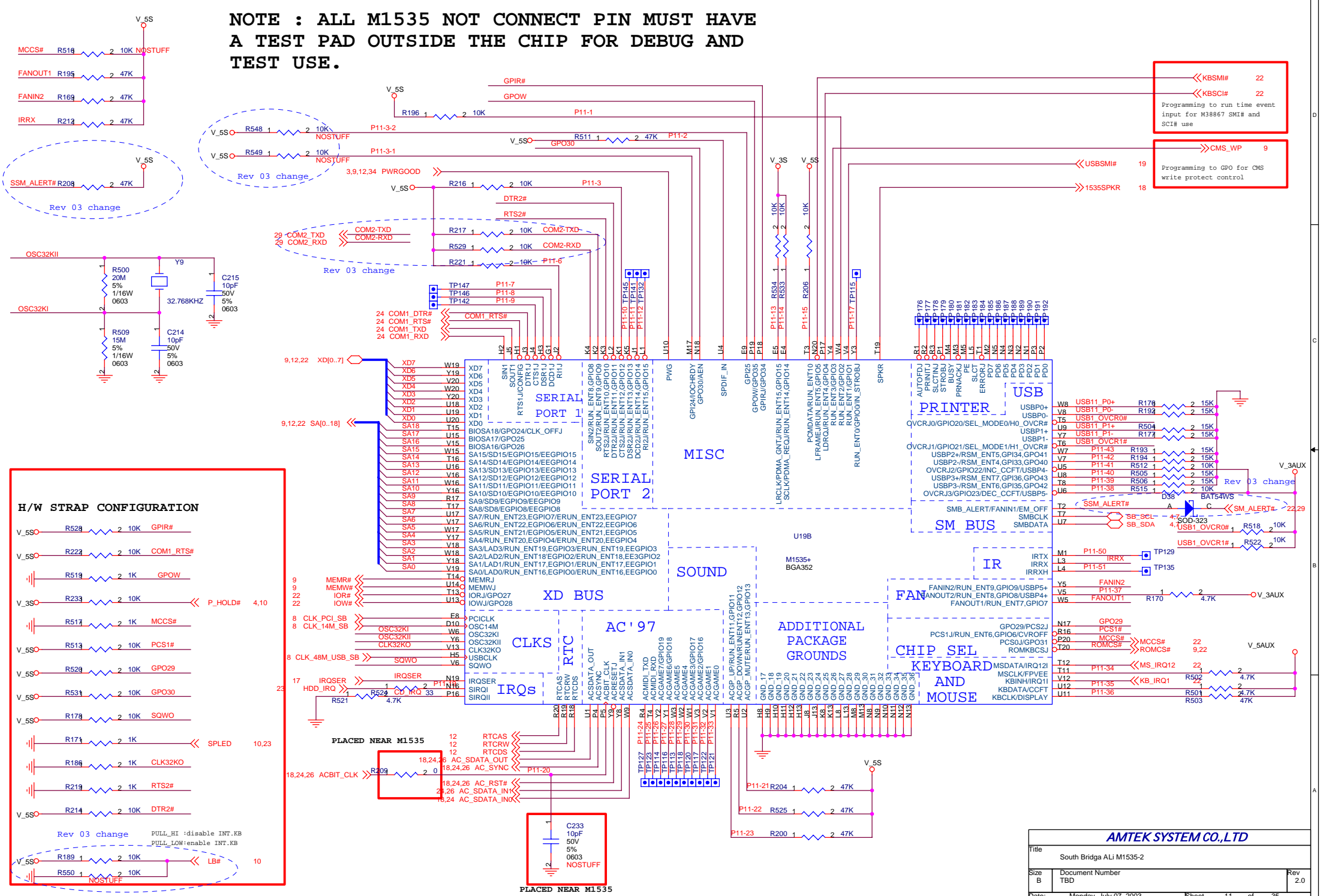
**PCI ID SELECT**  
 1535 PCI BRIDGE : AD18  
 1535 MODEM M5453 : AD19  
 1535 ADIO M5451 : AD17  
 1535 IDE M5229 : AD27  
 1535 PMU M7101 : AD28  
 1535 USB M5237 : AD31  
 SMI VGA : AD13  
 LAN : AD16  
 M5271 : AD15  
 ROMCIA : AD14

22 KBSW# >>>  
 Reserved for M38867 SWI# use.  
 Programming to RSM\_ENT

**AMTEK SYSTEM CO.,LTD**

Title		
South Bridga ALI M1535-1		
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**NOTE : ALL M1535 NOT CONNECT PIN MUST HAVE A TEST PAD OUTSIDE THE CHIP FOR DEBUG AND TEST USE.**



<<KBSM# 22  
 <<KBSC# 22  
 Programming to run time  
 input for M38867 SMI# and  
 SCI# use

>>USBSSM# 19  
 >>1535SPKR 18  
 Programming to GPO for CMS  
 write protect control

**H/W STRAP CONFIGURATION**

V\_5S R528 2 10K GPIR#  
 V\_5S R223 2 10K COM1\_RTS#  
 R519 2 1K GPOW  
 V\_3S R233 2 10K P\_HOLD# 4,10  
 R517 2 1K MCCS#  
 V\_5S R513 2 10K PCS1#  
 V\_5S R529 2 10K GPO29  
 V\_5S R531 2 10K GPO30  
 V\_5S R179 2 10K SQWO  
 R171 2 1K SPLED 10,23  
 R186 2 1K CLK32KO  
 R219 2 1K RTS2#  
 V\_5S R214 2 10K DTR2#  
 Rev 03 change  
 V\_5S R189 2 10K LB# 10  
 R550 2 10K NOSTUFF

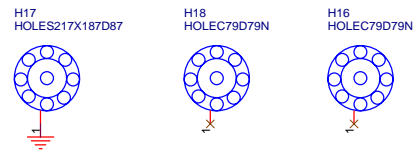
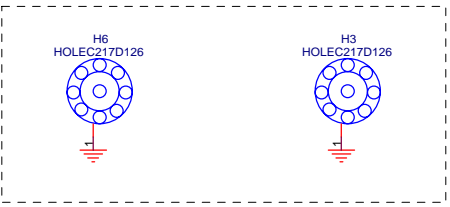
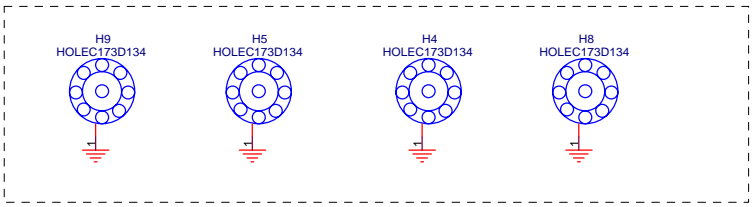
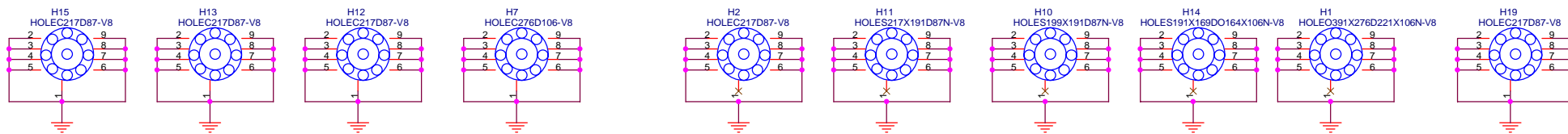
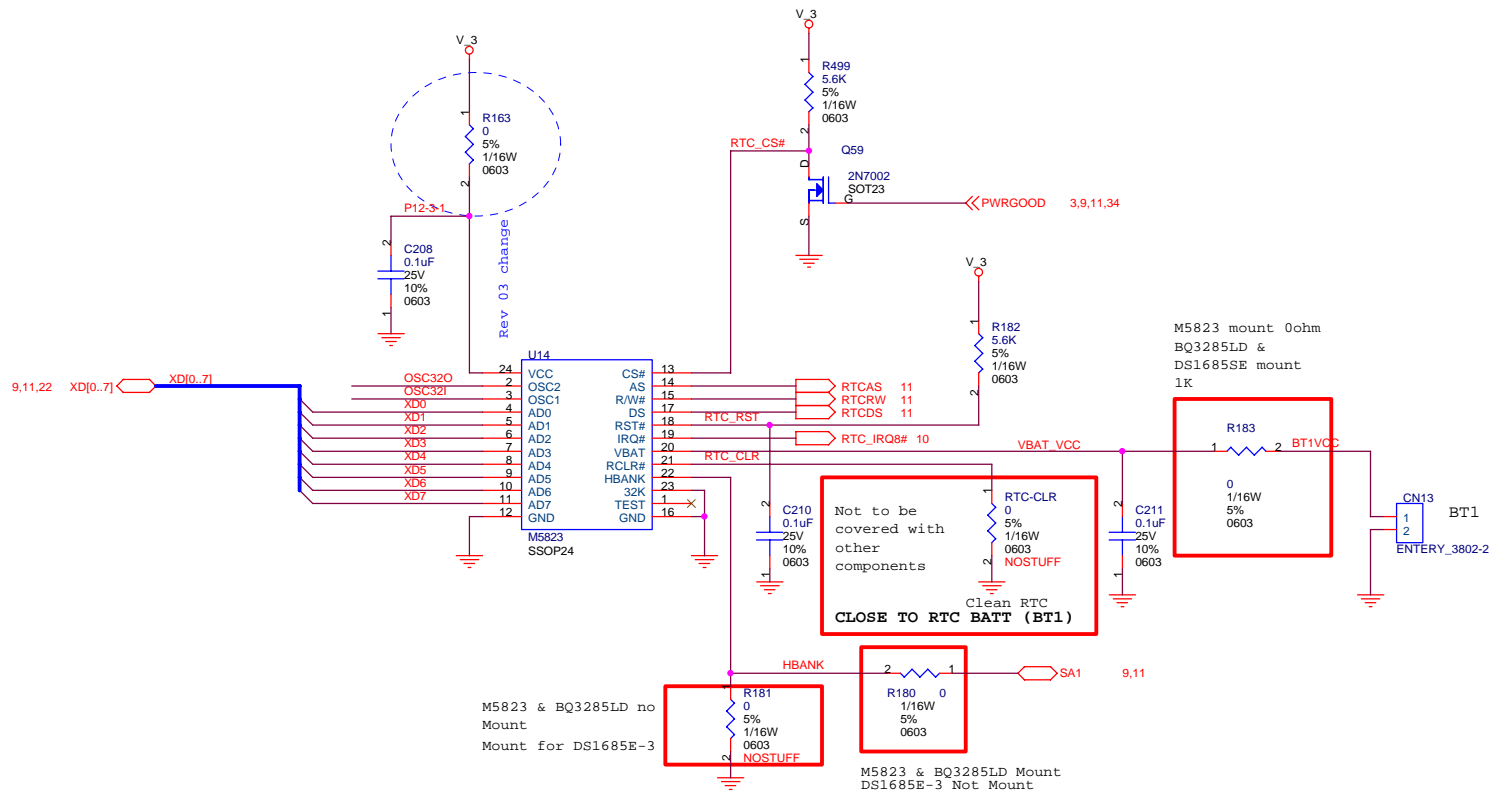
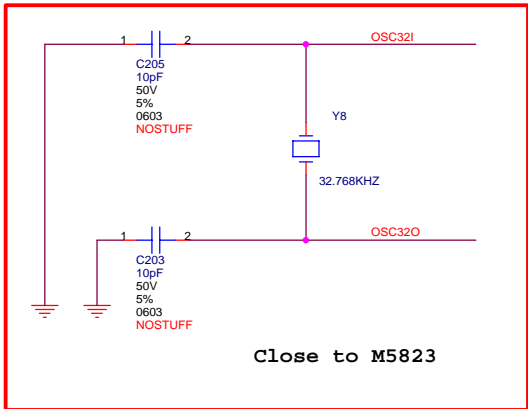
**PLACED NEAR M1535**

18,24,26 ACBIT\_CLK R209 2 0  
 18,24,26 AC\_SYNC R209 2 0  
 18,24,26 AC\_RST# R209 2 0  
 18,24,26 AC\_SDATA\_IN R209 2 0  
 18,24,26 AC\_SDATA\_IN R209 2 0

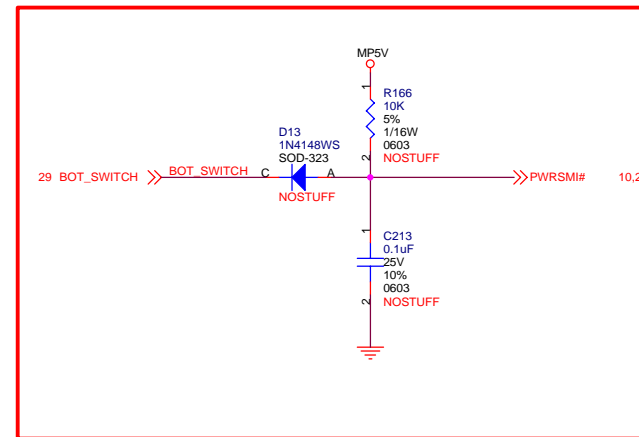
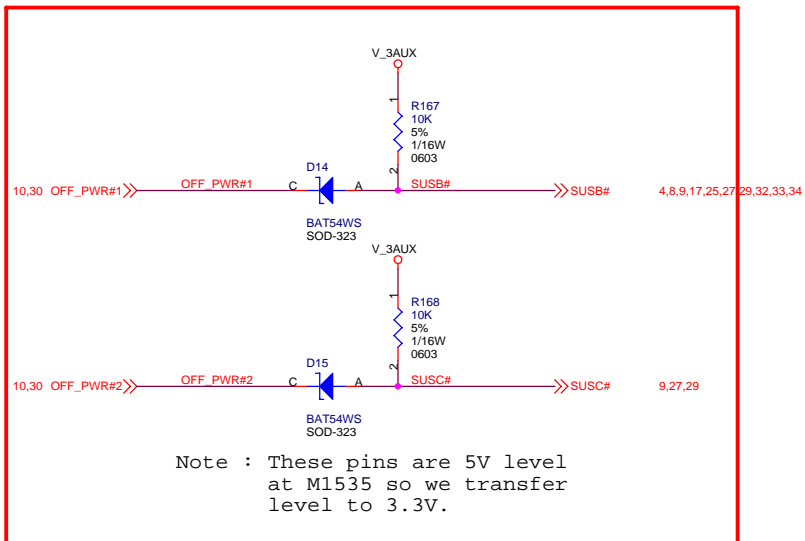
C233 10pF  
 50V  
 5%  
 0603  
 NOSTUFF

**PLACED NEAR M1535**

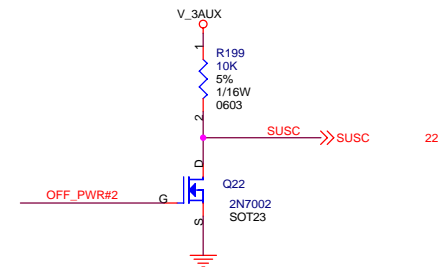
<b>AMTEK SYSTEM CO.,LTD</b>		
Title	South Bridga ALI M1535-2	
Size	Document Number	Rev
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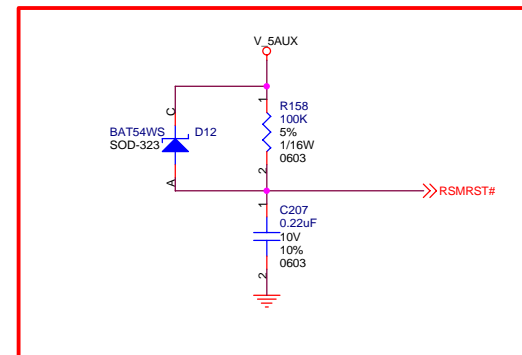
<b>AMTEK SYSTEM CO.,LTD</b>		
Title	RTC	
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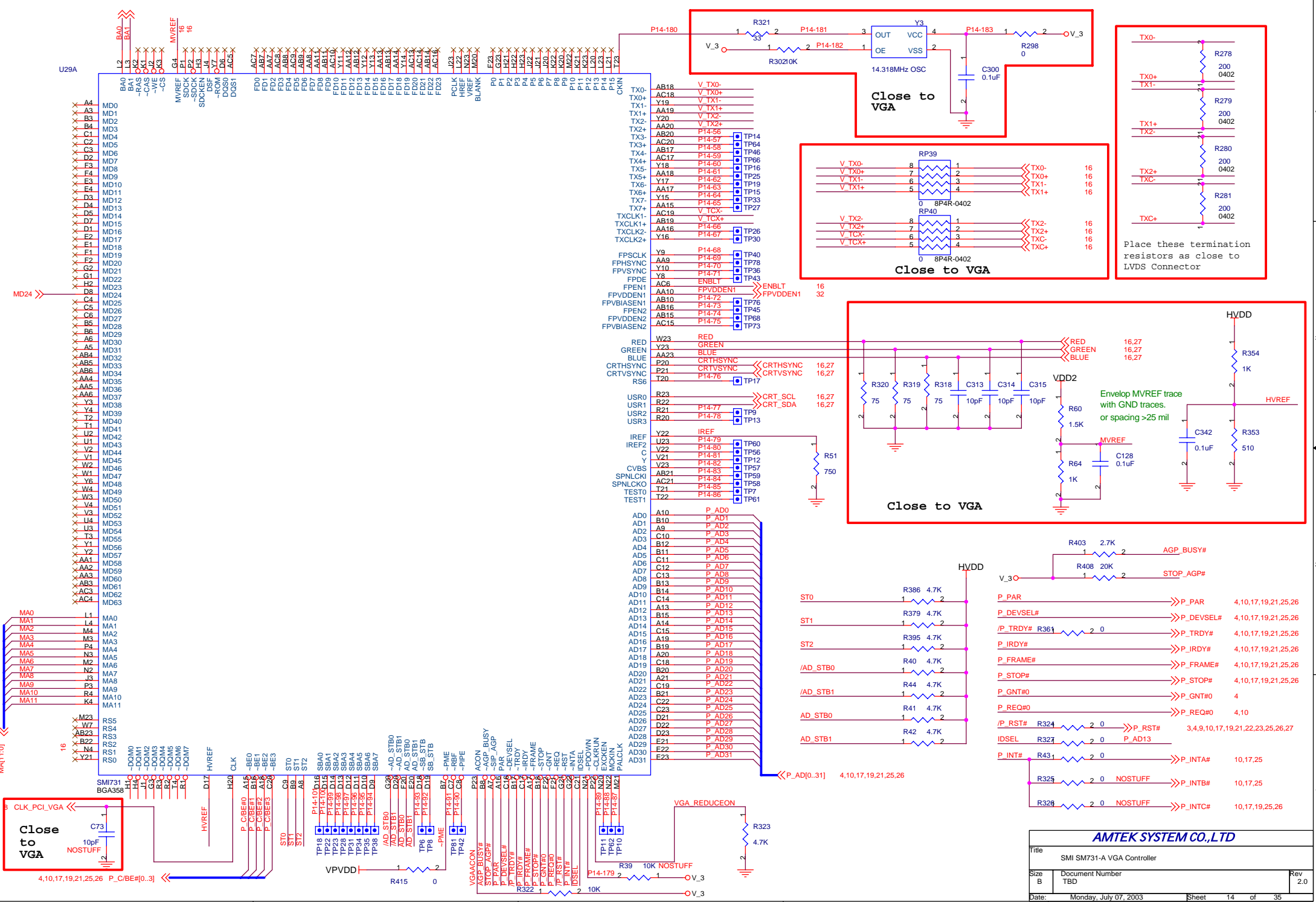
Reserve power bottom circuit to M1535



Check timing

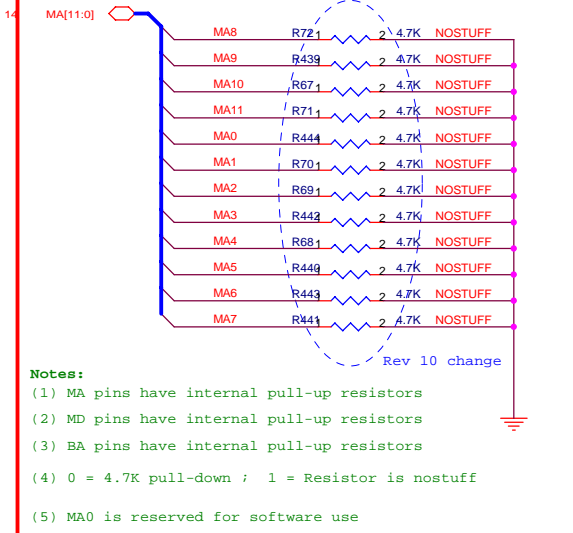


Title		
Reset & Power Plane Control		
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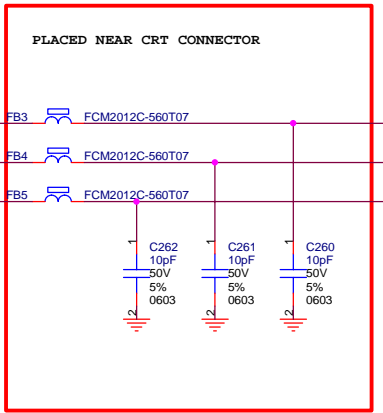
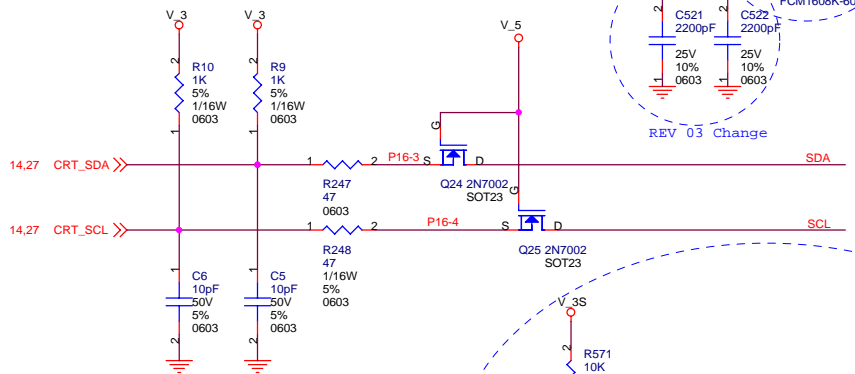
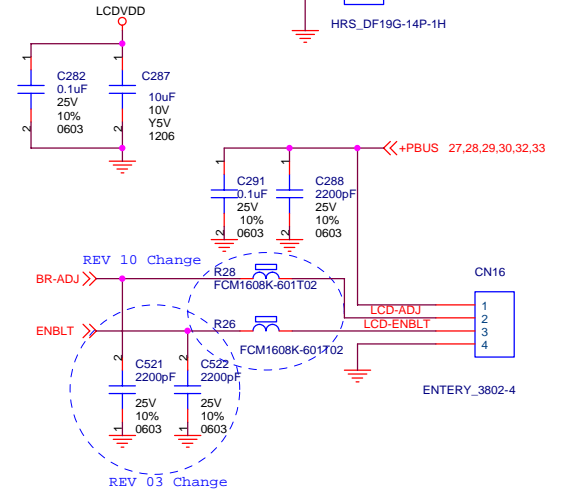
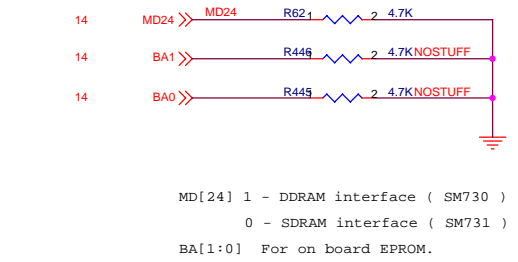
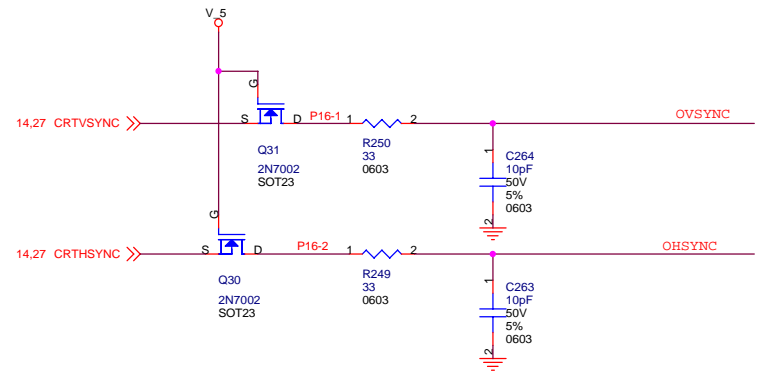
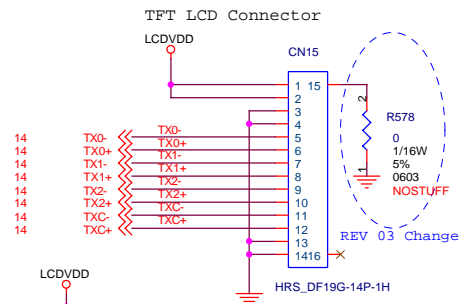
**Close to VGA**



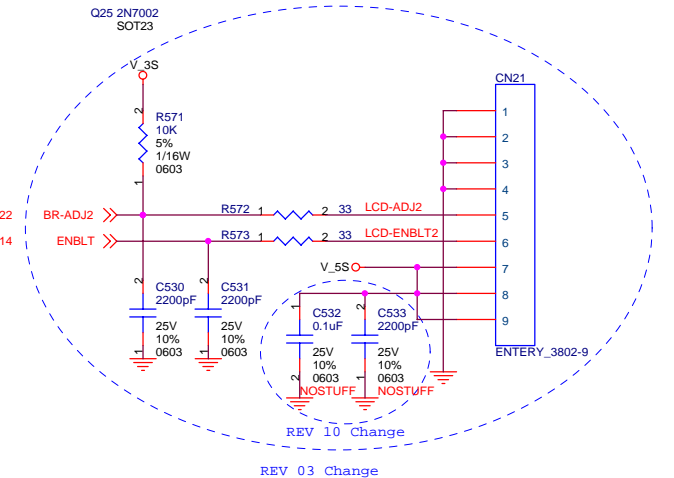
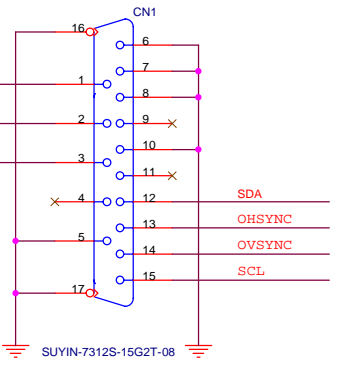
**Panel Display Settings:**

MA Bits	STATE	SETTING
MA[11:8]	0000	640X480 TFT
	0001	800X600 TFT
	0010	1024X768 TFT
	0011	1280X1024 TFT
	0100	1600X1200 TFT
MA3	0	Double LVDS
	1	Single LVDS
MA4	0	LCD1 SW Panel Sequence
	1	LCD1 HW Panel Sequence
MA5	0	Normal LVDS
	1	Hitachi LVDS
MA6	0	18 Bit TFT
	1	24 Bit TFT
MA7	0	AGP 1.5V
	1	AGP 3.3V

MA Bits	STATE	SETTING
MA[1:2]	11	Both LVDS1 and Digital Panel as primary (default)
	10	LVDS1 as primary panel
	01	Digital Panel as primary
	00	Not Defined



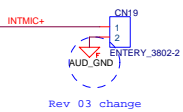
**CRT Output**







INT. MIC CONN.



Rev 03 change

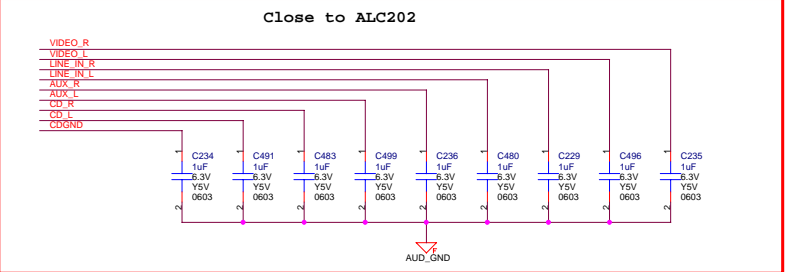
Rev 10 change

Rev 03 change

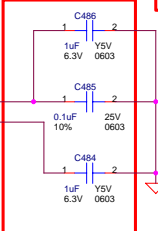
Rev 03 change

Rev 03 change

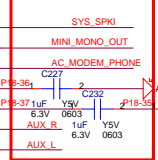
Close to ALC202



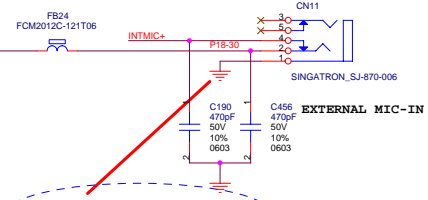
Close to ALC202



Close to ALC202

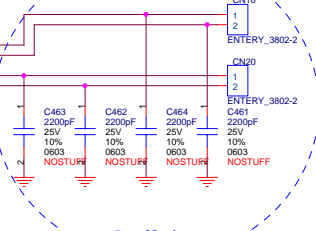


MIC IN



This GND route trace to FB37 Rev 03 change

INTERNAL SPEAKER CONNECTOR



Rev 03 change

AUDIO GND CONNECT TO DIGITAL GND AND CHASSIS GND VIA BOSS AND OVERLAP

This GND route trace to FB37 Rev 03 change

AMTEK SYSTEM CO.,LTD		
File	AC97 & AMPLIFIER	
Size	Document Number	Rev
C	TBD	2.0
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4,10,14,17,21,25,26 P\_AD[0..31]

4,10,14,17,21,25,26 P\_C/BE#[0..3]

4,10,14,17,21,25,26 P\_FRAME#

4,10,14,17,21,25,26 P\_IRDY#

4,10,14,17,21,25,26 P\_TRDY#

4,10,14,17,21,25,26 P\_DEVSEL#

4,10,14,17,21,25,26 P\_STOP#

4,10,14,17,21,25,26 P\_PAR#

4,10 P\_REQ#2

4 P\_GNT#2

3,4,9,10,14,17,21,22,23,25,26,27 P\_RST#

8 CLK\_PCI USB20

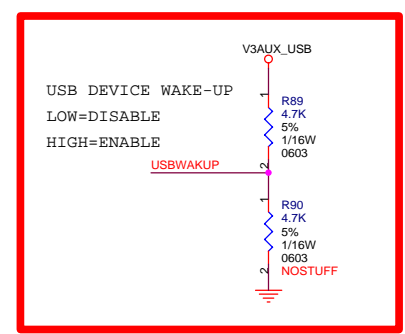
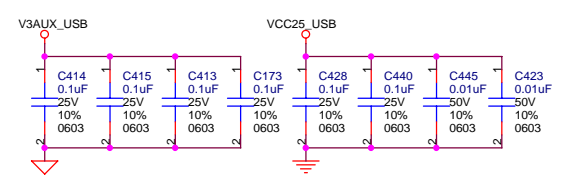
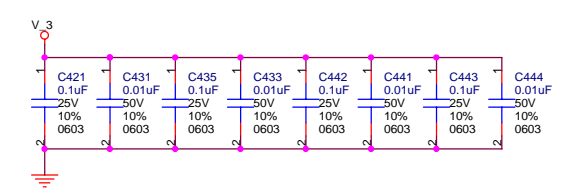
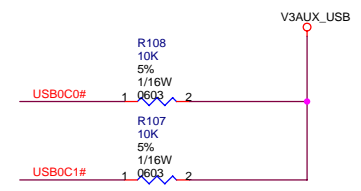
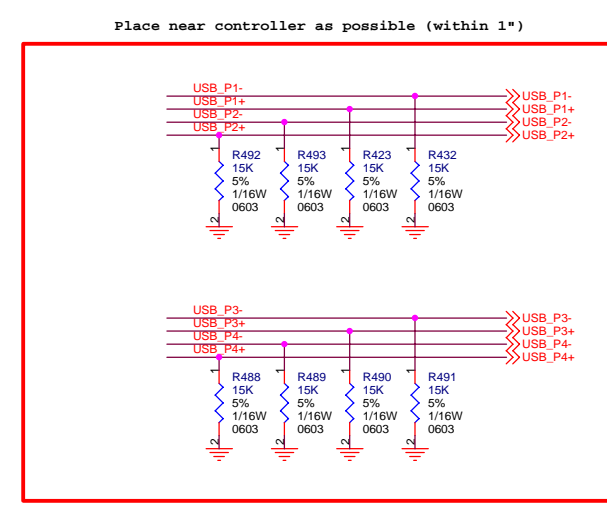
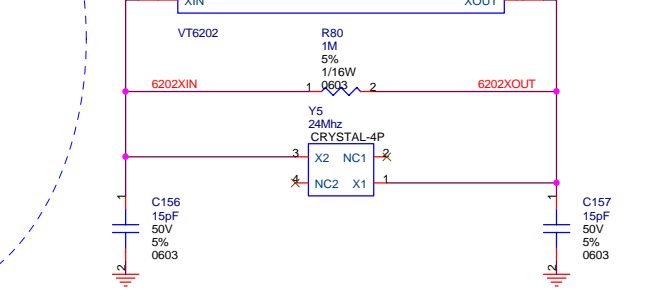
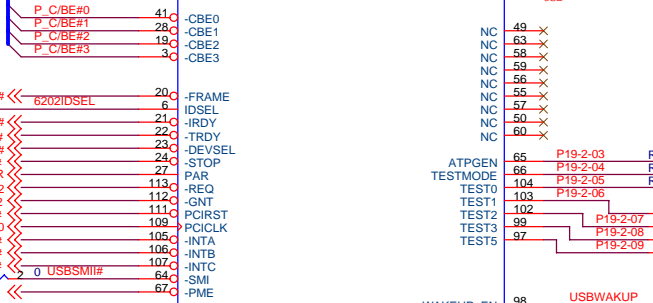
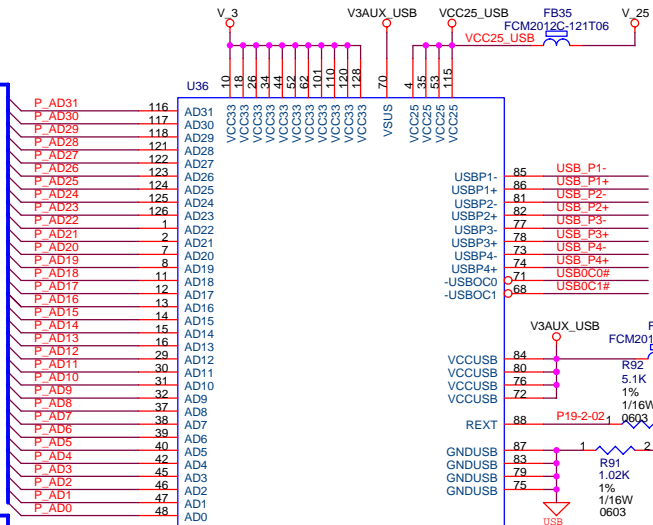
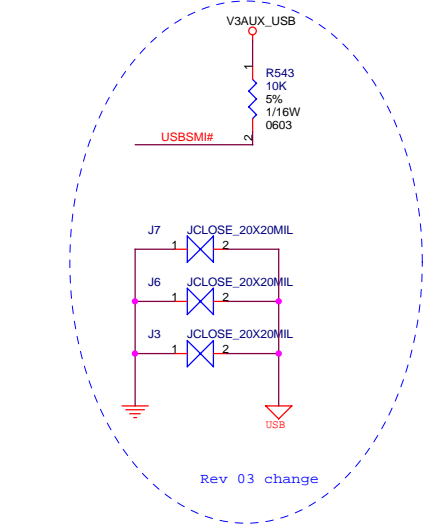
10,14,17,25,26 P\_INTC#

10,25 P\_INTD#

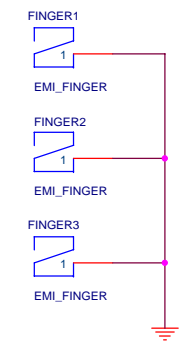
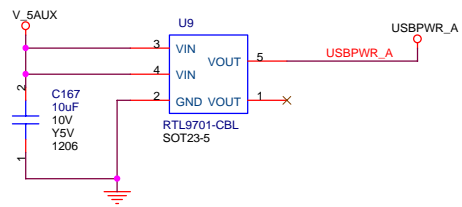
10 P\_INTE#

11 USBSMI#

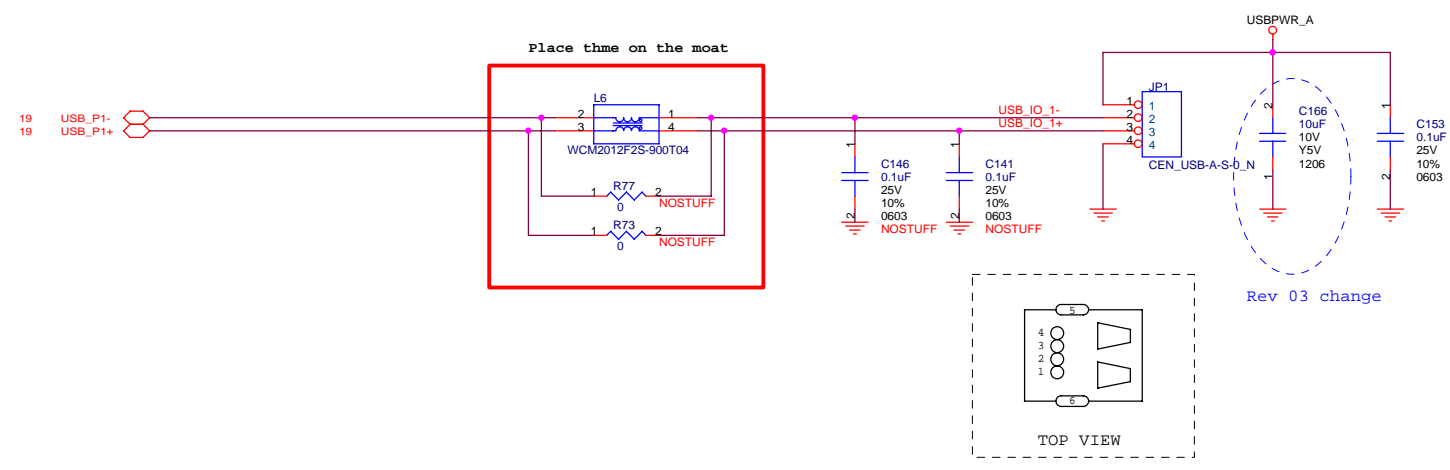
10,17,21,25,26 PME#



Title		
USB2.0-VIA VT6202		
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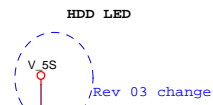
**USB 2.0 I/O CONN**



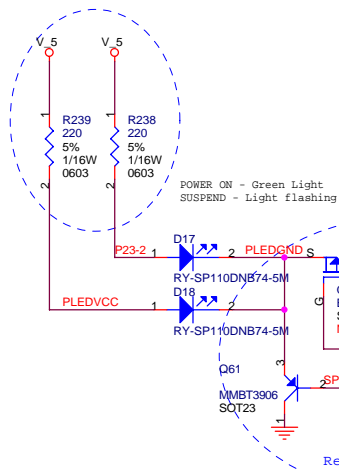
<b>AMTEK SYSTEM CO.,LTD</b>		
Title USB I/O Port		
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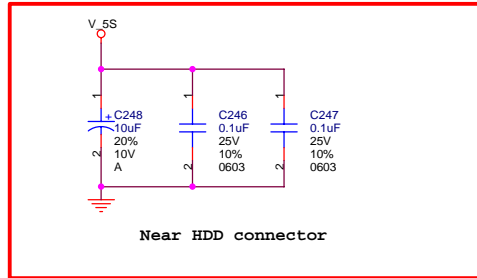
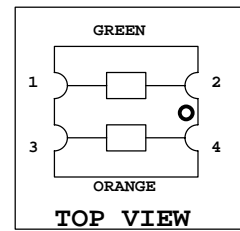
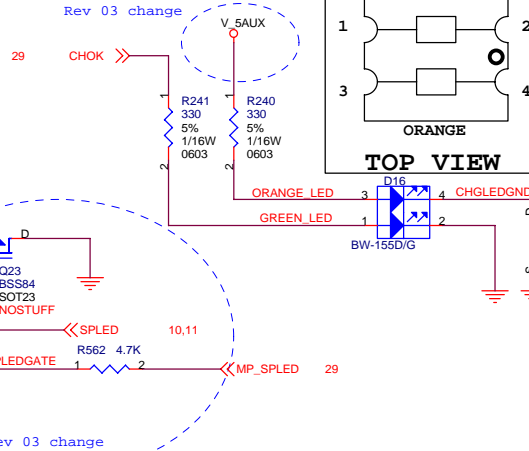


Rev 03 change SLEEP LED

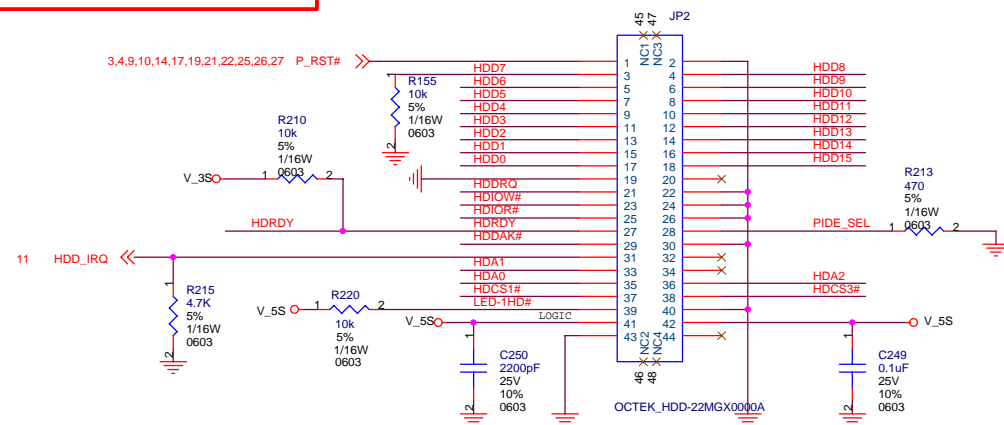


1-2: POWER\_ON LED  
3-4: CHARGER LED

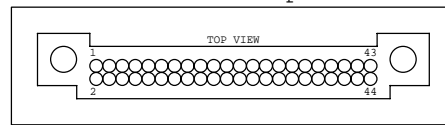
Rev 03 change



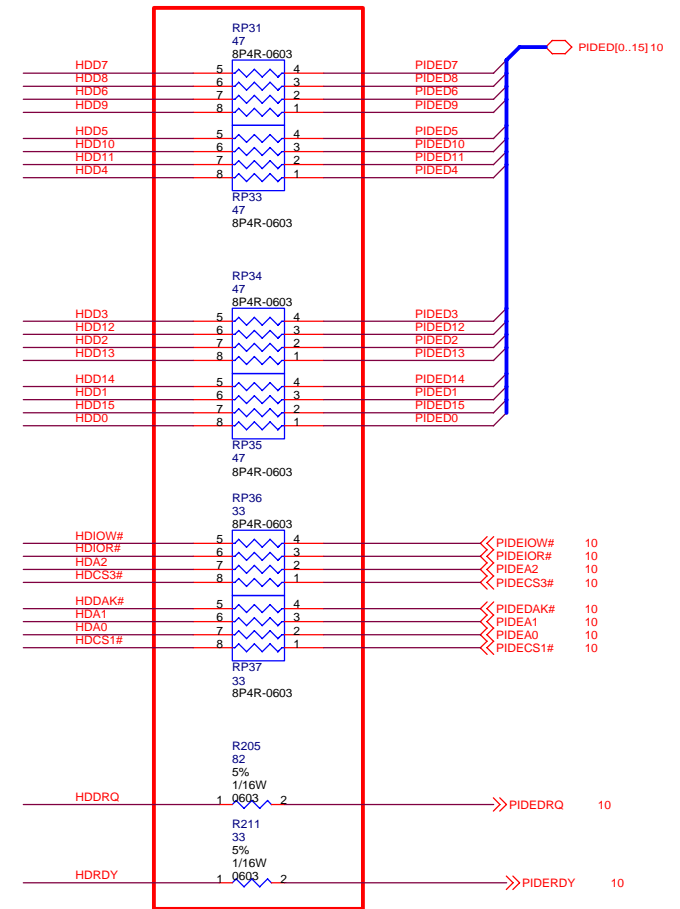
HDD CONNECTOR



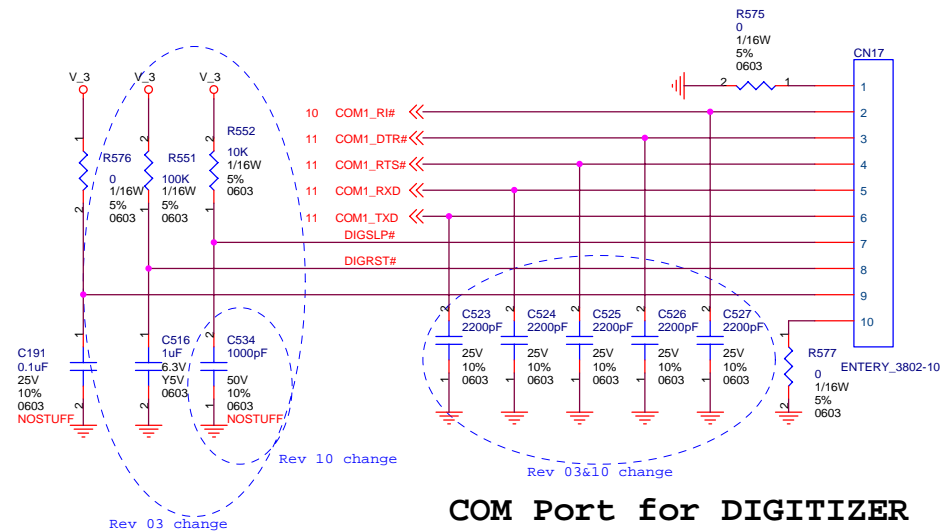
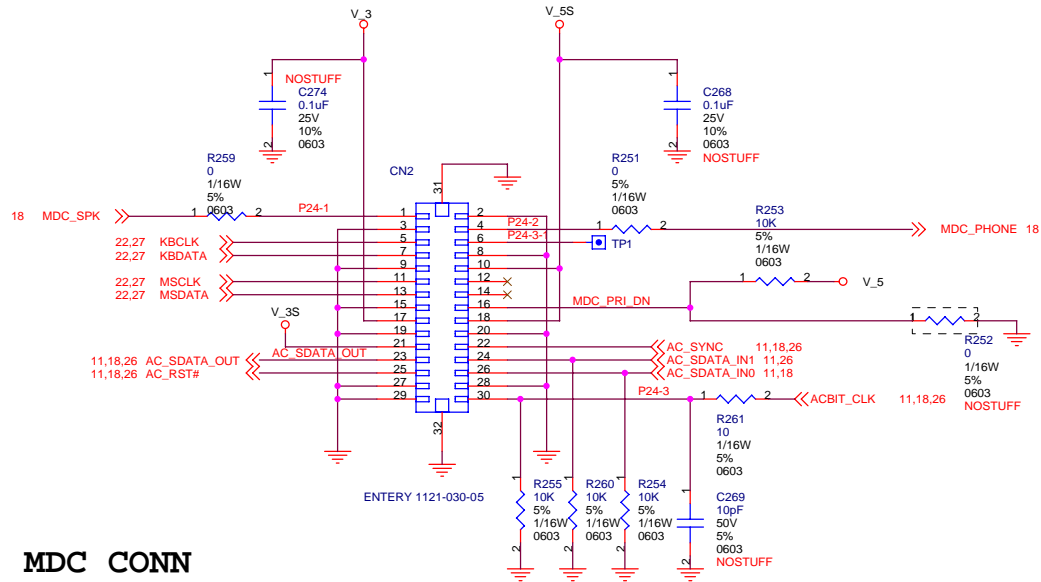
HDD connector pin out



PLACED NEAR HDD CONNECTOR



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Title HDD CONN. & LEDs		
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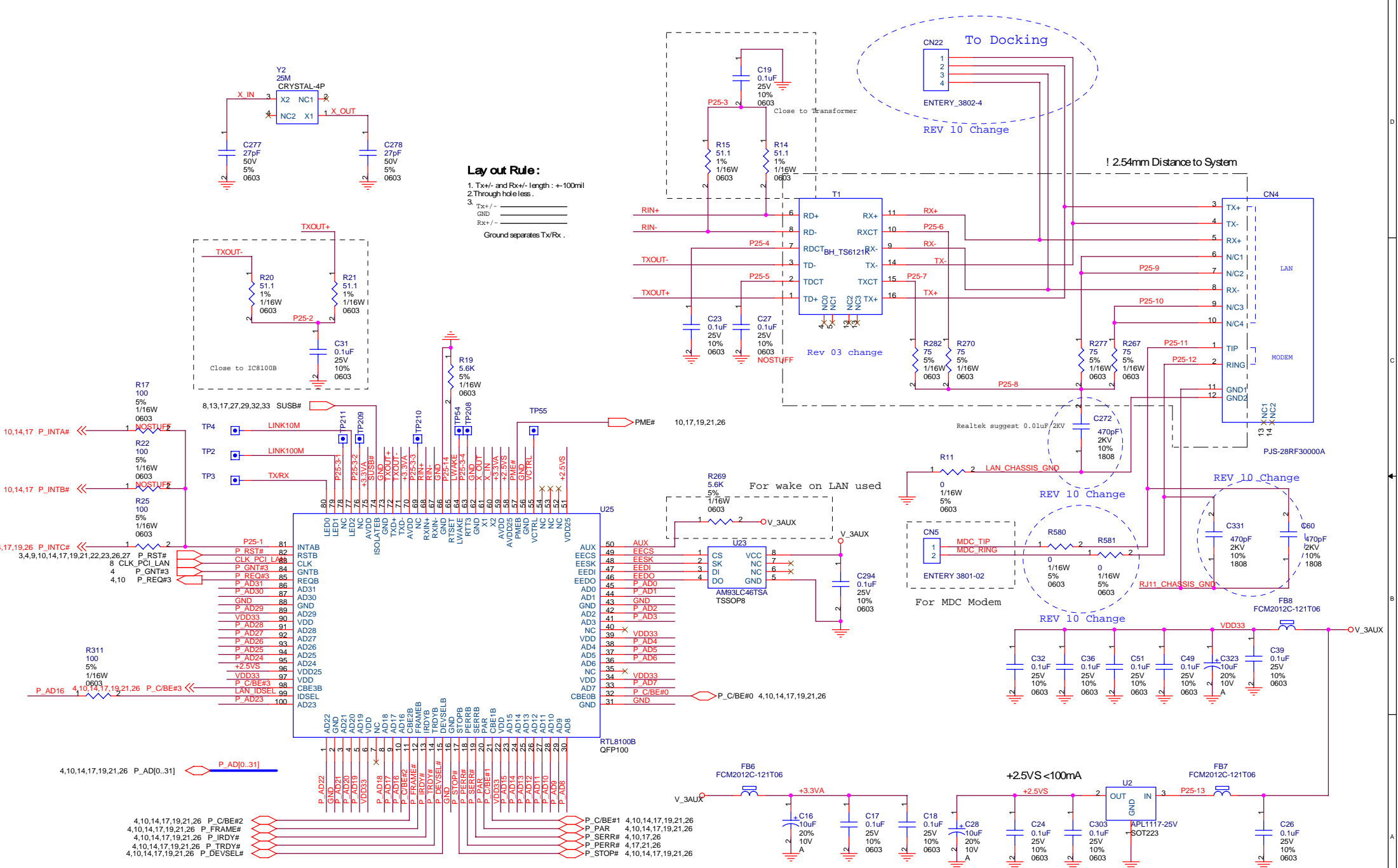


MDC CONN

COM Port for DIGITIZER

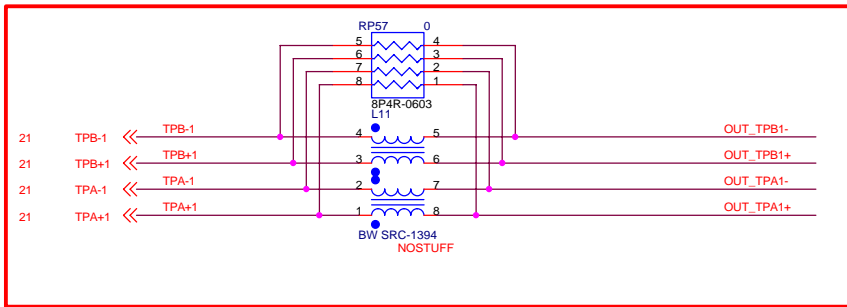
Title		
MDC & COM Port		
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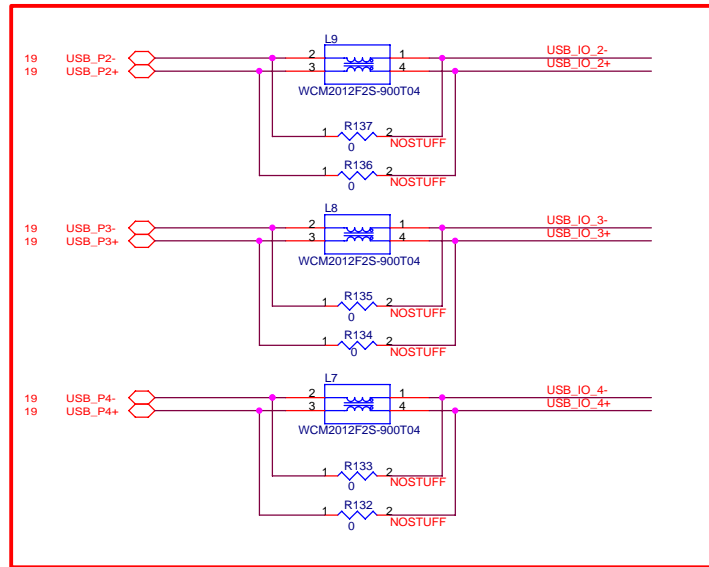




### 1394 to Docking

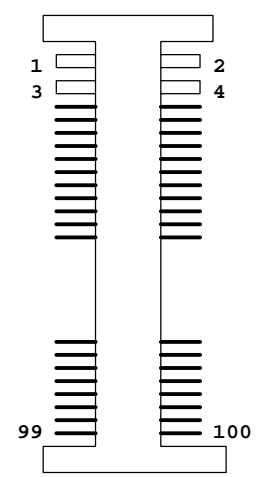
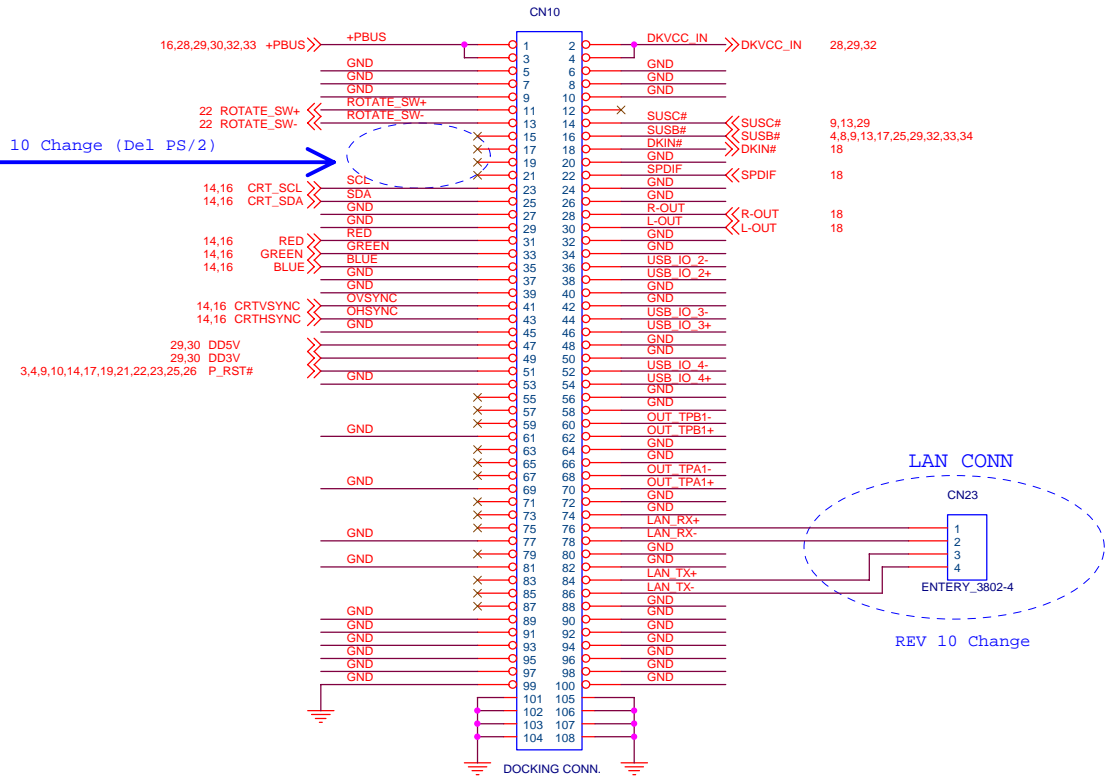


### USB2.0 to Docking



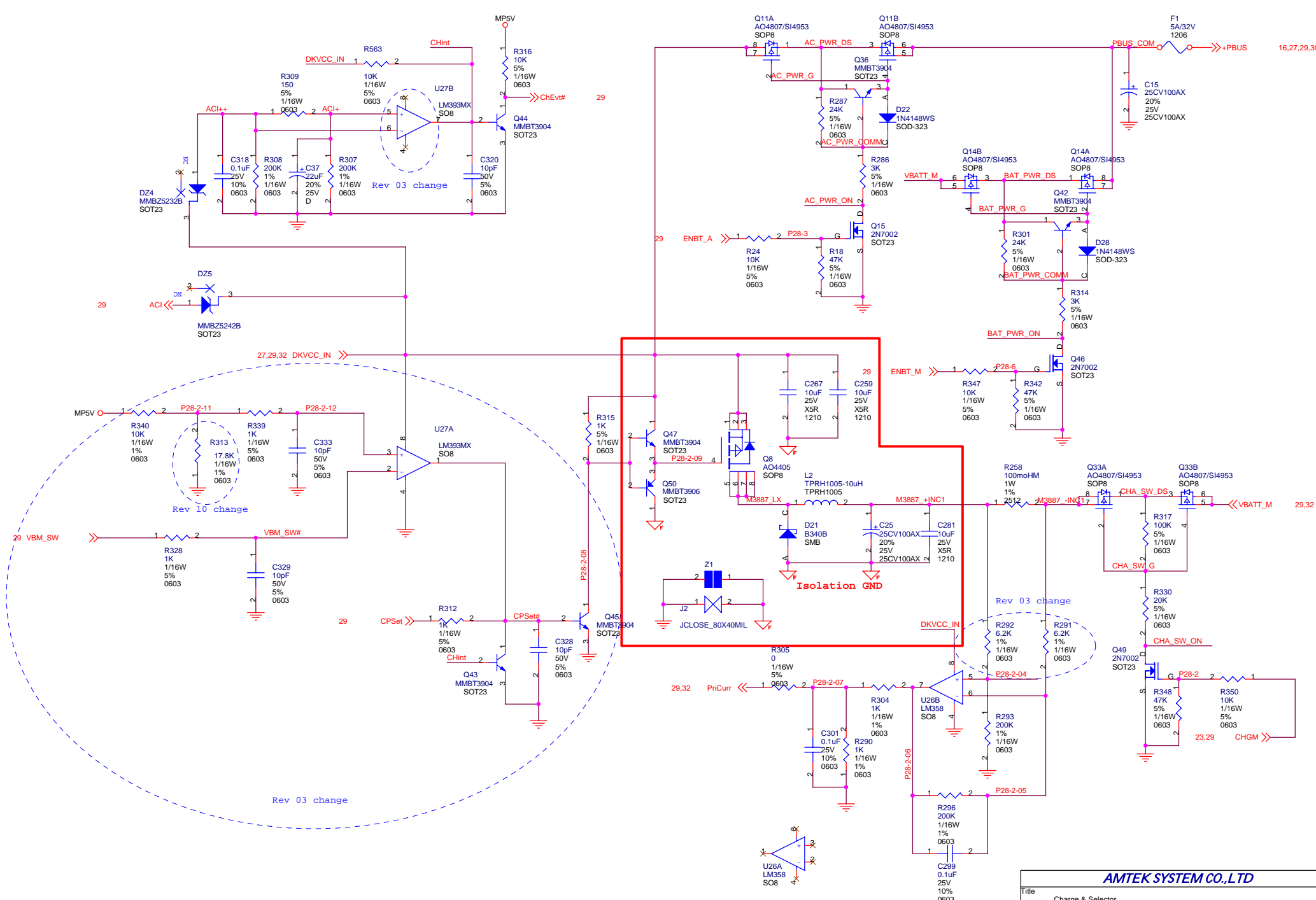
Close to the connector

REV 10 Change (Del PS/2)

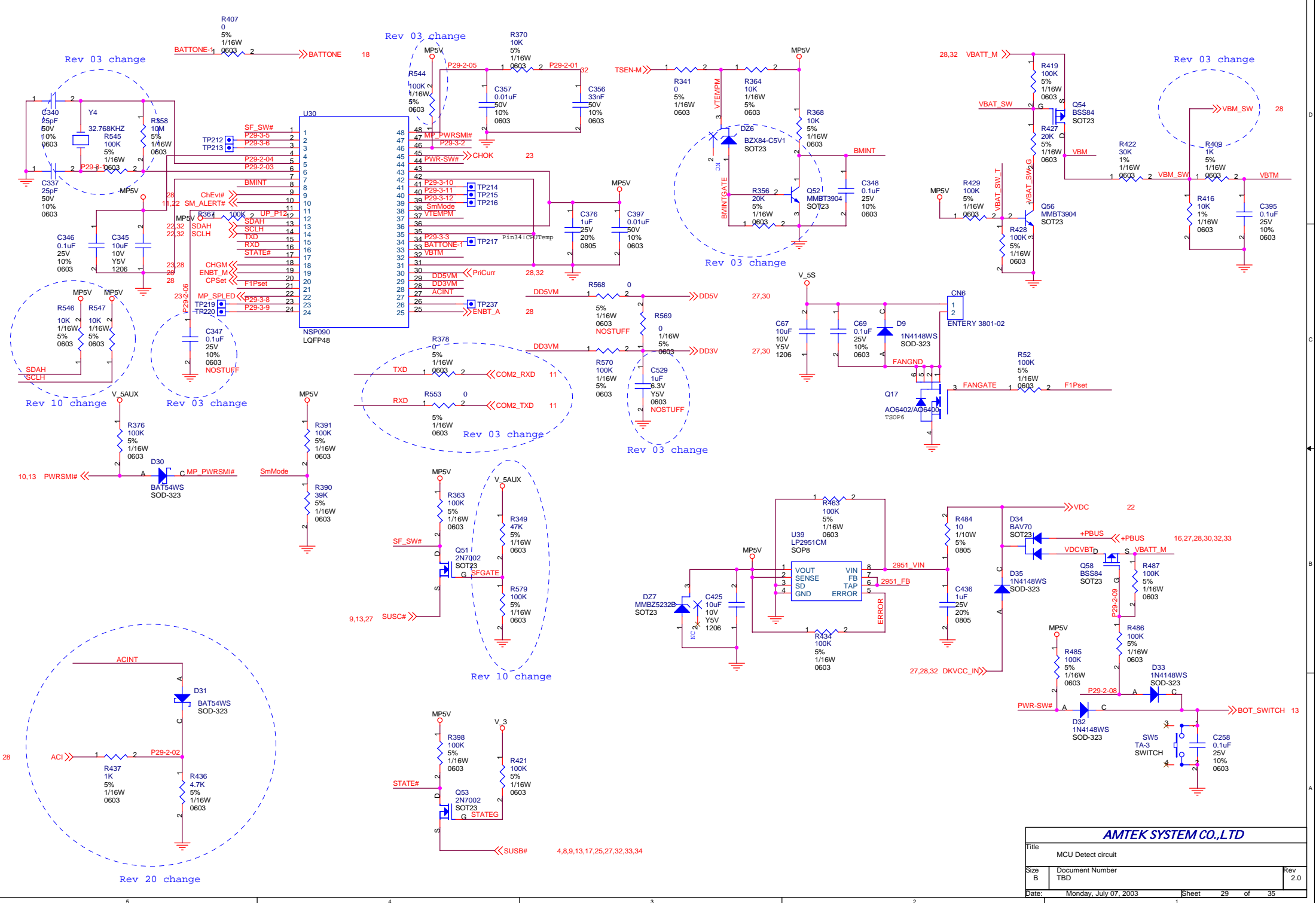


TOP VIEW

Title		
Docking Connector		
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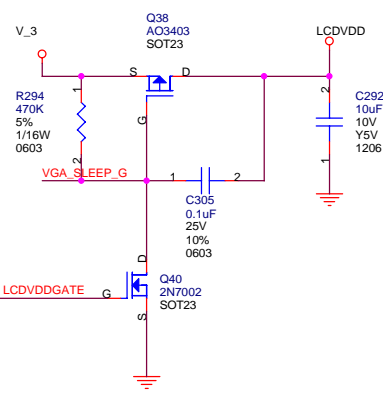
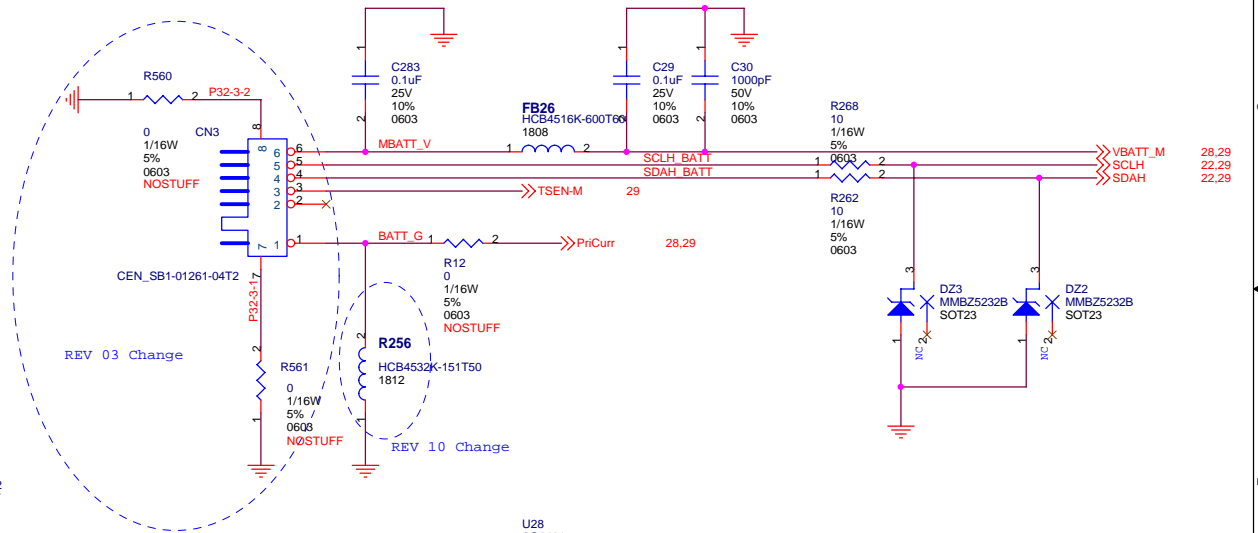
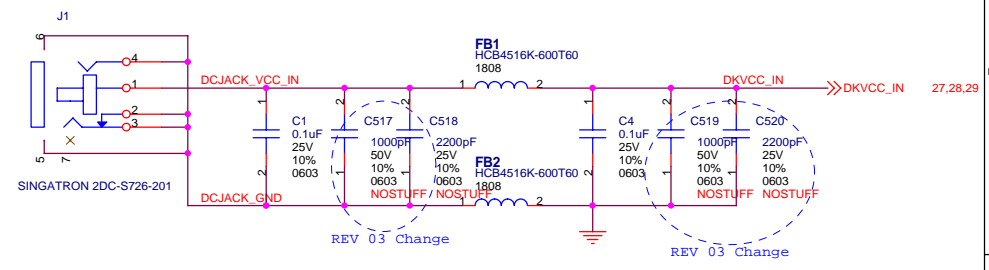
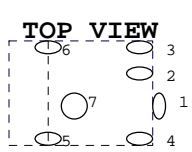
<b>AMTEK SYSTEM CO.,LTD</b>		
Title	Charge & Selector	
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<b>AMTEK SYSTEM CO.,LTD</b>		
Title	MCU Detect circuit	
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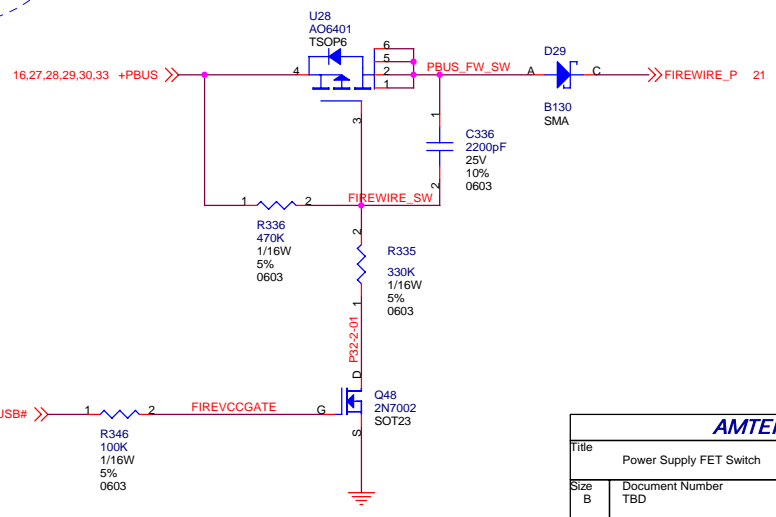


SMI731 ONLY

14 FPVDDEN1

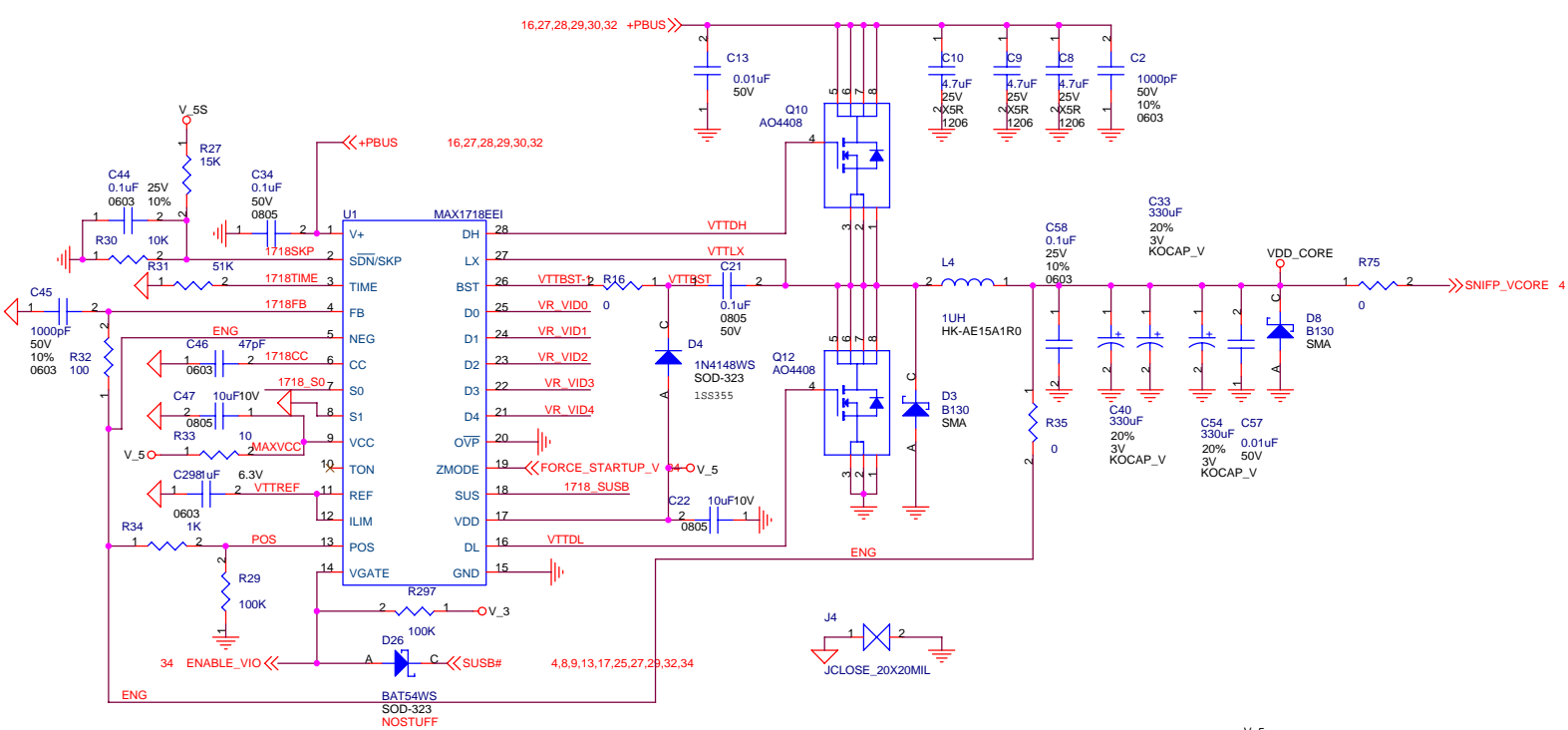
ATI M7 ONLY

14 DIGON

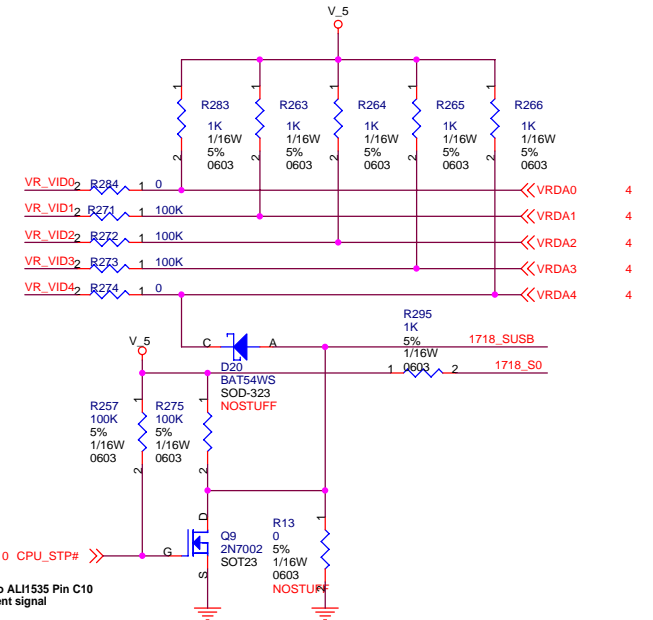


AMTEK SYSTEM CO.,LTD		
Title Power Supply FET Switch		
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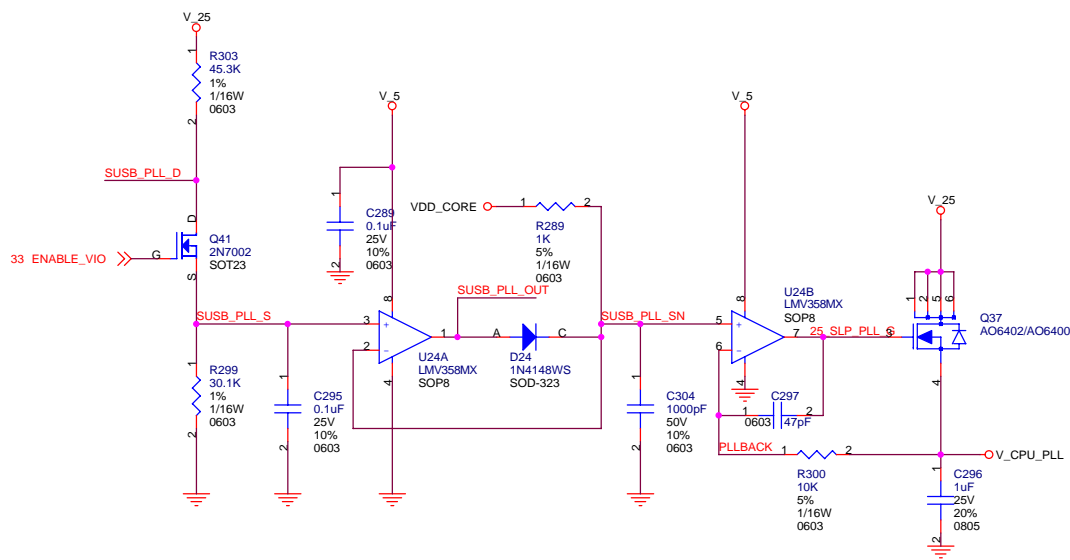
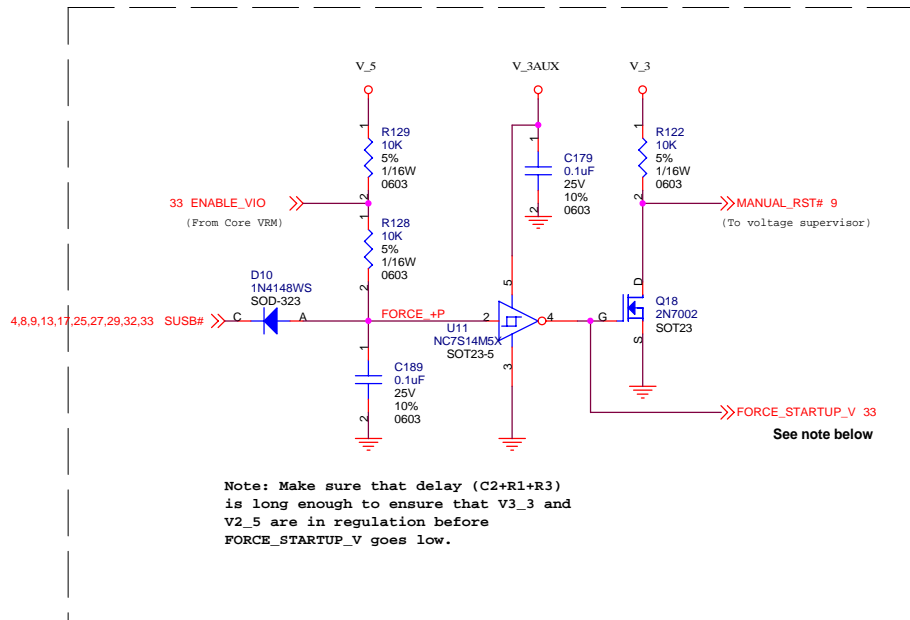




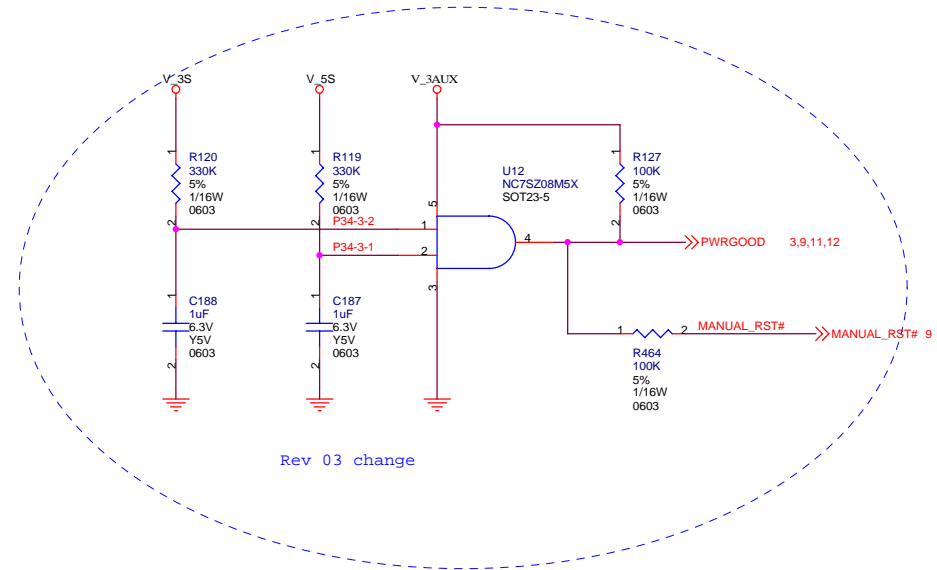
D4	D3	D2	D1	D0	Output Voltage
0	0	0	0	0	1.75V
0	0	0	0	1	1.70V
0	0	0	1	0	1.65V
0	0	0	1	1	1.60V
0	0	1	0	0	1.55V
0	0	1	0	1	1.50V
0	0	1	1	0	1.45V
0	0	1	1	1	1.40V
0	1	0	0	0	1.35V
0	1	0	0	1	1.30V
0	1	0	1	0	1.25V
0	1	0	1	1	1.20V
0	1	1	0	0	1.15V
0	1	1	0	1	1.10V
0	1	1	1	0	1.05V
0	1	1	1	1	1.00V
1	0	0	0	0	0.975V
1	0	0	0	1	0.950V
1	0	0	1	0	0.925V
1	0	0	1	1	0.900V
1	0	1	0	0	0.875V
1	0	1	0	1	0.850V
1	0	1	1	0	0.825V
1	0	1	1	1	0.800V
1	1	0	0	0	0.775V
1	1	0	0	1	0.750V
1	1	0	1	0	0.725V
1	1	0	1	1	0.700V
1	1	1	0	0	0.675V
1	1	1	0	1	0.650V
1	1	1	1	0	0.625V
1	1	1	1	1	0.600V



Connect to ALI1535 Pin C10 or equivalent signal



PLL\_VDD, 1V Minimum Clamping Circuit



<b>AMTEK SYSTEM CO.,LTD</b>		
Title PWRGD & ENABLEVIO Circuit		
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HISTORY:

Rev	Description
0.1	Project Initial
0.2	Change Platform
	Page4 MP5V SMBUS漏電, 將I617路徑分路, 新增R46、R48不上件, 預留接至SB(原路徑); R38、R49上0ohm接至KBC(此因防止MP5V漏電至系統, 間接KBC端, 而不直接接到uP)。
	Page7 1. SDRAM 之I2C改接至SB(U19)。 2. 預留EMI Solution, SDRAM SOCKET(CN8)Pin 145、146 預留電阻(R554、R555 不上件)到GND。
	Page8 EMI有基頻問題, 將Clock Gen(U38)HSS3打開(R532改XNC, R109上10Kohm)。
	Page11 1. uP MP5V漏電, 將EMIT_A和EMIT_B接到SB的線取消, 原SB(U19)R17和R9兩Pin預留電阻(R548、549 不上件)至V_SS。 2. 同上 原SM_ALERT接至SB中間串一DIOE(D39, 上R254WS), 並將SB處(Pin T2) pull-high(R208 上10K)至V_SS。 3. 要使用SB Multi Function Pin, 將LB#改pull-high(R189改XNC, 新增R550 10K 到GND)。 4. 支援uP Flash軟體, 將COM2接至uP(Pin K4為COM2_RXD, Pin K2為COM2_TXD)。
	Page12 RTC(U14)電源限流, 造成Crystal(Y8)不振, 將R163改為0ohm。
	Page16 1. 預留EMI Solution, CN15 Pin15預留電阻(R578, 不上件)到GND, BR-AD3和ENBLT兩訊號增加2200pF(C521、C522)到GND。 2. 增加pin INVERTER線路, 新增CN21(Entry_3802-9), R571(10Kohm)、R572、573(33ohm), C530、531(2200pF)。
	Page17 預留EMI Solution, CN14 Pin69~72各新增一電阻(R496、R542、R556、R557 不上件)到GND。
	Page18 1. HCl Audio測試有問題, 將CN15 Pin2改下AUX_GND, 並將CN9、11之Pin1改以相線接到P837。 2. PCMSPK造成AUDIO噪音, 新增U43(NC7804)將此訊號反向。 3. 機台組裝左右聲道相反, 將CN18、C461、C464與CN20、C462、C463對調。
	Page19 1. USBMIF無準位, 新增電阻(R543)pull-high到V3AUX_USB。 2. USB2.0不會動作, 將J3、J6、J7改成CLOSE。
	Page20 C166零件造成機構干涉, 改成10uF/10V 1206。
0.3	Page21 1394 Plug-IN會造成PBUS瞬間壓降, 在FIREWIRE_P靠P2處加一大電容(C515 上25CV100AX)。
	Page22 1. 同Page4, 將I617之I2C BUS改接KBC端。 2. 新增MicroSoft Speaker一鍵發CTRL+ALT+DEL功能之線路, 新增零件Q62-66(2N7002), R564、R565、R567(100K ohm), R566(10Kohm), C528(1uF/25V 0805), SW6(DTSG1-6)。 3. 快捷鍵的電容造成按鍵動作錯誤將C254-267刪除。 4. 將SM-ALERTpull-high電源修正為V_3, 同KBC電源。
	Page23 1. LED亮度不足, 將D12改pull V_SS, D17、18改pull V_5, D16pin3改pull V_5AUX。 2. 將Suspend LED改成變頻式閃爍, 原Q23改XNC, 新增一組線路, 由uP控制。
	Page24 1. 預留EMI Solution, 將CN17之Pin2~6預留電容(C523-527, 不上件)至GND。 2. Support S3 Digitizer wakeup, Pin7 pull-high V_3(新增R552 10Kohm), Pin8 由RC(新增R551 100Kohm, C516 1uF/6.3V 0603)做REST。
	Page26 EMI預留Solution, CN12 pin 125、126預留電阻(R558、559, 不上件)到GND。
	Page28 1. uP偵測充電電流, 將R291、292上6.2Kohm。 2. 預留uP當機, Charge保護線路, U27週邊線路改變。
	Page29 1. uP SMBUS無準位, 將其pull-high至MP5V(新增R546、R547 上100Kohm)。 2. uP線路修正, 將In pull-high至MP5V(新增R544 上100Kohm); 修正Crystal(Y4)線路(新增R545 100Kohm串於Y4和U30 pin6之間), U30 Reset訊號修正, C347改XNC。 3. AC-IN判斷式會誤動作, R437改為47Kohm, R436改為100Kohm。 4. 電池判斷式不會動作, 修正D26為B2X84-C5V1, R356改上20K。 5. 配合Charge保護線路, 將VBM_SW拉至U27。
	Page30 配合MAX1632線路, 將U3更正為TPRH1204B-100C
	Page32 預留EMI Solution, 新增C517、C518(不上件)並於DCJACK_VCC_IN與DCJACK_GND; 另於P81和P82 pin2間新增C519、C520(不上件); 於CN3 pin7、8預留電阻(R560、R561 不上件)到GND。
	Page34 修正PWRCOOD線路, 以RC和AND 兩產生。
	Page16 1. EMI增加 C532、C533給CN21的電源 2. Hardware strap 訊號改由 SW 設定, 所以R67、R69、R71、R72、R440、R441、R443皆不上。 3. EMI 將 R26、R28 由 33 ohm 改為 bead FCM1608K-601T02
	Page17 EMI將PCMCTIA的Socket連接至GND, 所以R557要上。
1.0	Page18 1. EMI將ACBIT_CLK對地之電容由10pF改為22pF 2. EMI要上C523、C524、C525、C526、C527 (2200pF)
	Page22 1. 將 Q62-Q66 的 d 與 s 極互換 2. 刪除SW6並將訊號改接至SW4, 原本SW4訊號改至SW3並刪除原EMAIL之Hotkey 3. Inverter 改為PWM方式, 故刪除U15、R161、C206及增加R582
	Page24 EMI增加 C534 給 CN17 的 電源
	Page25 1. 增加 CN22 以連接 LAN 訊號至 Docking 2. EMI在RJ11訊號上串接兩個 0 ohm 電阻 ( R580、R581 ) 3. 因MDC漏電問題, 所以C60、C272、C331 由 1000pF 改為 470pF
	Page27 1. 增加 CN22 以連接 LAN 訊號至 Docking 2. 刪除至docking的 PS/2 訊號(keyboard and Mouse) 3. 刪除至docking的 1394 訊號(TPA+2, TPB+2)
	Page29 1. R546、R547 的阻值由 100K 改為 10K 2. S4 wake up power button no light. R349 pull up 電源由 V_3 改為 V_5AUX, 且阻值改成47K, 並加一電阻R579(100K)對地 3. R313 由 17.4K 改為 17.8K 4. 因ODSV/DD3V timing 問題, 所以C529 改為 NOSTUFF
	Page32 EMI將 R256 由 10m ohm 改為 bead HCB4532K-151T50
2.0	Page20 增加EMI fingers FINGER1、FINGER2、FINGER3 給 USB 及 1394 I/O port。
	Page29 1. 修改uP之ACINT判斷線路, 所以刪除R410、R420、C396、Q55、Q57。 2. 修改uP之ACINT判斷線路, 將 R436 由 100K 改為 4.7K。 3. 修改uP之ACINT判斷線路, 將 R437 由 47K 改為 1K。

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