ANALOG DEVICES

CMOS 8/16 Channel Analog Multiplexers

FEATURES
- 44V Supply Maximum Rating
- V_{SS} to V_{DD} Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8V to 16.5V)
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (28mW max)
- Low Leakage (20pA typ)
- Superior Alternative to:
  - DG506A, HI-506
  - DG507A, HI-507

PMI	ADI	SILICONIX	HARRIS
Order P/N Below	Equivalent P/N		
PMADG506AKN	ADG506AKN	DG506ACJ	HI3-0506-5
PMADG506ABQ	ADG506ABQ	DG506ABK	HI1-0506-4
PMADG506AKP	ADG506AKP		HI4P0506-5
PMADG506ATE	ADG506ATE	DG506AAZ	
PMADG506ATE/883	ADG506ATE/883	DG506AAZ/883	HI4-0506/883
PMADG506ATQ	ADG506ATQ	DG506AAK	HI1-0506-2
PMADG506ATQ/883	ADG506ATQ/883	DG506AAK/883	HI1-0506/883
PMADG507AKN	ADG507AKN	DG507ACJ	HI3-0507-5
PMADG507ABQ	ADG507ABQ	DG507ABK	HI1-0507-4
PMADG507AKP	ADG507AKP		HI4P0507-5
PMADG507ATE	ADG507ATE	DG507AAZ	
PMADG507ATE/883	ADG507ATE/883	DG507AAZ/883	HI4-0507/883
PMADG507ATQ	ADG507ATQ	DG507AAK	HI1-0507-2
PMADG507ATQ/883	ADG507ATQ/883	DG507AAK/883	HI1-0506/883

GENERAL DESCRIPTION

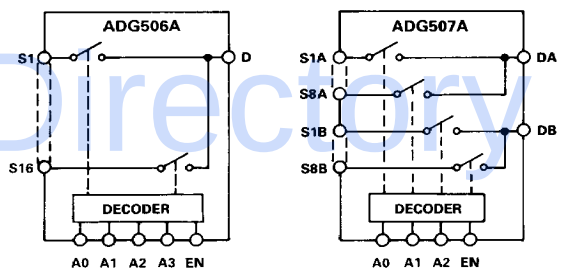
The ADG506A and ADG507A are CMOS monolithic analog multiplexers with 16 channels and dual 8 channels respectively. The ADG506A switches one of 16 inputs to a common output depending on the state of four binary addresses and an enable input. The ADG507A switches one of 8 differential inputs to a common differential output depending on the state of three binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG506A and ADG507A are designed on an enhanced LC²MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Extended Signal Range:
   The enhanced LC²MOS processing results in a high breakdown and an increased analog signal range of V_{SS} to V_{DD}.
3. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

FUNCTIONAL BLOCK DIAGRAMS



ORDERING INFORMATION[1]

Temperature Range and Package		
−40°C to +85°C	−40°C to +85°C	−55°C to +125°C
Plastic DIP	**Hermetic**	**Hermetic**
ADG506AKN	ADG506ABQ	ADG506ATQ
ADG507AKN	ADG507ABQ	ADG507ATQ
PLCC[2]		**LCCC[3]**
ADG506AKP		ADG506ATE
ADG507AKP		ADG507ATE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]PLCC: Plastic Leaded Chip Carrier.
[3]LCCC: Leadless Ceramic Chip Carrier.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

SPECIFICATIONS

Dual Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = −10.8V to −16.5V unless otherwise noted)

	ADG506A ADG507A K Version		ADG506A ADG507A B Version		ADG506A ADG507A T Version			
Parameter	+25°C	−40°C to +85°C	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C	**Units**	**Comments**
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	−10V≤V_S≤+10V, I_{DS} = 1mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15V(±10%), V_{SS} = −15V(±10%)
					300	400	Ω max	V_{DD} = 15V(±5%), V_{SS} = −15V(±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	−10V≤V_S≤+10V, I_{DS} = 1mA
R_{ON} Match	5		5		5		% typ	−10V≤V_S≤+10V, I_{DS} = 1mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 3
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = ±10V, V2 = ∓10V; Test Circuit 4
ADG506A	1	200	1	200	1	200	nA max	
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A only)		25		25		25	nA max	V1 = ±10V, V2 = ∓10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = =0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = ±10V, V2 = ∓10V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF} (EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 7V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		μA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

Single Supply (V_{DD} = +10.8V to +16.5V, V_{SS} = GND = 0V unless otherwise noted)

Parameter	ADG506A ADG507A K Version +25°C	ADG506A ADG507A K Version −40°C to +85°C	ADG506A ADG507A B Version +25°C	ADG506A ADG507A B Version −40°C to +85°C	ADG506A ADG507A T Version +25°C	ADG506A ADG507A T Version −55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	500		500		500		Ω typ	0V ≤ V_S ≤ +10V, I_{DS} = 0.5mA; Test Circuit 1
	700	1000	700	1000	700	1000	Ω max	
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	0V ≤ V_S ≤ +10V, I_{DS} = 0.5mA
R_{ON} Match	5		5		5		% typ	0V ≤ V_S ≤ +10V, I_{DS} = 0.5mA
I_S (OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
	1	50	1	50	1	50	nA max	Test Circuit 2
I_D (OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 3
ADG507A	1	100	1	100	1	100	nA max	
I_D (ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = +10V/0V, V2 = 0V/+10V;
ADG506A	1	200	1	200	1	200	nA max	Test Circuit 4
ADG507A	1	100	1	100	1	100	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG507A only)		25		25		25	nA max	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 5.
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	300		300		300		ns typ	V1 = +10V/0V, V2 = 0V/+10V; Test Circuit 6
	450	600	450	600	450	600	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
t_{OFF} (EN)[1]	250		250		250		ns typ	Test Circuit 8
	450	600	450	600	450	600	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF,
	50		50		50		dB min	V_S = 3.5V rms, f = 100kHz
C_S (OFF)	5		5		5		pF typ	V_{EN} = 0.8V
C_D (OFF)								
ADG506A	44		44		44		pF typ	V_{EN} = 0.8V
ADG507A	22		22		22		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0Ω, V_S = 0V; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
Power Dissipation	10		10		10		mW typ	
		25		25		25	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

TRUTH TABLES

A3	A2	A1	A0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

X = Don't Care

ADG506A

A2	A1	A0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

ADG507A

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Continuous Current, S or D	20mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	40mA
Digital Inputs[1]	
Voltage at A, EN	V_{SS} −4V to V_{DD} +4V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)	
Up to +75°C	470mW
Derates above +75°C by	6mW/°C
Operating Temperature	
Commercial (K Version)	−40°C to +85°C
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

NOTE

[1]Overvoltage at A, EN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

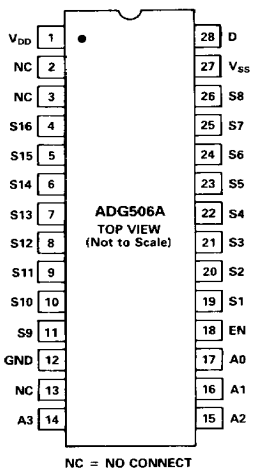
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

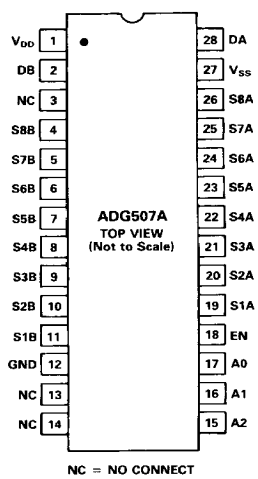
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP

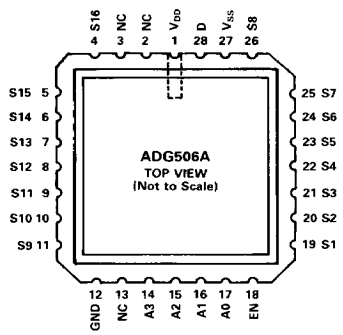


NC = NO CONNECT

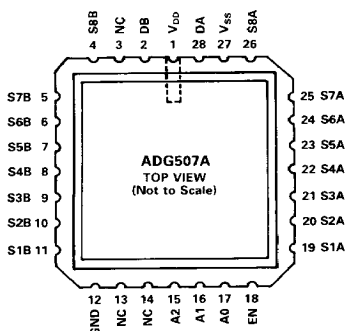


NC = NO CONNECT

LCCC

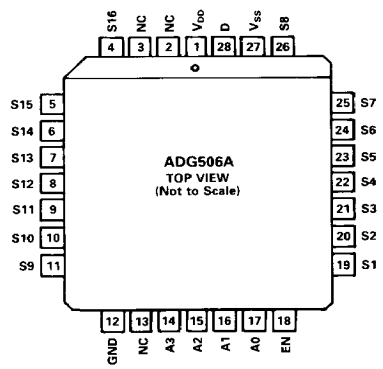


NC = NO CONNECT

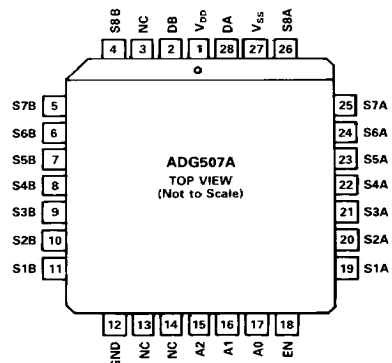


NC = NO CONNECT

PLCC

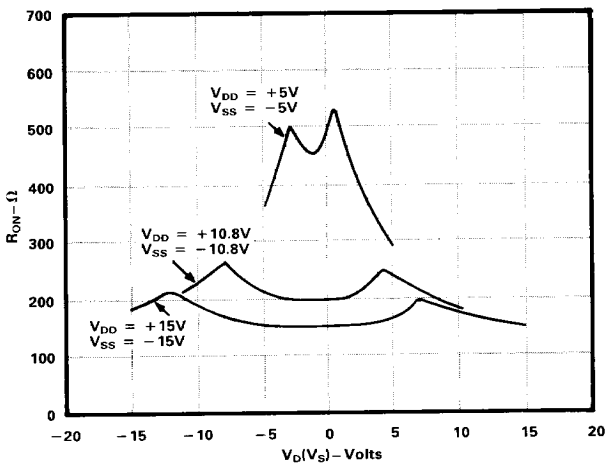


NC = NO CONNECT

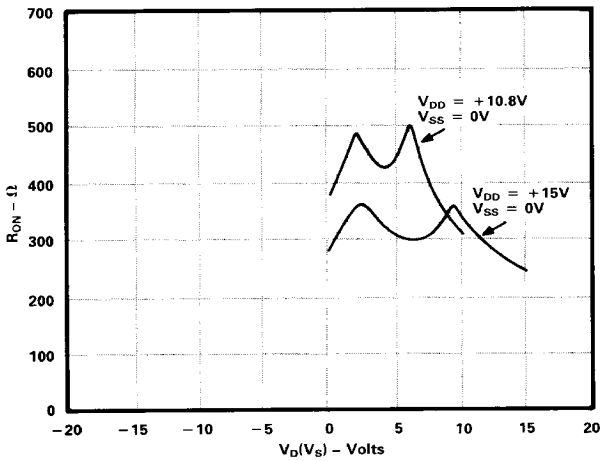


NC = NO CONNECT

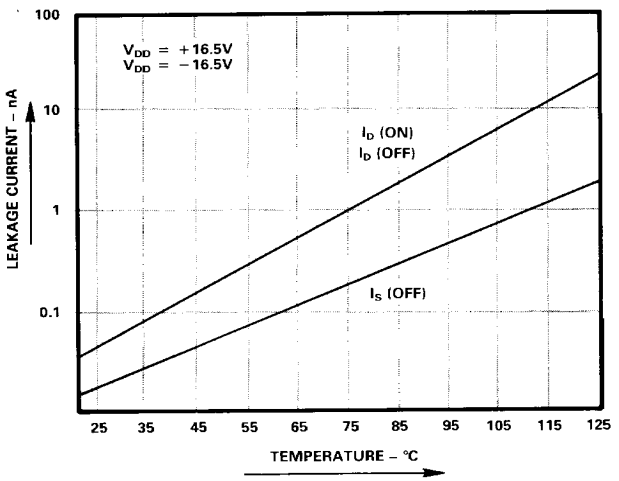
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



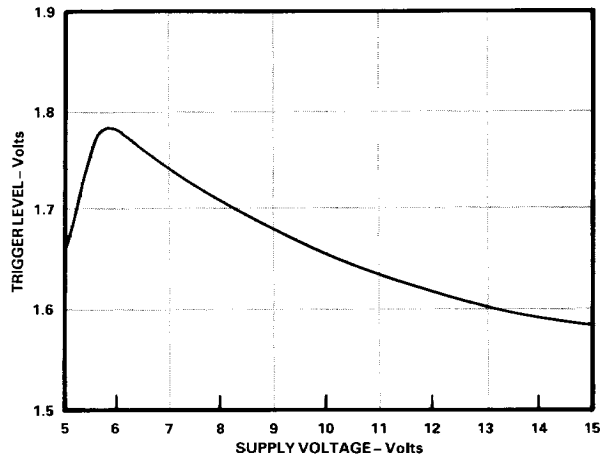
R_{ON} as a Function of $V_D(V_S)$: Dual Supply Voltage, T_A = +25°C



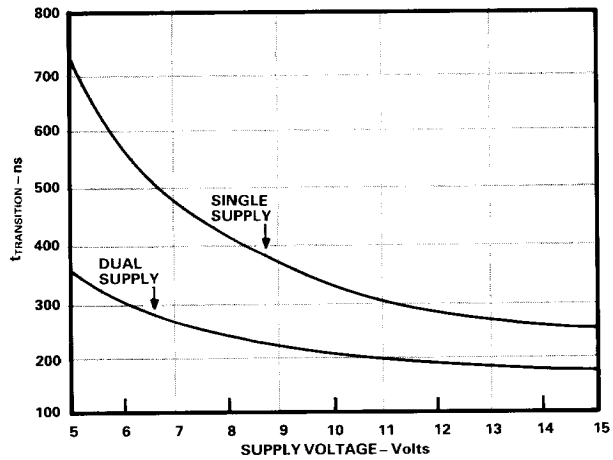
R_{ON} as a Function of $V_D(V_S)$: Single Supply Voltage, T_A = +25°C



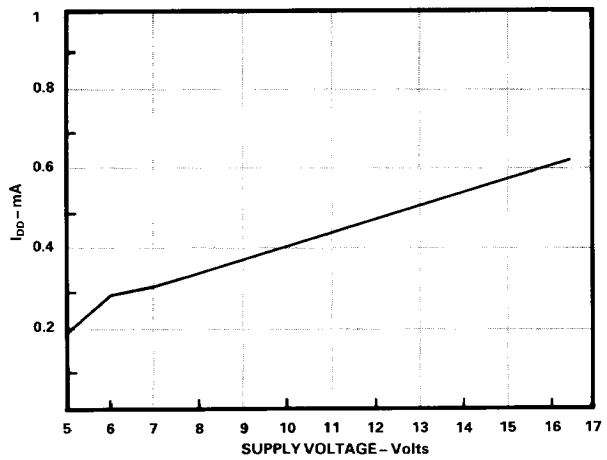
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, T_A = +25°C



$t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, T_A = +25°C (Note: For V_{DD} and $|V_{SS}| < 10V$; V1 = V_{DD}/V_{SS}, V2 = V_{SS}/V_{DD}. See Test Circuit 6)

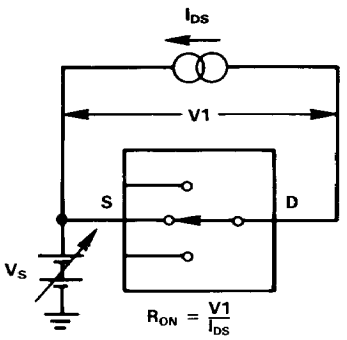


I_{DD} vs. Supply Voltage: Dual or Single Supply, T_A = +25°C

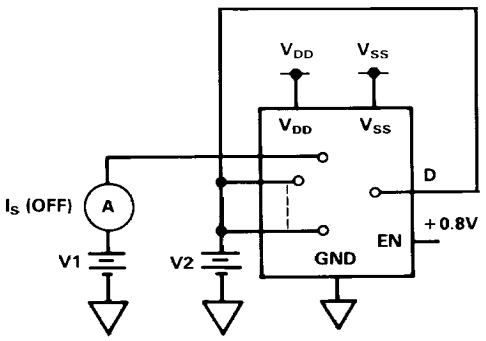
Test Circuits

Note: All Digital Input Signal Rise and Fall Times Measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

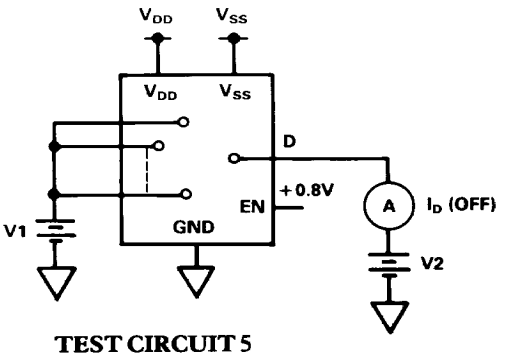
TEST CIRCUIT 1
R_{ON}



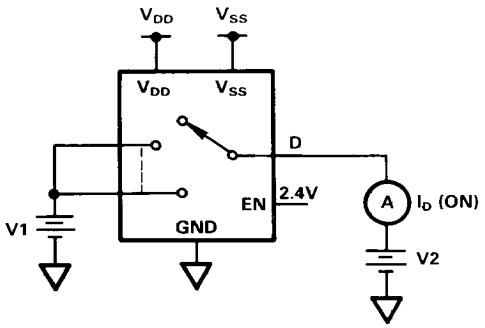
TEST CIRCUIT 2
I_S (OFF)



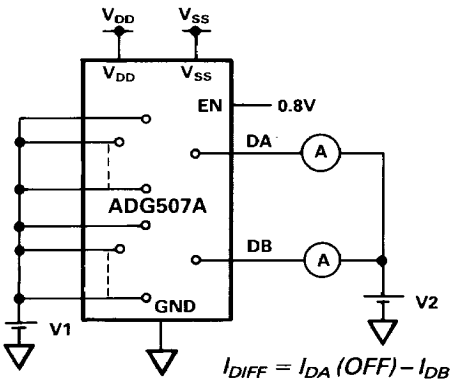
TEST CIRCUIT 3
I_D (OFF)



TEST CIRCUIT 4
I_D (ON)

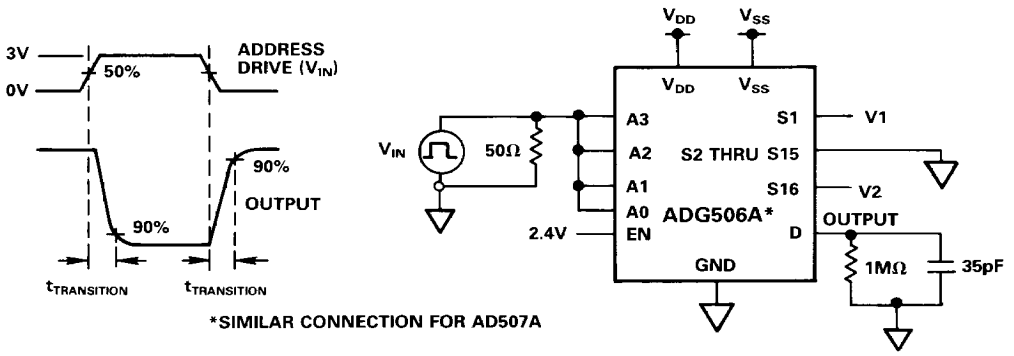


TEST CIRCUIT 5
I_{DIFF}



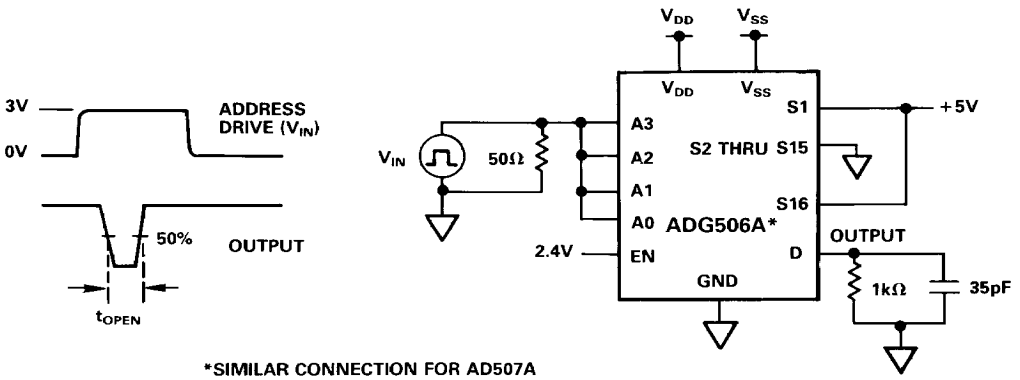
$I_{DIFF} = I_{DA}(OFF) - I_{DB}(OFF)$

TEST CIRCUIT 6
SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$



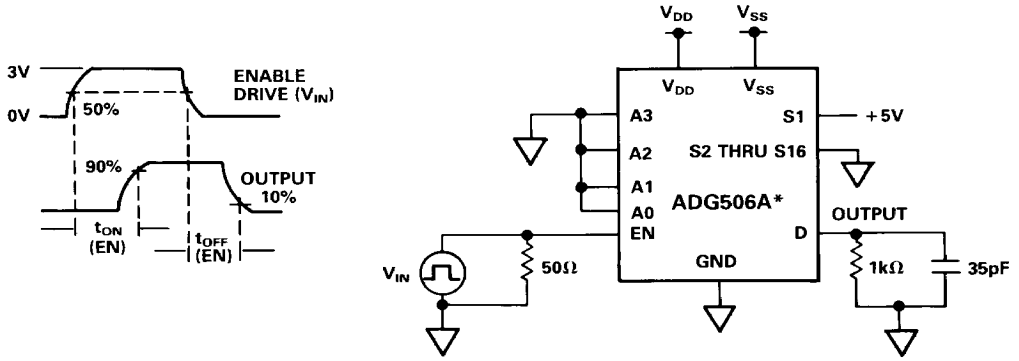
*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 7
BREAK-BEFORE-MAKE DELAY, t_{OPEN}



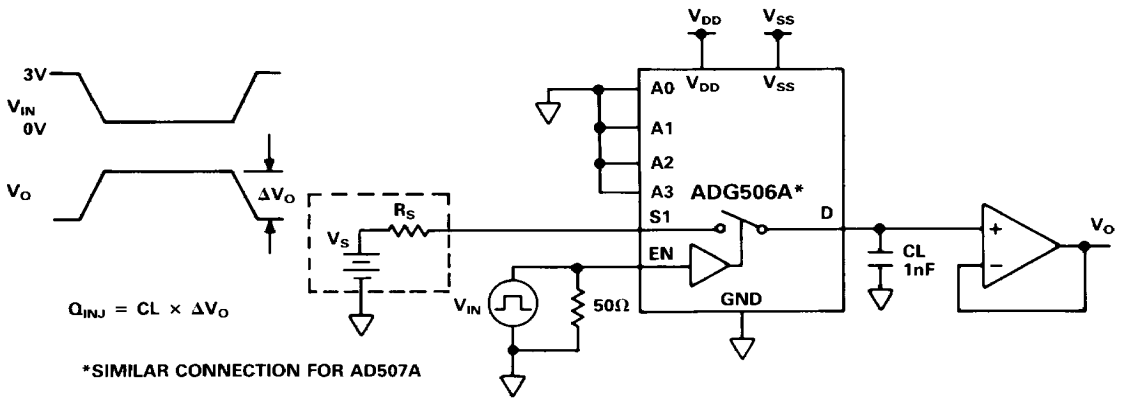
*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 8
ENABLE DELAY, t_{ON} (EN), t_{OFF} (EN)



*SIMILAR CONNECTION FOR AD507A

TEST CIRCUIT 9
CHARGE INJECTION

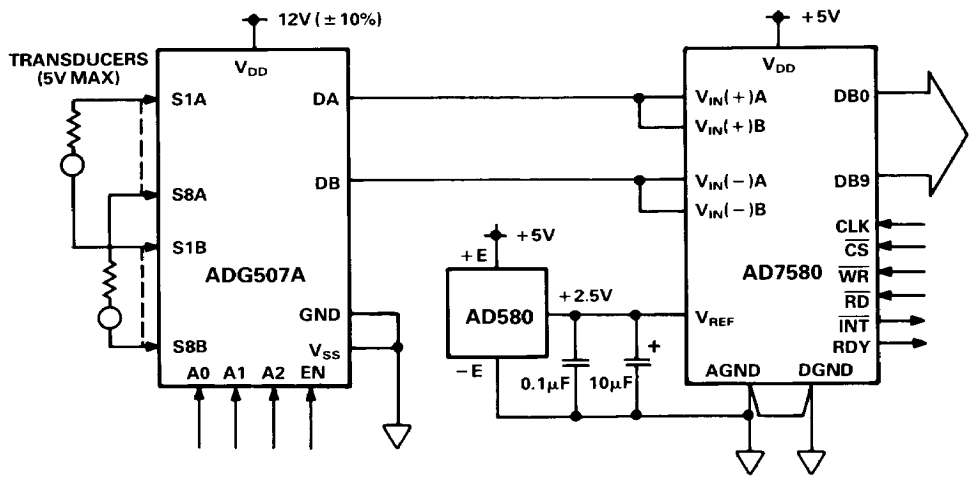


*SIMILAR CONNECTION FOR AD507A

SINGLE SUPPLY AUTOMATIVE APPLICATION

The excellent performance of the multiplexers under single supply conditions makes the ADG506A/ADG507A suitable in applications, such as automotive and disc drives, where only positive power supply voltages are normally available. The following application circuit shows the ADG507A connected as an 8-channel differential multiplexer in an automotive, data acquisition application circuit.

The AD7580 is a 10-bit successive approximation ADC which has an on-chip sample-hold amplifier and provides a conversion result in 20μs. The ADC has a differential analog inputs and is configured in the application circuit for a span of 2.5V over a common-mode range 0 to +5V. Wider common-mode ranges can be accomodated. See the AD7579/AD7580 data sheet for more details. The complete system operates from +12V (±10%) and +5V supplies. The analog input signals to the ADG507A contain information such as temperature, pressure, speed etc.

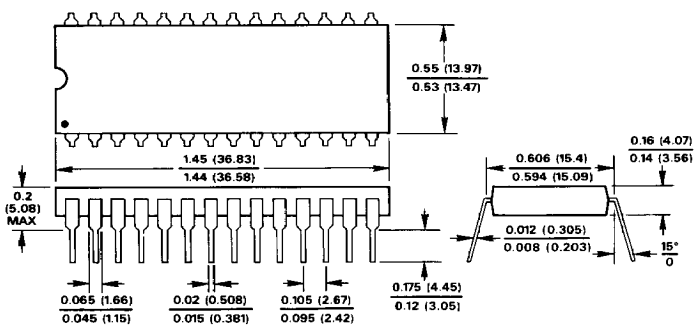


ADG507A in a Single Supply Automotive Data Acquisition Application.

OUTLINE DIMENSIONS

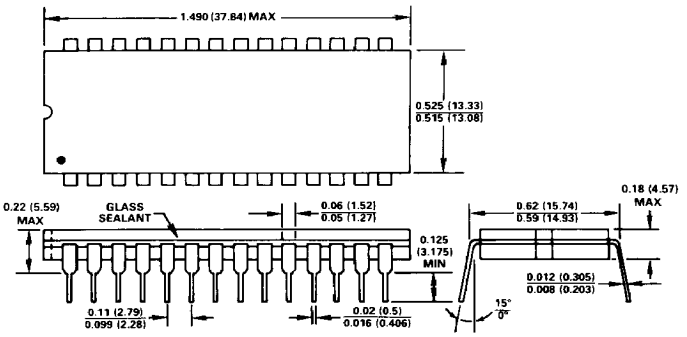
Dimensions shown in inches and (mm).

28-PIN PLASTIC DIP (SUFFIX N)



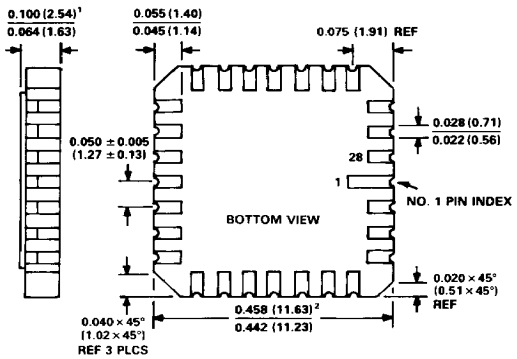
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

28-PIN CERDIP (SUFFIX Q)



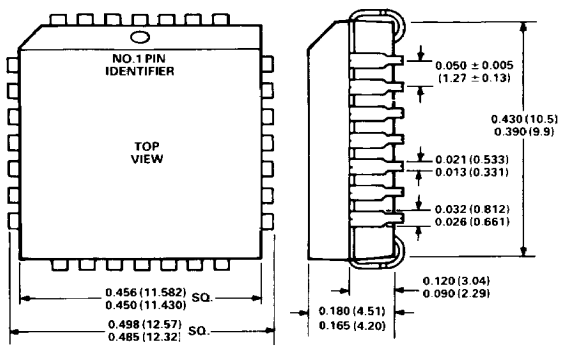
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

28-TERMINAL LEADLESS CERAMIC CHIP CARRIER (SUFFIX E)



NOTES
¹ THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
² APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

28-TERMINAL PLASTIC LEADED CHIP CARRIER (SUFFIX P)



TERMINOLOGY

R_{ON}	Ohmic resistance between terminals D and S
R_{ON} Match	Difference between the R_{ON} of any two channels
R_{ON} Drift	Change in R_{ON} versus temperature
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_S (V_D)	Analog voltage on terminal S or D
C_S (OFF)	Channel input capacitance for "OFF" condition
C_D (OFF)	Channel output capacitance for "OFF" condition
C_{IN}	Digital input capacitance
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF} (EN)	Delay time between the 50% and 10% points of the digital input and switch "OFF" condition
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Maximum input voltage for Logic "0"
V_{INH}	Minimum input voltage for Logic "1"
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

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