Application Note AN-1149

Designing a Wide Range Input Linear Dimming T5/54W Fluorescent Ballast using the IRS2158D

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INTRODUCTION

T5 lamps are popular due to their low profile and high lumen/watt output. These lamps, however, can be more difficult to control due to their higher ignition and running voltages. International Rectifier has one reference design kit dedicated for a dimming application of T5 lamp: the IRPLDIM3. The IRPLDIM3 is a high power factor and wide input voltage range dimming fluorescent ballast, with a fully isolated 0 to 10 V control interface, driving a single T5 28W lamp. The IRPLDIM3 contains an EMI filter, an active power factor correction and a dimming ballast control circuit utilizing the PDIP16 version of the IRS2158D.

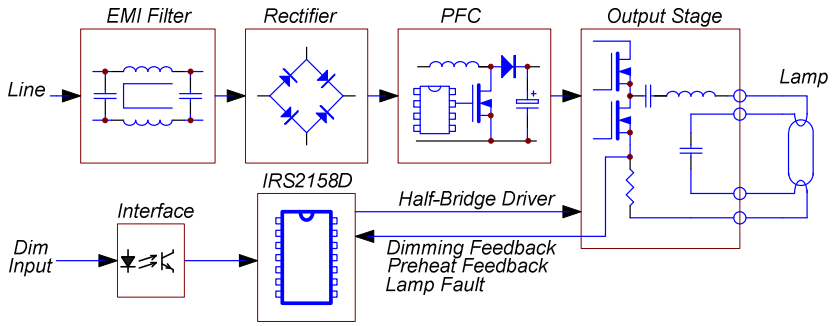


Figure 1: *IRPLDIM3 Block Diagram*

In this application note, we explore the design of a dimming ballast similar to the IRPLDIM3, but for a different wattage lamp, a 54W T5 lamp. The purpose of this note is twofold. First, this note will describe the design process, starting with the Ballast Design Assistant (BDA) software, available for download from the IR website. The BDA software can be used to calculate resonant circuit values, and to generate the schematics and the bill-of-materials. The design process also includes PCB layout consideration, inductor design, and the testing of the ballast. Second, this note will explain, in full detail, the functional description of the ballast, which includes the ballast performance, isolated dimming control interface, different modes of the IC, and the protection features.

DESIGN OF THE BALLAST

BDA Software

The initial step in designing the ballast is to determine values required for the resonant output inductor LRES and capacitor CRES. The *Ballast Design Assistant* (BDA) software, which can be downloaded from the International Rectifier website, is an extremely useful tool in doing this. The BDA software used should be Version 4.2.21 or above, this can be determined by clicking the Help button and clicking *About Ballast Designer.*

The following inputs were selected:

Input	Value
IC	IRS2158D
Input	90 to 265VAC/500VDC
Lamp	T5 54W
Configuration	Single lamp/Voltage mode heating

Using the *Advanced* mode, the next step is to click "*Calculate"*. This displays the operating points for the ballast and calculates the values of the tank components, i.e. LRES = 2.3mH and CRES = 3.3nF.

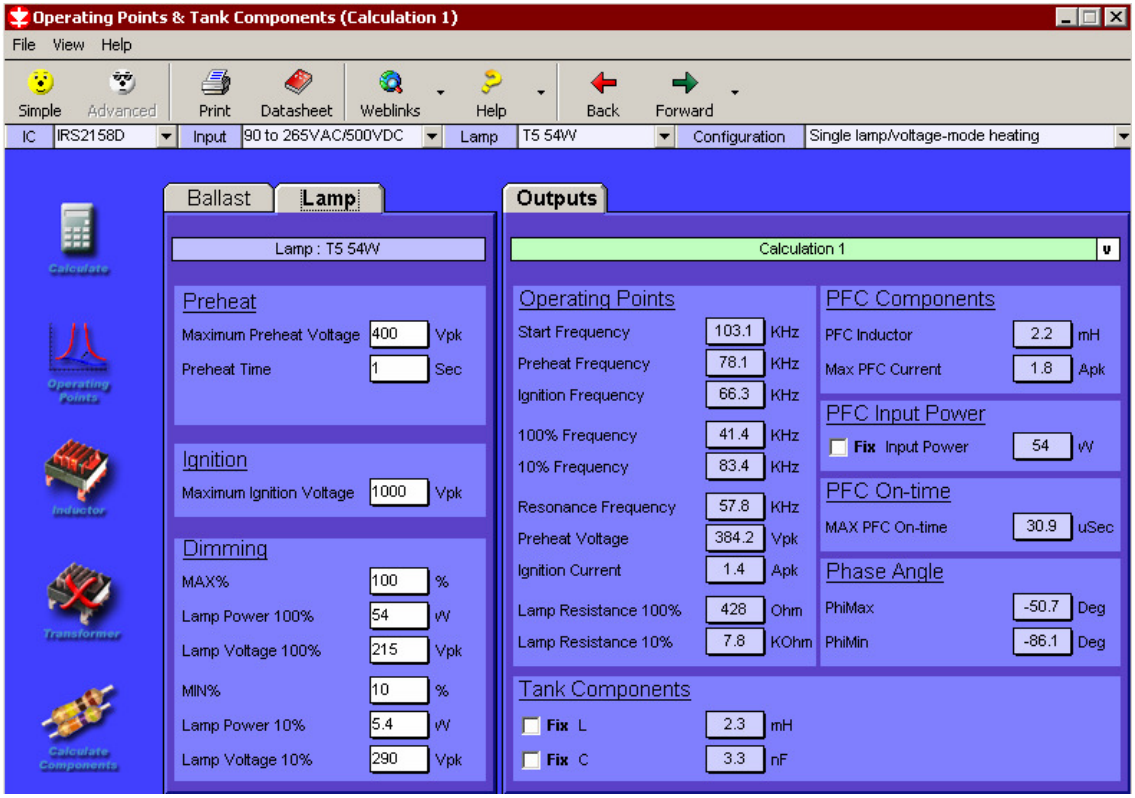


Figure 2: *BDA software window*

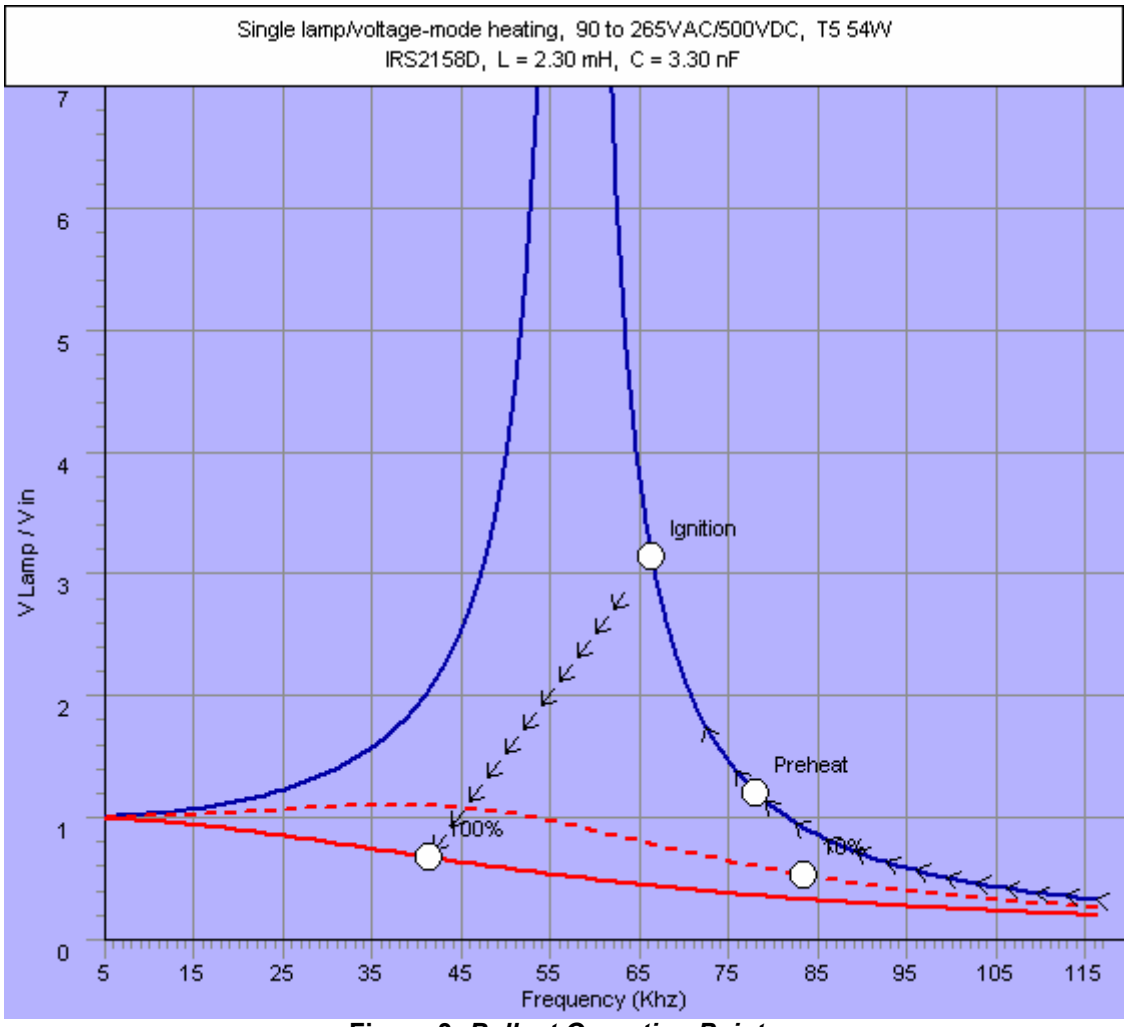


Figure 3: *Ballast Operating Points*

The operating points obtained here display an ideal condition where the ignition frequency is above the run frequency, and the preheat frequency is somewhat higher than the ignition frequency. The run frequency also meets the target of 40 kHz. In general it is preferable to keep the run frequency at 40 kHz or above to avoid possible interference with infra red remote controls, some of which operate at around 35 kHz.

In order to use a more practical value, it was decided to fix LRES at 2 mH for this design, which is more easily available. In the BDA “Tank Components” section the “Fix L” box should be checked and the value of 2.0mH entered in place of 2.3mH. After the “Calculate” button is clicked, the operating point graph is changed to:

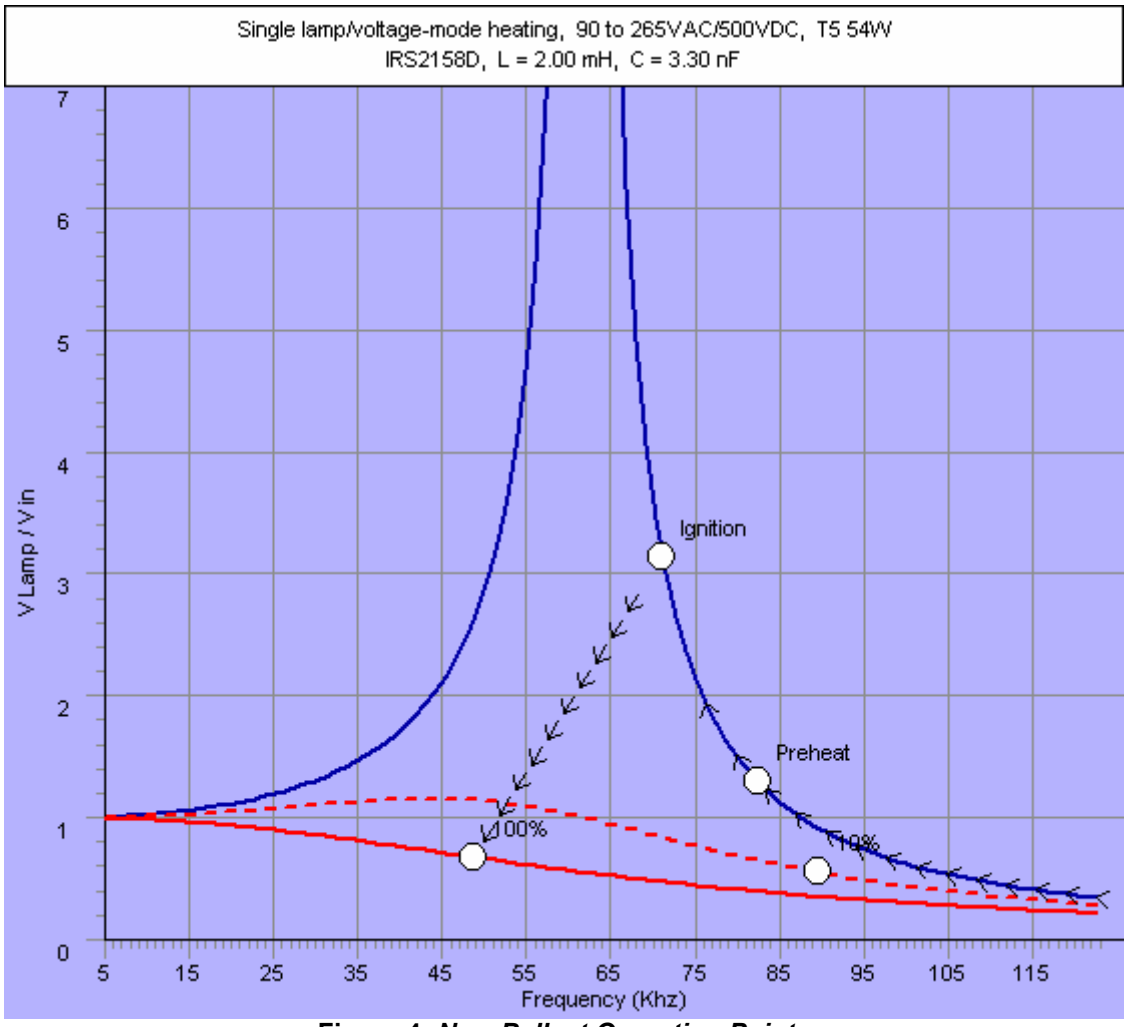


Figure 4: ***New Ballast Operating Points***

The operating points after the change are still ideal as the running frequency is still above 40 kHz, and the ignition frequency is higher than the running frequency. The operating points are as follow:

Operating Points	Value
Preheat Frequency	82.4 kHz
Ignition Frequency	71.1 kHz
Resonance Frequency	62.0 kHz
Run Frequency at 100%	48.7 kHz

After the "*Calculate Components"* is clicked, the BDA software will generate the schematics and the bill-of-materials. The minimum frequency set by CT and RFMIN should be set close to or below the resonance frequency in order to guarantee that the ballast is always capable of producing a high enough output voltage to ignite the lamp. If the minimum frequency is set too far above the resonance frequency, then during ignition the frequency will ramp down to the

minimum frequency and remain there indefinitely. The ballast would not be able to operate correctly as it would never reach a low enough frequency to enable the ignition regulation to function, and would never produce enough voltage at the output, to ignite the lamp.

PCB Layout Considerations

In order to successfully utilize the IRS2158D in a ballast design, it is necessary to follow the following PCB layout guidelines. This can avoid possible interference and ground loop issues that can occur in the ballast circuit. These connection techniques also prevent high current ground loops from interfering with sensitive timing component operation, and allow the entire control circuit to reject common-mode noise due to output switching.

Figure 5 and Figure 6 show the control section of a typical ballast designed around the IRS2158D, where the IC is located in the center. In this design all SMD devices are mounted under the PCB with discrete devices on top.

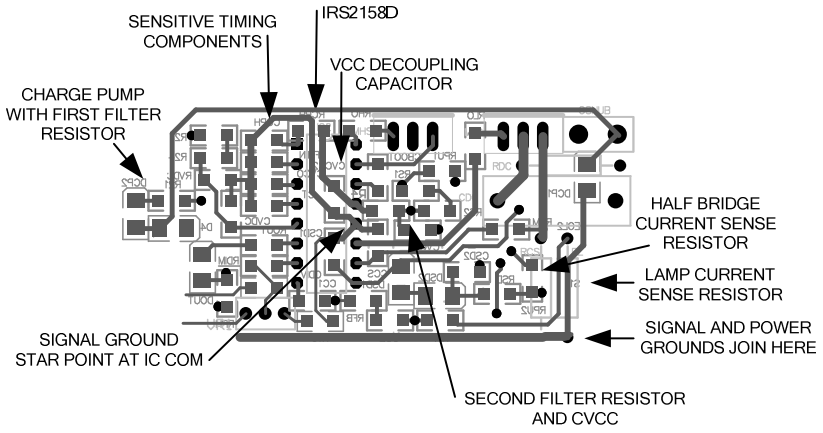


Figure 5: ***Critical traces on the bottom side of the PCB***

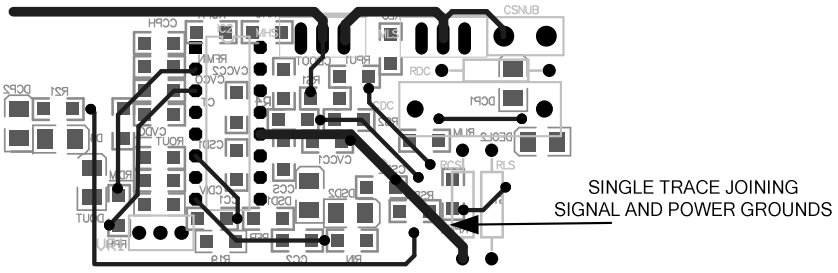


Figure 6: ***Critical traces on the top side of the PCB***

1. The signal ground (pin 12) should only be connected to the power ground at one single point to prevent ground loops from forming.
2. The point described in (1) should be where the grounds of the current sense resistors for both the half bridge MOSFETs and the lamp current feedback both meet.
3. The VCC decoupling capacitor should be placed as close to the IRS2158D VCC (pin 13) and COM (pin 12) as possible with the shortest possible traces.
4. The devices; CPH, RFMIN, CVCO, CT and CCS should all be located as close to the IRS2158D as possible with traces to the relevant pins being as short as possible.
5. The ground connections from the devices listed in (4) should be connected back to the COM pin of the IRS2158D through the shortest possible traces. These should be connected back to the COM pin of the IC without joining the power ground trace at any point. In the example shown above the power ground trace runs along the lower side of the board on the bottom Copper layer
6. The charge pump diode connection to ground should be made to the power ground not the signal ground.
7. The power factor correction section (if used) should be kept apart from the ballast control as shown in the example above. The power factor correction section is at the left side of the PCB.

VCC Double Filter

It is recommended to utilize a double filter arrangement from the charge pump (CSNUB, DCP1 and DCP2) to VCC as shown in the schematic of Figure 7. This circuit is designed to protect the VCC supply pin of the IRS2158D from high peak currents that occur when the MOSFET MHS switches VS from COM to VBUS. DCP2 should be an 18 V rated zener diode and RSUPPLY should connect to the cathode of DCP2. This is to protect the VCC input of the IRS2158D from possible surges and transient voltages.

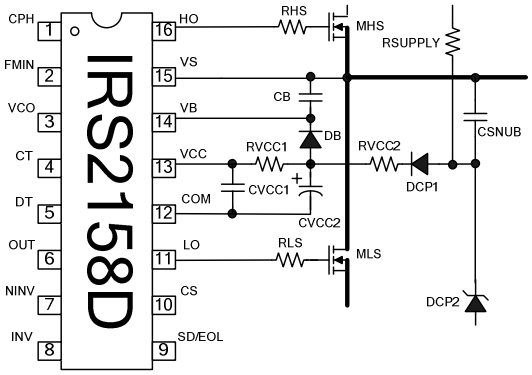


Figure 7: ***VCC Double Filter Arrangement***

Output Inductor Design

The output inductor LRES should be designed to allow a sufficient peak ignition current without saturating. This is important as the ballast will be unable to ignite if it is unable to deliver sufficient voltage at the lamp. The ignition current depends on the type of lamp being used and must be kept to a minimum by ensuring that the cathodes are sufficiently preheated. To minimize eddy current losses in the inductor windings multi-stranded wire should be used. Ferrite cores of sufficiently good quality should also be used to allow a high peak flux density at increased temperature and low core losses. It is important to have a large enough air gap to produce the highest available peak current before allowing the inductor to saturate. If the air gap is too large however, losses can occur because the magnetic field emanating from the gap extends far enough to induce eddy currents in the windings.

When the cores are hot the saturation point and hence the peak current for the inductor will be lower therefore a poorly designed inductor may result in the ballast failing to ignite the lamp during an attempted hot re-strike.

The inductor design process can be greatly simplified by using the Ballast Designer software. For this application it is recommended to fix the core size to EF25.

Lamp Preheating

It is necessary in order to achieve the maximum possible lamp life to heat the cathodes to the correct temperature before ignition. Accelerated deterioration occurs if lamps are ignited when the cathodes are either not sufficiently heated or over heated. The cathode temperature at ignition is determined by the preheat current, which in turn is determined by the preheat frequency through RPH and the preheat time set by CCPH. The correct preheat current can be determined from published data or from International Rectifier's Ballast Designer software.

Cathode Heating after Ignition (Run Mode)

The lamp filament (Cathode) resistance over the range of dimming levels should be between 3 and 5.5 times the resistance when cold. A simple method for determining the hot resistance is to first connect one cathode to a DC power supply via an ammeter and slowly increase the voltage from zero, noting the current at 1 V intervals. This should be done until the cathode can be seen to be glowing red. When this occurs the voltage should not be increased further or the cathode is likely to overheat and become open circuit. With these results, the resistance can be calculated for each voltage and hence the acceptable voltage

range can be found to comply within the 3 to 5.5 times cold resistance limits. The cold resistance can be easily measured with a digital multi-meter (DMM).

When the ballast is running, a true RMS digital voltmeter or differential oscilloscope probe can be connected across the lower cathode and the voltage can be observed at maximum and minimum brightness. The cathode voltage normally increases as the ballast is dimmed. The values of COUT1 and COUT2 plus the resonant output inductor heater windings will control how much. Reducing the capacitance will reduce the amount by which the voltage rises. The COUT1 and COUT2 values should be chosen to prevent the voltage exceeding the upper limit at minimum output to prevent premature end blackening of the lamps and reduced life.

Note that utilizing additional windings on the inductor to provide cathode heating means that power is transferred through the core and consequently the core losses will increase and hence the core operating temperature. The core will reach its highest operating temperature when the ballast is running at minimum brightness.

The component values in this design have been selected for a 54W T5 linear lamp. The circuit will need to be optimized for the particular lamp used to obtain best performance.

Low Voltage Test

After carefully populating the PCB with all the components, a low voltage test can be used to ensure that the ballast will run and preheat at the correct frequency, and to ensure that the IC is not defective before testing it in the high voltage conditions. The run frequency can be measured by supplying the Vcc pin with 15V and the VDC pin with 5.5V to drive the IC out of the UVLO mode. Then the LO-pin waveform can be captured to measure the run frequency of the ballast.

From the BOM generated by the BDA software, CT is 1 nF and RFMIN is 13 kΩ giving a minimum frequency of approximately 51 kHz and a dead time of 1.5 µs.

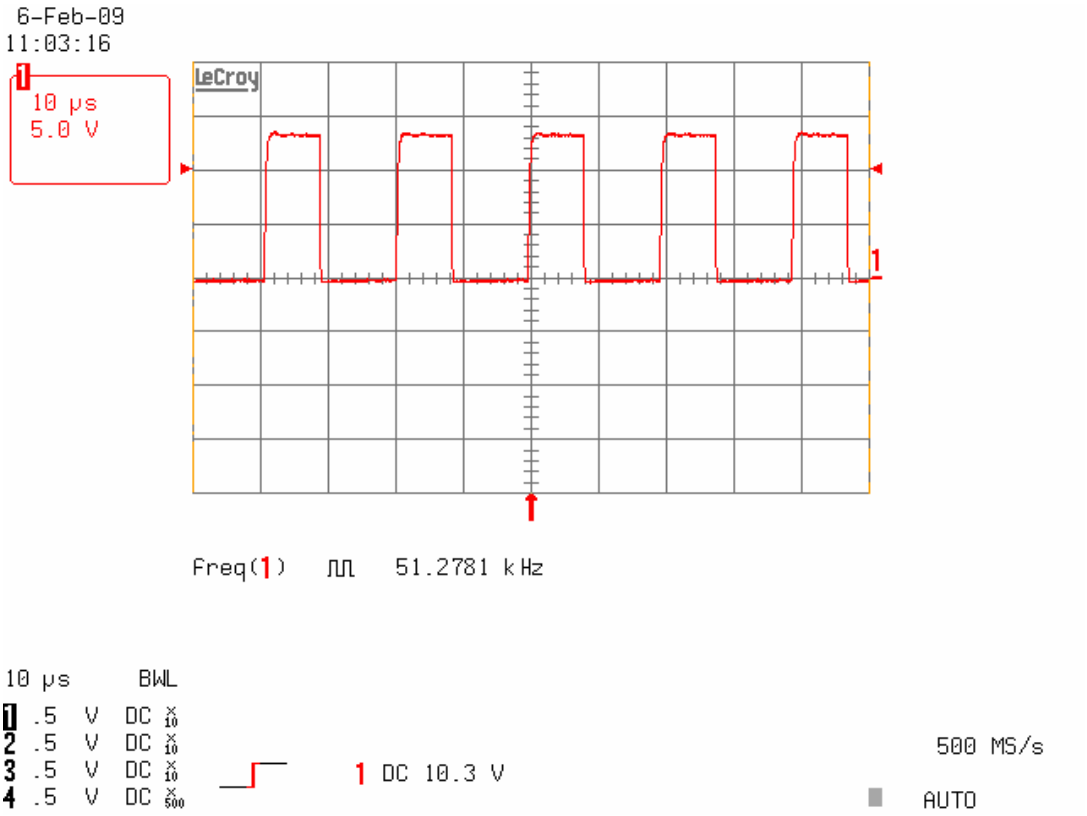


Figure 8: ***Run Frequency***

The minimum frequency is a little too high since the target run frequency is 48 kHz. When running at higher frequency, the power delivered to the lamp can be too low. The minimum frequency can be reduced by using a higher value of RFMIN. Using RFMIN of 15 kΩ sets the minimum frequency to 44 kHz.

The value of RPH sets the preheat frequency and has been determined by BDA software to be 15 kΩ. To measure the preheat frequency, the LO-pin voltage waveform has to be captured in the PREHEAT mode. This can be done by using the CPH-pin voltage as a trigger signal when capturing the waveform.

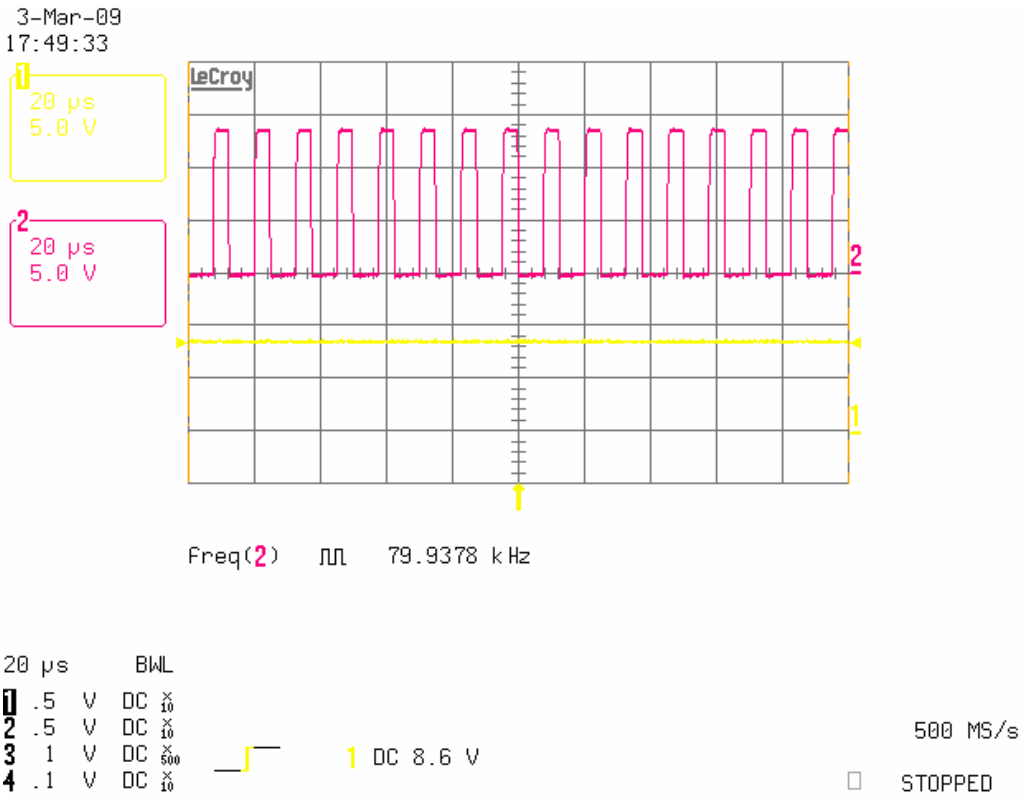


Figure 9: ***Preheat Frequency***

Fine Tuning Circuit

Often times, the design must be fine-tuned after it is tested at high voltage. Since the minimum frequency is now slightly below the run frequency, it is important to set the maximum lamp output in order to prevent over-driving the lamp. The value of the lamp current sensing resistor RLS will determine the feedback voltage provided to the op-amp feedback circuit of the IRS2158D. RLS is chosen to be as large as possible, to produce a sufficient feedback voltage, without dissipating too much power. A value of 10 Ω given by the BDA software is ideal to produce an average feedback voltage of 1.5 V when the lamp current is at its maximum value of 300 mA (RMS).

In this particular design, the glowing filament at the minimum output was observed. This shows that the cathode voltage increase excessively during dimming. To mitigate this, the values of COUT1 and COUT2 were changed from the original values generated by the BDA, 100nF, to 47nF.

These formulas may be useful when fine-tuning the circuit:

1) Program Deadtime

The deadtime is programmed with the timing resistor RDT at the DT pin. The deadtime is given by:

$$t_{DT} = 1500 \cdot C_T \quad \text{[Seconds]} \quad (1)$$

$$C_T = \frac{t_{DT}}{1500} \quad \text{[Farads]} \quad (2)$$

2) Program Run Frequency

The run frequency is programmed with the timing resistor RMIN at the FMIN pin. The run frequency is given as:

$$f_{OSCRUN} = \frac{1}{2.15 \cdot C_T \cdot \left(\frac{3}{5} \cdot R_{MIN} + 1500\right)} \quad \text{[Hz]} \quad (3)$$

$$R_{MIN} = \frac{5}{3} \cdot \left(\frac{1}{(2.15 \cdot f_{OSCRUN} \cdot C_T)} - 1500\right) \quad \text{[Ohms]} \quad (4)$$

3) Program Preheat Frequency

The preheat frequency is programmed with timing resistors RMIN and RPH. The timing resistors are connected in parallel for the duration of the preheat time. The preheat frequency is therefore given as:

$$f_{OSCPH} = \frac{1}{2.15 \cdot C_T \cdot \left(\frac{3}{5} \cdot \frac{(R_{MIN} \cdot R_{PH})}{(R_{MIN} + R_{PH})} + 1500\right)} \quad \text{[Hertz]} \quad (5)$$

4) Program Preheat Time

The preheat time is defined by the time it takes for the external capacitor on pin CPH to charge up to 2/3*VCC. An external resistor (RCPH) connected to VCC charges capacitor CPH. The preheat time is therefore given as:

$$t_{PH} = R_{CPH} \cdot C_{PH} \quad \text{[Seconds]} \quad (6)$$

or

$$C_{PH} = \frac{t_{PH}}{R_{CPH}} \quad \text{[Farads]} \quad (7)$$

5) Program Ignition Ramp Time

The preheat time is defined by the time it takes for the external capacitor on pin VCO to charge up to 5V. The external timing resistor (RPH) connected to FMIN charges capacitor CVCO. The ignition ramp time is therefore given as:

$$t_{RAMP} = R_{PH} \cdot C_{VCO} \quad \text{[Seconds]} \quad (8)$$

or

$$C_{VCO} = \frac{t_{RAMP}}{R_{PH}} \quad \text{[Farads]} \quad (9)$$

6) Program Maximum Ignition Current

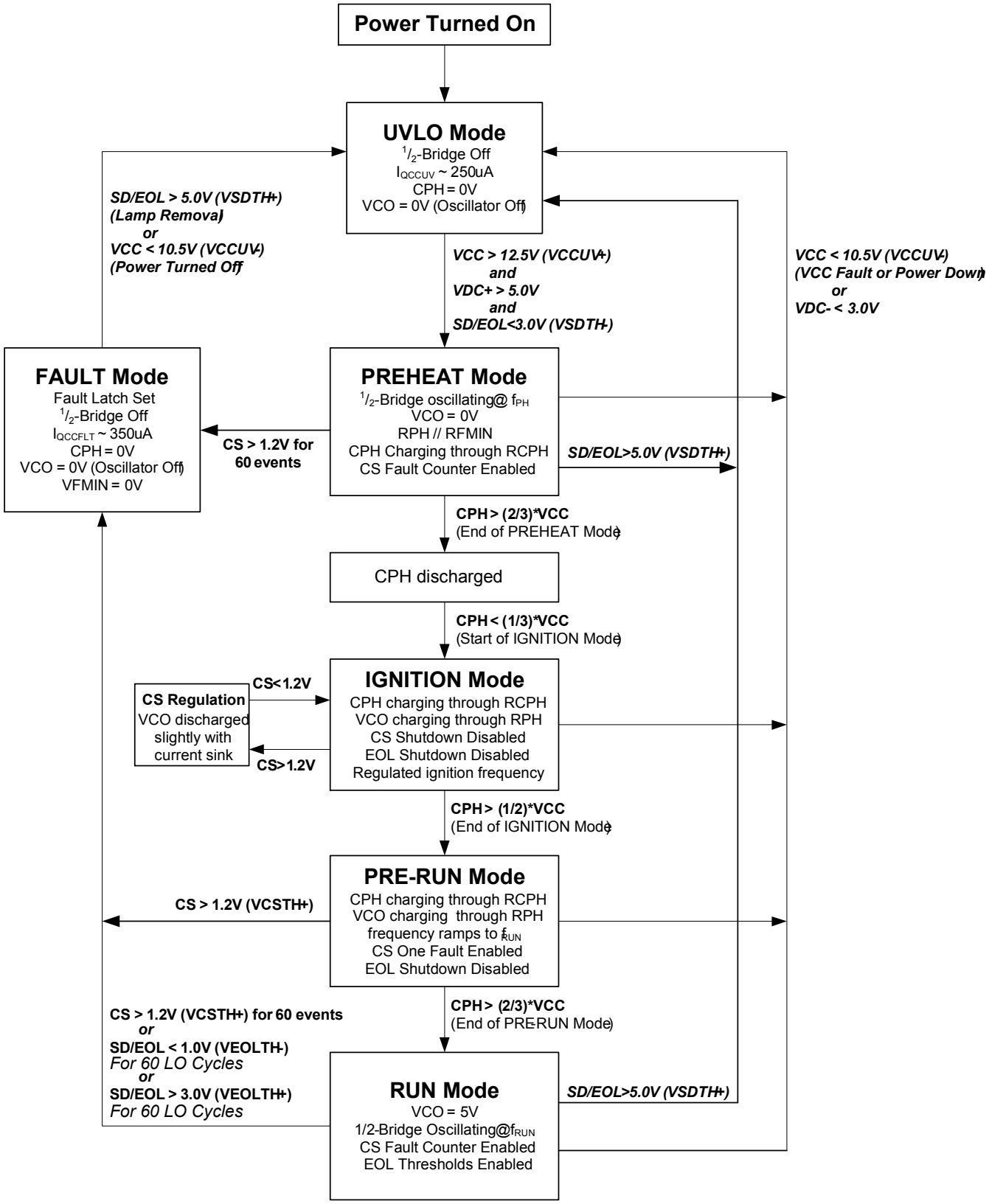
The maximum ignition current is programmed with the external resistor RCS and an internal threshold of 1.2V. This threshold determines the over-current limit of the ballast, which will be reached when the frequency ramps down towards resonance during ignition and the lamp does not ignite. The maximum ignition current is given as:

$$I_{IGN} = \frac{1.2}{R_{CS}} \quad \text{[Amps Peak]} \quad (10)$$

or

$$R_{CS} = \frac{1.2}{I_{IGN}} \quad \text{[Ohms]} \quad (11)$$

IRS2158D State Diagram



Schematics

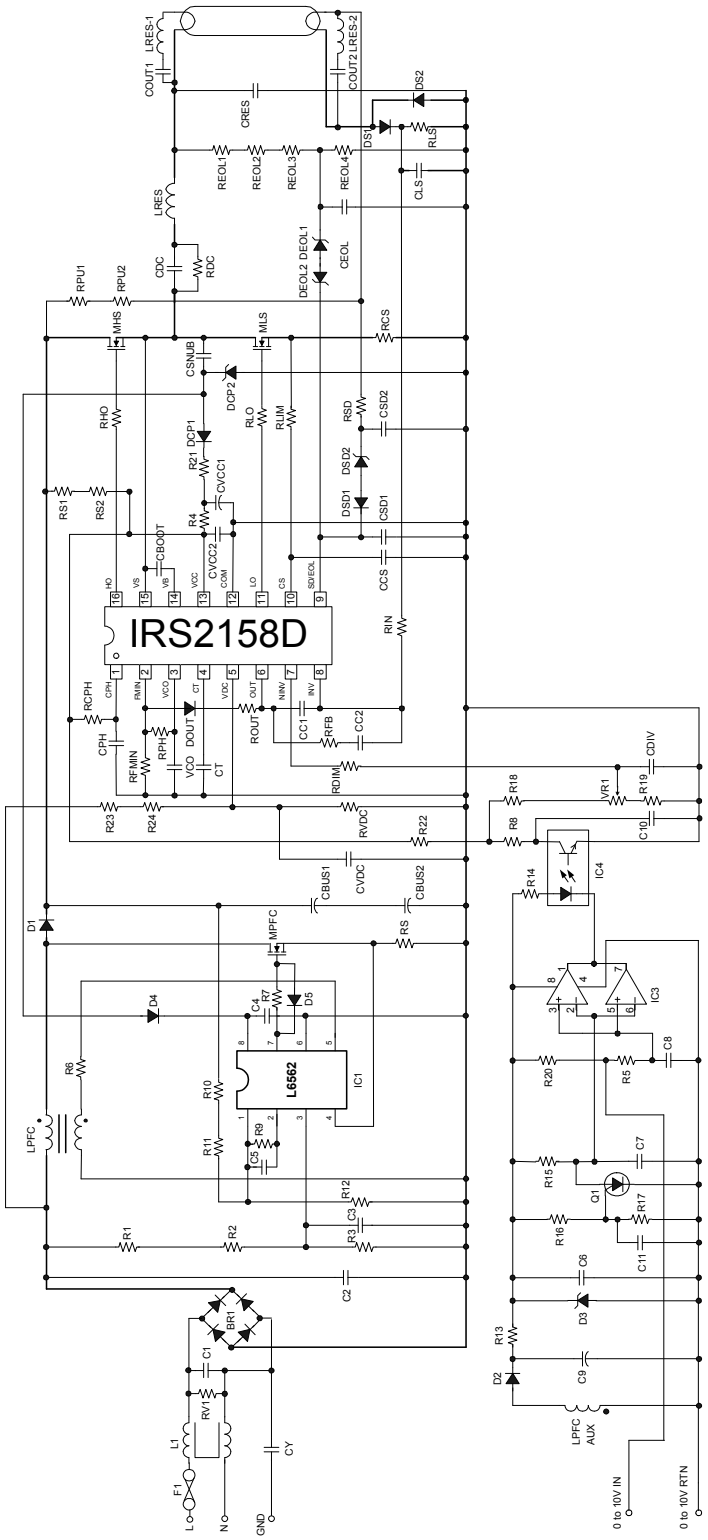
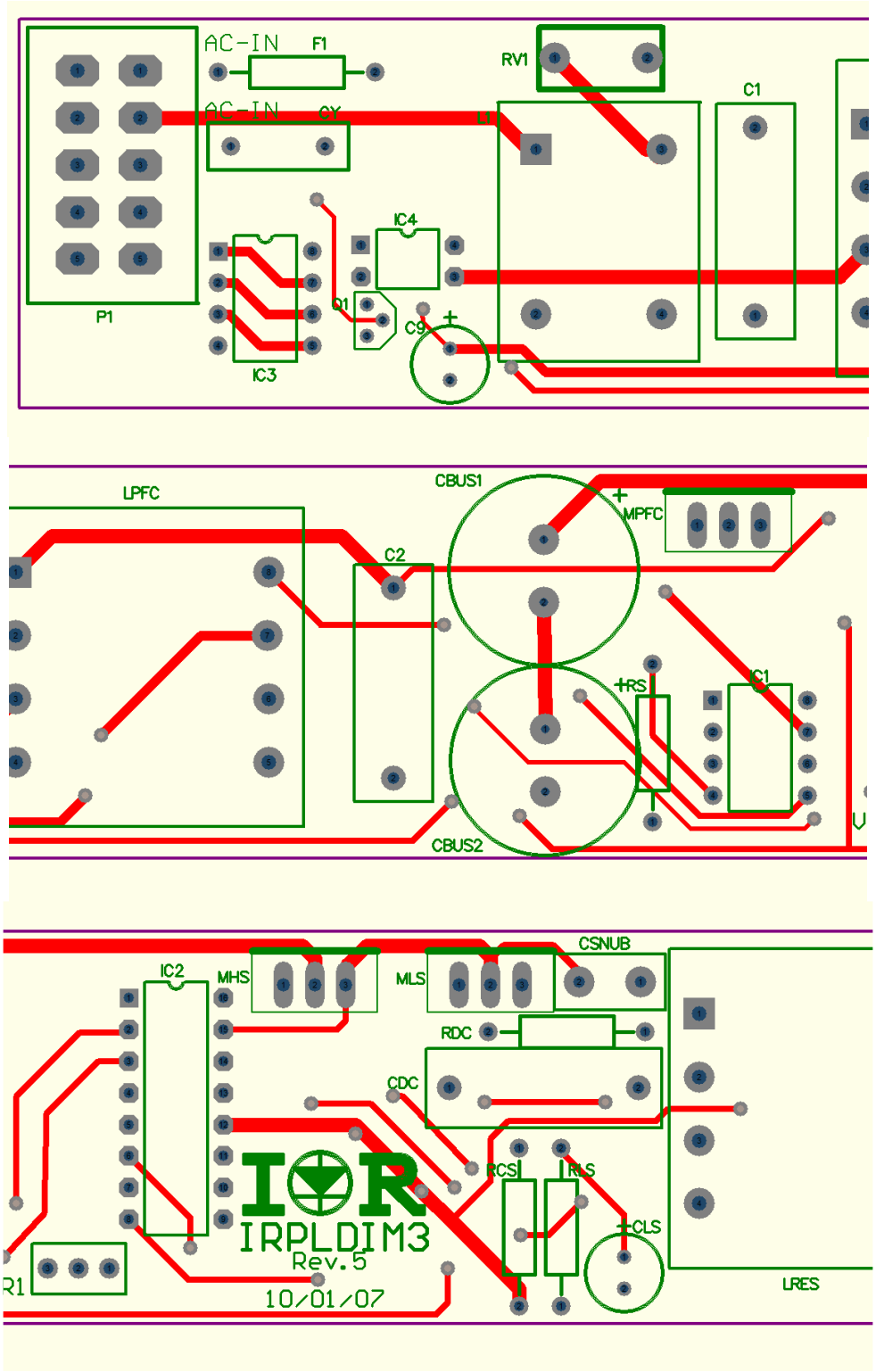


Figure 10: ***Schematics***

PCB Component Placement Diagram and Board Fabrication



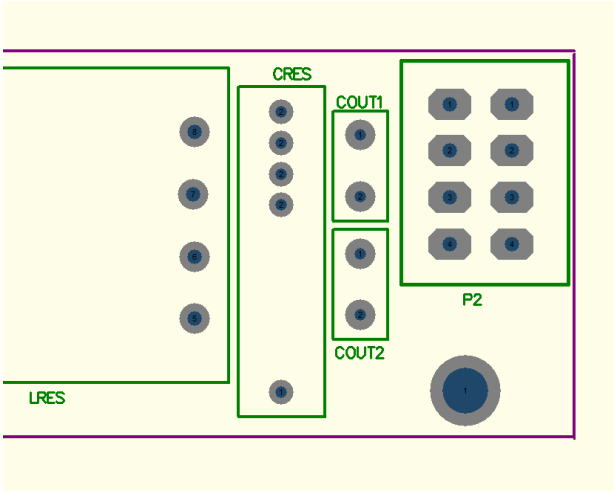
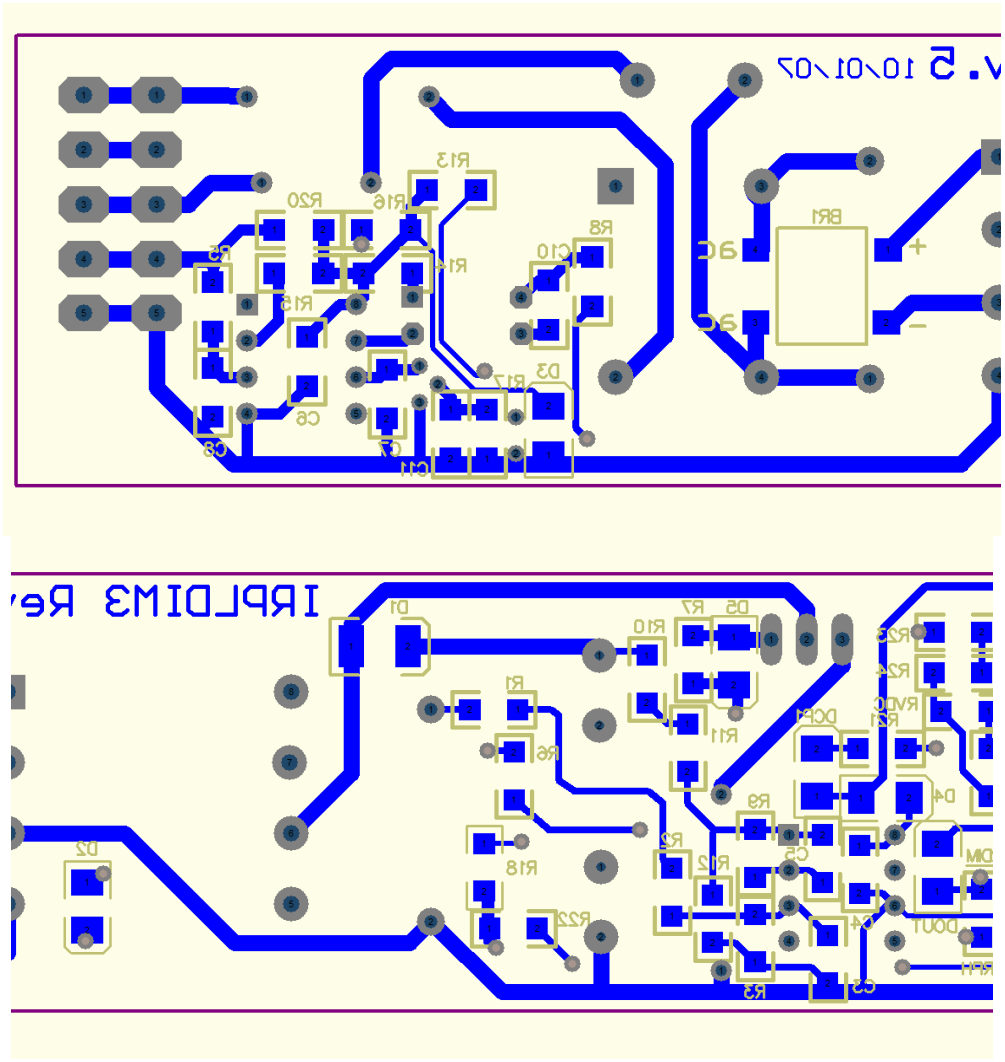


Figure 11: ***Top Layer***



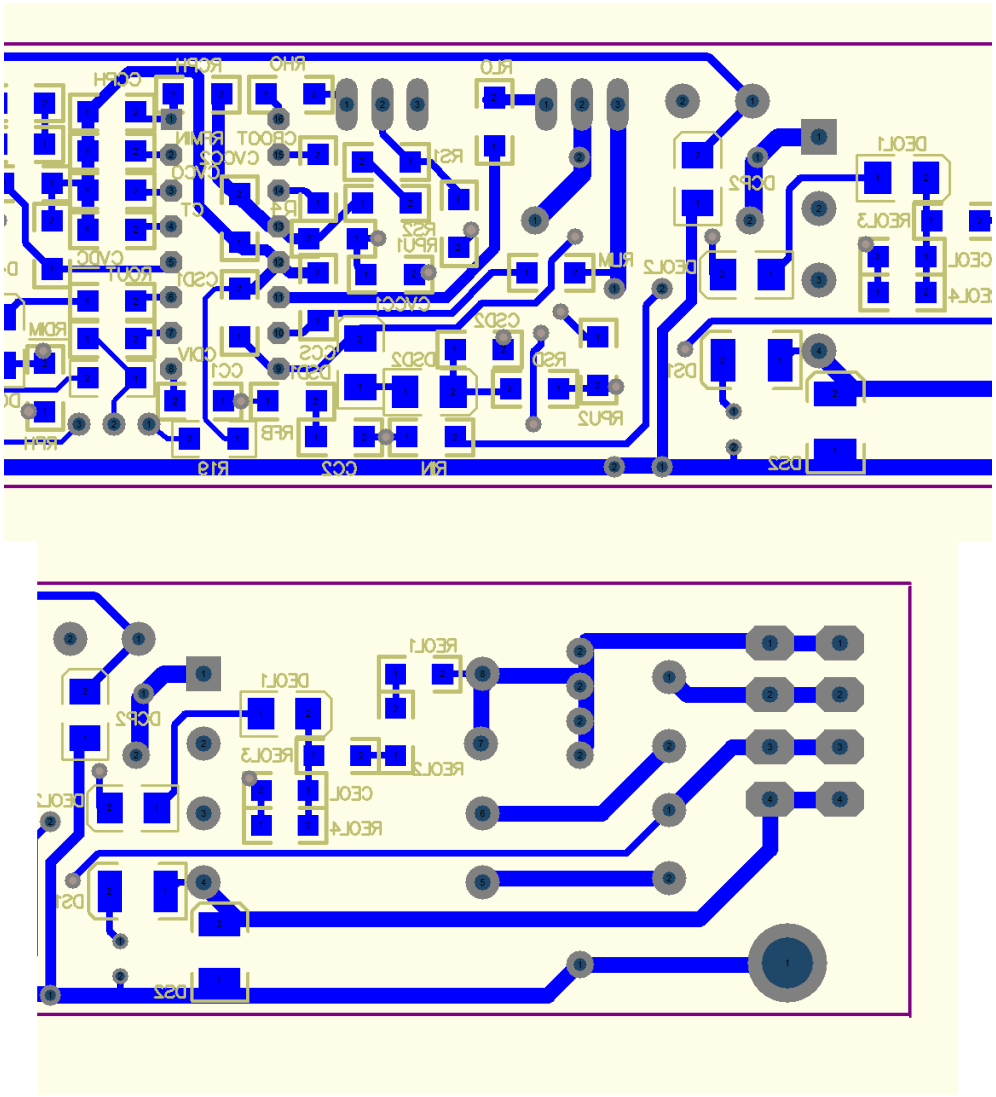


Figure 12: ***Bottom Layer***

Bill of Material and Inductor Specification

Item	Qty	Manufacturer	Part Number	Description	Reference
1	1	ST Microelectronics	L6562N	PFC Control IC	IC1
2	1	International Rectifier	IRS2158D	Ballast Control IC	IC2
3	1	ST Microelectronics	LM393N	Dual Comparator IC	IC3
4	1	Panasonic	CNC1S101	Opto Isolator	IC4
5	1	ON Semiconductor	2N6027RLRAG	Programmable Unijunction Transistor	Q1
6	2	International Rectifier	IRFU840	N-MOSFET	MHS, MLS
7	1	IR / Vishay	IRFB9N60A	Transistor, MOSFET	MPFC
8	1	Fairchild Semiconductor	DF10S	Bridge Rectifier	BR1
9	6	Diodes Inc	LL4148-13	Diode	DCP1, DOUT, DSD1, D2, D4, D5
10	1	Diodes Inc	ZMM5236B-7	Zener Diode 7V5	DEOL1
11	1	Diodes Inc	ZMM5231B-7	Zener Diode 5V1	DEOL2
	2	Diodes Inc	ZMM5248B-7	Zener Diode 18V	D3, DCP2
12	1	Diodes Inc	ZMM5242B-7	Zener Diode 12V	DSD2
13	3	Diodes Inc	US1J-13-F	Diode	DS1, DS2, D1
14	1	Panasonic-ECG	ELF-15N007A	Common mode Choke	L1
15	1	Vogt Electronics		PFC Inductor, 2mH	LPFC
16	1	Vogt Electronics	IL 060 320 51 01	Resonant Inductor, 2mH, 2A peak	LRES
17	1	Epcos	B32922A2224M	Capacitor 220nF, 305VAC	C1
18	1	BC Components	2222 338 14104	Capacitor 100nF, 440V	C2
19	1	Panasonic-ECG	ECU-V1H103KBM	Capacitor 10n, 50V, 1206	C3
20	2	Panasonic-ECG	ECJ-3YX1C106K	Capacitor 10u, 16V, 1206	C4, C6
21	1	Panasonic-ECG	ECJ-3VB1C684K	Capacitor 0.68µF, 16V, 1206	C5
22	5	Panasonic-ECG	ECJ-3VB1C104K	Capacitor 100n, 16V, 1206	C11, CBOOT, CC2, CSD2, CVCC2
23	1	Panasonic-ECG	ECU-V1H333KBM	Capacitor 33nF, 50V, 1206	C7
24	3	Panasonic-ECG	ECJ-3YB1C105K	Capacitor 1µF, 16V, 1206	C8, CDIV, CVDC
25	2	Panasonic-ECG	ECA-2EHG470	Capacitor, 47µF, 250V, 105C	CBUS1, CBUS2
26	2	Panasonic-ECG	ECJ-3YB1C225K	Capacitor 2.2µF, 25V, 1206	CVCC1, CCPH
27	1	Panasonic-ECG	EEU-FC1H470	Capacitor 47µF, 50V, 105C	C9
28	1	Panasonic-ECG	ECU-V1H471KBM	Capacitor, 470pF, 50V, 1206	CCS
29	1	Panasonic-ECG	ECQ-E6104KF	Capacitor, 100nF, 630V	CDC
30	2	Panasonic-ECG	ECJ-3VB1C474K	Capacitor, 0.47µF, 16V, 1206	CEOL, CSD1
31	1	Kemet	T356D226K006AS	Capacitor, 22µF, 6.3V, Tantalum	CLS
32	2	WIMA	MKS2 Series	Capacitor, 47nF, 400V	COUT1, COUT2
33	1	Panasonic-ECG	ECW-H16332HL	Capacitor, 3.3nF, 1600V	CRES
34	1	Panasonic-ECG	ECK-A3A102KBP	Capacitor, 1nF, 1 kV, Radial	CSNUB
35	2	Panasonic-ECG	ECJ-3YC2D102J	Capacitor, 1nF, 200V, 1206, NPO	CT, C10
36	1	Panasonic-ECG	ECJ-3YB2A223K	Capacitor, 1uF, 25V, 1206	CVCO
37	1	Panasonic-ECG	ECJ-3VC2A222J	Capacitor, 2.2nF, 100V, 1206, NPO	CC1
38	1	TDK	CS13-E2GA332MYGS	Capacitor, 3.3nF, Y	CY
39	2	Panasonic-ECG	ERJ-P08J684V	Resistor, 680kΩ, 0.25W, 1206	R1, R2
40	1	Panasonic-ECG	ERJ-8ENF7501V	Resistor, 7.5kΩ, 0.25W, 1206	R3
41	2	Panasonic-ECG	ERJ-P08J223V	Resistor, 22 kΩ, 0.25W, 1206	R6, R19
42	2	Panasonic-ECG	ERJ-P08J150V	Resistor, 15 Ω, 0.25W, 1206	RLO, RHO

43	3	Panasonic-ECG	ERJ-P08J104V	Resistor, 100 kΩ, 0.25W, 1206	R9, R20, RSD
44	2	Panasonic-ECG	ERJ-P08J824V	Resistor, 820 kΩ, 0.25W, 1206	R10, R11
45	1	Panasonic-ECG	ERJ-P08J912V	Resistor, 8.25 kΩ, 0.25W, 1206	R12
46	1	Panasonic-ECG	ERJ-8ENF1001V	Resistor, 1 kΩ, 0.25W, 1206	RLIM
47	1	Panasonic-ECG	ERJ-P08J472V	Resistor, 4.7 kΩ, 0.25W, 1206	R14
48	6	Panasonic-ECG	ERJ-8ENF1002V	Resistor, 10kΩ, 0.25W, 1206	R16, R17, RDIM, RFB, RIN, ROUT
49	1	Panasonic-ECG	ERJ-P08J334V	Resistor, 330kΩ, 0.25W, 1206	R18
50	2	Panasonic-ECG	ERJ-P08J100V	Resistor, 10 Ω, 0.25W, 1206	R4, R21
1	3	Panasonic-ECG	ERJ-P08J153V	Resistor, 15kΩ, 0.25W, 1206, 1%	R22, RFMIN, RPH
52	2	Panasonic-ECG	ERJ-P08J105V	Resistor, 1MΩ, 0.25W, 1206	RPU1, RPU2
53	1	Panasonic-ECG	P0.82W-1BK-ND	Resistor, 0.82 Ω, 1W, Axial	RCS
54	1	Panasonic-ECG	ERJ-P08J433V	Resistor, 56kΩ, 0.25W, 1206	RVDC
55	4	Panasonic-ECG	ERJ-P08J224V	Resistor, 220kΩ, 0.25W, 1206	REOL1, REOL2, REOL3, R15
56	1	Panasonic-ECG	ERJ-P08J203V	Resistor, 20kΩ, 0.25W, 1206	REOL4
57	1	Panasonic-ECG	ERJ-P08J101V	Resistor, 100Ω, 0.25W, 1206	R7
58	1	Panasonic-ECG	PPC10W-1CT-ND	Resistor, 10Ω, 0.25W, Axial	RLS
59	1	Panasonic-ECG	ERJ-P08J473V	Resistor, 47kΩ, 0.25W, 1206	R5
60	1	Panasonic-ECG	ERJ-P08J471V	Resistor, 470 Ω, 0.25W, 1206	R8
61	1	Panasonic-ECG	ERJ-P08J511V	Resistor, 510 Ω, 0.25W, 1206	R13
62	2	Panasonic-ECG	ERJ-P08J104V	Resistor, 100 kΩ, 0.25W, 1206	RS1, RS2
63	3	Panasonic-ECG	ERJ-P08J474V	Resistor, 470 kΩ, 0.25W, 1206	R23, R24, RCPH
64	1	BC Components	PPC.47CTR-ND	Resistor, 0.47 Ω, 1W, Axial	RS
65	0	DNP	DNP	DNP	RDC
66	1	Copal Electronics	CT-94EW203	Potentiometer, 20 kΩ, top adjust	VR1
67	1	Panasonic-ECG	ERZ-V10D431	Varistor, 275VAC, 10mm	RV1
68	1	Phoenix Passive	5063FM1R000J12 AFX	Fusible Resistor, 1 Ω	F1
69	1	Wago	235 Series	Connector, 5 Way	P1
70	1	Wago	234 Series	Connector, 4 way	P2

Table 1: ***Bill of Materials. Lamp type: T5/54W***

International
IOR Rectifier

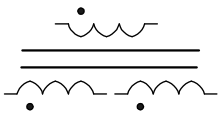
INDUCTOR SPECIFICATION

TYPE : LPFC

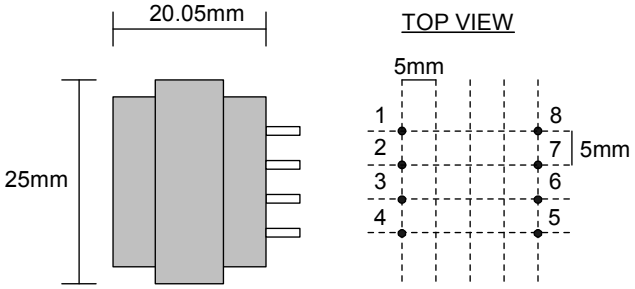
CORE SIZE	E25/13/7 (EF25)	GAP LENGTH	1	mm
BOBBIN	HORIZONTAL	PINS	8	
CORE MATERIAL	Philips 3C85, Siemens N27 or equivalent			
NOMINAL INDUCTANCE	2	mH		
MAXIMUM CURRENT	1	Apk		
MAXIMUM CORE TEMPERATURE	100	ºC		

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
MAIN	1	6	TBD	4 strands of AWG32
ZX	3	8	10	Insulated single strand
AUX	4	7	15	Insulated single strand

ELECTRICAL LAYOUT



PHYSICAL LAYOUT

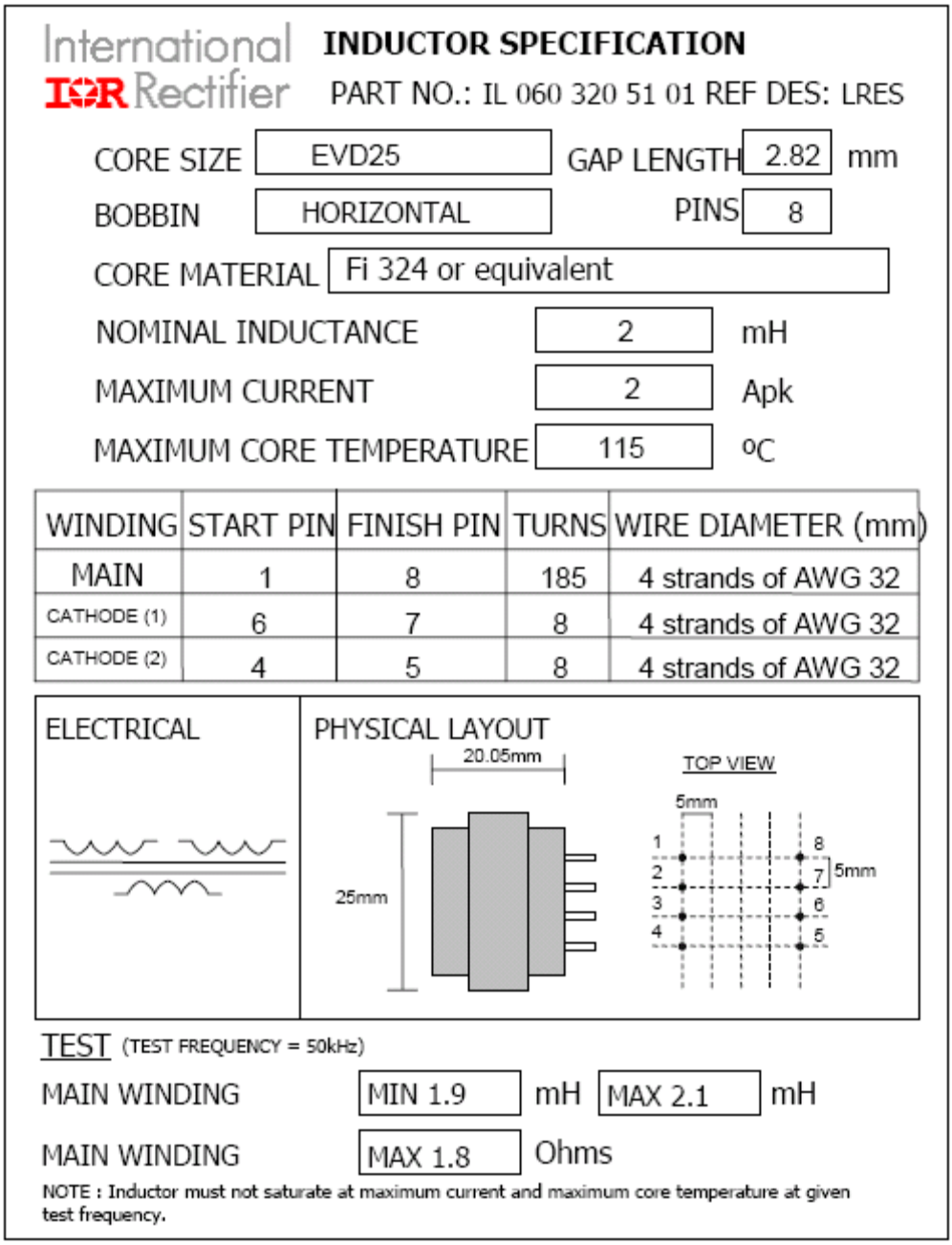


TEST (TEST FREQUENCY = 50kHz)

MAIN WINDING INDUCTANCE	MIN 1.9	mH	MAX 2.1	mH
MAIN WINDING RESISTANCE	MAX 1.5	Ohms		

NOTE : Inductor must not saturate at maximum current and maximum core temperature at given test frequency.

Figure 13: *LPFC specification*



International
IOR Rectifier

INDUCTOR SPECIFICATION

PART NO.: IL 060 320 51 01 REF DES: LRES

CORE SIZE	EVD25	GAP LENGTH	2.82	mm
BOBBIN	HORIZONTAL	PINS	8	
CORE MATERIAL	Fi 324 or equivalent			
NOMINAL INDUCTANCE	2	mH		
MAXIMUM CURRENT	2	Apk		
MAXIMUM CORE TEMPERATURE	115	°C		

WINDING	START PIN	FINISH PIN	TURNS	WIRE DIAMETER (mm)
MAIN	1	8	185	4 strands of AWG 32
CATHODE (1)	6	7	8	4 strands of AWG 32
CATHODE (2)	4	5	8	4 strands of AWG 32

ELECTRICAL

PHYSICAL LAYOUT

TEST (TEST FREQUENCY = 50kHz)

MAIN WINDING	MIN 1.9	mH	MAX 2.1	mH
MAIN WINDING	MAX 1.8	Ohms		

NOTE : Inductor must not saturate at maximum current and maximum core temperature at given test frequency.

Figure 14: *LRES specification*

Electrical Characteristics

Parameter	Units	Value
Lamp Type		54W TL5
Input Power	[W]	55W
Lamp Running Voltage	[Vpp]	410
Run Mode Frequency	[kHz]	46.5
Preheat Mode Frequency	[kHz]	80.0
Preheat Time	[s]	1
Lamp Preheat Voltage	[Vpp]	720
Lamp Ignition Voltage	[kVpp]	1
Input AC Voltage Range	[VAC]	90-305 VAC
Power Factor		0.999 at 120VAC 0.995 at 220VAC

Table 2: ***Electrical Characteristics of the Ballast***

Fault Protection Characteristics

Fault	Protection	Ballast	Restart Operation
Brownout	VDC Brown-out detect	Shutdown	Line voltage increase
Upper filament broken	CS Over Current detect	Deactivates	Lamp Exchange
Lower filament broken	SD Open filament detection SD/EOL pin	Deactivates	Lamp exchange
Failure to ignite	CS ignition detection timeout	Deactivates	Lamp Exchange
No Lamp	SD Open filament detection SD/EOL pin	Deactivates	Lamp Inserted
End of Life	EOL lamp voltage detection on SD/EOL pin	Deactivates	Lamp Exchange

Table 3: ***Fault Protection Characteristics of the Ballast***

FUNCTIONAL DESCRIPTION

Description

The design of dimmable ballast for linear lamps requires that the lamp power can be reduced smoothly to a low output level, less than 5% of nominal lumen output. It is necessary that the lamp output is able to be held at any level and that there will be no discernable flicker or instability at any level. In order to accomplish this, a closed loop control scheme is required. The fluorescent lamp represents a complex load, the impedance of which changes depending on the arc current and temperature of the gasses within the lamp. Like all discharge lamps, the fluorescent lamp displays a *negative resistance* behavior, meaning that as the current in the lamp increases the effective resistance of the lamp will reduce. The lamp impedance is strongly dependent on the arc current, however the relationship is not linear and temperature is also a factor.

In this design, the ballast supplies the lamp through a resonant output circuit. The lamp power is adjusted by changing the oscillation frequency of the MOSFET half bridge, which is driven by the IRS2158D. In this system the lamp current against ballast frequency characteristic of the system exhibits a sharp “knee” characteristic such that as the frequency increases the lamp current is gradually reduced up to a point at which a small increase of frequency will result in a large reduction in the lamp current.

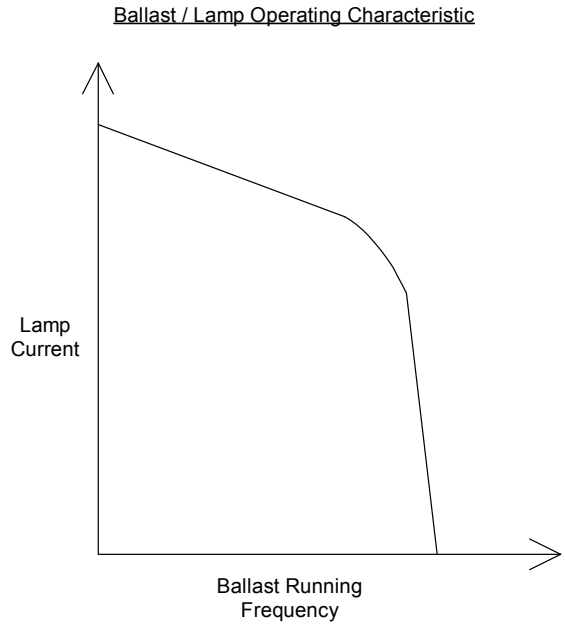


Figure 15: ***Lamp Current against Ballast Frequency***

Consequently it becomes necessary to include a stabilized closed loop feedback system to control the lamp current by adjusting the ballast frequency by means of

a voltage controlled oscillator (VCO). In this example the VCO within the IRS2158D is driven by the output of an error amplifier and compensation network that senses the lamp arc current directly and compares it with a reference.

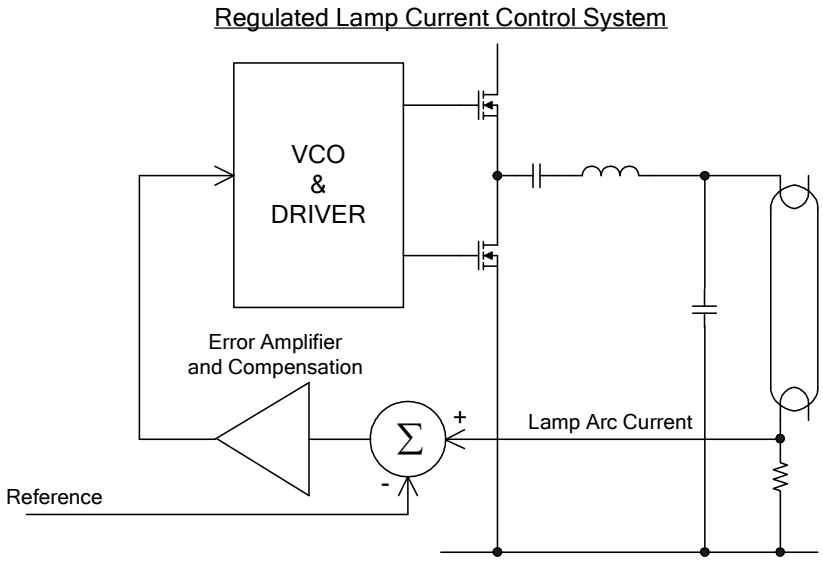


Figure 16: ***Closed Loop Dimming Control***

Isolated 0 to 10V Control Interface

The isolated 0 to 10 V control interface operates by means of a simple circuit, is described in the Design Tip DT-02. This operates in the same way as many other commercially available 0 to 10 V dimming ballasts. The input internally biased at 10 V if nothing is connected and can be reduced to 0 V by sinking current only. Isolation between the dimming input and the ballast circuitry is provided by means of an opto-isolator (IC4) and an additional isolated winding of the PFC boost inductor LPFC.

This winding must be isolated from the other two windings and from the ferrite cores and should be flash tested to 4 kV. In order to obtain sufficient voltage, this winding will need to have several more turns than the zero current detection winding. It is necessary to ensure that the voltage across the 18 V zener diode (D3) never falls below 18 V when the ballast output is dimmed and also over the range of line supply voltage. The next part of the circuit, centered around the *programmable unijunction transistor* Q1, generates an approximate ramp waveform across capacitor C7, which peaks at approximately 10 V guaranteeing maximum output when 10 V input is applied at the dimming input.

A trigger voltage provided by a potential divider of 9 V is applied to the gate of Q1. C7 charges through R15 until the voltage reaches a point one diode drop above the 9 V trigger voltage. Q1 then fires and remains switched on until the current drops below the valley current of the device which is small, discharging

C7 again. This produces a continuously oscillating ramp waveform. It is important that R15 is sufficiently large that it does not supply a current larger than the valley current, otherwise Q1 remains on indefinitely and the circuit does not oscillate. It necessary for this oscillator to run at a frequency of several hundred Hz to prevent it from being a source of visible flicker.

This sawtooth signal is fed into the inverting input of a comparator. Note that this circuit makes use of a dual comparator IC by placing both comparators in parallel so as to provide greater current sinking capability to drive the input of IC4. However, there is no need for this provided the comparator used is capable of sinking the opto-isolator diode current, which in this case is around 13 mA. The opto-isolator diode current should be chosen to be as low as possible to guarantee saturation of the transistor when it sinks 1mA and consequently R14 is as large as possible. The non-inverting input is connected to the control input and pulled high via R20, which provides a sink current of 1 mA. C8 removes any noise that may be picked up at the comparator input.

The comparator output is open collector providing current to the input of IC4 when low. The diode will be continuously off when the input is at maximum and on when it is zero. Hence the opto-isolator output transistor will be fully on when the control voltage is at minimum and fully off when it is at maximum, providing a reasonably linear change in the duty cycle at intermediate levels. It is important in production to ensure that the opto-isolator used is rated to the correct voltage and has been certified to the necessary safety standards. The transistor side of the opto-isolator has the emitter connected to 0 V (COM) and the collector connected to the IRS2158D VCC supply of 15.6 V via a pull up resistor R22. The collector node is then connected via R18 to CDIV and R19 to 0 V (COM). This averages the PWM signal and provides a DC reference to connect to the IRS2158D, which varies between 0V and the maximum voltage set. The range can be changed if necessary by adjusting the value of R19.

The value of the lamp current sensing resistor RLS will determine the feedback voltage provided to the op-amp feedback circuit of the IRS2158D. The value of RLS should be selected to provide as large a feedback as possible without dissipating too much power at maximum light output. It is recommended to keep the power dissipation in RLS below 0.25 W.

A delay is usually incorporated into dimming ballasts to provide a smooth fade from one dimming level to the next. For example, if the control inputs were to be shorted together, the lamp would fade down to minimum brightness over a period determined by the values used. This neatly avoids any flicker that may be caused by sudden changes in load in the PFC boost regulator section. In this case delay is provided via the time constant of R18 and CDIV. As the frequency of the PWM signal from the opto-isolator is of the order of tens of Hz, the delay has been designed to be long enough to ensure minimal ripple on the DC control voltage

input to the IC. This can be increased if a longer fade time is desired by making CDIV larger.

Since the lamp arc current is being sensed with a resistor, it is necessary to use voltage mode preheating to avoid detecting the sum of the current in the arc added to the resonant output capacitor (CRES) current. This has an additional advantage that during preheat and prior to ignition of the lamp the arc current will always be zero and consequently the feedback circuit will not influence the oscillator frequency at all until the lamp is running. This means that by setting the value of RPH the preheat will occur in exactly the same way independent of the dimming control voltage achieving optimum preheat and ignition under all conditions.

Power Factor Correction Section

The power factor correction stage at the front end of the ballast is based on a standard critical conduction mode circuit using an industry standard control IC. This stage has been designed to provide a DC bus of 480 V and operates with the AC line input voltage from 90 Vrms up to 305 Vrms, which is the maximum voltage that may occur on a 277 VAC line, allowing virtually world wide operation. In a dimming design with a wide voltage input range it is necessary to select the optimum value for the PFC inductor.

The inductance must be sufficiently large to allow the PFC controller IC1 to maintain stable operation when the line input at maximum and the dimming level is at minimum. Under these conditions the COMP voltage at pin 2 will be very low and the PWM on time will be very short. If the inductor value is too small the on time will become too small for the control IC to be able to maintain a stable DC bus.

The result of an unstable DC bus is a slight but visible flicker seen when the lamp is dimmed. Such instability is usually caused by instability of the power factor correction section rather than the lamp current regulation loop incorporated within the IRS2158D (IC2).

The trade off is that if the value of LPFC is too high the bus voltage will start to drop at low line input and maximum load since the COMP pin voltage has reached maximum and therefore the maximum on time limit has been reached. The lamp current control loop is however able to lower the ballast frequency in order to compensate for this to some degree if necessary.

Ignition

The IRS2158D incorporates regulated ignition control. At the end of the preheat period the IRS2158D VCO pin voltage increases and so the frequency decreases until the voltage at the CS pin reaches the internal threshold of 1.25 V. At this point the IRS2158D internally pulls down the VCO pin voltage and therefore regulates the circulating current in the resonant output circuit of the ballast and maintains a constant voltage across the lamp (blue trace). This voltage will remain while the CPH pin voltage (red trace) charges from 1/3VCC to 1/2VCC. If the lamp has not ignited at this point the IRS2158D will shut down. If preheat is insufficient the ballast will fail to ignite and shut down at the end of the ignition phase as shown in *Fig 17*. In this design the ignition voltage has been set at 1.25 kV peak and 2 kV peak to peak. This ignition voltage is correct for worst case conditions in a 54W TL5 lamp and can be set by using an RCS value of 0.82R.

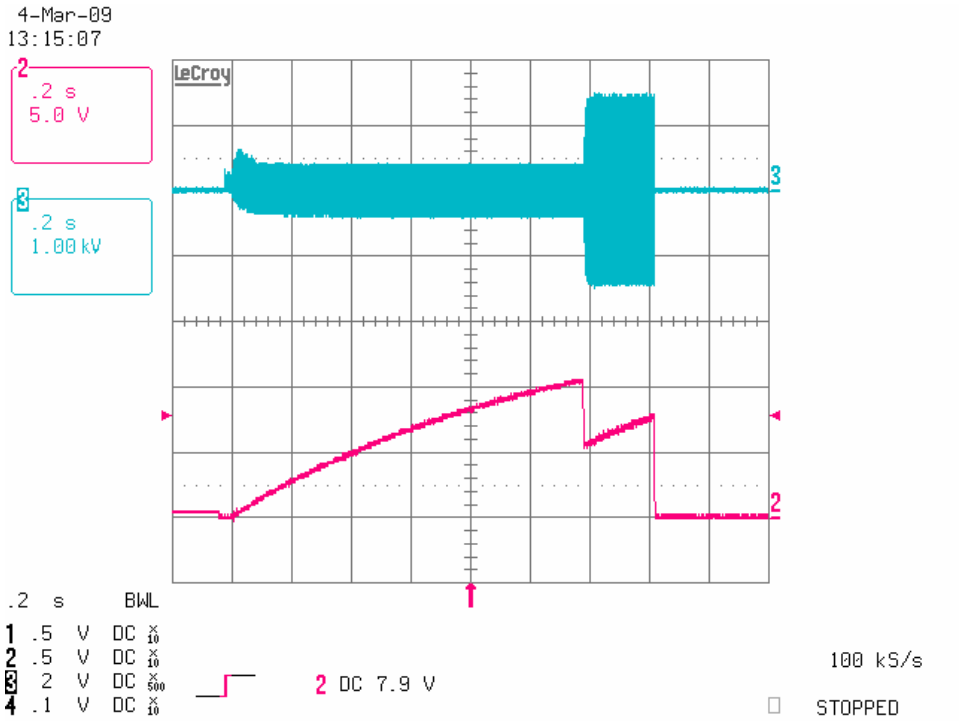


Figure 17: ***Lamp Voltage (blue) and CPH pin voltage - No Ignition***

A good lamp normally ignites as the output voltage ramps up to the ignition regulation level as shown in *Fig 18*.

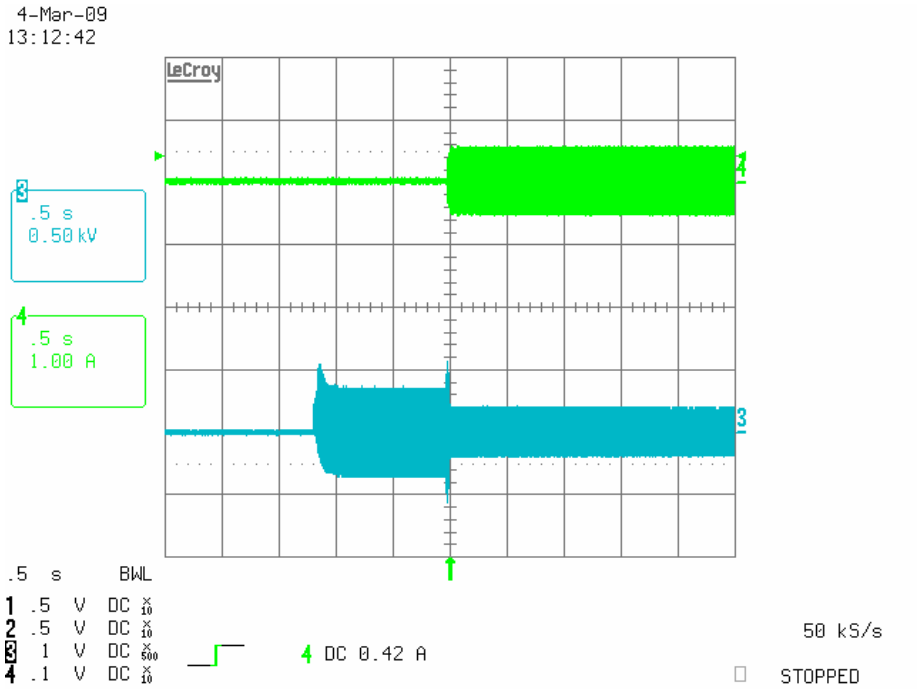


Figure 18: ***Lamp Voltage (blue) and Current – Correct Ignition***

Dimming

The following waveforms captures demonstrate the performance of the ballast at 10V (maximum) brightness and 0V (minimum) brightness.

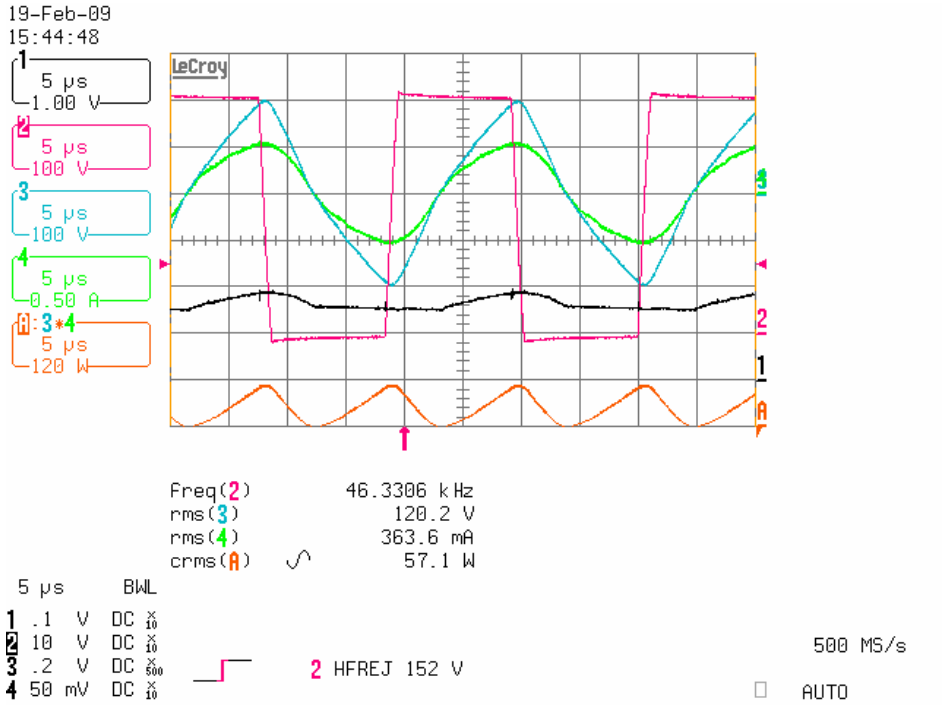


Figure 19: ***Ballast Waveforms for Maximum Brightness***

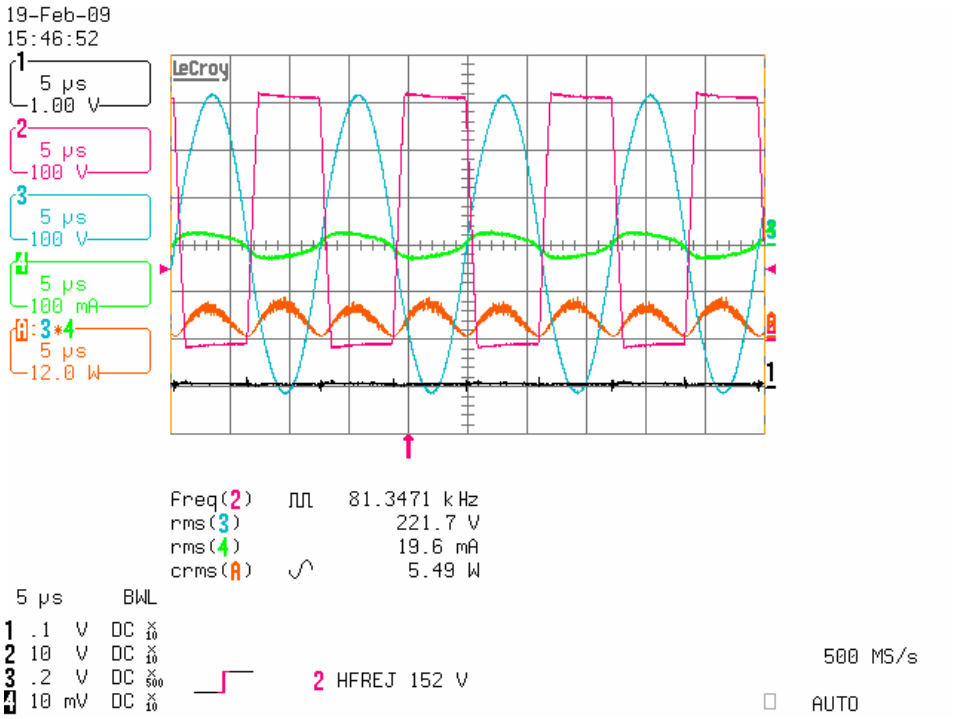


Figure 20: ***Ballast Waveforms at Minimum Brightness***

Trace	Color	Signal
1	Black	Feedback Voltage at RLS (and DS1 Cathode)
2	Red	Half Bridge Voltage – VS
3	Blue	Lamp Voltage
4	Green	Lamp Arc Current
A	Orange	Lamp Power (3 multiplied by 4)

The values of R18 and R19 have been selected so that when the opto-isolator IC4 is completely off the voltage at the input of the error amplifier, at RDIM connection with the wiper of VR1, will be 1.5 V. This will set the error amplifier input voltage to 1.5 V when the 0 to 10 V dimming control voltage is a 10 V and maximum output is required. This effectively limits the maximum lamp power because the error amplifier will regulate the frequency in order to maintain equal voltage at RLS to the input voltage at RDIM.

The minimum dimming level can be set by R19 and adjusted by RV1, which prevents the opto-isolator transistor from pulling the error amplifier input voltage all the way to zero. If the opto-isolator were on continuously the input voltage to the error amplifier would be so low that the lamp would extinguish or enter an unstable state of partial ignition. Tests have indicated that the T5 lamp behaves differently when cold and hot at very low light levels. When the lamp is cold the arc tends to become unstable as the lamp repeatedly extinguishes and re-ignites, however when the lamp is hot it is possible to dim all the way down to virtually zero output and a state can be observed where the lamp is in a stable state of

semi ignition, characterized by an faint emission of light along only part of the length of the tube.In a practical design it is desirable to limit the minimum output level to the minimum current at which the lamp can maintain stable operation when cold.

The ballast was measured over the input dimming range:

Control input (V)	Frequency (kHz)	Ballast Power (W)	Lamp Voltage (V)	Arc Current (mA rms)	Arc Power (W rms)	Feedback RLS (V)
1	79.6	18.6	247	35	9.1	0.075
2	80.1	23.5	229	57	13.8	0.212
3	80.4	28.1	207	86	20.0	0.361
4	79.5	32.6	190	118	25.7	0.514
5	77.2	36.8	176	156	31.8	0.690
6	72.4	41.4	166	202	39.5	0.895
7	65.9	45.7	154	240	44.2	1.080
8	57.9	49.7	142	289	50.1	1.303
9	49.7	53.7	132	344	56.0	1.539
10	46.2	55.1	125	366	57.2	1.644

Table 4: ***Overall Ballast Performance***

These are average values as there is some frequency modulation occurring at all times as the system regulates and compensates for impedance changes in the lamp. The measured results on the next page show that the lamp arc current and power are reasonably linear with respect to the input control voltage.

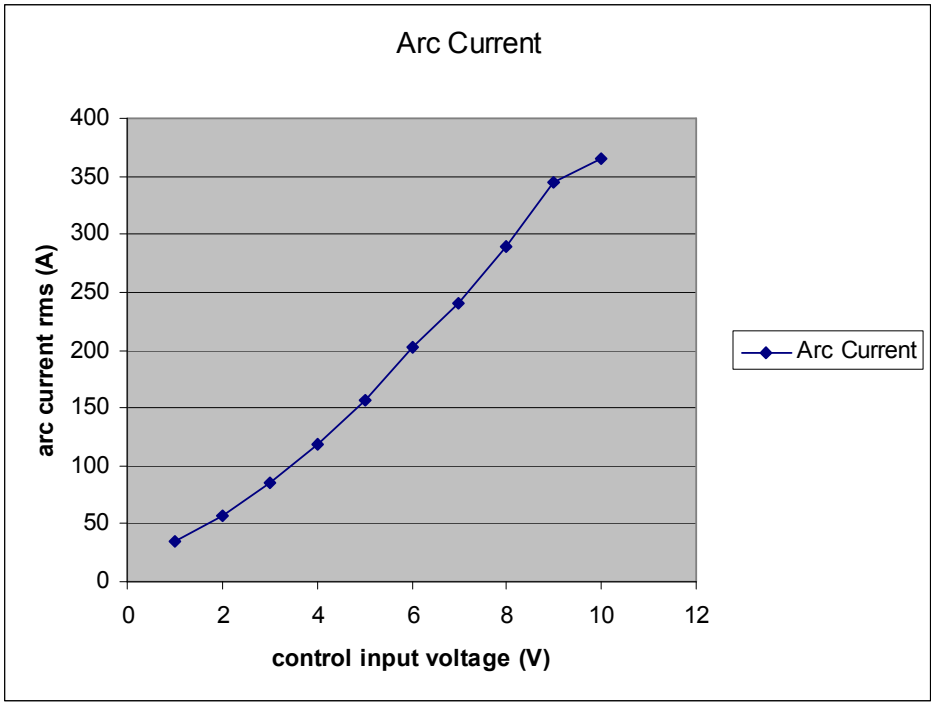


Figure 21: ***Graph of lamp arc current vs. control voltage input***

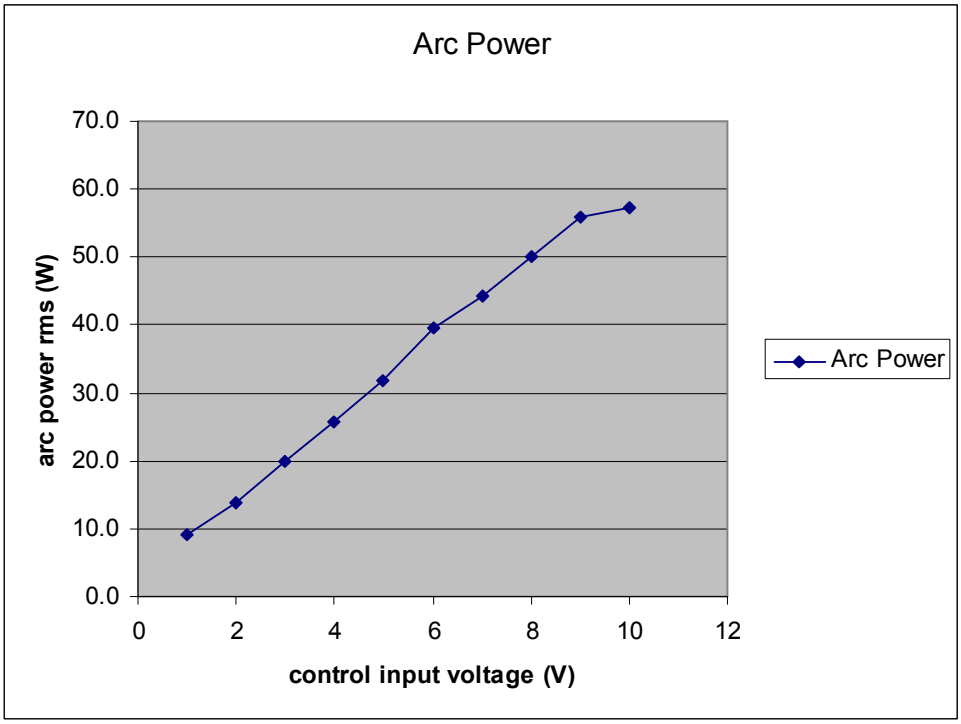


Figure 22: ***Graph of lamp arc power vs. control voltage input***

Protection Circuits

The SD pin of the IRS2158D is used for lamp removal protection. If there is no lamp present the voltage at SD pin will be pulled above the 5 V threshold via RPU1, RPU2 and RSD, charging CSD1 and CSD2 through DSD1 and DSD2. When a lamp is in circuit the voltage at the junction of RPU2 and RSD will be held low via DS1 and RLS. In this way when a lamp is removed the ballast shuts down and the lamp is replaced with a good one the ballast starts up again. In the IRPLDIM3 design the pull up of the SD pin for lamp removal detection is connected to the DC bus instead of VCC as in some other designs. This is because an additional 12 V zener diode DSD2 has been added, so that any voltage at the lower cathode produced during preheat, which can contain some DC offset will never be sufficient to falsely trip the lamp removal shut down circuit. In addition to this pulling up through resistors to the DC bus provides a more rapid response without draining current from VCC and maintains the SD pin voltage firmly above the 5 V threshold when no lamp is present under all conditions of line input voltage.

During preheat and ignition modes the end of life protection function, which monitors the lamp voltage through the SD pin is not enabled, therefore the ballast

will operate as long as the SD pin remains below 5 V. The SD pin is normally biased at 2 V from an internal voltage source within the IRS2158D.

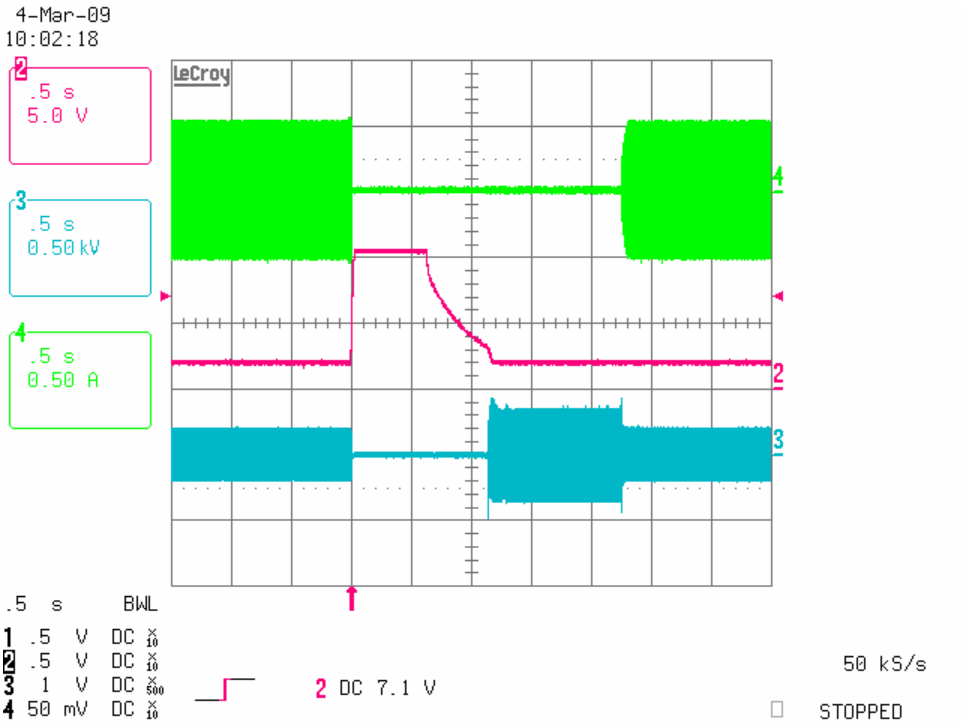


Figure 23: ***Lamp removal and replacement***

Trace	Color	Signal
1	Red	SD Pin Voltage
3	Green	Lamp Arc Current
4	Blue	Lamp Voltage

The VDC pin of the IRS2158D (IC2) is also connected to the DC bus through the divider formed by R23 and R24, with CVDC to COM to remove ripple and noise. This provides brown out protection for the ballast which works by sensing the rectified AC line voltage at the positive output of BR1. When the VDC voltage falls below 3 V the IRS2158D shuts down. The values of R23 and R24 are selected so that this condition occurs when the AC line input drops below the minimum level at which the ballast can maintain sufficient DC bus voltage for the lamp to remain ignited and run at the correct power. When the ballast has shut down the voltage at the VDC pin will rise because the voltage at BR1 will no longer be full wave rectified as there is no load and C2 is sufficient to maintain a DC level. To prevent the ballast from immediately re-starting there is a 2 V hysteresis such that the VDC pin must rise above 5 V in order for the IRS2158D to restart. This will only happen after the AC line has been restored to a sufficient level.

Without the brownout protection provided by the VDC pin if a brownout did occur the ballast would shut down in the event of any hard switching at VS because

voltage spikes would appear at the CS pin. This would cause the fault counter to count up until the ballast shut down. In that event the ballast would shut down and remain off until the line is switched off and then back on again. This is undesirable and with the implementation of the VDC pin of the IR2158D can easily be avoided so that the ballast will automatically recover from a Brownout event and switch the light back on.

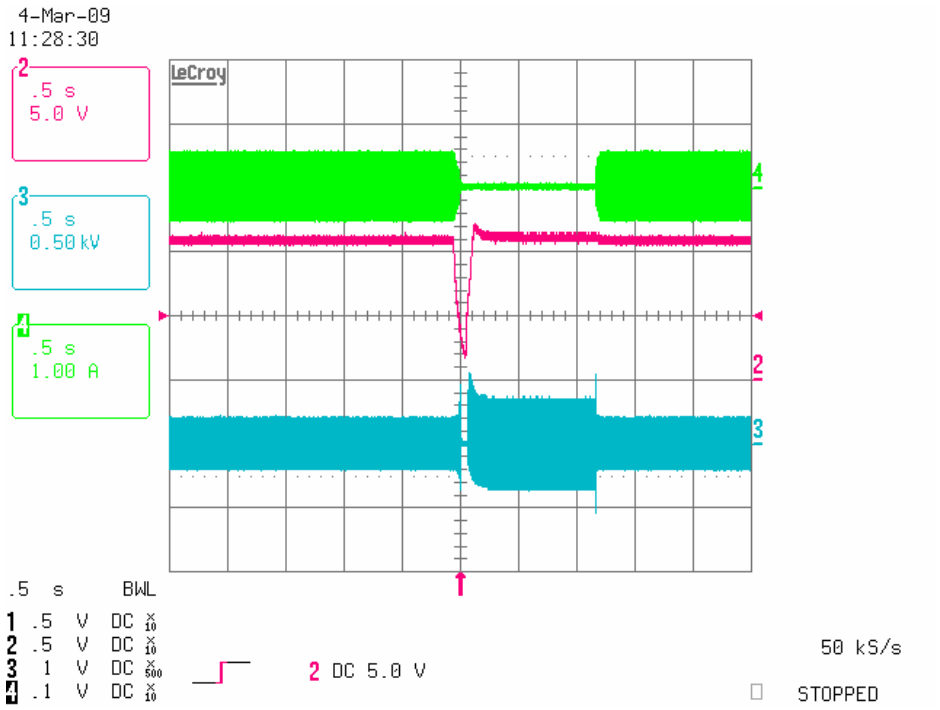


Figure 24: *Brownout shutdown and restart*

Trace	Color	Signal
1	Red	VDC Pin Voltage
3	Green	Lamp Arc Current
4	Blue	Lamp Voltage

The IRPLDIM3 ballast also includes end of life protection, which is enabled only after successful ignition when the ballast is in run mode. The lamp voltage is divided down through REOL1, REOL2, REOL3 and REOL4. This divided voltage is fed to two back to back zener diodes, DEOL1 (7.5 V) and DEOL2 (5.1 V). The SD pin is internally biased at 2 V with a window comparator that has 1 V and 3 V thresholds. If the positive peak of the lamp voltage becomes large enough to allow DEOL1 to reverse breakdown then the SD pin voltage will rise above 3 V. A delay is incorporated by clocking the oscillator pulses with the fault counter so that after a number of cycles the IRS2158D will shut down. The delay is normally around 1ms and was added to provide some immunity to transients and false shutting down of the end of life circuit. In the same way if the negative peak of the lamp voltage drops low enough for DEOL2 to reverse breakdown then the SD pin will fall below 1 V. After the same delay period the IRS2158D will also shut

down. This end of life circuit will therefore cause the ballast to shut down if an aging lamp is connected if it produces an asymmetric voltage in either direction, due to the rectifying effect. End of lamp life shutdown is often a mandatory requirement for electronic ballasts.

In the event of a ballast output becoming open circuit during running, for example if the lamp is broken or cracked but the filament is still intact, the SD pin will not detect a fault. However the ballast will still shut down because the CS pin will detect the transients caused by hard switching of the half bridge MOSFETs. In this case the fault counter will be active so that approximately 60 consecutive transients need to be detected by the CS pin before shut down. The *broken lamp test* is easily simulated by disconnecting the high voltage end of the lamp during running, which is the end that is not connected to the SD pin lamp out detection circuit.

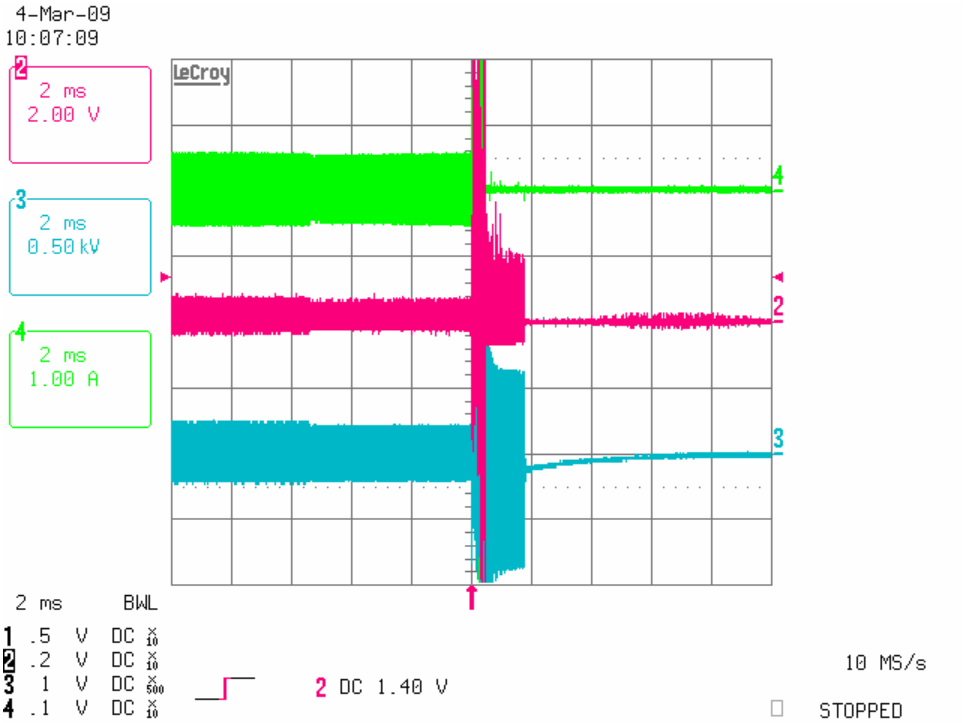


Figure 25: *Broken Lamp Test*

Trace	Color	Signal
2	Red	CS Pin Voltage
3	Green	Lamp Arc Current
4	Blue	Lamp Voltage

The above waveforms illustrate the delay of approximately 1ms introduced by the fault counter. This avoids any possibility of false tripping occurring if random transients occur.

CONCLUSIONS

The IRPLDIM3 is a high power factor and wide input voltage range dimming fluorescent ballast, with a fully isolated 0 to 10 V control interface, driving a single T5 28W lamp containing an EMI filter, an active power factor correction and a dimming ballast control circuit utilizing the PDIP16 version of the IRS2158D.
The IRPLDIM3 can be modified for a T5 54W design as shown in this application note. The design process is described, starting from the component calculations using the BDA software, the bill-of-materials, and schematics, to the layout consideration, the inductor design, and the testing of the ballast. This application note also explains in full detail the functional description of the ballast, which includes the ballast performance, isolated dimming control interface, different modes of the IC, and the protection features.

Ballast Designer software may be downloaded free of charge from:
www.irf.com/whats-new/nr051026.html