3.0 Volt-Only Flash & SRAM COMBO with Stacked Multi-Chip Package (MCP) — 16 Mbit Simultaneous Operation Flash Memory and 4 Mbit Static RAM

PRELIMINARY INFORMATION
JUNE 2002

MCP FEATURES

- Power supply voltage 2.7V to 3.3V
- High performance:
  Flash: 85ns maximum access time
  SRAM: 85ns maximum access time
- Package: 69-ball BGA
- Operating Temperature: -25C to +85C

FLASH FEATURES

- Power Dissipation:
  Read Current at 1 Mhz: 7 mA maximum
  Read Current at 5 Mhz: 18 mA maximum
  Sleep Mode: 5 µA maximum
- Simultaneous Read and Write Operations:
  Zero latency between read and write operations; Data can be programmed or erased in one bank while data is simultaneously being read from the other bank
- Low-Power Mode:
  A period of no activity causes flash to enter a low-power state
- Erase Suspend/Resume:
  Suspends of erase activity to allow a read in the same bank.
- Sector Erase Architecture:
  8 words of 4k size and 31 words of 32K size (16 Mbit)
  Any combination of sectors, or the entire flash can be simultaneously erased
- Erase Algorithms:
  Automatically preprograms/erases the flash memory entirely, or by sector
- Program Algorithms:
  Automatically writes and verifies data at specified address
- Hidden ROM Region:
  64KB with a Factory-serialized secure electronic serial number (ESN), which is accessible through a command sequence
- Data Polling and Toggle Bit:
  Allow for detection of program or erase cycle completion
- Ready-Busy output (RY/$\overline{BY}$): Detection of program or erase cycle completion
- Over 100,000 write/erase cycles
- Low supply voltage (Vccf ≤ 2.5V) inhibits writes
- $\overline{WP}$/ACC input pin:
  If V_{IL}, allows protection of boot sectors
  If V_{IH}, allows removal of boot sector protection
  If Vacc, program time is reduced by 40%
- Boot sector: Top or Bottom

SRAM FEATURES (4 Mb density)

- Power Dissipation:
  Operating: 40 mA maximum
  Standby: 7 µA maximum
- Chip Selects: $\overline{CE1}$s, CE2s
- Power down feature using $\overline{CE1}$s, or CE2s
- Data retention supply voltage: 1.5 to 3.3 volt
- Byte data control: $\overline{LB}$s (DQ0–DQ7), $\overline{UB}$s (DQ8–DQ15) — in x16 mode

GENERAL DESCRIPTION

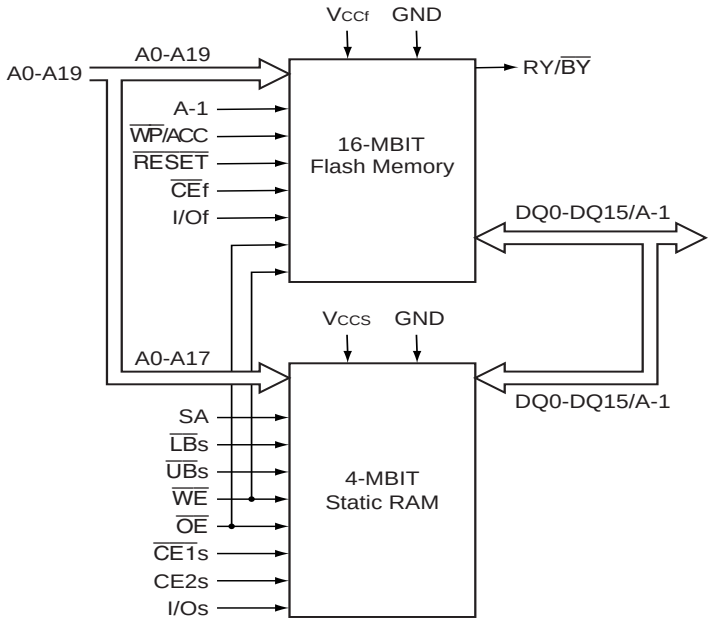
The flash and SRAM MCP is available in 16 Mbit Flash/4 Mbit SRAM having a data bus of either x8 or x16. The 16 Mbit flash is composed of 1,048,576 words of 16 bits or 2,097,152 bytes of 8 bits. The 4Mb SRAM has 262,144 words of 16 bits or 524,288 bytes of 8 bits. Data lines DQ0-DQ7 handle the x8 format, while lines DQ0-DQ15 handle the x16 format.

The package uses a 3.0V power supply for all operations. No other source is required for program and erase operations. The flash can be programmed in system using this 3.0V supply, or can be programmed in a standard EPROM programmer.

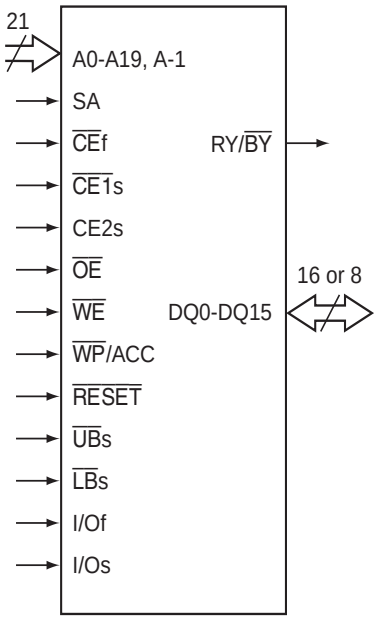
The 16 Mbit flash/4 Mbit SRAM is offered in a 69-ball BGA package. The flash is compatible with the JEDEC Flash command set standard . The flash access time is 85ns and the SRAM access time is 85ns.

The Flash architecture is composed of two banks which allows simultaneous operation on each. Optimized performance can be achieved by first initializing a program or erase function in one bank, then immediately starting a read from the other bank. Both operations would then be operating simultaneously, with zero latency.

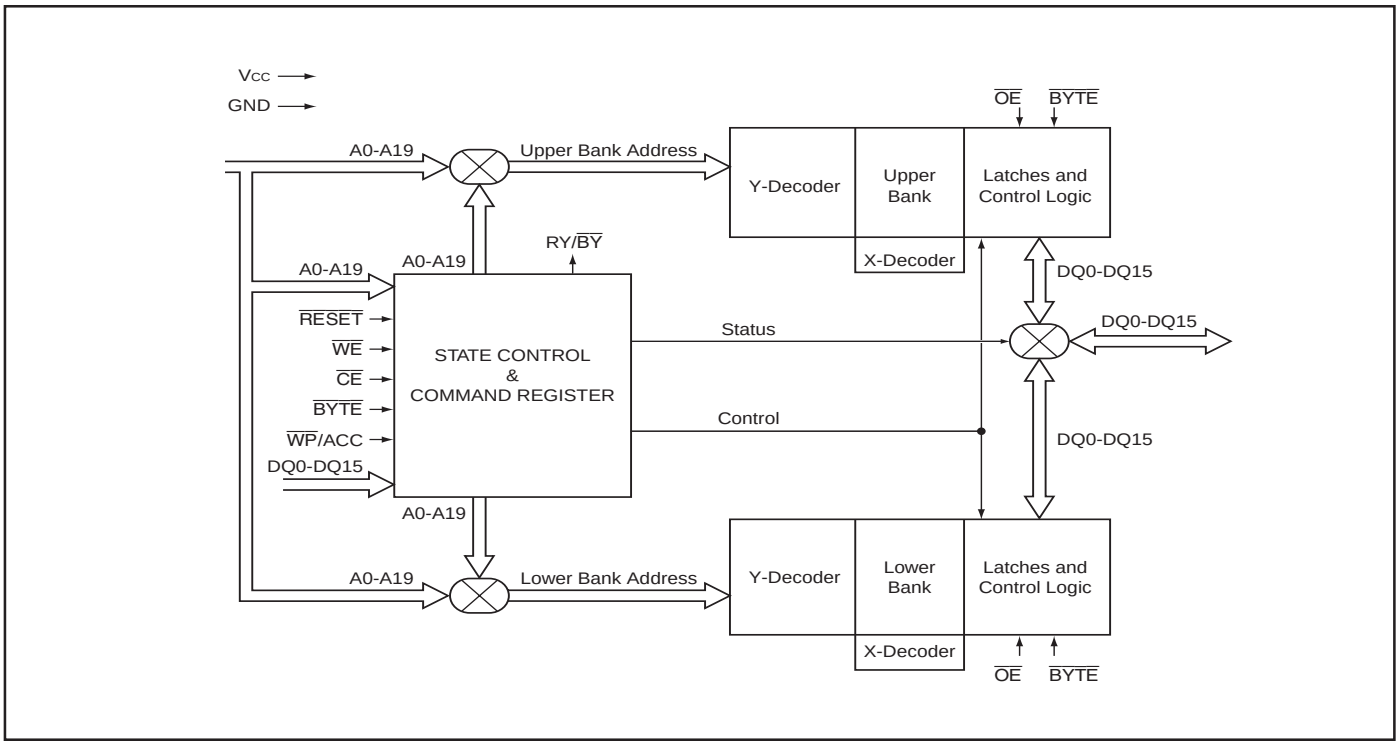
MCP BLOCK DIAGRAM



LOGIC SYMBOL



FLASH MEMORY BLOCK DIAGRAM



FLASH BANK ORGANIZATION

Organization Type	Bank 1 Size	Bank 2 Size	Boot Block
Type H	0.5Mb	15.5Mb	Top
Type J	2Mb	14Mb	Top
Type K	4Mb	12Mb	Top
Type L	8Mb	8Mb	Top
Type M	0.5Mb	15.5Mb	Bottom
Type N	2Mb	14Mb	Bottom
Type P	4Mb	12Mb	Bottom
Type Q	8Mb	8Mb	Bottom

Note:
For device part number, see Part Number Logic Diagram or Ordering Information

PIN CONFIGURATION (16 Mb Flash and 4 Mb SRAM)

69 BALL FBGA (Top View)

	1	2	3	4	5	6	7	8	9	10
A	NC				NC	NC				NC
B	NC		A7	$\overline{LB}$	$\overline{WP}$/ACC	$\overline{WE}$	A8	A11		
C		A3	A6	$\overline{UB}$	$\overline{RESET}$	CE2s	A19	A12	A15	
D		A2	A5	A18	RY/$\overline{BY}$	NC	A9	A13	NC	
E	NC	A1	A4	A17			A10	A14	NC	NC
F	NC	A0	GND	DQ1			DQ6	SA	A16	NC
G		$\overline{CE}$f	$\overline{OE}$	DQ9	DQ3	DQ4	DQ13	DQ15/A-1	I/Of	
H		$\overline{CE1}$s	DQ0	DQ10	Vccf	Vccs	DQ12	DQ7	GND	
J			DQ8	DQ2	DQ11	I/Os	DQ5	DQ14		
K	NC				NC	NC				NC

Shared
Flash only
SRAM only

PIN DESCRIPTIONS

A0-A17	Address Inputs, Common
A18-A19, A-1	Address Inputs, Flash
DQ0-DQ15/A-1	Data Inputs/Outputs
$\overline{RESET}$	Reset
$\overline{CE1}$s, CE2s	Chip Selects, SRAM
I/Of	I/O Configuration, Flash
$\overline{CE}$f	Chip Enable Input, Flash
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/Os	I/O Configuration, SRAM

$\overline{LB}$s	Lower-byte Control(DQ0-DQ7), SRAM
$\overline{UB}$s	Upper-byte Control (DQ8-DQ15), SRAM
$\overline{WP}$/ACC	Write Protect/Acceleration Pin, Flash
RY/$\overline{BY}$	Ready/Busy Output
SA	High Order Address Pin, SRAM (x8)
NC	No Connection
Vccf	Power, Flash
Vccs	Power, SRAM
GND	Ground

DEVICE BUS OPERATIONS

User Bus Operations (Flash=Word mode: I/Of = Vccf, SRAM= Word Mode: I/Os = Vccs)

OPERATION[1,3]	$\overline{CE}$f	$\overline{CE}$1s	CE2s	$\overline{OE}$	$\overline{WE}$	SA[6]	$\overline{LB}$s	$\overline{UB}$s	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$	$\overline{WP}$/ACC[5]
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash[2]	L	H	X	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	L	H	X	L	L	DOUT	DOUT	H	X
	H	L	H	L	H	X	H	L	High-Z	DOUT	H	X
	H	L	H	L	H	X	L	H	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	L	X	L	L	DIN	DIN	H	X
	H	L	H	X	L	X	H	L	High-Z	DIN	H	X
	H	L	H	X	L	X	L	H	DIN	High-Z	H	X
Temporary Sector Group Unprotection[4]	X	X	X	X	X	X	X	X	X	X	V_{ID}[8]	X
Flash Hardware	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
Reset	X	X	L	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Notes:

1. Any operations not indicated this column are inhibited.
2. $\overline{WE}$ can be VIL if $\overline{OE}$ is VIL, $\overline{OE}$ at VIH initiates the write operations.
3. Do not apply $\overline{CE}$f = VIL, $\overline{CE}$1s = VIL and CE2s = VIH all at once.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = VIL: protection of boot sectors.
   $\overline{WP}$/ACC = VIH: removal of boot sectors protection.
   $\overline{WP}$/ACC = VACC (9V): Program time will reduce by 40%.
6. SA: Don't care or open.
7. L = VIL, H = VIH, X = VIL or VIH.
8. See DC CHARACTERISTICS.

DEVICE BUS OPERATIONS

User Bus Operations (Flash=BYTE mode: I/Of = GND, SRAM= Word Mode: I/Os = Vccs)

OPERATION[1,3]	$\overline{CE}$f	$\overline{CE1}$s	CE2s	DQ_{15}/A-1	$\overline{OE}$	$\overline{WE}$	SA[6]	$\overline{LB}$s	$\overline{UB}$s	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$	WP/ACC[5]
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	A-1	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	A-1	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash[2]	L	H	X	A-1	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	A-1	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	A-1	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	A-1	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	X	L	H	X	L	L	DOUT	DOUT	H	X
	H	L	H	X	L	H	X	H	L	High-Z	DOUT	H	X
	H	L	H	X	L	H	X	L	H	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	X	L	L	DIN	DIN	H	X
	H	L	H	X	X	L	X	H	L	High-Z	DIN	H	X
	H	L	H	X	X	L	X	L	H	DIN	High-Z	H	X
Temporary Sector Group Unprotection[4]	X	X	X	X	X	X	X	X	X	X	X	V_{ID}[8]	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
	X	X	L	X	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Notes:

1. Any operations not indicated this column are inhibited..
2. $\overline{WE}$ can be VIL if $\overline{OE}$ is VIL, $\overline{OE}$ at VIH initiates the write operations.
3. Do not apply $\overline{CE}$f = VIL, $\overline{CE}$1s = VIL and CE2s = VIH all at once.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = VIL: protection of boot sectors.
   $\overline{WP}$/ACC = VIH: removal of boot sectors protection.
   $\overline{WP}$/ACC = VACC (9V): Program time will reduce by 40%.
6. SA: Don't care or open.
7. L = VIL, H = VIH, X = VIL or VIH.
8. See DC CHARACTERISTICS.

DEVICE BUS OPERATIONS

User Bus Operations (Flash=WORD mode: I/Of = Vccf, SRAM= Byte Mode: I/Os = GND

OPERATION[1,3]	$\overline{CE}$f	$\overline{CE}$1s	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$s[6]	$\overline{UB}$s[6]	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$	$\overline{WP}$/ACC[5]
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash[2]	L	H	X	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	L	H	SA	X	X	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	DIN	High-Z	H	X
Temporary Sector Group Unprotection[4]	X	X	X	X	X	X	X	X	X	X	VID[8]	X
Flash Hardware	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
Reset	X	X	L	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Notes:

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DEVICE BUS OPERATIONS

User Bus Operations (Flash=Byte mode: I/Of = GND, SRAM= Byte Mode: I/Os = GND)

OPERATION[1,3]	$\overline{CE}$f	$\overline{CE1}$s	CE2s	DQ_{15}/A-1	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$s[6]	$\overline{UB}$s[6]	DQ_0-DQ_7	DQ_8-DQ_{15}	$\overline{RESET}$	WP/ACC[5]
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
	H	X	L	X	X	X	X	X	X	High-Z	High-Z	H	X
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
	H	L	H	X	X	X	X	H	H	High-Z	High-Z	H	X
	L	H	X	A-1	H	H	X	X	X	High-Z	High-Z	H	X
	L	X	L	A-1	H	H	X	X	X	High-Z	High-Z	H	X
Read from Flash[2]	L	H	X	A-1	L	H	X	X	X	DOUT	DOUT	H	X
	L	X	L	A-1	L	H	X	X	X	DOUT	DOUT	H	X
Write to Flash	L	H	X	A-1	H	L	X	X	X	DIN	DIN	H	X
	L	X	L	A-1	H	L	X	X	X	DIN	DIN	H	X
Read from SRAM	H	L	H	X	L	H	SA	X	X	DOUT	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	SA	X	X	DIN	High-Z	H	X
Temporary Sector Group Unprotection[4]	X	X	X	X	X	X	X	X	X	X	X	VID[8]	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
	X	X	L	X	X	X	X	X	X	High-Z	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Notes:

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3. Do not apply $\overline{CE}$f = VIL, $\overline{CE}$1s = VIL and CE2s = VIH all at once.
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5. $\overline{WP}$/ACC = VIL: protection of boot sectors.
   $\overline{WP}$/ACC = VIH: removal of boot sectors protection.
   $\overline{WP}$/ACC = VACC (9V): Program time will reduce by 40%.
6. $\overline{LB}$s, $\overline{UB}$s: Don't care or open.
7. L = VIL, H = VIH, X = VIL or VIH.
8. See DC CHARACTERISTICS.

FLASH - TOP BOOT SECTOR ADDRESS

Type L	Type K	Type J	Type H	Sector	Sector Address A19-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank2	Bank2	Bank2	Bank2	SA0	00000xxx	64/32	000000h–00FFFFh	000000h–007FFFh
Bank2	Bank2	Bank2	Bank2	SA1	00001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh
Bank2	Bank2	Bank2	Bank2	SA2	00010xxx	64/32	020000h–02FFFFh	010000h–017FFFh
Bank2	Bank2	Bank2	Bank2	SA3	00011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
Bank2	Bank2	Bank2	Bank2	SA4	00100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
Bank2	Bank2	Bank2	Bank2	SA5	00101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
Bank2	Bank2	Bank2	Bank2	SA6	00110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
Bank2	Bank2	Bank2	Bank2	SA7	00111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
Bank2	Bank2	Bank2	Bank2	SA8	01000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
Bank2	Bank2	Bank2	Bank2	SA9	01001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
Bank2	Bank2	Bank2	Bank2	SA10	01010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
Bank2	Bank2	Bank2	Bank2	SA11	01011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
Bank2	Bank2	Bank2	Bank2	SA12	01100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
Bank2	Bank2	Bank2	Bank2	SA13	01101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
Bank2	Bank2	Bank2	Bank2	SA14	01110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
Bank2	Bank2	Bank2	Bank2	SA15	01111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
Bank1	Bank2	Bank2	Bank2	SA16	10000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
Bank1	Bank2	Bank2	Bank2	SA17	10001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
Bank1	Bank2	Bank2	Bank2	SA18	10010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
Bank1	Bank2	Bank2	Bank2	SA19	10011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
Bank1	Bank2	Bank2	Bank2	SA20	10100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
Bank1	Bank2	Bank2	Bank2	SA21	10101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
Bank1	Bank2	Bank2	Bank2	SA22	10110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh
Bank1	Bank2	Bank2	Bank2	SA23	10111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
Bank1	Bank1	Bank2	Bank2	SA24	11000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
Bank1	Bank1	Bank2	Bank2	SA25	11001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
Bank1	Bank1	Bank2	Bank2	SA26	11010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
Bank1	Bank1	Bank2	Bank2	SA27	11011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
Bank1	Bank1	Bank1	Bank2	SA28	11100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
Bank1	Bank1	Bank1	Bank2	SA29	11101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh

FLASH - TOP BOOT SECTOR ADDRESS (Continued)

Type L	Type K	Type J	Type H	Sector	Sector Address A19-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank1	Bank1	Bank1	Bank2	SA30	11110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
Bank1	Bank1	Bank1	Bank1	SA31	11111000	8/4	1F0000h–1F1FFFh	F8000h–F8FFFh
Bank1	Bank1	Bank1	Bank1	SA32	11111001	8/4	1F2000h–1F3FFFh	F9000h–F9FFFh
Bank1	Bank1	Bank1	Bank1	SA33	11111010	8/4	1F4000h–1F6FFFh	FA000h–FAFFFh
Bank1	Bank1	Bank1	Bank1	SA34	11111011	8/4	1F6000h–1F7FFFh	FB000h–FBFFFh
Bank1	Bank1	Bank1	Bank1	SA35	11111100	8/4	1F8000h–1F9FFFh	FC000h–FCFFFh
Bank1	Bank1	Bank1	Bank1	SA36	11111101	8/4	1FA000h–1FBFFFh	FD000h–FDFFFh
Bank1	Bank1	Bank1	Bank1	SA37	11111110	8/4	1FC000h–1FDFFFh	FE000h–FEFFFh
Bank1	Bank1	Bank1	Bank1	SA38	11111111	8/4	1FE000h–1FFFFFh	FF000h–FFFFFh

Note:
The address range is A19:A-1 in byte mode (I/Of=VIL) or A19:A0 in word mode (I/Of=VIH). The bank address bits are A19–A15 for Type H, A19 - A17 for Type J, and A19 and A18 for Type K, and A19 for Type L.

FLASH - TOP BOOT SECURITY SECTOR ADDRESSES

(Hidden-ROM)

Device	Sector Address A19-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
Types H, J, K, L	11111xxx	64/32	1F0000h-1FFFFFh	F8000h-FFFFFh

FLASH - BOTTOM BOOT SECTOR ADDRESS

Type Q	Type P	Type N	Type M	Sector	Sector Address A19-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank 1	Bank1	Bank1	Bank1	SA0	00000000	8/4	000000h–001FFFh	000000h–000FFFh
Bank1	Bank1	Bank1	Bank1	SA1	00000001	8/4	002000h–003FFFh	001000h–001FFFh
Bank1	Bank1	Bank1	Bank1	SA2	00000010	8/4	004000h–005FFFh	002000h–002FFFh
Bank1	Bank1	Bank1	Bank1	SA3	00000011	8/4	006000h–007FFFh	003000h–003FFFh
Bank1	Bank1	Bank1	Bank1	SA4	00000100	8/4	008000h–009FFFh	004000h–004FFFh
Bank1	Bank1	Bank1	Bank1	SA5	00000101	8/4	00A000h–00BFFFh	005000h–005FFFh
Bank1	Bank1	Bank1	Bank1	SA6	00000110	8/4	00C000h–00DFFFh	006000h–006FFFh
Bank1	Bank1	Bank1	Bank1	SA7	00000111	8/4	00E000h–00FFFFh	007000h–007FFFh
Bank1	Bank1	Bank1	Bank2	SA8	00001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh
Bank1	Bank1	Bank1	Bank2	SA9	00010xxx	64/32	020000h–02FFFFh	010000h–017FFFh
Bank1	Bank1	Bank1	Bank2	SA10	00011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh
Bank1	Bank1	Bank2	Bank2	SA11	00100xxx	64/32	040000h–04FFFFh	020000h–027FFFh
Bank1	Bank1	Bank2	Bank2	SA12	00101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh
Bank1	Bank1	Bank2	Bank2	SA13	00110xxx	64/32	060000h–06FFFFh	030000h–037FFFh
Bank1	Bank1	Bank2	Bank2	SA14	00111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh
Bank1	Bank2	Bank2	Bank2	SA15	01000xxx	64/32	080000h–08FFFFh	040000h–047FFFh
Bank1	Bank2	Bank2	Bank2	SA16	01001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh
Bank1	Bank2	Bank2	Bank2	SA17	01010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh
Bank1	Bank2	Bank2	Bank2	SA18	01011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh
Bank1	Bank2	Bank2	Bank2	SA19	01100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh
Bank1	Bank2	Bank2	Bank2	SA20	01101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh
Bank1	Bank2	Bank2	Bank2	SA21	01110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh
Bank1	Bank2	Bank2	Bank2	SA22	01111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh
Bank2	Bank2	Bank2	Bank2	SA23	10000xxx	64/32	100000h–10FFFFh	080000h–087FFFh
Bank2	Bank2	Bank2	Bank2	SA24	10001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh
Bank2	Bank2	Bank2	Bank2	SA25	10010xxx	64/32	120000h–12FFFFh	090000h–097FFFh
Bank2	Bank2	Bank2	Bank2	SA26	10011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh
Bank2	Bank2	Bank2	Bank2	SA27	10100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh
Bank2	Bank2	Bank1	Bank2	SA28	10101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh
Bank2	Bank2	Bank1	Bank2	SA29	10110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh

FLASH - BOTTOM BOOT SECTOR ADDRESS (Continued)

Type Q	Type P	Type N	Type M	Sector	Sector Address A19-A12	Sector Size KB/KW	(x8) Address Range	(x16) Address Range
Bank2	Bank2	Bank2	Bank2	SA30	10111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh
Bank2	Bank2	Bank2	Bank2	SA31	11000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh
Bank2	Bank2	Bank2	Bank2	SA32	11001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh
Bank2	Bank2	Bank2	Bank2	SA33	11010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh
Bank2	Bank2	Bank2	Bank2	SA34	11011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh
Bank2	Bank2	Bank2	Bank2	SA35	11100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh
Bank2	Bank2	Bank2	Bank2	SA36	11101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
Bank2	Bank2	Bank2	Bank2	SA37	11110xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh
Bank2	Bank2	Bank2	Bank2	SA38	11111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh

Note:
The address range is A19:A-1 in byte mode (I/Of=VIL) or A19:A0 in word mode (I/Of=VIH). The bank address bits are A19–A15 for Type M, A19 - A17 for Type N, and A19 - A18 for Type P, and A19 for Type Q.

FLASH - BOTTOM BOOT SECURITY SECTOR ADDRESSES

(Hidden-ROM)

Device	Sector Address A19-A12	Size KB/KW	(x8) Address Range	(x16) Address Range
Types M,N,P,Q	00000xxx	64/32	000000h-00FFFFh	00000h-07FFFh

SECTOR GROUP ADDRESS (TYPE H, TYPE J, TYPE K, TYPE L)

(Top Boot Block)

Sector Group	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0 1 1	1 0 1	X	X	X	SA1 to SA3
SGA2	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	1	1	1	0 0 1	0 1 0	X	X	X	SA28 to SA30
SGA9	1	1	1	1	1	0	0	0	SA31
SGA10	1	1	1	1	1	0	0	1	SA32
SGA11	1	1	1	1	1	0	1	0	SA33
SGA12	1	1	1	1	1	0	1	1	SA34
SGA13	1	1	1	1	1	1	0	0	SA35
SGA14	1	1	1	1	1	1	0	1	SA36
SGA15	1	1	1	1	1	1	1	0	SA37
SGA16	1	1	1	1	1	1	1	1	SA38

SECTOR GROUP ADDRESS (TYPE M, TYPE N, TYPE P, TYPE Q)

(Bottom Boot Block)

Sector Group	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0 1 1	1 0 1	X	X	X	SA8 to SA10
SGA9	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	1	1	1	0 0 1	0 1 0	X	X	X	SA35 to SA37
SGA16	1	1	1	1	1	X	X	X	SA38

FLASH MEMORY AUTOSELECT CODES

Type		A_{12} to A_{19}	A_6	A_1	A_0	$A_{-1(1)}$	Code (HEX)
Manufacturer's Code		X	VIL	VIL	VIL	VIL	04h
TYPE H Device ID	Byte	X	VIL	VIL	VIH	VIL	36h
	Word	X	VIL	VIL	VIH	X	2236h
TYPE M Device ID	Byte	X	VIL	VIL	VIH	VIL	39h
	Word	X	VIL	VIL	VIH	X	2239h
TYPE J Device ID	Byte	X	VIL	VIL	VIH	VIL	2Dh
	Word	X	VIL	VIL	VIH	X	222Dh
TYPE N Device ID	Byte	X	VIL	VIL	VIH	VIL	2Eh
	Word	X	VIL	VIL	VIH	X	222Eh
TYPE K Device ID	Byte	X	VIL	VIL	VIH	VIL	28h
	Word	X	VIL	VIL	VIH	X	2228h
TYPE P Device ID	Byte	X	VIL	VIL	VIH	VIL	2Bh
	Word	X	VIL	VIL	VIH	X	222Bh
TYPE L Device ID	Byte	X	VIL	VIL	VIH	VIL	33h
	Word	X	VIL	VIL	VIH	X	2233h
TYPE Q Device ID	Byte	X	VIL	VIL	VIH	VIL	35h
	Word	X	VIL	VIL	VIH	X	2235h
Sector Group Protect		Sector Group Address	VIL	VIH	VIL	VIL	01h(2)

Note:
1. A–1 is only used for Byte mode.
2. Output 01h at protected sector address and output 00h at unprotected sector address.

FLASH MEMORY COMMAND DEFINITIONS

Command Sequence Bus		Bus Write Cycle Req'd	First Bus Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write		Fifth Bus Cycle		Sixth Bus Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read / Reset			XXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read / Reset * 1	Word Byte	1	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	F0H	RA	RD	—	—	—	—
Autoselect	Word Byte	3	555H AAAH	AAH	2AAH 555H	55H	(BA) 555H (BA) AAAH	90H	—	—	—	—	—	—
Program	Word Byte	3	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	A0H	PA	PD	—	—	—	—
Chip Erase	Word Byte	4	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	80H	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	10H
Sector Erase	Word Byte	6	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	80H	555H AAAH	AAH	2AAH 555H	55H	SA	30H
Sector Erase Suspend	Word Byte	1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Sector Erase Resume	Word Byte	1	BA	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word Byte	3	555H AAH	AAH	2AAH 555H	55H	555H AAAH	20H	—	—	—	—	—	—
Fast Program * 2	Word Byte	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode * 2	Word Byte	2	BA	90H	XXXH	F0H*6	—	—	—	—	—	—	—	—
Extended Sector Group Protection * 3	Word Byte	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
Query * 4	Word Byte	1	55H AAH	98h	—	—	—	—	—	—	—	—	—	—
Hidden-ROM Entry	Word Byte	3	555H AAAH	AAh	2AAH 555H	55H	555H AAAH	88H	—	—	—	—	—	—
Hidden-ROM Program * 5	Word Byte	4	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	A0H	PA	PD	—	—	—	—
Hidden-ROM Erase * 5	Word Byte	6	555H AAAH	AAH	2AAH 555H	55H	555H AAAH	80H	555H AAAH	AAH	2AAH 555H	55H	HRA	30H
Hidden-Rom Exit * 5	Word Byte	4	555H AAAH	AAH	2AAH 555H	55H	(HRBA) 555H (HRBA) AAAH	90H	XXXH	00H	—	—	—	—

Note:

*1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
*2: This command is valid during Fast Mode.
*3: This command is valid while RESET=VID.
*4: The valid Address is A0 to A6.
*5: This command is valid during Hi-ROM mode.
*6: The data “00h” is also acceptable.

Address bits A12 to A19 = X = “H” or “L” for all address commands except for Program Address (PA), Sector Address (SA),and Bank Address (BA).

Bus operations are defined in “Device Bus Operations”.
RA = Address of the memory location to be read
PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased.

The combination of A19 , A18 , A17 , A16 , A15 , A14 , A13 , and A12 will uniquely select any sector.
BA = Bank address (A15 to A19)
SPA = Sector group address to be protected.

Set sector group address (SGA) and (A6 , A1 , A0) = (0, 1, 0) for protect; or SGA and (A6, A1, A0) = (1,1,0) for unprotect.

HRA= Address of the Hidden-ROM area
Type H, Type J, Type K, Type L (Top Boot Type)
Word mode: 0F8000h to 0FFFFFh
Byte mode: 1F0000h to 1FFFFFh
Type M, Type N, Type P, Type Q (Bottom Boot Type)
Word mode: 000000h to 007FFFh
Byte mode: 000000h to 00FFFFh
HRBA = Bank address of the Hidden-ROM area
Type H, Type J, Type K, Type L (Top Boot Type) :
A15 = A16 = A17 = A18 = A19 = 1
Type M, Type N, Type P, Type Q (Bottom Boot Type) :
A15 = A16 = A17 = A18 = A19 = 0

RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA.
SD = Sector protection verify data.

Output 01h at protected sector addresses and output 00h at unprotected sector addresses.

The system should generate the following address patterns;
Word mode : 555h or 2AAh to addresses A0 to A10
Byte mode : AAAh or 555h to addresses A–1 and A0 to A10

MCP ABSOLUTE MAXIMUM RATINGS(1,2,3)

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–25 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for Data,	–0.3 to $V_{CC}f$ + 0.4	V
	Address and Control Pins	–0.3 to $V_{CC}s$ + 0.4	V
V_{IN}	$\overline{RESET}$(5)	-0.5 to +13.0	V
V_{IN}	$\overline{WP}$/ACC(6)	-0.5 to +10.5	V
$V_{CC}f$/$V_{CC}s$	Voltage on Vcc Supply Relative to GND(4)	–0.3 to 4.0	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.
4. Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot VSS to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$+0.3 V or $V_{CC}s$+0.3 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$+2.0 V or $V_{CC}s$+2.0 V for periods of up to 20 ns.
5. Minimum DC input voltage on RESET pin is –0.5 V. During voltage transitions, RESET pin may undershoot VSS to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-$V_{CC}f$ or $V_{CC}s$) does not exceed 9.0 V. Maximum DC input voltage on RESET pin is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
6. Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0V for periods of up to 20 ns, when $V_{CC}f$ is applied.

MCP OPERATING RANGE

Range	Ambient Temperature	V_{CCF},V_{CCS}
Industrial	–25°C to +85°C	2.7–3.3V

STANDARD VOLTAGE RANGE V_{CC} = 2.7-3.3 V

	Flash Memory		SRAM		Units
Max Access Time	70	85	70	85	ns
$\overline{CE}$ Access	70	85	70	85	ns
$\overline{OE}$ Access	30	40	35	45	ns

CAPACITANCE(1)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	16	pF
$C_{IN}2$	Control Pin Capacitance	V_{IN} = 0V	14	16	pF
$C_{IN}3$	$\overline{WP}$/ACC Pin Capacitance	V_{IN} = 0V	17	20	pF

Notes:
1. Test conditions: T_A = 25°C, f = 1 MHz

MCP DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage	V_{IN}=V_{SS} to V_{CCf}, V_{CCS}	-1.0	1.0	µA
I_{LO}	Output Leakage	V_{OUT}=V_{SS} to V_{CCf}, V_{CCS}	-1.0	1.0	µA
V_{IL}	Input Low Level		-0.2	0.5	V
V_{IH}	Input High Level		2.4	$V_{CC} \pm 0.3$(2)	V
V_{ID}	Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$)(1)		11.5	12.5	V
V_{ACC}	Voltage for Program Acceleration ($\overline{WP}$/Acc)(1)		8.5	9.5	V
V_{OL}	Output Low Level	V_{CCf} = V_{CCf} min., V_{CCS}=V_{CCS} min. I_{OL} = 1.0mA	—	0.45	V
V_{OH}	Output High Level	V_{CCf} = V_{CCf} min., V_{CCS}=V_{CCS} min. I_{OH} = -0.5mA	2.4	—	V
V_{LKO}	Flash Low Vccf		2.3	2.5	V

Notes:
1. Applicable for only V_{CCf} applying.
2. V_{CC} indicates lower of V_{CCf} or V_{CCS}.

FLASH DC CHARACTERISTICS

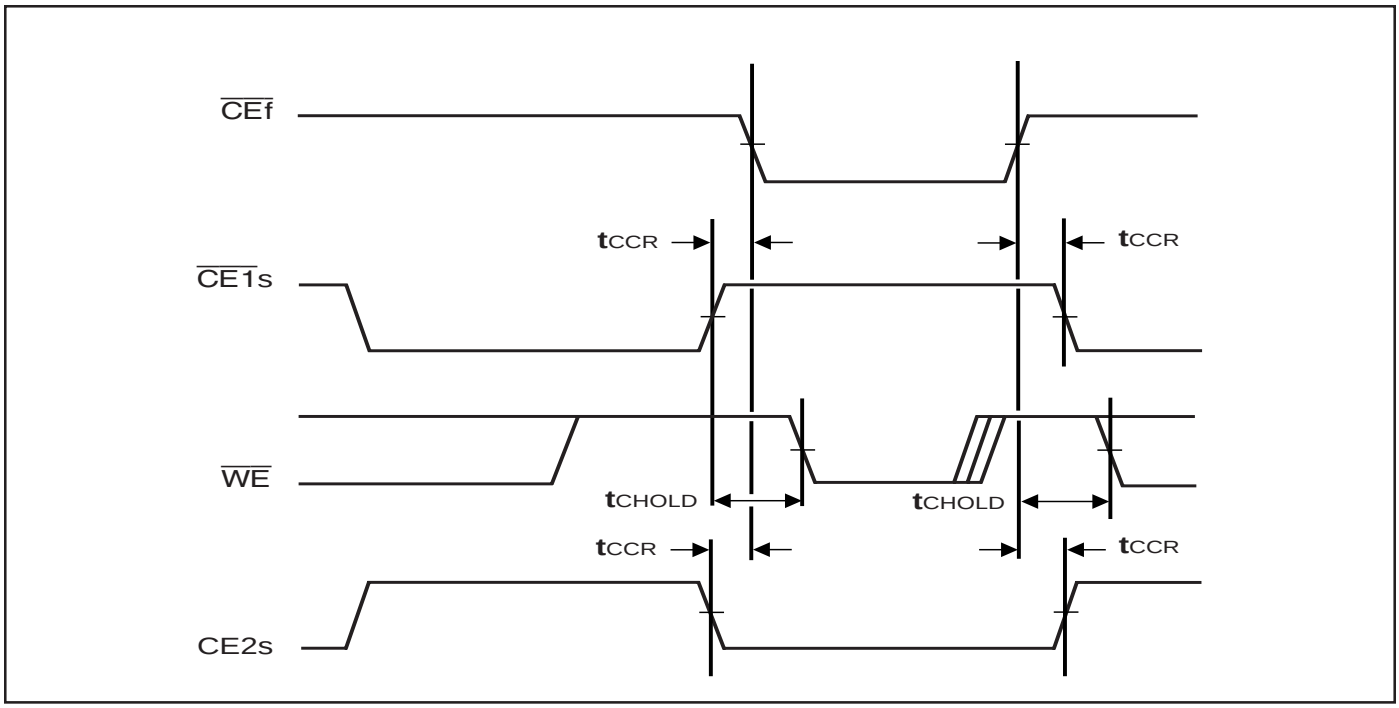
Symbol	Parameter	Test Conditions		Min.	Max.	Unit
I_{LIT}	$\overline{RESET}$ Inputs Leakage Current	V_{CCf}=V_{CCf} max., V_{CCS}=V_{CCS} max. $\overline{RESET}$ = 12.5V		—	35	µA
I_{LIA}	ACC Inputs Leakage Current	V_{CCf}=V_{CCf} max., V_{CCS}=V_{CCS} max. $\overline{WP}$/ACC = Vacc max.		—	20	µA
I_{CC1f}	FLASH Vcc [1] Active Current (Read)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	tCycle = 5Mhz Byte	—	13	mA
			tCycle = 5Mhz Word	—	15	
			tCycle = 1Mhz Byte	—	7	
			tCycle = 1Mhz Word	—	7	
I_{CC2f}	FLASH Vcc Active[2] Current(Program/Erase)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}		—	35	mA
I_{CC3f}	FLASH Vcc Active[4] Current (Read-While-Program)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	Byte	—	48	mA
			Word		50	
I_{CC4f}	FLASH Vcc Active[4] Current (Read-While-Erase)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}	Byte	—	48	mA
			Word		50	
I_{CC5f}	FLASH Vcc Active Current (Erase-Suspend-Program)	$\overline{CE}$f=V_{IL} $\overline{OE}$=V_{IH}		—	35	mA
I_{SB1f}	FLASH Vcc Standby Current	V_{CCf} = Vcc max, $\overline{CE}$f= V_{CCf} = ± 0.3V $\overline{RESET}$, $\overline{CE}$f, $\overline{WP}$/ACC = V_{CCf} = ± 0.3V		—	5	µA
I_{SB2f}	FLASH Vcc Standby Current ($\overline{RESET}$)	V_{CCf} = Vcc max, $\overline{RESET}$= V_{SS} = ± 0.3V $\overline{WP}$/ACC = V_{CCf} = ± 0.3V		—	5	µA
I_{SB3f}	FLASH Vcc[3] Standby Current (Auto Sleep Mode)	V_{CCf} = Vcc max. $\overline{CE}$f, = V_{SS} = ± 0.3V $\overline{RESET}$, $\overline{WP}$/ACC = V_{CCf} = ± 0.3V V_{IN} = V_{CCf} ± 0.3V OR V_{SS} ± 0.3V		—	5	µA

Notes:
1. The ICC current listed includes both the DC operating current and the frequency dependent component.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns..
4. Embedded Algorithm (program or erase) is in progress. (@5 MHz)

AC CHARACTERISTICS - $\overline{CE}$ TIMING

Parameter	JEDEC Symbol	Standard Symbol	Condition	Min	Unit
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	ns
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	ns

TIMING DIAGRAM FOR ALTERNATING SRAM TO FLASH



FLASH READ ONLY SWITCHING CHARACTERISTICS

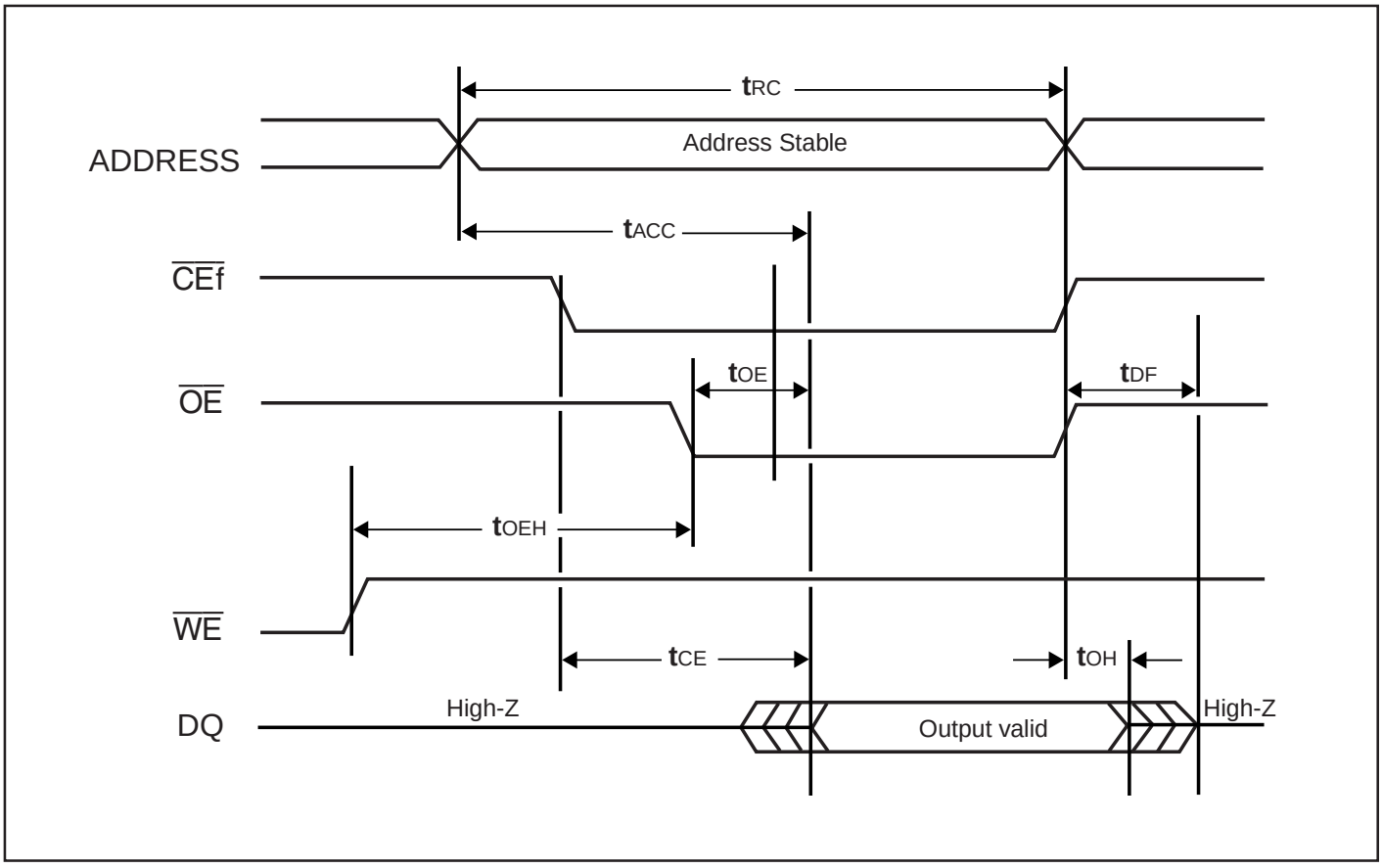
(Over Operating Range)

Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{RC}	Cycle Time	70		85	—	ns
t_{ACC}	Address to Output Delay	—	70	—	85	ns
t_{CE}	Chip Enable to Output Delay	—	70	—	85	ns
t_{OE}	Output Enable to Output Delay	—	30	—	35	ns
t_{DF}	Chip Enable to Output High-Z	—	25	—	30	ns
t_{DF}	Output Enable to Output High-Z	—	25	—	30	ns
t_{OH}	Output Hold Time from Addresses, $\overline{CE}$f or $\overline{OE}$, Whichever Occurs First	0	—	0	—	ns
t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	20	—	20	µs

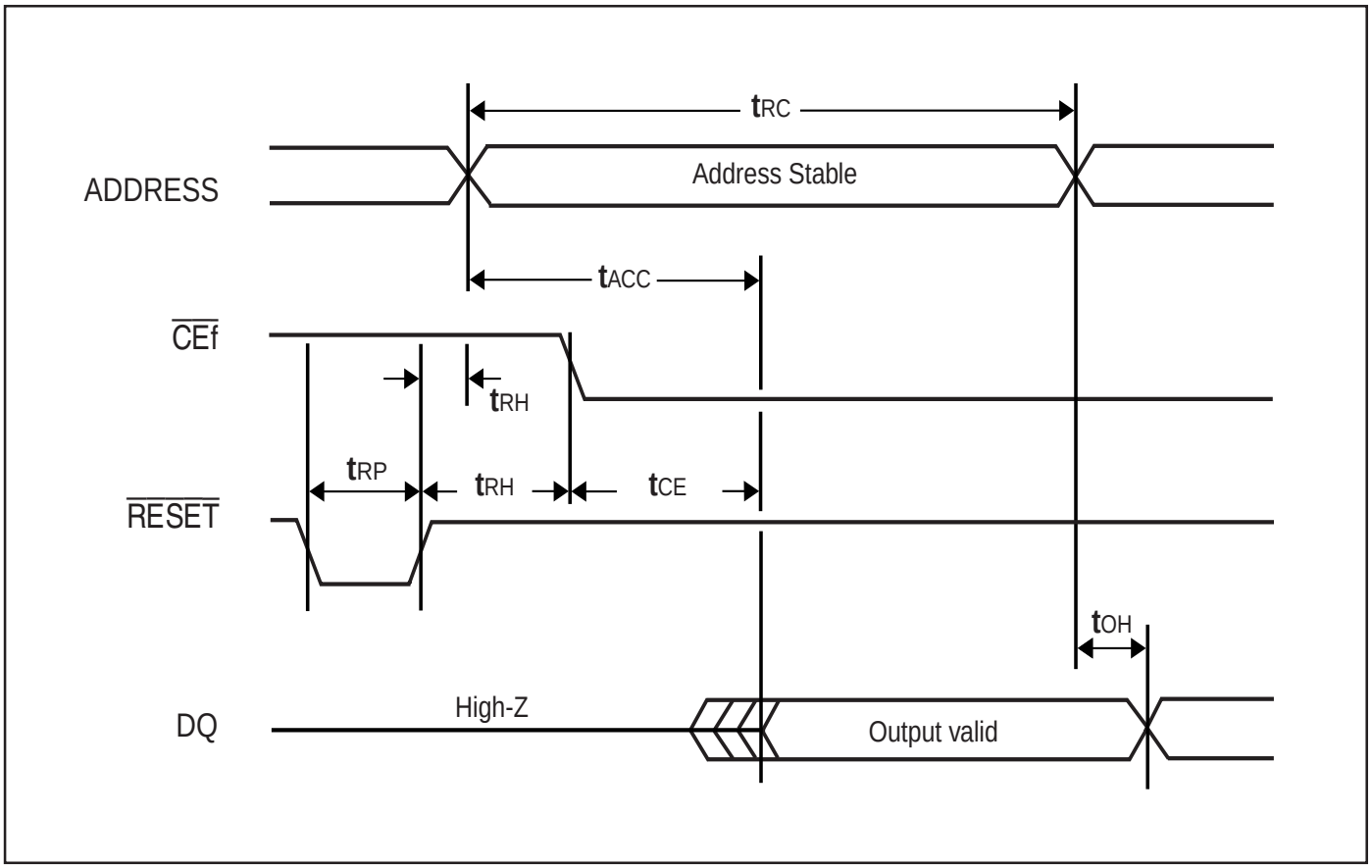
FLASH AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	1 TTL gate and 30pF

FLASH READ CYCLE



FLASH HARDWARE $\overline{\text{RESET}}$ / READ OPERATION TIMING DIAGRAM



FLASH ERASE/PROGRAM OPERATION CHARACTERISTICS

(Over Operating Range)

Symbol	Parameter	-70 ns		-85ns		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	70	-	85	-	ns
t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)	0	-	0	-	ns
t_{ASO}	Address Setup Time to $\overline{CE}$f Low During Toggle Bit Polling	12	-	15	-	ns
t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)	45	-	45	-	ns
t_{AHT}	Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling	0	-	0	-	ns
t_{DS}	Data Setup Time	30	-	35	-	ns
t_{DH}	Data Hold Time	0	-	0	-	ns
t_{OES}	Output Enable Setup Time	0	-	0	-	ns
t_{OEH}	Output Enable Hold Time Read	0	-	0	-	ns
t_{OEH}	Output Enable Hold Time Toggle and $\overline{Data}$ Polling	10	-	10	-	ns
t_{CEPH}	$\overline{CE}$f High During Toggle Bit Polling	20	-	20	-	ns
t_{OEPH}	$\overline{OE}$ High During Toggle Bit Polling	20	-	20	-	ns
t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)	0	-	0	-	ns
t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)	0	-	0	-	ns
t_{WS}	WE Setup Time (CEf to WE)	0	-	0	-	ns
t_{CS}	$\overline{CE}$f Setup Time (WE to CEf)	0	-	0	-	ns
t_{WH}	$\overline{WE}$ Hold Time (CEf to WE)	0	-	0	-	ns
t_{CH}	$\overline{CE}$f Hold Time (WE to CEf)	0	-	0	-	ns
t_{WP}	Write Pulse Width	30	-	35	-	ns
t_{CP}	$\overline{CE}$f Pulse Width	30	-	35	-	ns
t_{WPH}	Write Pulse Width High	25	-	30	-	ns
t_{CPH}	$\overline{CE}$f Pulse Width High	25	-	30	-	ns
t_{WHWH1}	Byte Programming Operation	-	12	-	15	µs
t_{WHWH1}	Word Programming Operation	-	15	-	20	µs
t_{WHWH2}	Sector Erase Operation (1)	-	0.7	-	1	s
t_{VCS}	V_{CC}f Setup Time	50	-	50	-	µs

Note:

1. This does not include the preprogramming time.

FLASH ERASE/PROGRAM OPERATION CHARACTERISTICS (Continued)

(Over Operating Range)

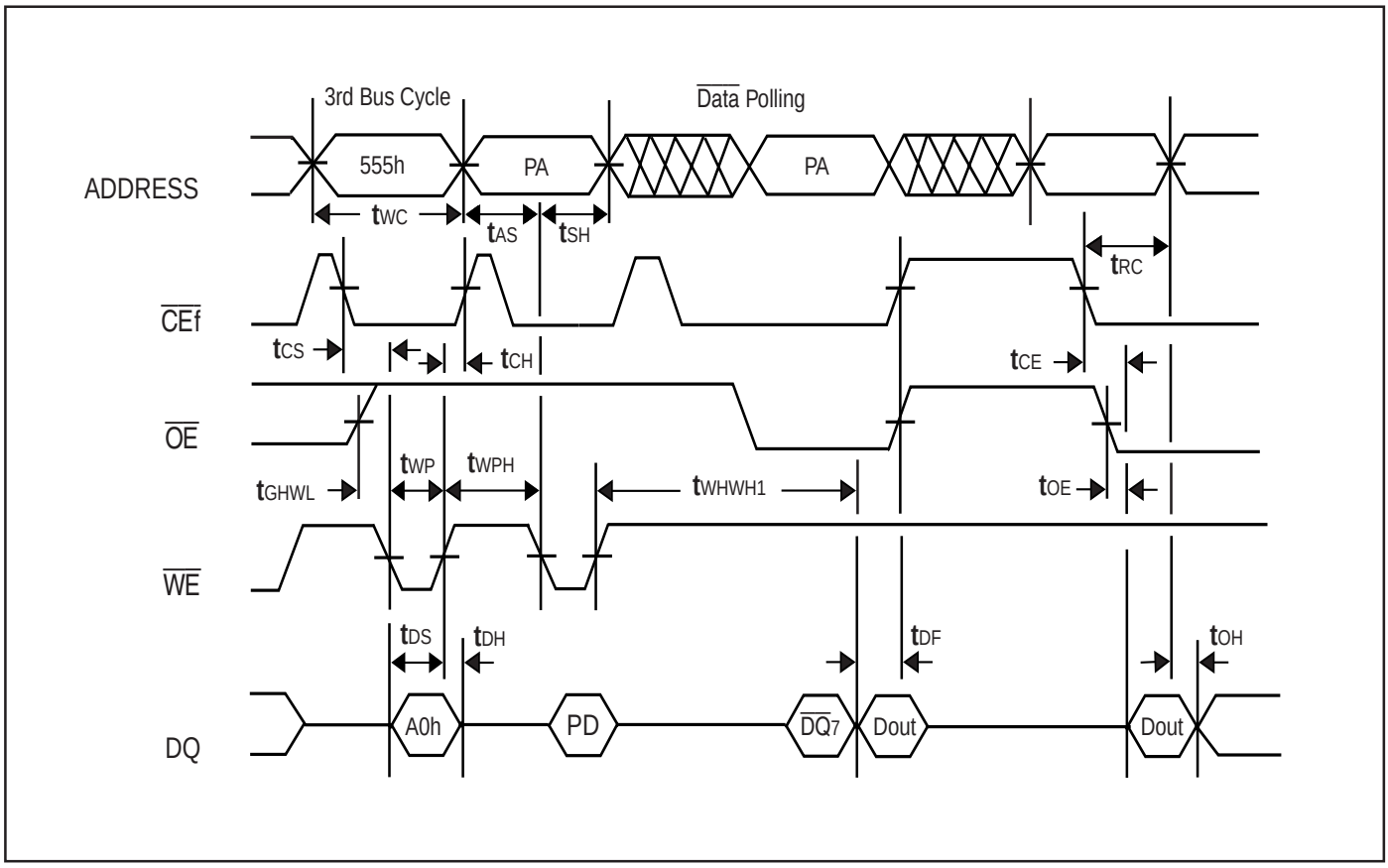
Symbol	Parameter	-70 ns Min.	-70 ns Max.	-85ns Min.	-85ns Max.	Unit
t_{VLHT}	Voltage Transition Time[2]	4	-	4	-	µs
t_{VIDR}	Rise Time to V_{ID}[2]	500	-	500	-	ns
t_{VACCA}	Rise Time to V_{ACC}	500	-	500	-	ns
t_{RB}	Recovery Time from RY/$\overline{BY}$	0	-	0	-	ns
t_{RP}	$\overline{RESET}$ Pulse Width	500	-	500	-	ns
t_{EOE}	Delay Time from Embedded Output Enable	-	70	-	85	ns
t_{RH}	$\overline{RESET}$ High Level Period Before Read	200	-	200	-	ns
t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	-	90	-	90	ns
t_{TOW}	Erase Time-out Time [3]	50	-	50	-	µs
t_{SPD}	Erase Suspend Transition Time [4]	-	20	-	20	µs

Note:

2. This timing is for Sector Protection Operation.
3. The time between writes must be less than “tTOW ” otherwise that command will not be accepted and erasure will start. A time-out or “tTOW ” from the rising edge of last $\overline{CE}$f or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s).
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of “tSPD ” to suspend the erase operation.

FLASH WRITE CYCLE

($\overline{WE}$ Control)

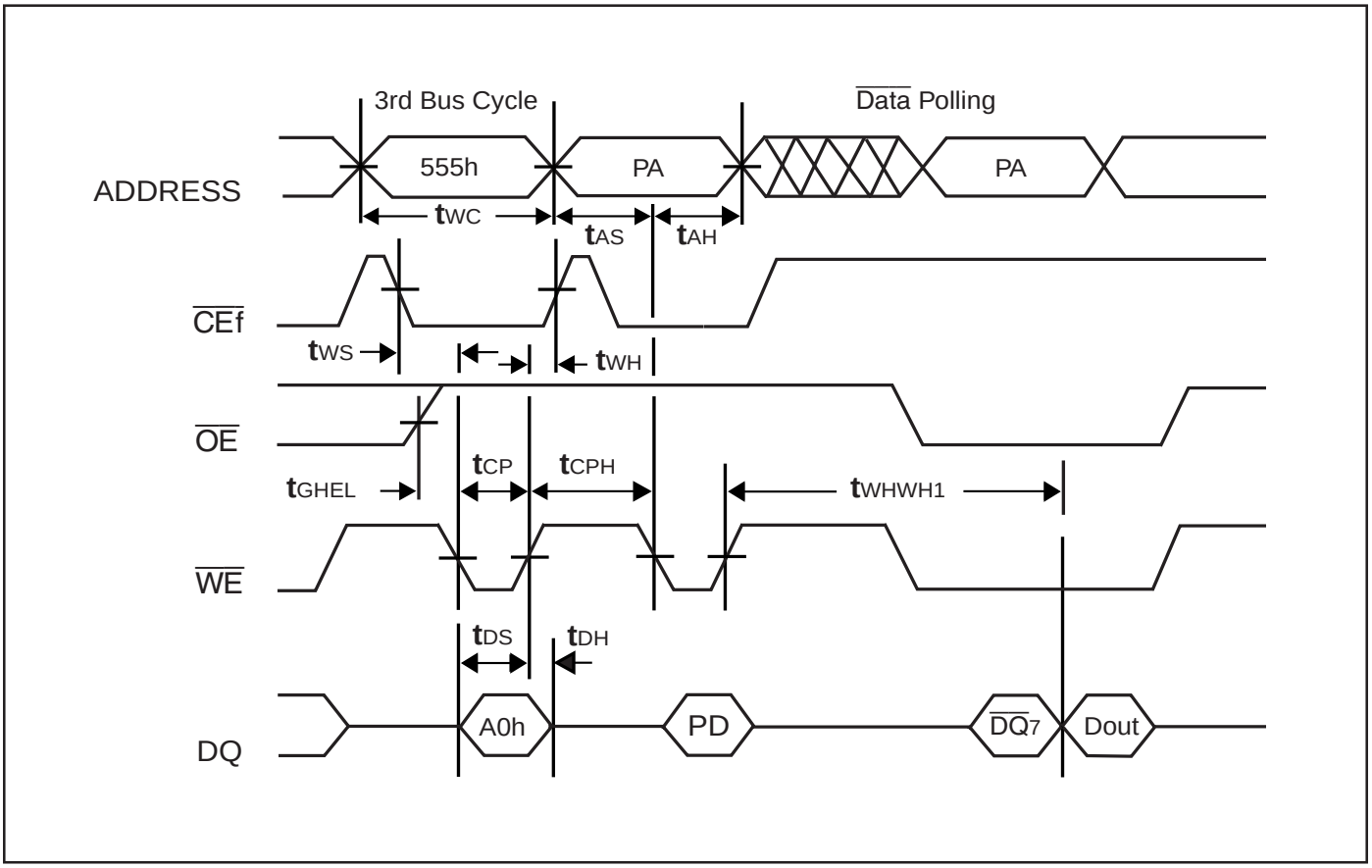


Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode (the addresses differ from ×8 mode, i.e. AAAh).

FLASH WRITE CYCLE

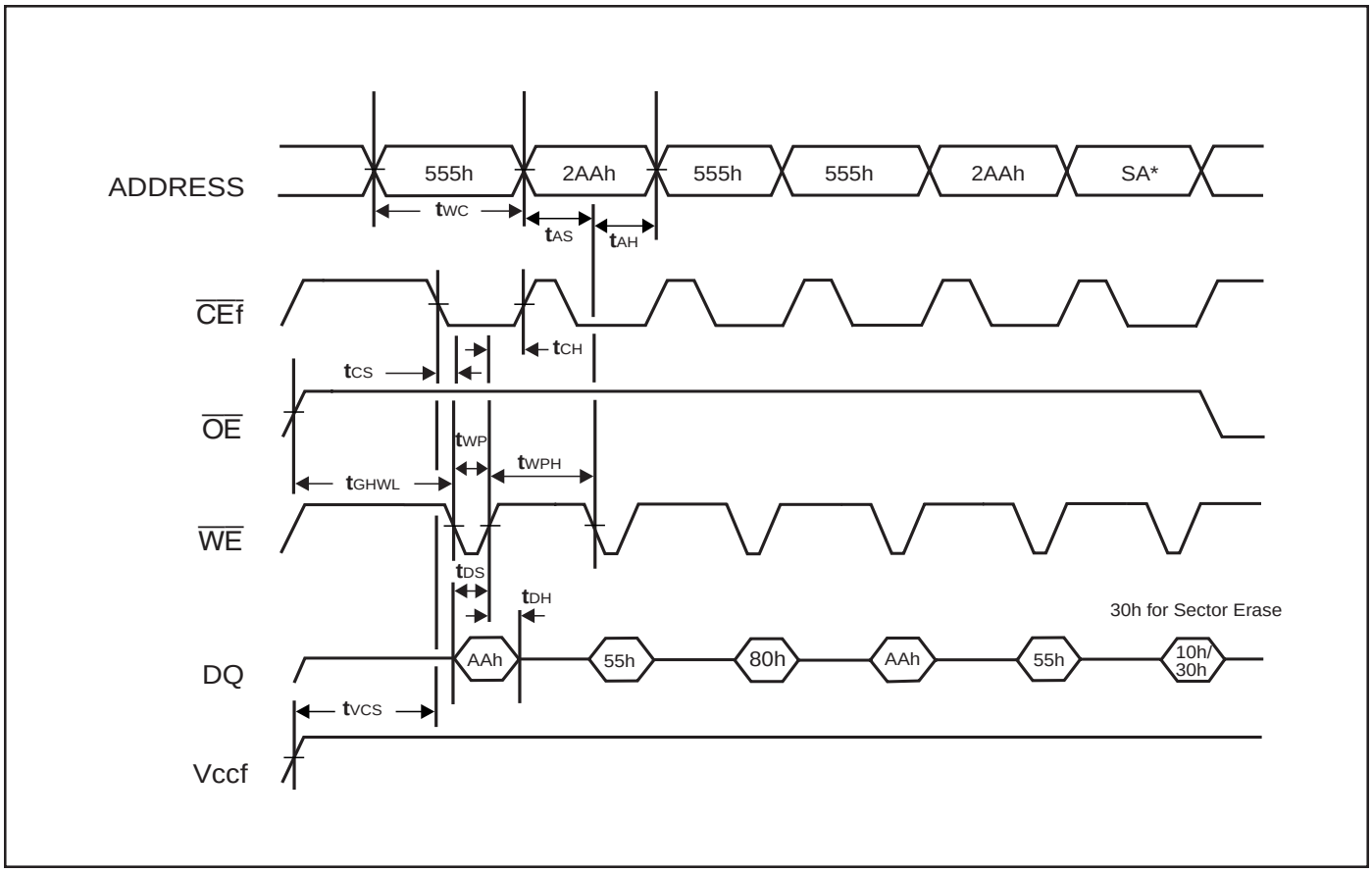
($\overline{CE}$f Control)



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. DQ7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode (the addresses differ from ×8 mode, i.e. AAAh).

FLASH AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

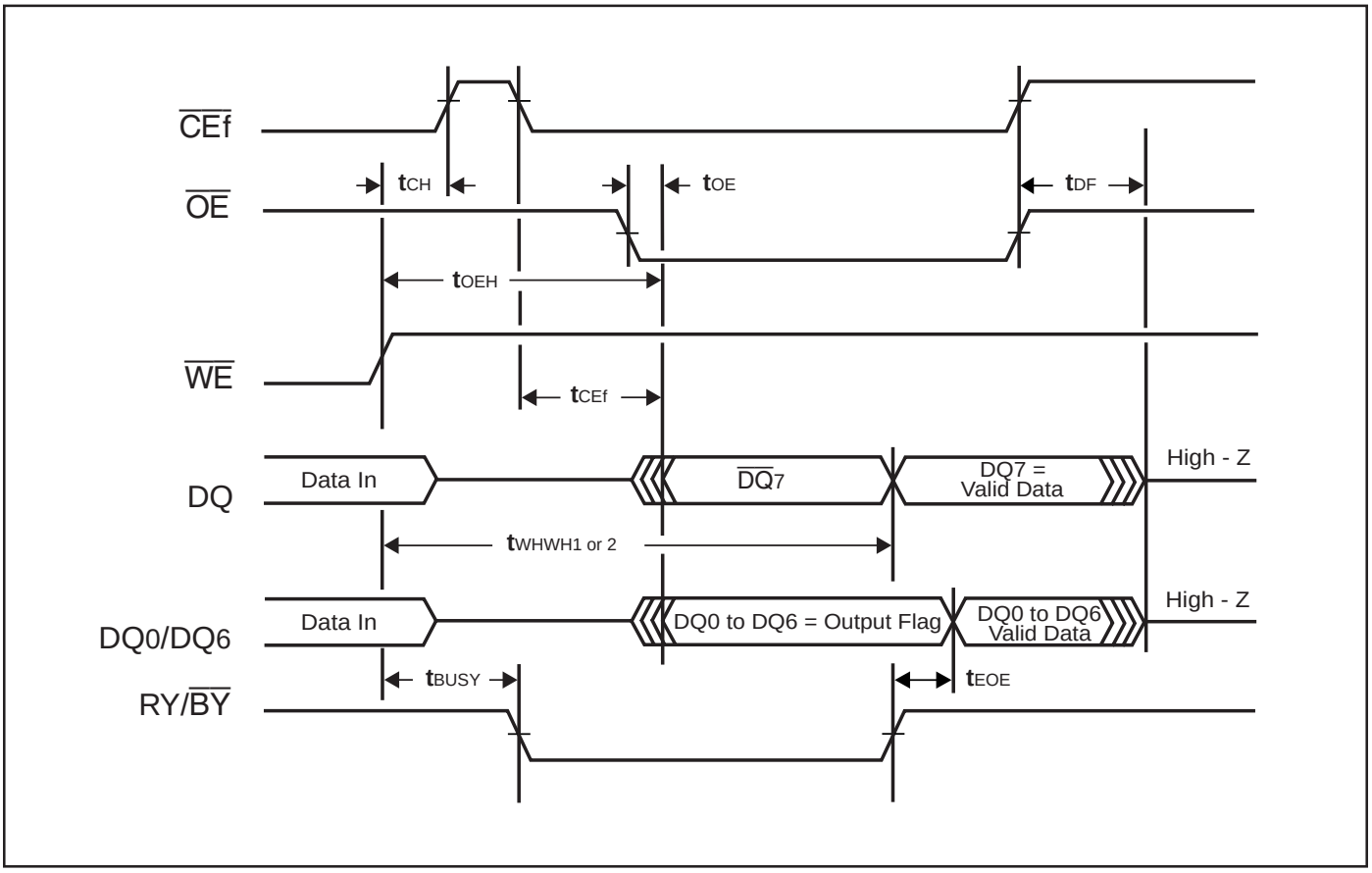


*SA is the sector address for Sector Erase. Address = 555h for Chip Erase.

Note:

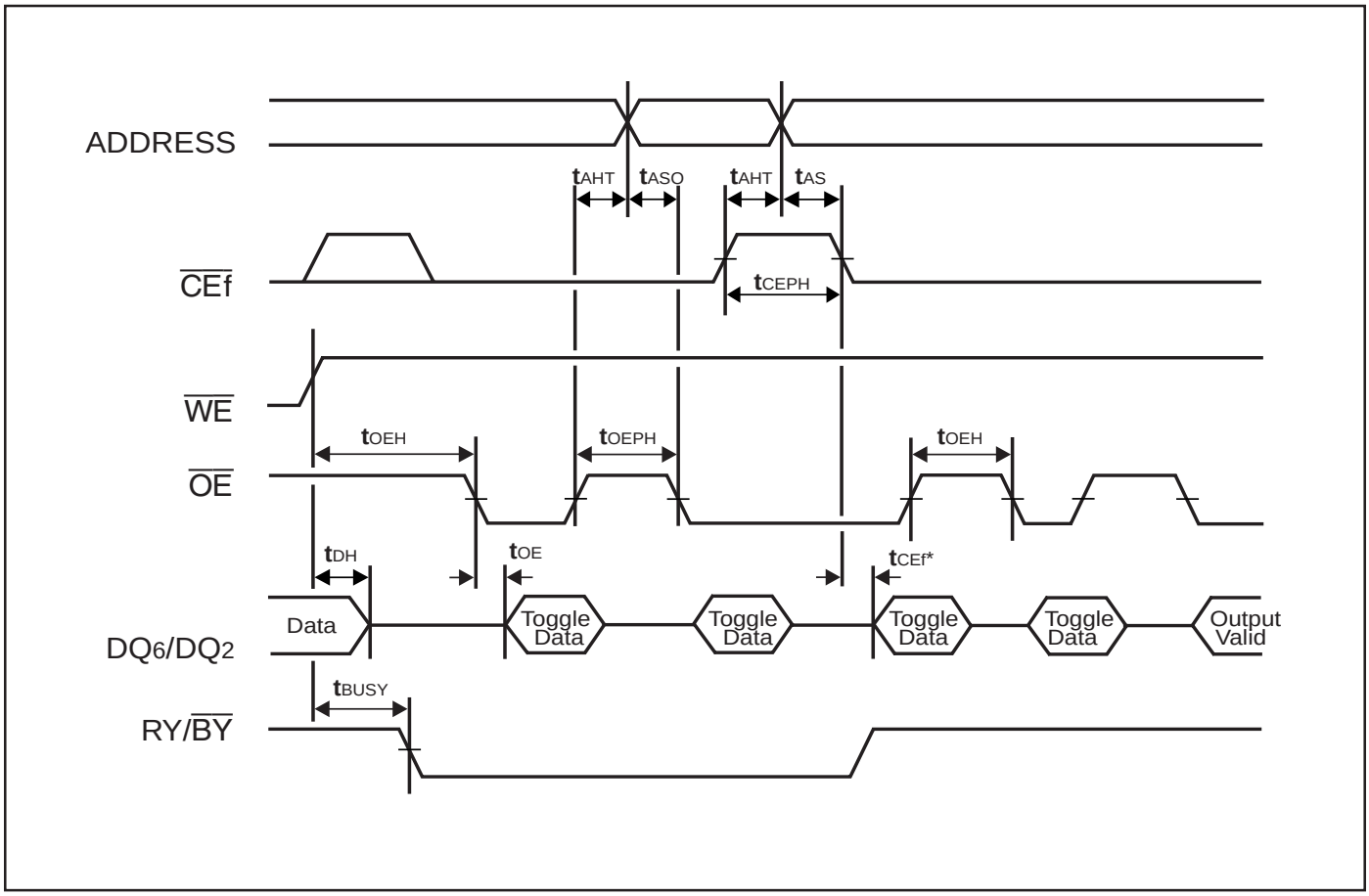
These waveforms are for the ×16 mode (the addresses differ from ×8 mode: AAAh, 555h, AAAh, AAAh, 555h, SA*).

FLASH AC WAVEFORMS
FOR DATA POLLING DURING EMBEDDED ALOGRITHM OPERATIONS



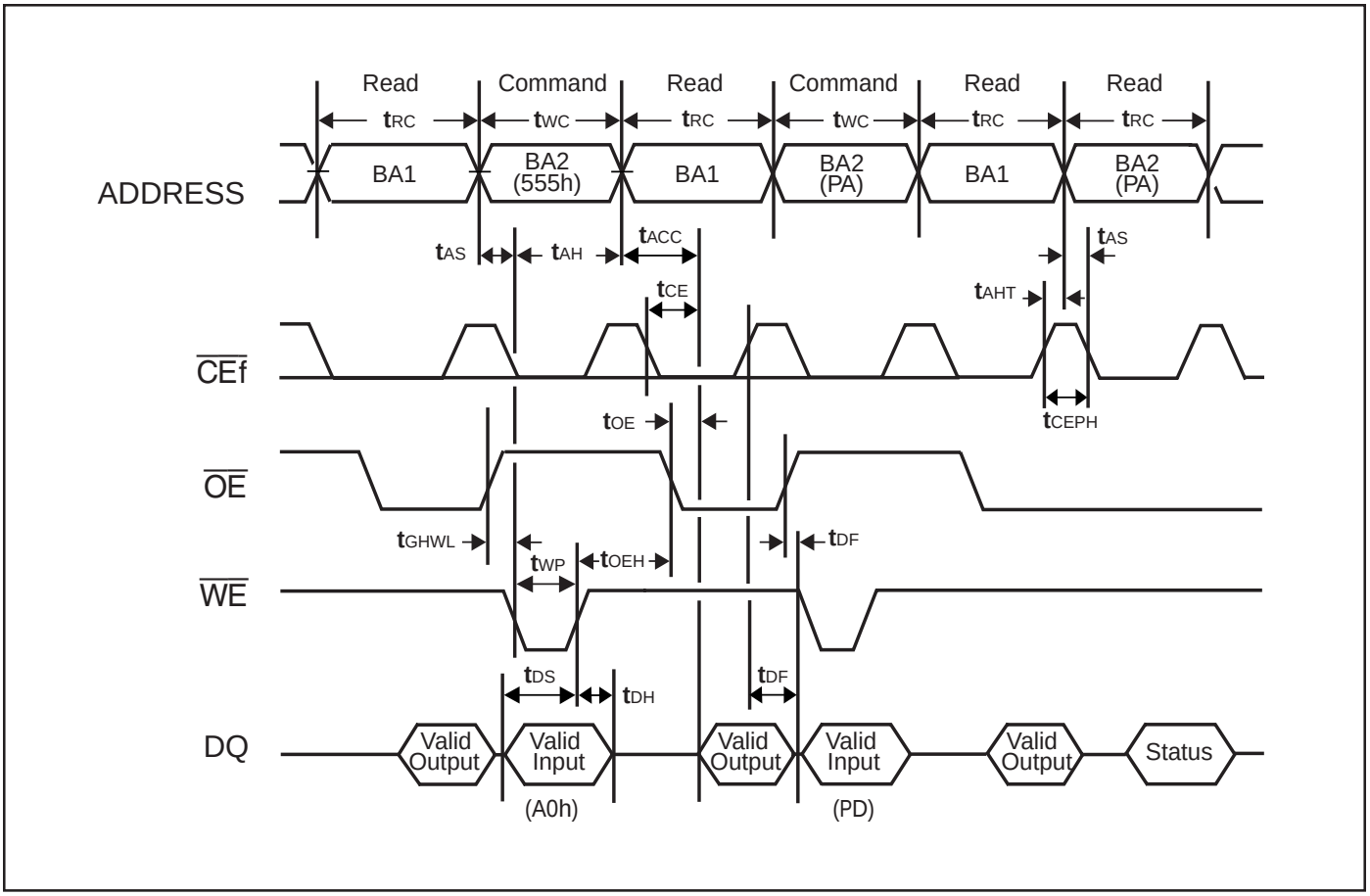
*DQ7 = Valid Data (the device has completed the Embedded operation.)

FLASH AC WAVEFORMS FOR TOGGLE BIT DURING EMBEDDED ALGORITHM OPERATIONS



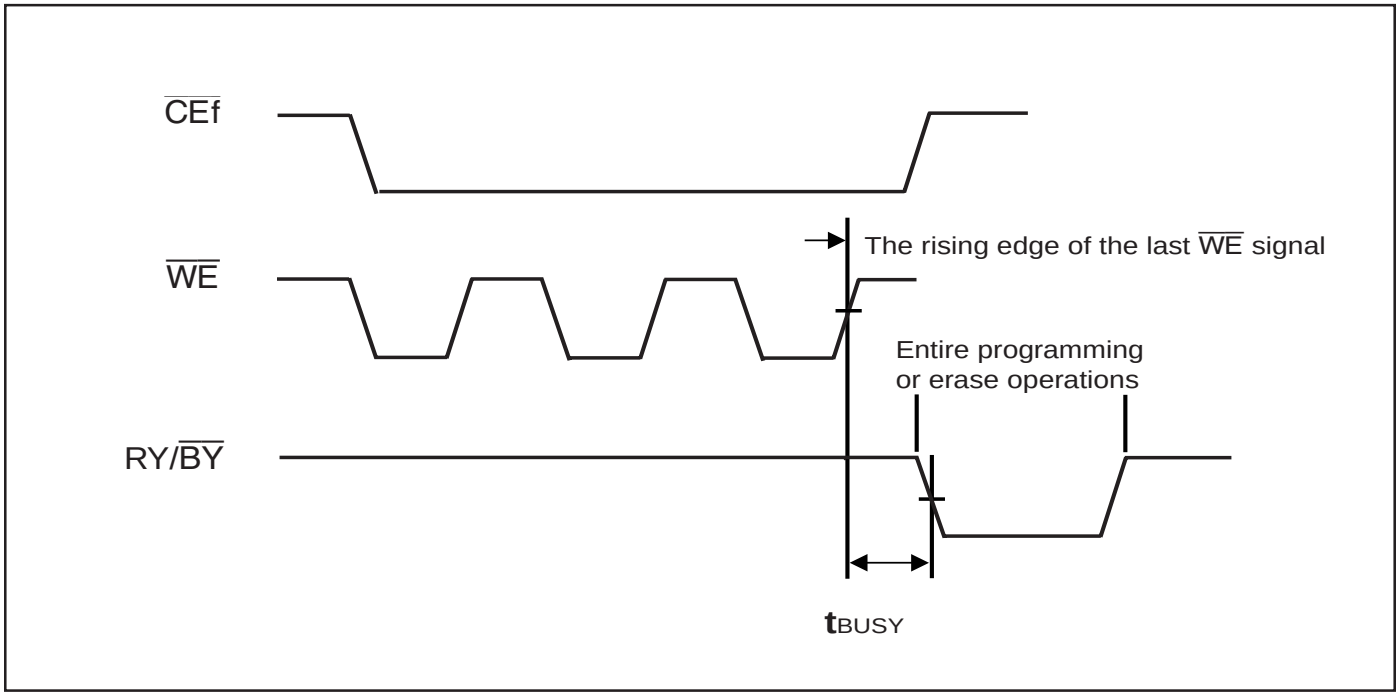
* DQ6 stops toggling (the device has completed the Embedded operation).

FLASH BACK-TO-BACK READ/WRITE TIMING DIAGRAM

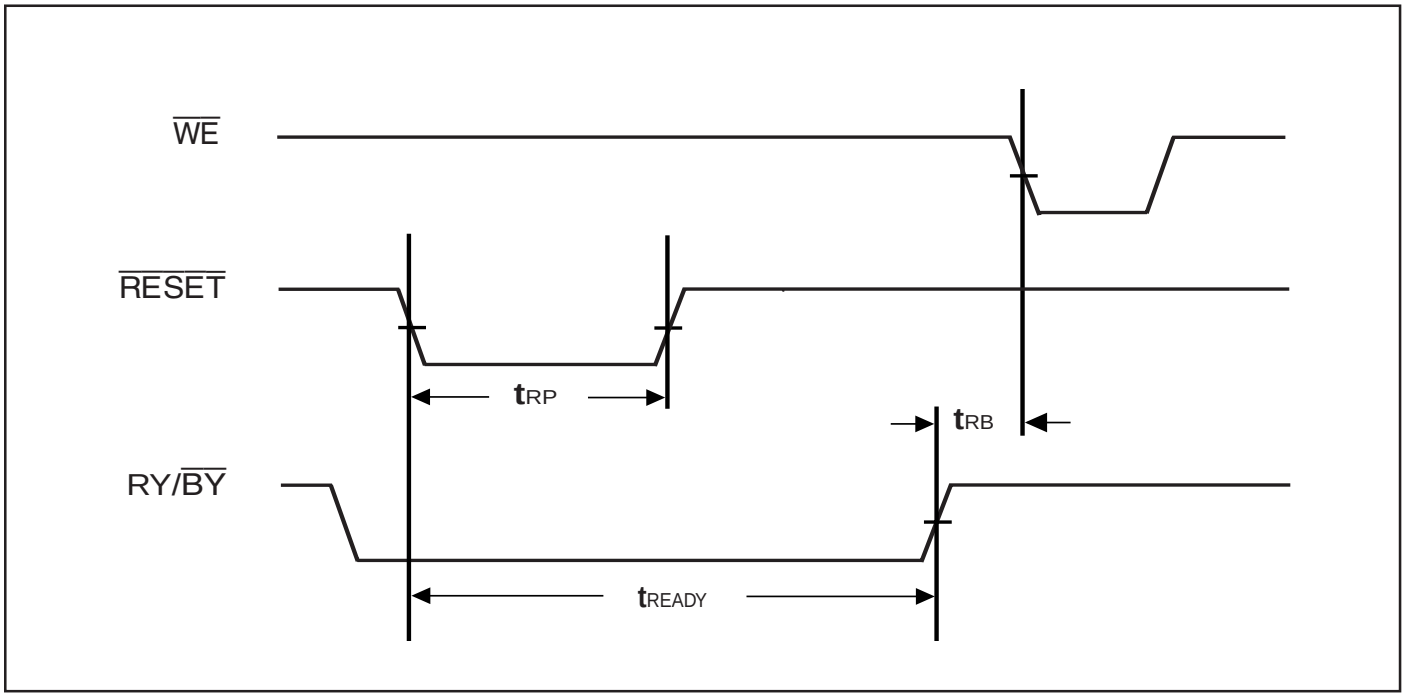


Note:
This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

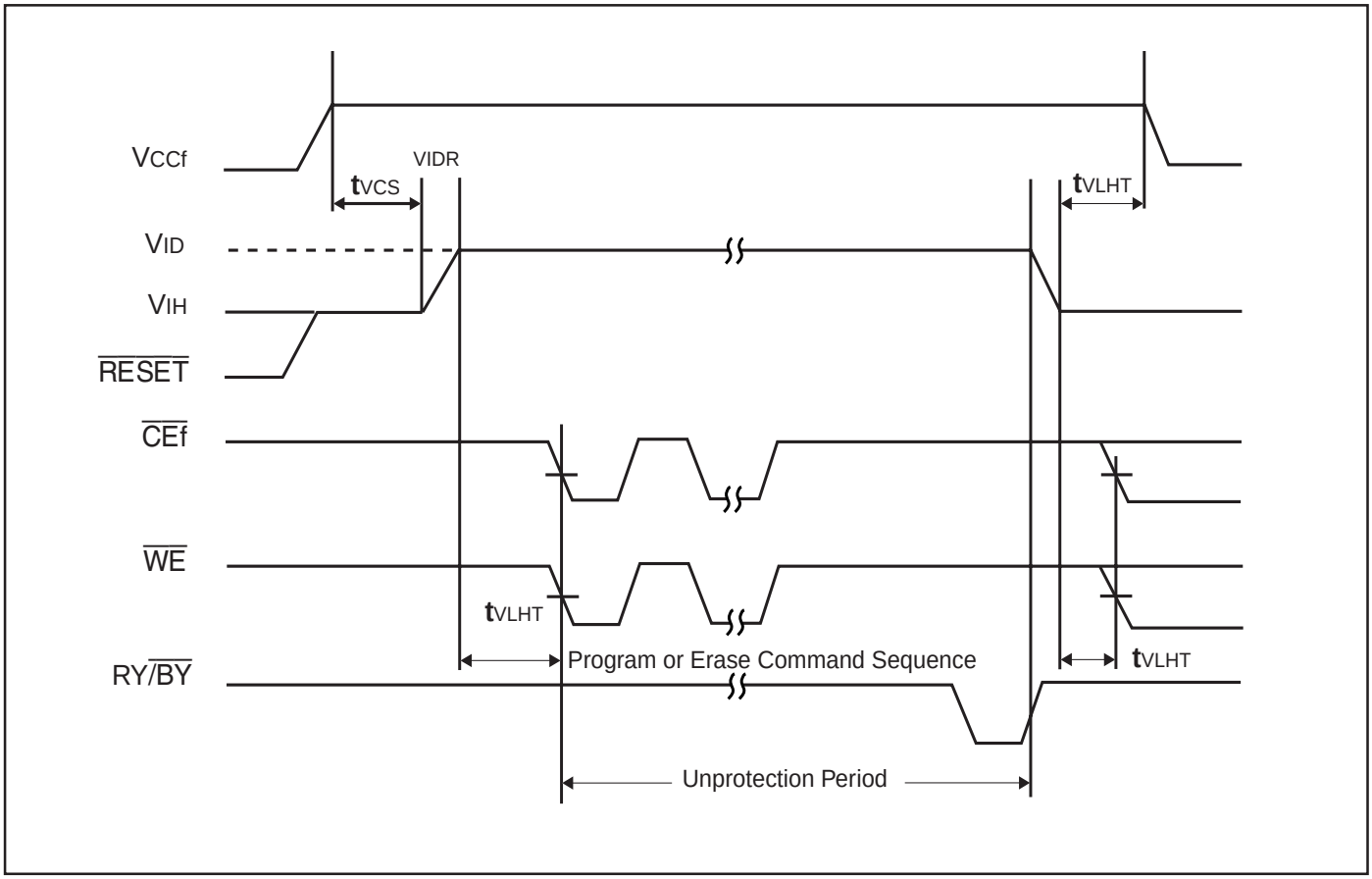
FLASH RY/$\overline{BY}$ TIMING DIAGRAM DURING WRITE/ERASE OPERATIONS



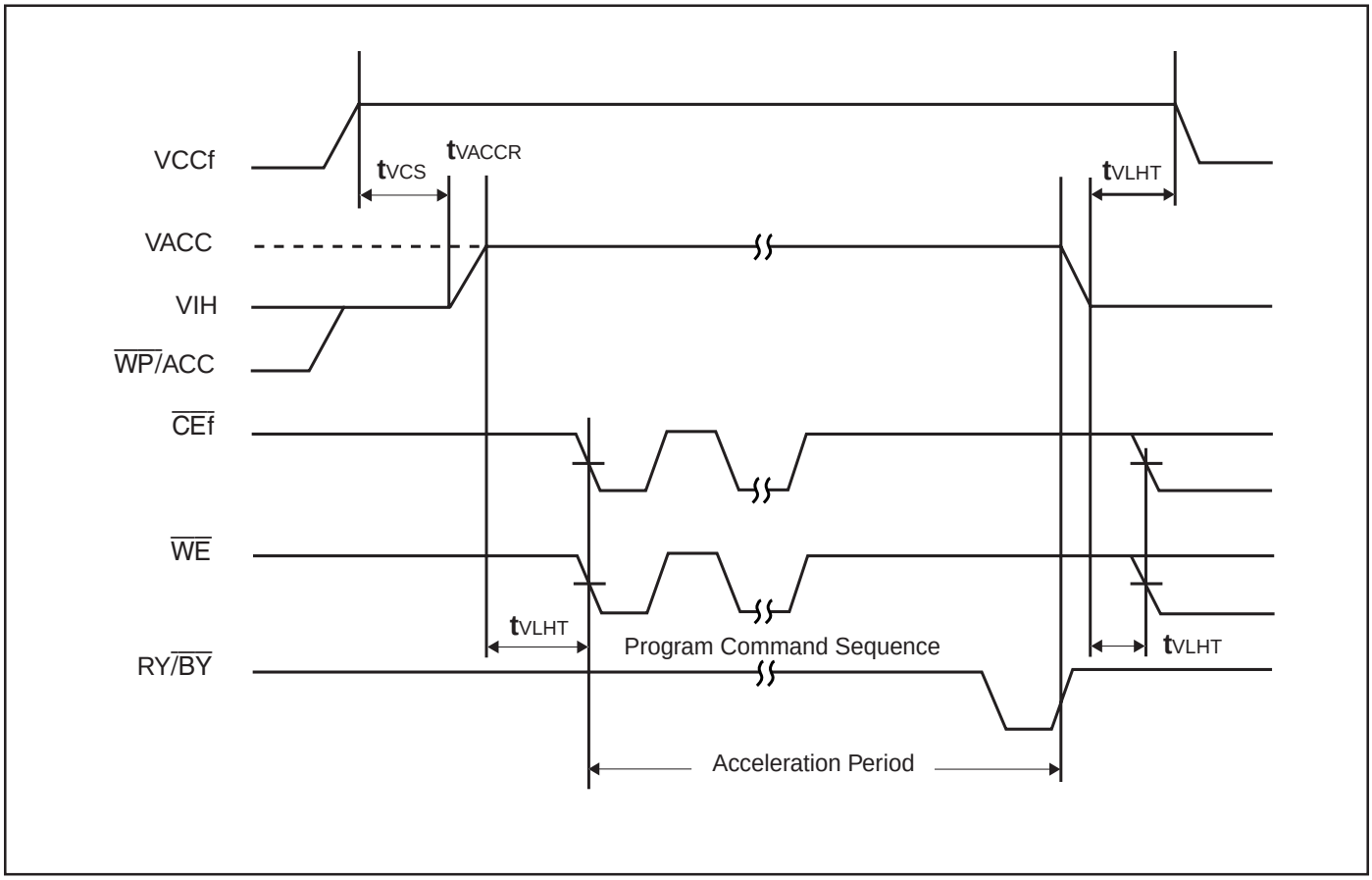
FLASH $\overline{RESET}$ RY/$\overline{BY}$ TIMING DIAGRAM



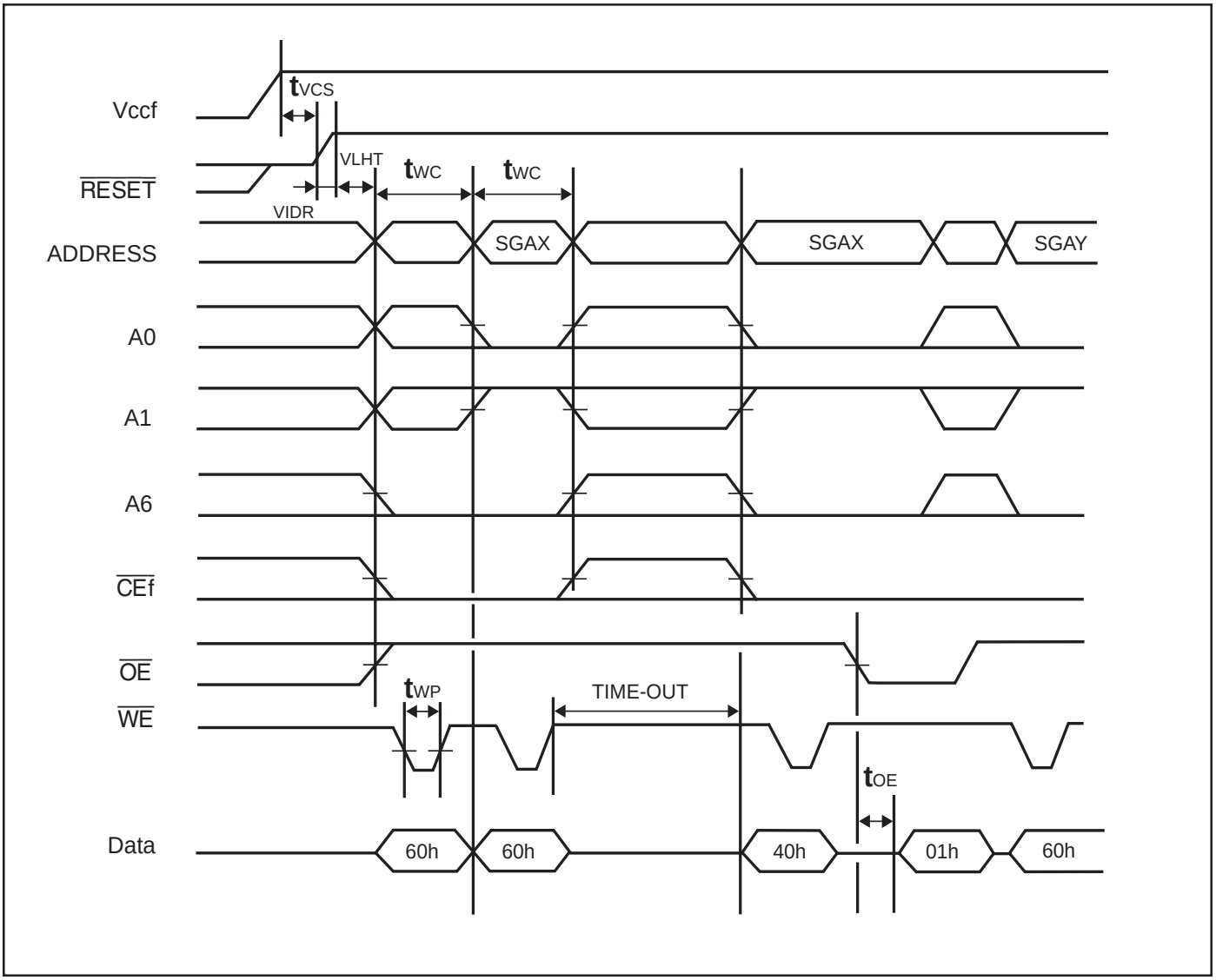
FLASH TEMPORARY SECTOR GROUP UNPROTECTION



FLASH ACCELERATED PROGRAM



FLASH EXTENDED SECTOR GROUP PROTECTION



SGAx: Sector Group Address to be protected. SGAy: Next Group Sector Address to be protected
UNPROTECTION: Implement with A6 = 1, A1 = 1, A0 = 0. Time-out approximately 15 ms.
TIME-OUT : Time-Out window = 250 µs (Min.)

SRAM POWER SUPPLY CHARACTERISTICS[1]

(Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CCS} = Max., I_{OUT} = 0 mA, f = f_{MAX}	—	40	mA
I_{CC1}	Operating Supply Current	V_{CCS} = Max., I_{OUT} = 0 mA, f = 0	—	8	mA
I_{SB}	CMOS Standby Current (CMOS Inputs)	V_{CCS} = Max., $\overline{CE1}_s \geq V_{CCS} - 0.2V$, $CE2_s \leq 0.2V$, $V_{IN} \geq V_{CCS} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	—	7	µA

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

SRAM READ CYCLE SWITCHING CHARACTERISTICS[1]

(Over Operating Range)

		70 ns		85ns		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	70	—	85	—	ns
t_{AA}	Address Access Time	—	70	—	85	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACE1}	$\overline{CE1}_s$ Access Time	—	70	—	85	ns
t_{DOE}	$\overline{OE}$ Access Time	—	35	—	45	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	25	—	35	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCE1}[2]	$\overline{CE1}_s$ to High-Z Output	0	25	0	35	ns
t_{LZCE1}[2]	$\overline{CE1}_s$ to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}_s$, $\overline{UB}_s$ Access Time	—	70	—	85	ns
t_{HZB}	$\overline{LB}_s$, $\overline{UB}_s$ to High-Z Output	0	25	0	50	ns
t_{LZB}	$\overline{LB}_s$, $\overline{UB}_s$ to Low-Z Output	0	—	0	—	ns

Notes:

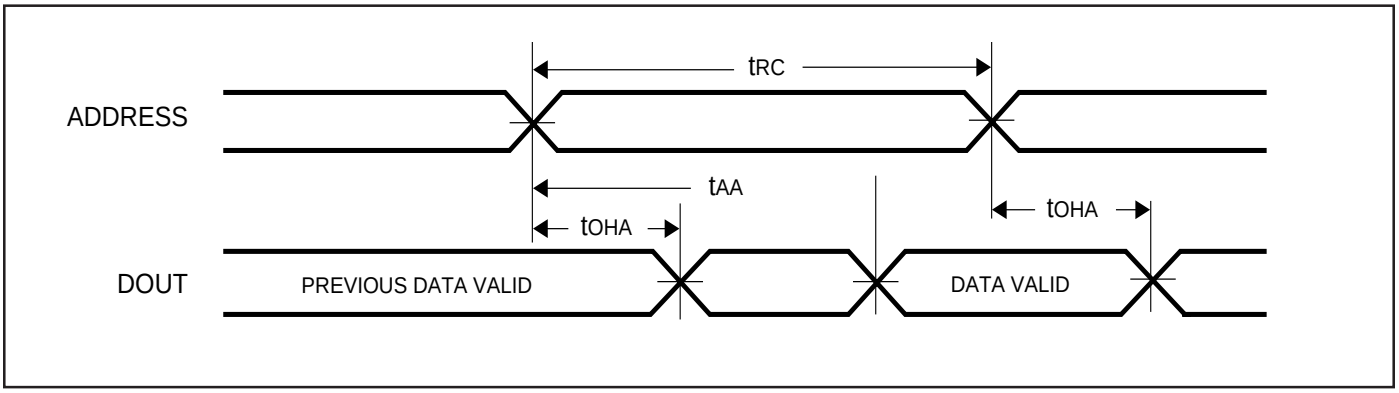
1. See SRAM AC TEST CONDITIONS.
2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

SRAM AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	1 TTL gate and 30pF

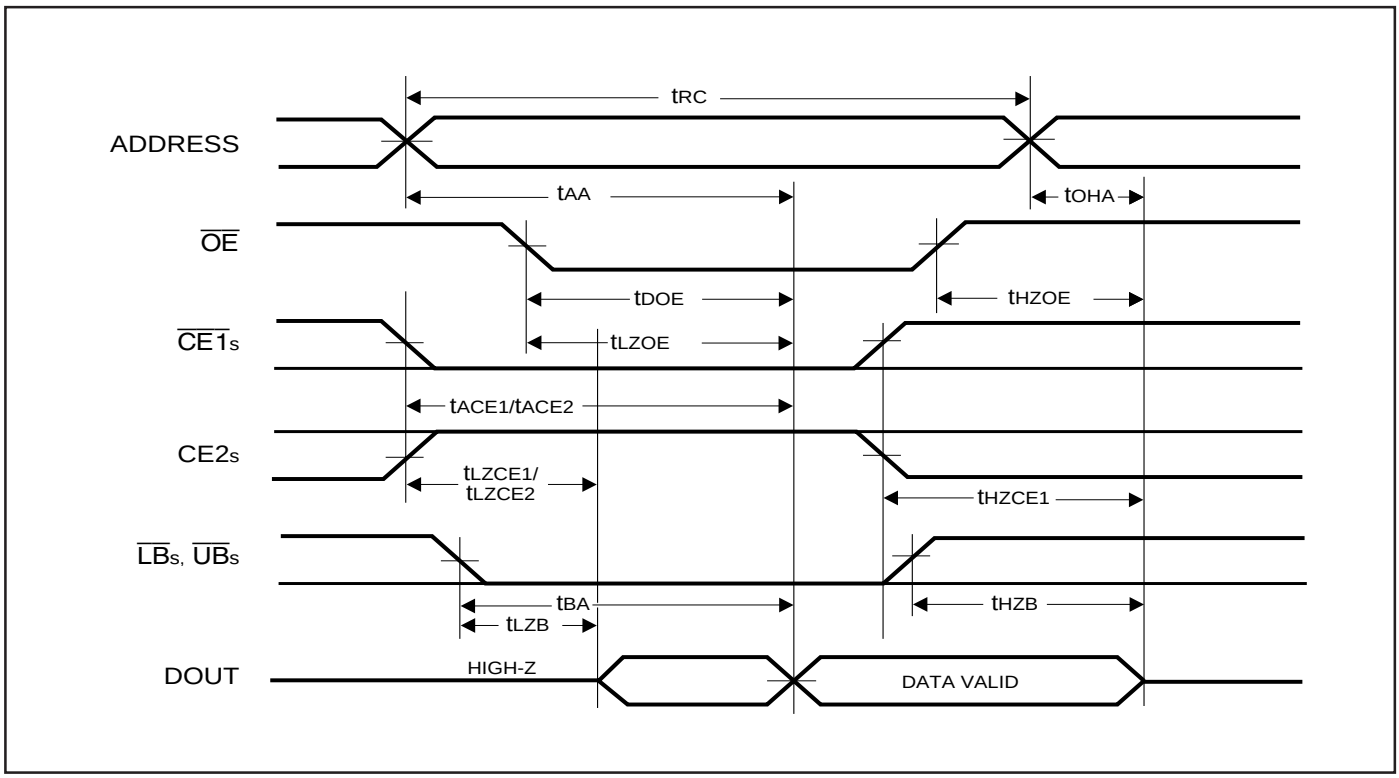
AC WAVEFORMS SRAM READ CYCLE NO. 1[1,2]

(Address Controlled) ($\overline{CE1}_s$ = $\overline{OE}$ = V_{IL}, $\overline{UB}_s$ or $\overline{LB}_s$ = V_{IL})



AC WAVEFORMS SRAM READ CYCLE NO. 2[1,3]

($\overline{CE1}_s$, $\overline{OE}$, AND $\overline{UB}_s$/ $\overline{LB}_s$ Controlled)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$, $\overline{UB}_s$, or $\overline{LB}_s$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2]

(Over Operating Range)

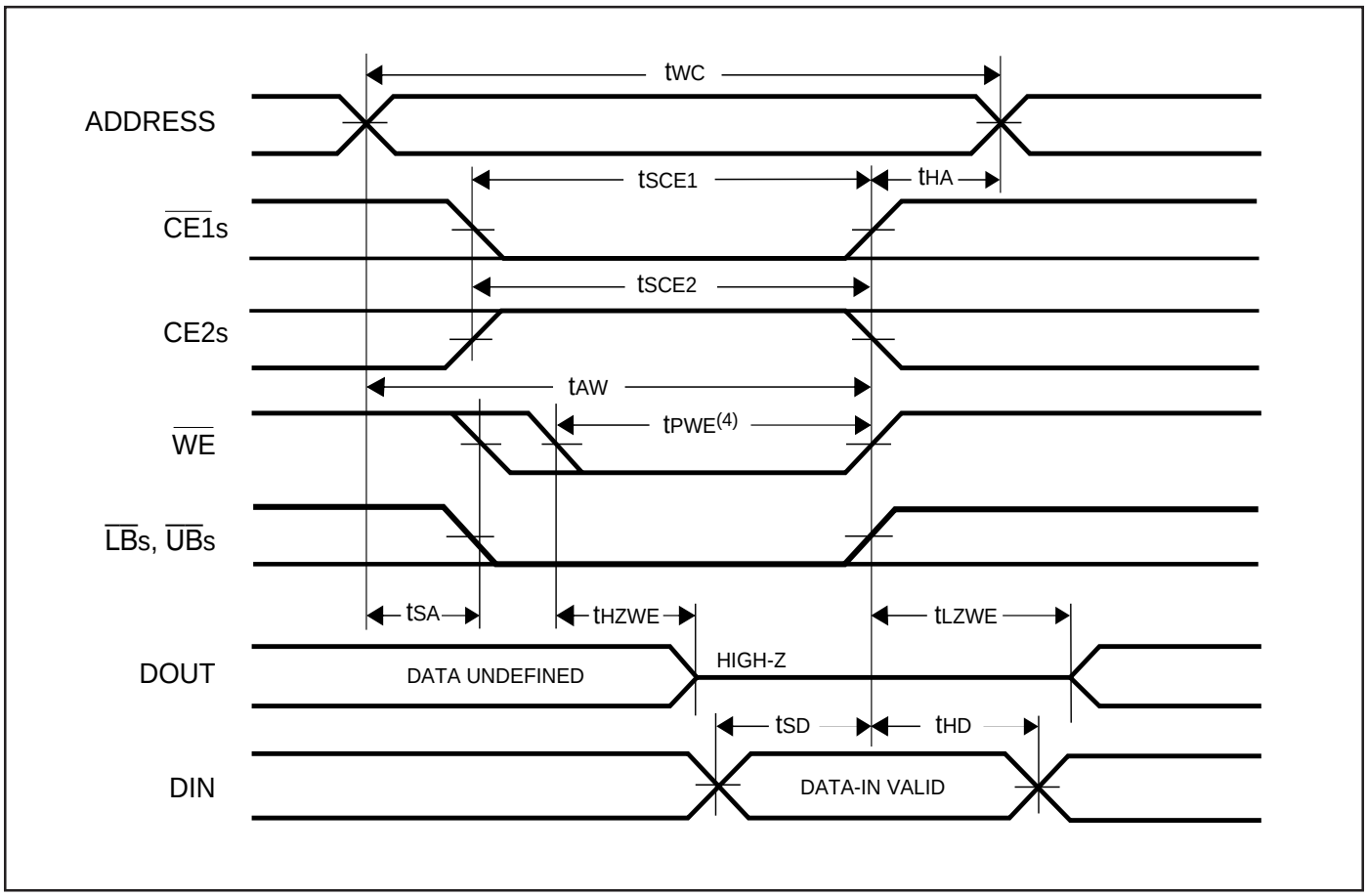
Symbol	Parameter	70ns Min.	70ns Max.	85ns Min.	85ns Max.	Unit
t_{WC}	Write Cycle Time	70	—	85	—	ns
t_{SCE1}	$\overline{CE1}_s$ to Write End	60	—	70	—	ns
t_{AW}	Address Setup Time to Write End	60	—	70	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}_s$,$\overline{UB}_s$ Valid to End of Write	60	—	70	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	50	—	60	—	ns
t_{SD}	Data Setup to Write End	30	—	35	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	25	—	35	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

Notes:

1. See SRAM AC TEST CONDITIONS.
2. The internal write time is defined by the overlap of $\overline{CE1}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS SRAM WRITE CYCLE NO. 1[1,2]

($\overline{CE1}_S$ Controlled, $\overline{OE}$ = HIGH or LOW)

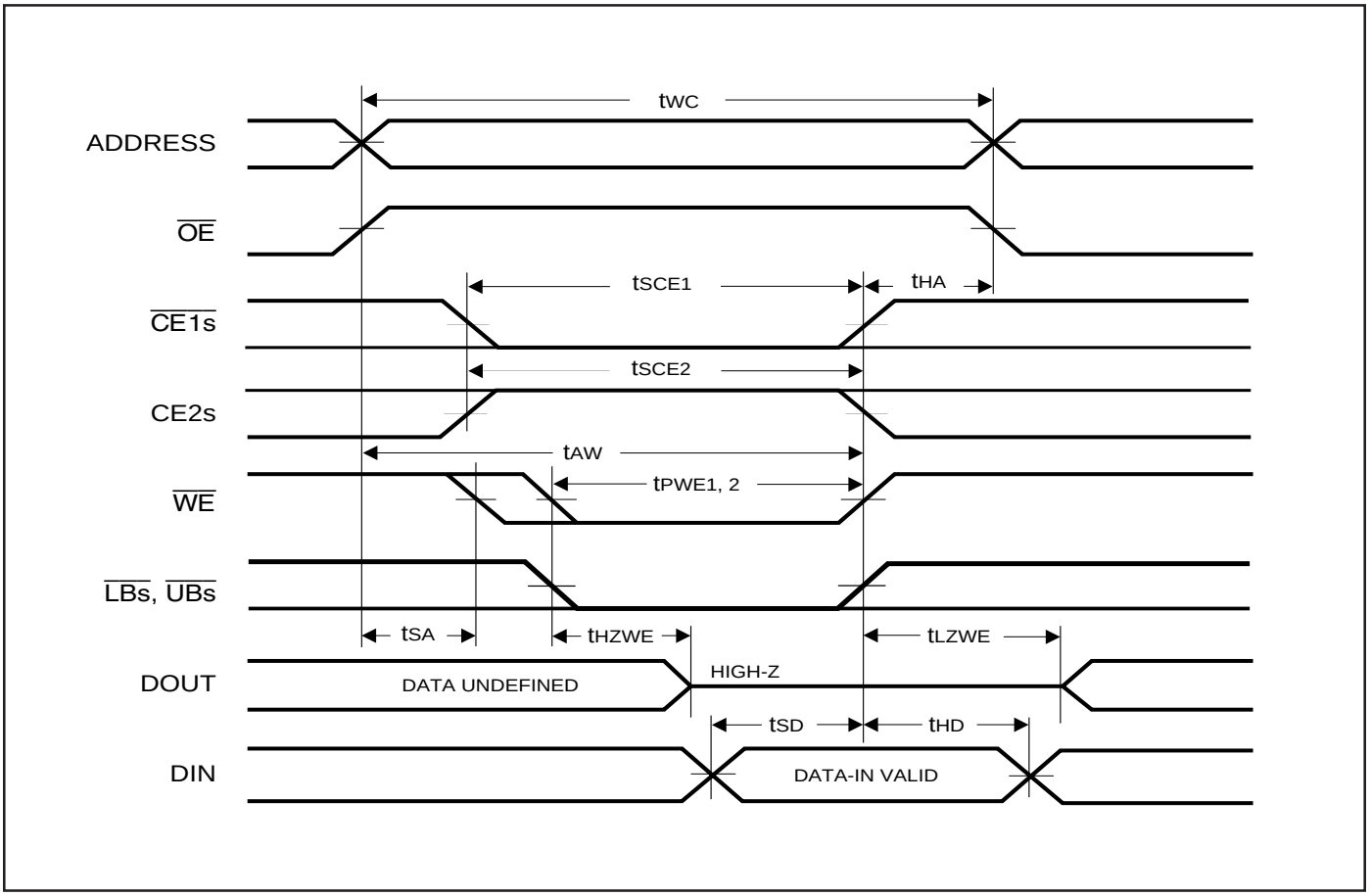


Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CE1}_s$ and $\overline{WE}$ inputs and at least one of the $\overline{LB}_s$ and $\overline{UB}_s$ inputs being in the LOW state.
2. WRITE = ($\overline{CE1}_s$) [($\overline{LB}_s$) = ($\overline{UB}_s$)] ($\overline{WE}$).

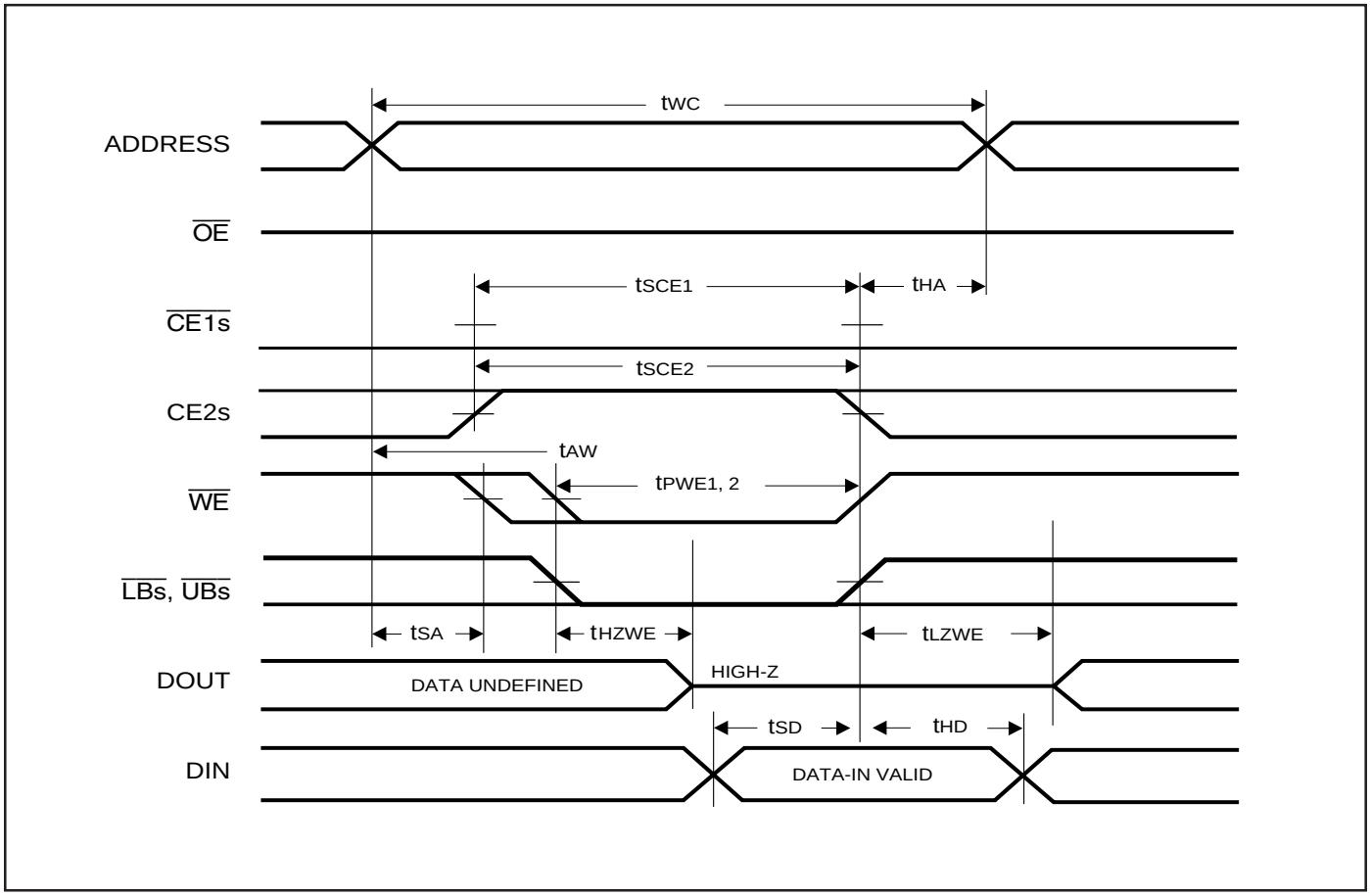
AC WAVEFORMS SRAM WRITE CYCLE NO. 2

($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



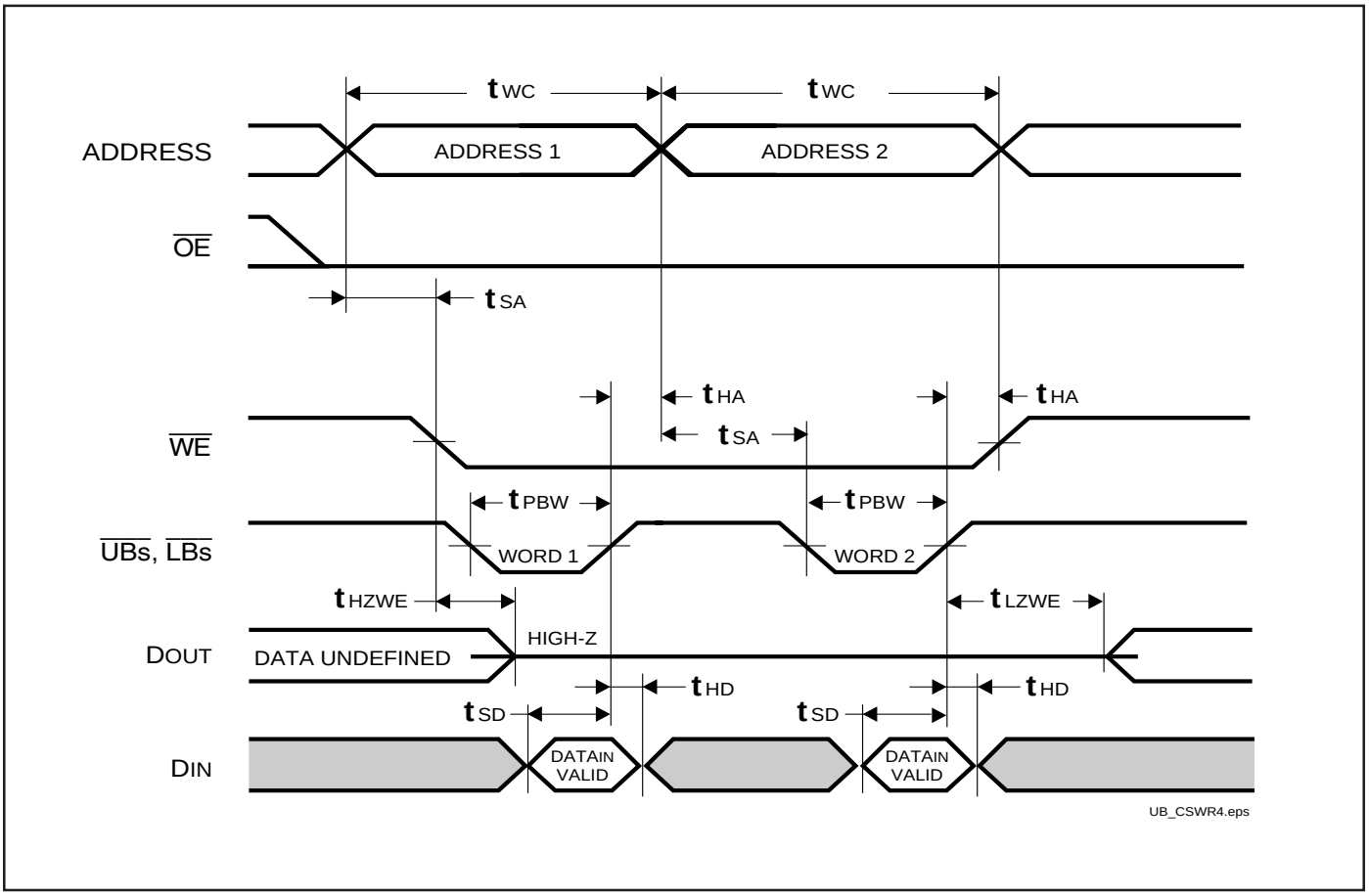
AC WAVEFORMS SRAM WRITE CYCLE NO. 3

($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4

($\overline{UB}_s$/$\overline{LB}_s$ Controlled, $\overline{CE1}$s is LOW, CE2s is HIGH)

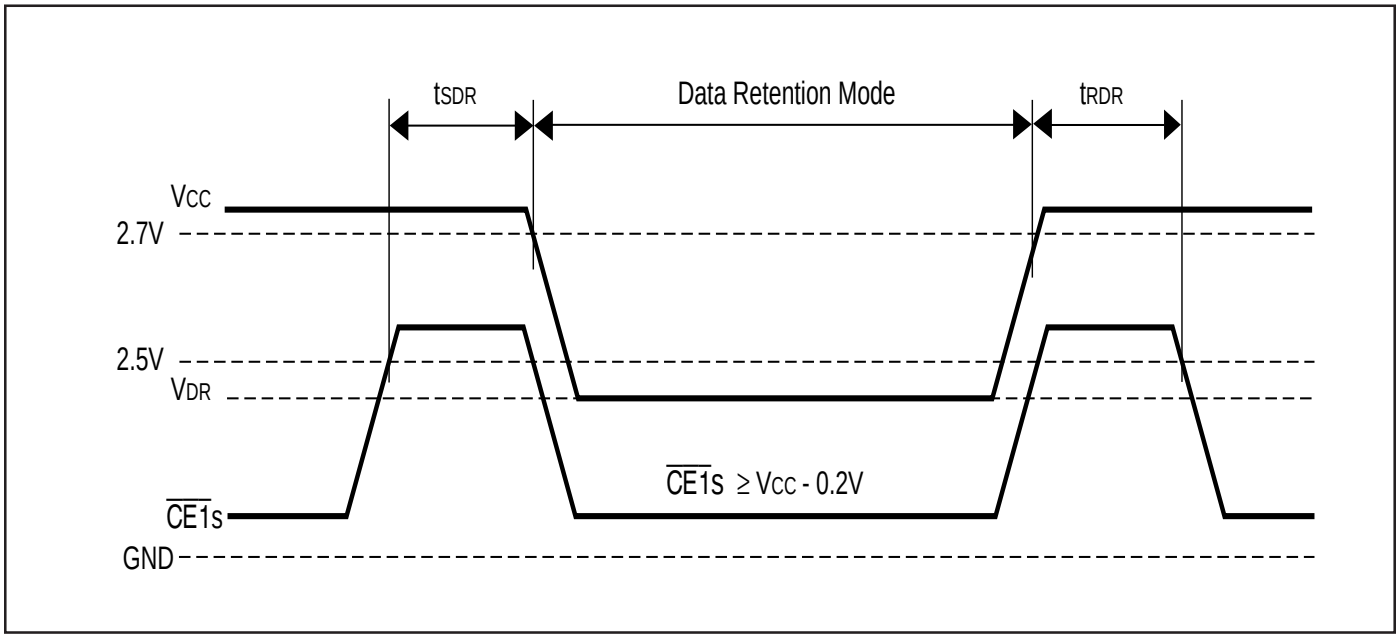


SRAM DATA RETENTION SWITCHING CHARACTERISTICS

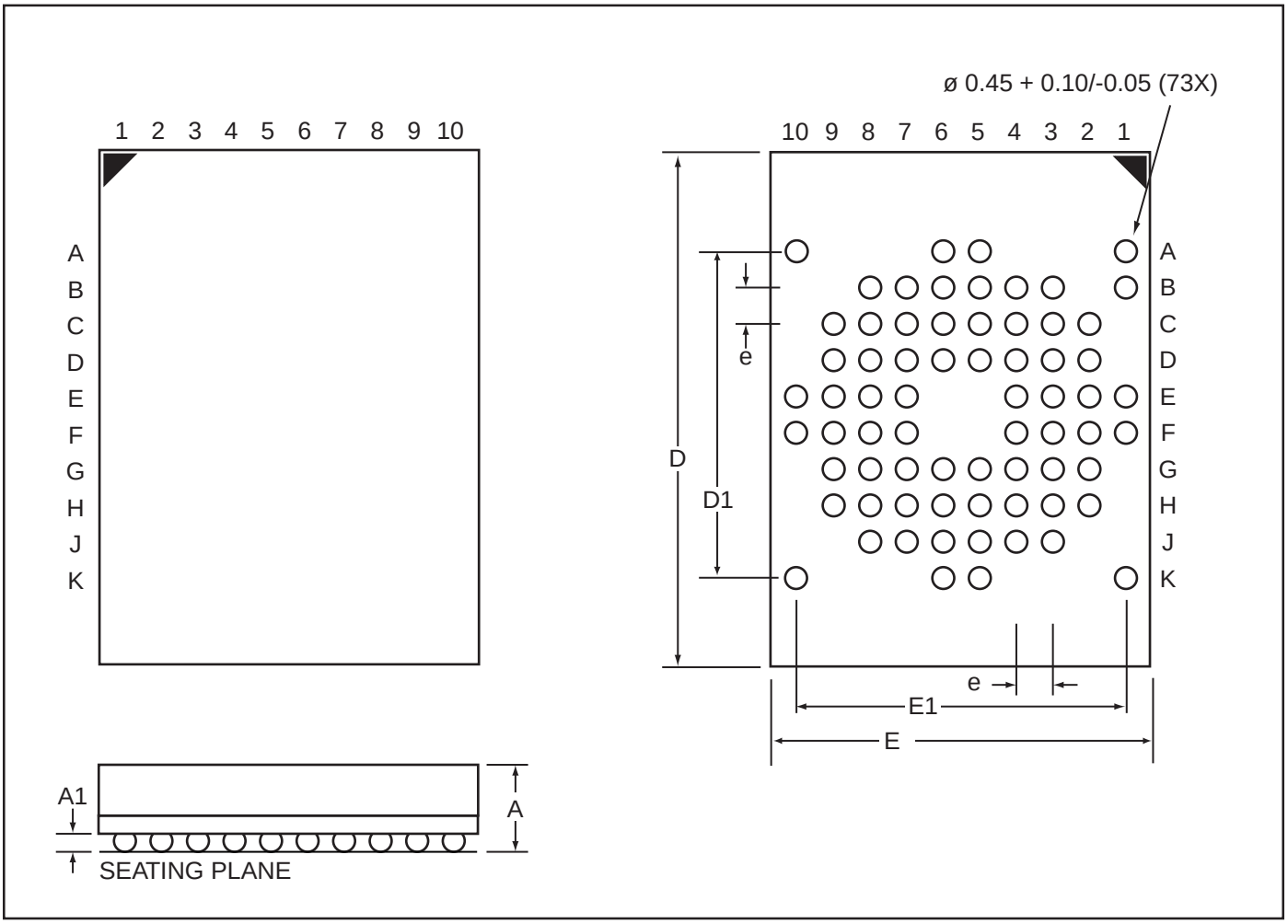
Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform	1.5	3.3	V
I_{DR}	Data Retention Current	Vcc = 1.5V, $\overline{CS1} \geq$ Vcc – 0.2V	—	7	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

SRAM DATA RETENTION WAVEFORM

($\overline{CE1}$ Controlled)

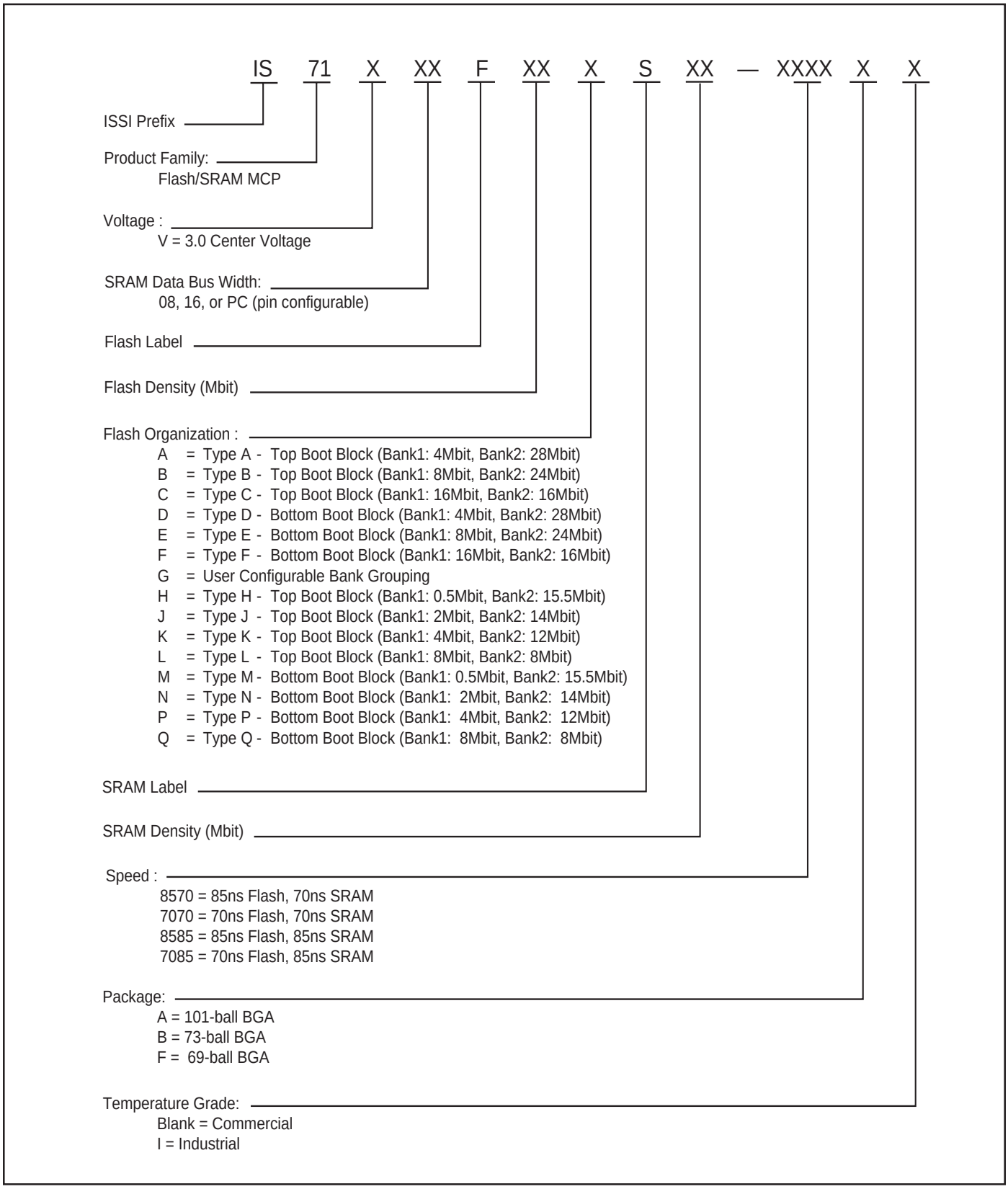


MINI BALL GRID ARRAY – 69-Ball BGA
PACKAGE CODE: F - **8.0 mm x 11.0 mm Body, 0.8 mm Ball Pitch**



Symbol	Min.	Typ.	Max.	Units
A	—	—	1.40	mm
A1	0.28	0.38	0.48	mm
D	11.50	11.00	11.10	mm
D1	—	7.20	—	mm
E	7.90	8.00	8.10	mm
E1	—	7.20	—	mm
e	—	0.80	—	mm

PART NUMBER LOGIC



ORDERING INFORMATION

Industrial Range: -25ºC to +85ºC

Order Part No.	SRAM Data Bus	Boot Section	Flash Bank Organization	Flash Speed (ns)	SRAM Speed (ns)	Package
IS71VPCF16HS04-8585FI	8/16	Top	0.5Mb, 15.5Mb	85	85	69-ball BGA
IS71VPCF16JS04-8585FI	8/16	Top	2Mb, 14Mb	85	85	69-ball BGA
IS71VPCF16KS04-8585FI	8/16	Top	4Mb, 12Mb	85	85	69-ball BGA
IS71VPCF16LS04-8585FI	8/16	Top	8Mb, 8Mb	85	85	69-ball BGA
IS71VPCF16MS04-8585FI	8/16	Bottom	0.5Mb, 15.5Mb	85	85	69-ball BGA
IS71VPCF16NS04-8585FI	8/16	Bottom	2Mb, 14Mb	85	85	69-ball BGA
IS71VPCF16PS04-8585FI	8/16	Bottom	4Mb, 12Mb	85	85	69-ball BGA
IS71VPCF16QS04-8585FI	8/16	Bottom	8Mb, 8Mb	85	85	69-ball BGA