SX-A Automotive Family FPGAs

FuseLock™

Specifications

- 12,000 to 108,000 Available System Gates
- Up to 360 User-Programmable I/O Pins
- Up to 2,012 Dedicated Flip-Flops
- 0.22µ CMOS Process Technology

Features

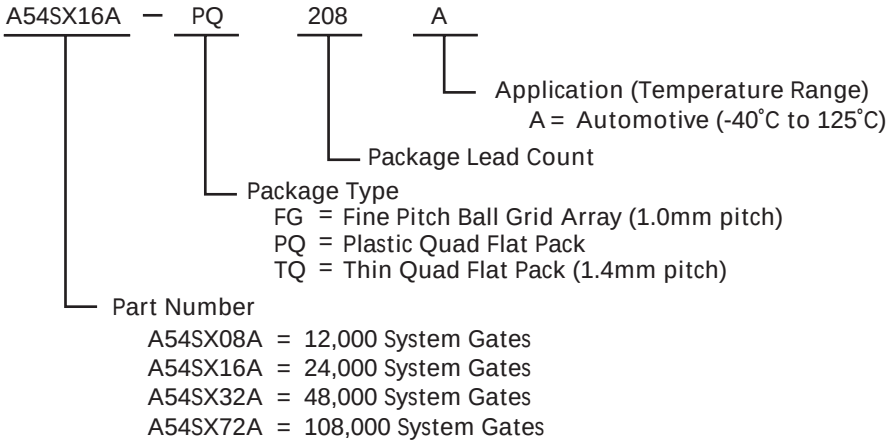
- 250 MHz Internal Performance
- Hot-Swap Compliant I/Os
- Power-up/down Friendly (No Sequencing Required for Supply Voltages)
- 66 MHz PCI Compliant
- Single-Chip Solution
- Nonvolatile
- Configurable I/O Support for 3.3V PCI, 3.3V LVTTL, 2.5V LVCMOS2
- Configurable Weak-Resistor Pull-up or Pull-down for Outputs at Power-up
- Individual Output Slew Rate Control
- Up to 100% Resource Utilization and 100% Pin Locking
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Actel's Secure Programming Technology with FuseLock™ Prevents Reverse Engineering and Design Theft

SX-A Automotive-Grade Product Profile

Device	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Capacity				
Typical Gates	8,000	16,000	32,000	72,000
System Gates	12,000	24,000	48,000	108,000
Logic Modules	768	1,452	2,880	6,036
Combinatorial Cells	512	924	1,800	4,024
Register Cells				
Dedicated Flip-Flops	256	528	1,080	2,012
Maximum Flip-Flops	512	990	1,980	4,024
Maximum User I/Os	130	180	249	360
Global Clocks	3	3	3	3
Quadrant Clocks	0	0	0	4
Boundary Scan Testing	Yes	Yes	Yes	Yes
3.3V PCI	Yes	Yes	Yes	Yes
Speed Grades	Std	Std	Std	Std
Temperature Grades*	A	A	A	A
Package (by pin count)				
PQFP	208	208	208	208
TQFP	100, 144	100, 144	100, 144	–
FBGA	144	144, 256	144, 256	256, 484

Note: **The SX-A family is also offered in commercial, industrial and military temperature grades with -F, -1, -2 and -3 speed grades, in addition to the Std speed grade. Refer to the SX-A Family FPGAs datasheet and HiRel SX-A Family FPGAs datasheet for more details.*

Ordering Information



Plastic Device Resources

Device	User I/Os (including clock buffers)					
	PQFP 208-Pin	TQFP 100-Pin	TQFP 144-Pin	FBGA 144-Pin	FBGA 256-Pin	FBGA 484-Pin
A54SX08A	130	81	113	111	–	–
A54SX16A	175	81	113	111	180	–
A54SX32A	174	81	113	111	203	–
A54SX72A	171	–	–	–	203	360

Note: *Contact your Actel sales representative for product availability.*
Package Definitions: *PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, FBGA = 1.0mm Fine Pitch Ball Grid Array*

Product Plan

	Speed Grade**					Application			
	–F	Std	–1	–2	–3	C	I†	M‡	A•
A54SX08A Device									
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	✔
A54SX16A Device									
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	✔
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	✔
A54SX32A Device									
100-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
144-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
176-Pin Thin Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	✔	–
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
208-Pin Ceramic Quad Flat Pack (CQFP)*	–	✔	✔	–	–	✔	–	✔	–
256-Pin Ceramic Quad Flat Pack (CQFP)*	–	✔	✔	–	–	✔	–	✔	–
144-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	✔
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	✔
329-Pin Plastic Ball Grid Array (PBGA)	✔	✔	✔	✔	✔	✔	✔	✔	–
484-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	–
A54SX72A Device									
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	✔	✔
208-Pin Ceramic Quad Flat Pack (CQFP)*	–	✔	✔	–	–	✔	–	✔	–
256-Pin Ceramic Quad Flat Pack (CQFP)*	–	✔	✔	–	–	✔	–	✔	–
256-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	✔
484-Pin Fine Pitch Ball Grid Array (FBGA)	✔	✔	✔	✔	✔	✔	✔	✔	✔

Contact your Actel sales representative for product availability. Refer to the SX-A Family FPGAs datasheet for more details on commercial, industrial and military grade offerings.

*For more information about the CQFP package options, refer to the HiRel SX-A datasheet at: *www.actel.com/documents/HRSXADS.pdf*

Applications: C = Commercial
I = Industrial
M = Military
A = Automotive

Availability: ✔ = Available

**Speed Grade: –1 = Approx. 15% faster than Standard
–2 = Approx. 25% faster than Standard
–3 = Approx. 35% faster than Standard
–F = Approx. 40% **slower** than Standard

† *Only Std, –1, –2 Speed Grade*

‡ *Only Std, –1 Speed Grade*

• *Only Std Speed Grade*

Table of Contents

General Description

Actel's SX-A family of FPGAs features a sea-of-modules architecture. SX-A devices simplify design time, enable dramatic reductions in design costs and power consumption, and further decrease time-to-market for performance-intensive applications. With the automotive temperature grade support (-40°C to 125°C), the SX-A devices can address many in-cabin telematics and automobile interconnect applications.

Actel's SX-A architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. The routing and interconnect resources are in the metal layers above the logic modules, providing optimal use of silicon. This enables the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules"), which reduces the distance signals have to travel between logic modules. To minimize signal propagation delay, SX-A devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (90 percent of connections typically use only three or fewer antifuses). The unique local and general routing structure featured in SX-A devices gives fast and predictable performance, allows 100% pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with minimum effort.

Further complementing SX-A's flexible routing structure is a hardwired, constantly loaded clock network that has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SX-A devices have easy-to-use I/O cells that do not require HDL instantiation, facilitating design re-use and reducing design and verification time.

SX-A Family Architecture

Programmable Interconnect Element

The SX-A family provides efficient use of silicon by locating the routing interconnect resources between the top two metal layers (Figure 1-1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

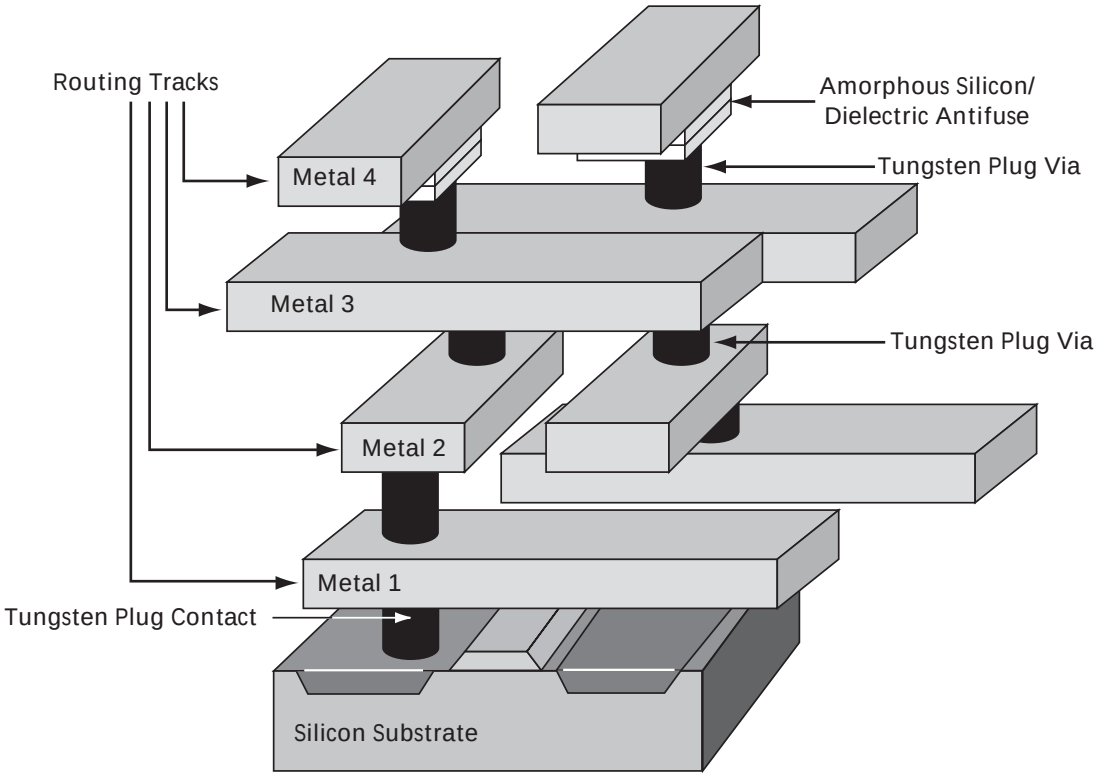
The extremely small size of these interconnect elements gives the automotive-grade SX-A devices abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and since SX-A is a nonvolatile, single-chip solution, there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design

The SX-A family architecture is described as a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's SX-A family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-2 on page 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the SX-A FPGA. The clock source for the R-cell can be chosen from either the hardwired clock, the routed clocks, or internal logic.



Note: *A54SX72A has four layers of metal with the antifuse between Metal 3 and Metal 4. A54SX08A, A54SX16A, and A54SX32A have three layers of metal with antifuse between Metal 2 and Metal 3.*

Figure 1-1 • **SX-A Family Interconnect Elements**

The C-cell implements a range of combinatorial functions of up to five inputs (Figure 1-3 on page 1-3). Inclusion of the DB input and its associated inverter function allows more than 4,000 combinatorial functions to be implemented in a single module in the SX-A architecture. The inverter function improves flexibility in the architecture; for instance a 3-input exclusive-OR function can be integrated into a single C-cell. At the same time, the C-cell structure is extremely synthesis friendly, simplifying the overall design and reducing synthesis time.

Two C cells can be combined together to create a flip-flop to imitate an R-cell via the user of the CC macro. This is particularly useful when implementing paths which are not timing-critical or if the designer needs more R-cells. More information about CC macro can be found in Actel's *Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros* Application Note.

Chip Architecture

The SX-A family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

The C-cell and R-cell logic modules are arranged into horizontal groups called Clusters. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

Clusters are further organized into SuperClusters for even better design efficiency and device performance (Figure 1-4 on page 1-4). SuperCluster 1 is a two-wide grouping of Type 1 Clusters. SuperCluster 2 is a two-wide group containing one Type 1 Cluster and one Type 2 Cluster. SX-A devices feature more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

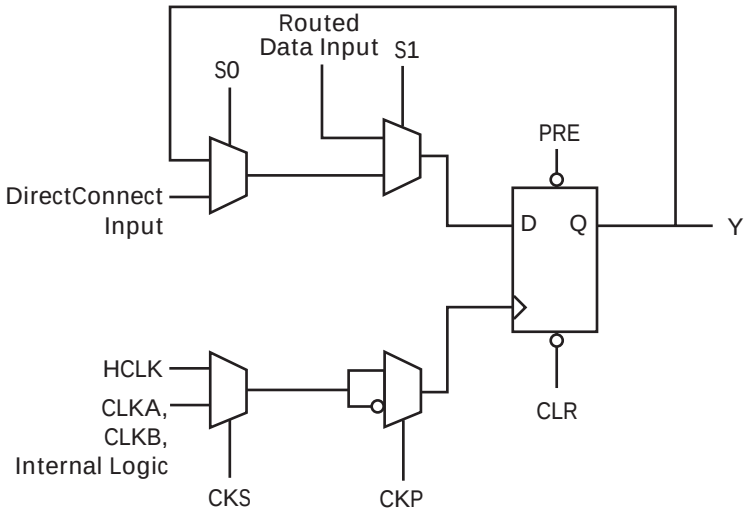


Figure 1-2 • **R-Cell**

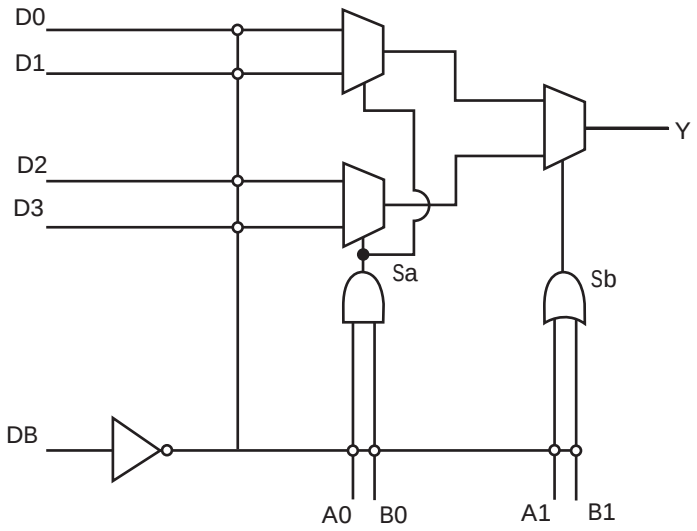


Figure 1-3 • **C-Cell**

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-5 on page 1-4 and Figure 1-6 on page 1-5). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hardwired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum pin-to-pin propagation time of 0.5 ns.

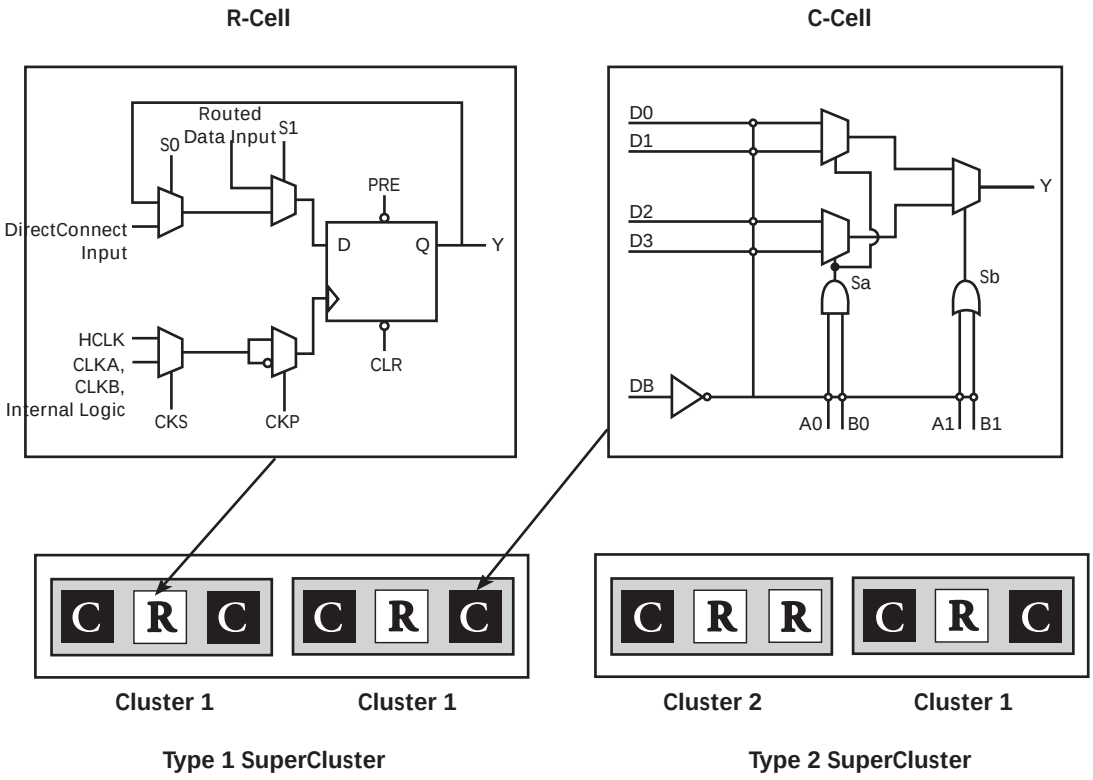


Figure 1-4 • **Cluster Organization**

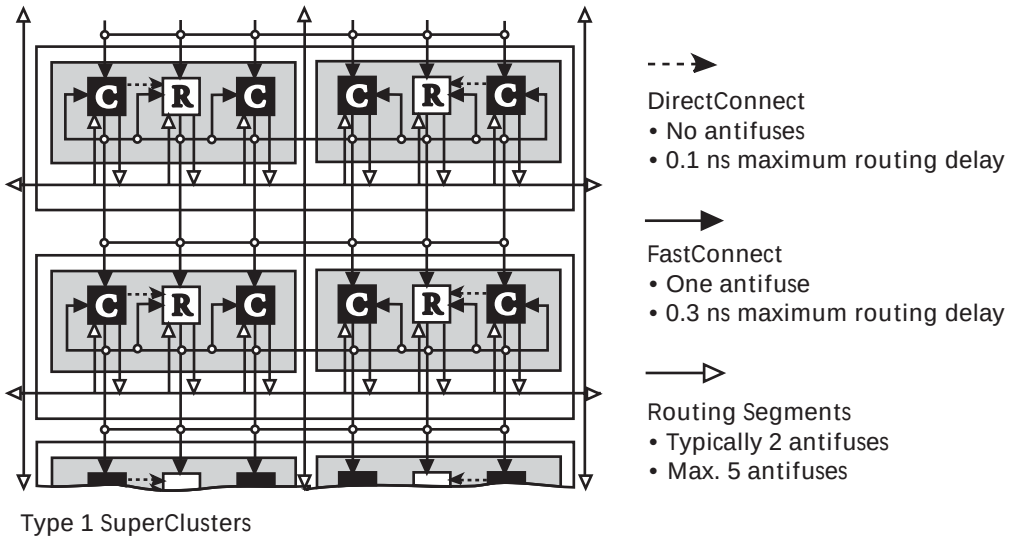


Figure 1-5 • **DirectConnect and FastConnect for Type 1 SuperClusters**

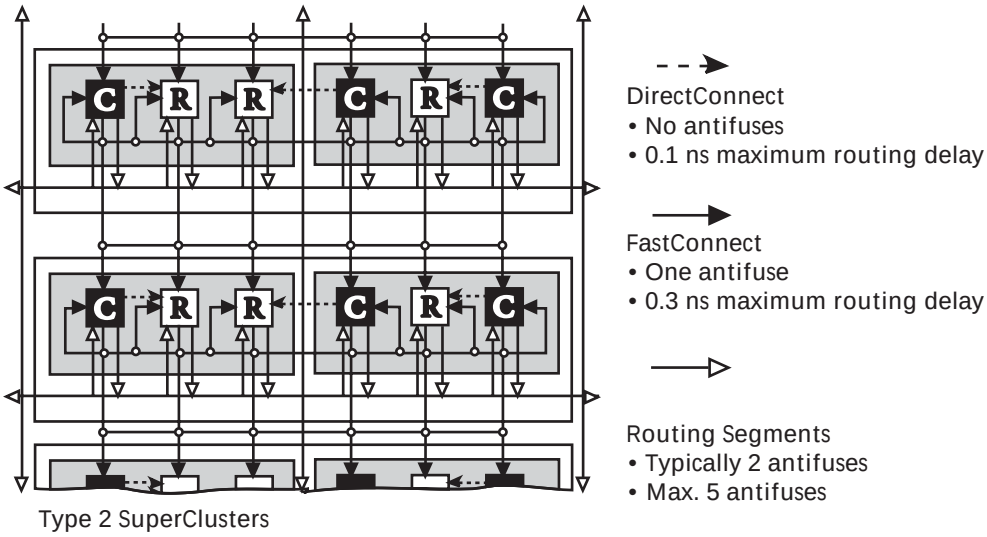


Figure 1-6 • **DirectConnect and FastConnect for Type 2 SuperClusters**

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.

Clock Resources

Actel's high-drive routing structure provides three clock networks (Table 1-1). The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinatorial logic. This provides a fast propagation path for the clock signal, enabling the 5.6 ns clock-to-out (pad-to-pad) performance of the auotmotive-grade SX-A devices. The hardwired clock is tuned to provide clock skew less than 0.3 ns worst case. If not used, this pin must be set as LOW or HIGH on the board. It must not be left floating. Figure 1-7 on page 1-6 describes the clock circuit used for the constant load HCLK. When the device is powered up and TRST is not grounded, HCLK does not function until the fourth clock cycle. This prevents possible false outputs due to a slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, TRST pin must be reserved in the Designer software and the pin must be tied to GND on the board.

Two additional clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the automotive-grade SX-A device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB pins are not used or sourced from signals, then these pins must be set as LOW or HIGH on the board. They must not be left floating (except in the A54SX72A where these clocks can be configured as regular I/Os and can float). Figure 1-8 on page 1-6 describes the CLKA and CLKB circuit used in SX-A devices with the exception of A54SX72A.

In addition to CLKA and CLKB, the A54SX72A device provides four quadrant clocks (QCLKA, QCLKB, QCLKC, QCLKD – corresponding to bottom-left, bottom-right, top-left, and top-right locations on the die, respectively), which can be sourced from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. If QCLKs are not used as quadrant clocks, they will behave as regular I/Os. Bidirectional clock buffers are also available on the A54SX72A. The CLKA, CLKB, and QCLK circuits for A54SX72A are shown in Figure 1-9 on page 1-7. Note that bidirectional clock buffers are only available in A54SX72A. For more information, refer to the "Pin Description" on page 1-38.

For more information on how to use quadrant clocks in the A54SX72A device, refer to the *Global Clock Networks in Actel's Antifuse Devices* and *Using A54SX72A and RT54SX72S Quadrant Clocks* application notes.

Table 1-1 • **SX-A Clock Resources**

	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Routed Clocks (CLKA, CLKB)	2	2	2	2
Hardwired Clocks (HCLK)	1	1	1	1
Quadrant Clocks (QCLKA, QCLKB, QCLKC, QCLKD)	0	0	0	4

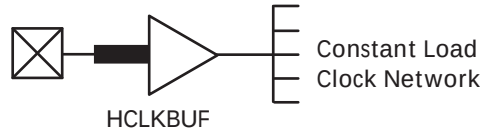


Figure 1-7 • **SX-A HCLK Clock Pad**

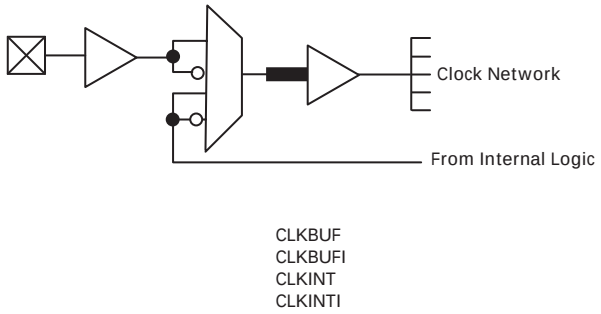


Figure 1-8 • **SX-A Routed Clock Structure Except for A54SX72A**

Other Architectural Features

Technology

The automotive-grade SX-A devices are implemented on a high-voltage, twin-well CMOS process using 0.22µ design rules. The metal-to-metal antifuse is comprised of a combination of amorphous silicon and dielectric material with barrier metals and has a programmed ("on" state) resistance of 25Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables automotive-grade SX-A devices to operate with internal clock frequencies of 250 MHz, enabling fast execution of even complex logic functions at extended tempetature ranges. Thus, the automotive-grade SX-A devices are an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can be integrated into an SX-A device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

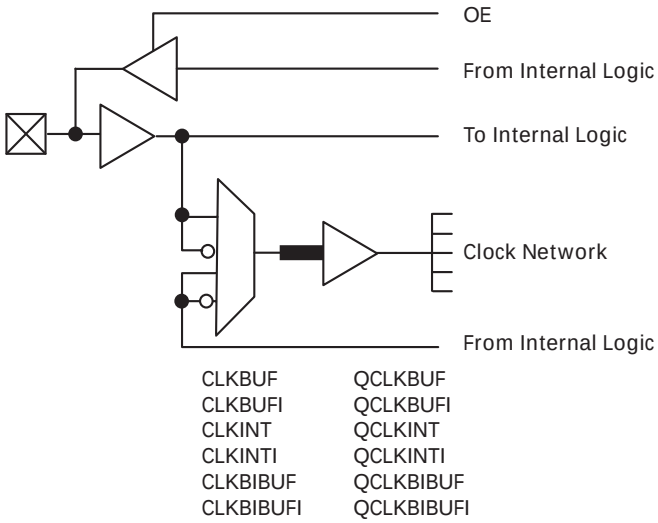


Figure 1-9 • **A54SX72A Routed Clock and QClock Structure**

Look for this symbol to ensure your valuable IP is secure.

FuseLock™

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

I/O Modules

Each user I/O on an automotive-grade SX-A device can be configured as an input, an output, a tristate output, or a bidirectional pin. I/O pins can be set for 2.5V or 3.3V operation through V_{CCI}. SX-A I/Os, combined with array registers, can achieve clock-to-output-pad timing of 5.6 ns even without the dedicated I/O registers. In most FPGAs, I/O cells that have embedded latches and flip-flops require instantiation in HDL code; this is a design complication not encountered in SX-A FPGAs. Fast pin-to-pin timing ensures that the device is able to interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. All unused I/Os are configured as tristate outputs by Actel's Designer software, for maximum flexibility when designing new boards or migrating existing designs.

SX-A inputs should be driven by high-speed push-pull devices with a low-resistance pull-up device. If the input voltage is greater than V_{CCI} and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the internal circuitry of the SX-A I/O may create a voltage divider. This voltage divider could pull the input voltage below specification for some devices connected to the driver. A logic '1' may not be correctly presented in this case. For example, if an open drain driver is used with a pull-up resistor to 3.3V to provide the logic '1' input, and V_{CCI} is set to 2.5 V on the SX-A device, the input signal may be pulled down by the SX-A input.

Each I/O module has an available power-up resistor of approximately 50kΩ that can configure the I/O in a known state during power-up. Just slightly before V_{CCA} reaches 2.5V, the resistors are disabled, so the I/Os will be controlled by user logic. See Table 1-2 on page 1-8 and Table 1-3 on page 1-8 for more information concerning available I/O features.

Hot Swapping

During power-up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power-up/down. After the SX-A device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Table 1-4 on page 1-8 summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for an SX-A device at room temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5V. For more information on power-up and hot-swapping, refer to the application note, *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*.

Table 1-2 • **I/O Features**

Function	Description
Input Buffer Threshold Selections	• 3.3V PCI, LVTTL • 2.5V LVCMOS2
Flexible Output Driver	• 3.3V PCI, LVTTL • 2.5V LVCMOS2
Output Buffer	"Hot-Swap" Capability (except 3.3V PCI) • I/O on an unpowered device does not sink current • Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable slew rate, high slew or low slew (The default is high slew rate). The slew is only affected on the falling edge of an output. Rising edges of outputs are not affected.
Power-Up	Individually selectable pull-ups and pull-downs during power-up (default is to power-up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

Table 1-3 • **I/O Characteristics for All I/O Configurations**

	Hot Swappable	Slew Rate Control	Power-Up Resistor
LVTTL, LVCMOS2	Yes	Yes. Only affects falling edges of outputs	Pull-up or pull-down
3.3V PCI	No	No. High slew rate only	Pull-up or pull-down

Table 1-4 • **Power-up Time at which I/Os Become Active**

Supply Ramp Rate	0.25V/µs	0.025V/µs	5V/ms	2.5V/ms	0.5V/ms	0.25V/ms	0.1V/ms	0.025V/ms
Units	**µs**	**µs**	**ms**	**ms**	**ms**	**ms**	**ms**	**ms**
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2

Boundary-Scan Testing (BST)

Automotive-grade SX-A devices are IEEE 1149.1 compliant and offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. The BST function is controlled through the special JTAG pins (TMS, TDI, TCK, TDO, and TRST). The functionality of the JTAG pins is defined by two available modes: Dedicated and Flexible. TMS cannot be employed as user I/O in either mode.

Dedicated Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Actel's Designer software. To reserve the JTAG pins, users can check the "Reserve JTAG" box in "Device Selection Wizard" (Figure 1-10).

Figure 1-10 • **Device Selection Wizard**

Flexible Mode

In Flexible mode, TDI, TCK, and TDO may be employed as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are not present in flexible JTAG mode.

To select the Flexible mode, users need to uncheck the "Reserve JTAG" box in "Device Selection Wizard" in Actel's Designer software. In Flexible mode, TDI, TCK and TDO pins may function as user I/Os or BST pins. The functionality is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK and TDO function as user I/Os. The TDI, TCK, and TDO are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logic low. To return to Test-Logic Reset state, TMS must be high for at least five TCK cycles. An external 10KΩ pull-up resistor to V_{CCI} should be placed on the TMS pin to pull it HIGH by default.

Table 1-5 describes the different configuration requirements of BST pins and their functionality in different modes.

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the "Reserve JTAG Test Reset" option is selected as shown in Figure 1-10 on page 1-8. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. Actel recommends connecting this pin to ground in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or be driven high.

When the "Reserve JTAG Test Reset" option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

Table 1-5 • **Boundary-Scan Pin Configurations and Functions**

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

Probing Capabilities

Automotive-grade SX-A devices also provide an internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic Hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user assigns the selected internal nets in Actel's Silicon Explorer II software to the PRA/PRB output pins for observation. Silicon Explorer II automatically places the device into JTAG mode. However, probing functionality is only activated when the TRST pin is driven high or left floating, allowing the internal pull-up resistor to pull TRST to HIGH. If the TRST pin is held LOW, the TAP controller remains in the Test-Logic-Reset state so no probing can be performed. However, the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When selecting the "Reserve Probe Pin" box as shown in Figure 1-10 on page 1-8, direct the layout tool to reserve the PRA and PRB pins as dedicated outputs for probing. This "reserve" option is merely a guideline. If the designer assigns user I/Os to the PRA and PRB pins and selects the "Reserve Probe Pin" option, Designer Layout will override the "Reserve Probe Pin" option and place the user I/Os on those pins.

To allow probing capabilities, the security fuse must not be programmed. Programming the security fuse disables the probe circuitry. Table 1-6 on page 1-10 summarizes the possible device configurations for probing once the device leaves the "Test-Logic-Reset" JTAG state.

SX-A Probe Circuit Control Pins

Automotive-grade SX-A devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100% real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy-to-use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary-scan ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 1-11 on page 1-11 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Table 1-6 • **Device Configuration Options for Probe Capability (TRST pin reserved)**

JTAG Mode	TRST[1]	Security Fuse Programmed	PRA, PRB[2]	TDI, TCK, TDO[2]
Dedicated	LOW	No	User I/O[3]	Probing Unavailable
Flexible	LOW	No	User I/O[3]	User I/O[3]
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Note:

1. If the TRST pin is not reserved, the device behaves according to TRST=HIGH as described in the table.
2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by the Designer software.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuit. Actel recommends that you use a 70Ω series termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination, effective for traces of fewer than 8 inches, is used to prevent data transmission corruption during probing and reading back the checksum.

Development Tool Support

The automotive-grade SX-A family of FPGAs is fully supported by both Actel's Libero™ Integrated Design Environment and Designer FPGA Development software. Actel Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (Figure 1-12)). Libero IDE includes Synplify® for Actel from Synplicity®, ViewDraw for Actel from Mentor Graphics, ModelSim™ HDL Simulator from Model Technology™, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel.

Actel's Designer software provides a comprehensive suite of backend development tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and Unix operating systems.

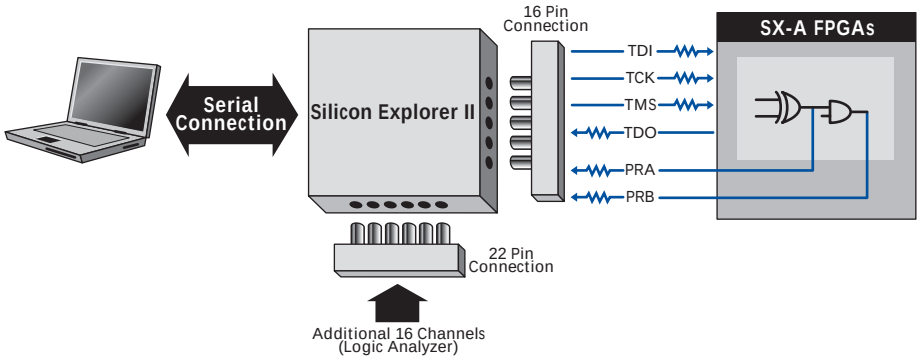
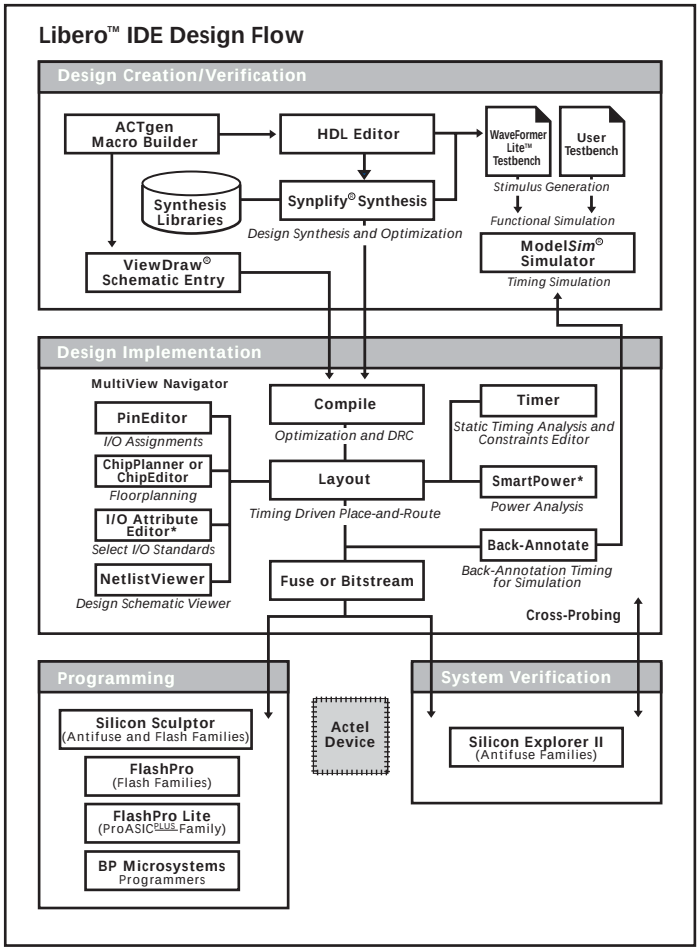


Figure 1-11 • **Probe Setup**



Note: **Available in Axcelerator and ProASIC^{PLUS} devices*

Figure 1-12 • **Design Flow**

Operating Conditions

Table 1-7 • **Absolute Maximum Ratings***

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage for I/Os	–0.3 to +4.0	V
V_{CCA}	DC Supply Voltage for Array	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to V_{CCI} +0.5	V
V_O	Output Voltage	–0.5 to +V_{CCI}	V
T_{STG}	Storage Temperature	–65 to +150	°C

Note: **Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*

Table 1-8 • **Recommended Operating Conditions**

Parameter	Automotive	Units
Temperature Range*	–40 to +125	°C
2.5V Power Supply Range	2.375 to 2.625	V
3.3V Power Supply Range	3.135 to 3.465	V

Note: **Ambient temperature (T_A).*

Table 1-9 • **3.3V LVTTL Electrical Specifications**

Symbol	Parameter		Automotive		Units
			Min	Max	
V_{OH}	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	IOH = –2mA	2.4		V
V_{OL}	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	IOL = 2mA		0.4	V
V_{IL}	Input Low Voltage			0.7	V
V_{IH}	Input High Voltage		2.1		V
I_{IL} / I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–20	20	µA
I_{OZ}	3-State Output Leakage Current		–20	20	µA
t_R, t_F[1,2]	Input Transition Time t_R, t_F			10	ns
C_{IO}	I/O Capacitance			10	pF
I_{CC}[3]	Standby Current			45	mA
IV Curve	Can be derived from the IBIS model at *www.actel.com/custsup/models/ibis.html*.				

Note:

1. t_R is the transition time from 0.7V to 2.1V.
2. t_F is he transition time from 2.1V to 0.7V.
3. $I_{CC} = I_{CCI} + I_{CCA}$

Table 1-10 • **2.5V LVCMOS2 Electrical Specifications**

Symbol	Parameter		Automotive		Units
			Min.	Max.	
V_{OH}	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	IOH = -1mA	1.8		V
V_{OL}	V_{CCI} = MIN, $V_I = V_{IH}$ or V_{IL}	IOL = 1mA		0.5	V
V_{IL}	Input Low Voltage, V_{OUT} =< VV_{OL} (max)			0.6	V
V_{IH}	Input High Voltage, V_{OUT} >= VV_{OH} (min)		1.7		V
I_{IL} / I_{IH}	Input Leakage Current, $V_{IN} = V_{CCI}$ or GND		–20	20	µA
I_{OZ}	3-State Output Leakage Current		–20	20	µA
t_R, t_F[1,2]	Input Transition Time t_R, t_F			10	ns
C_{IO}	I/O Capacitance			10	pF
I_{CC}[3]	Standby Current			35	mA
IV Curve	Can be derived from the IBIS model at *www.actel.com/custsup/models/ibis.html*.				

Note:

1. t_R is the transition time from 0.6V to 1.7V.
2. t_F is he transition time from 1.7V to 0.6V.
3. $I_{CC} = I_{CCI} + I_{CCA}$

PCI Compliance for the Automotive-Grade SX-A Family

The automotive-grade SX-A devices support 3.3V PCI and are compliant with the PCI Local Bus Specification Rev. 2.1.

Table 1-11 • **DC Specifications (3.3V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.375	2.625	V
V_{CCI}	Supply Voltage for I/Os		3.135	3.465	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CCI}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$	–20	+20	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CCI}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Note:

1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers should ensure that the input buffer is conducting minimum current at this input voltage in applications sensitive to static power utilization.
2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
3. Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).

Table 1-12 • **AC Specifications (3.3V PCI Operation)**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \leq 0.3V_{CCI}$ [1]	$-12V_{CCI}$		mA
		$0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI}$ [1]	$(-17.1(V_{CCI} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2]		EQ 1-1 on page 1-16	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \geq 0.6V_{CCI}$ [1]	$16V_{CCI}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ [1, 2]		EQ 1-2 on page 1-16	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ - $0.6V_{CCI}$ load [3]	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ - $0.2V_{CCI}$ load [3]	1	4	V/ns

Note:

1. Refer to the V/I curves in Figure 1-13 on page 1-15. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.
2. Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 1-13 on page 1-15. The equation defined maximum should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.

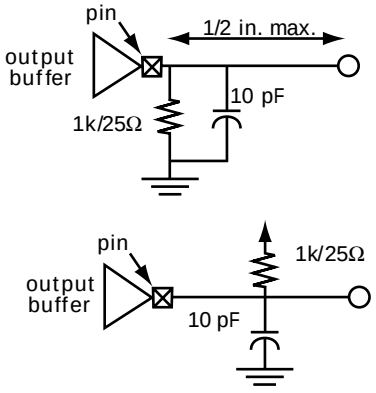


Figure 1-13 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the automotive-grade SX-A devices.

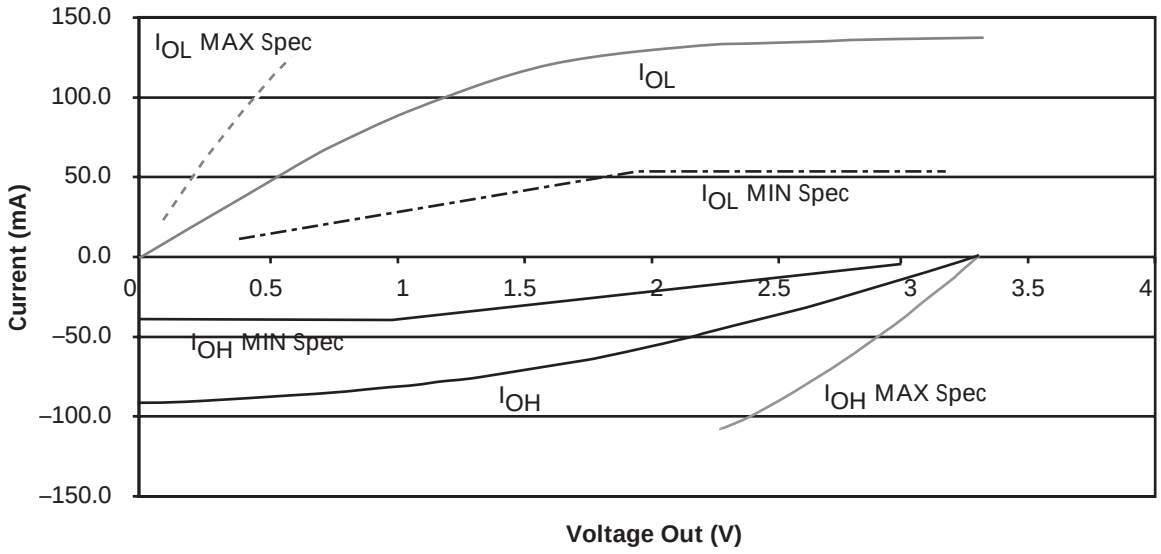


Figure 1-13 • **3.3V PCI V/I Curve for Automotive-Grade SX-A Devices**

Equation C

$$IOH = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$

$$\text{for } 0.7\ V_{CCI} < V_{OUT} < V_{CCI}$$

Equation D

$$IOL = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$

$$\text{for } 0V < V_{OUT} < 0.18\ V_{CCI}$$

Junction Temperature (T_J)

The temperature variable in the Designer Series software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 1, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a + \qquad \textit{EQ 1-1}$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P \qquad \textit{EQ 1-2}$$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics table below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc}, and the junction-to-ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 144-pin package at automotive temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{32\text{°C/W}} = 0.78\text{W}$$

Table 1-13 • **Package Thermal Characteristics**

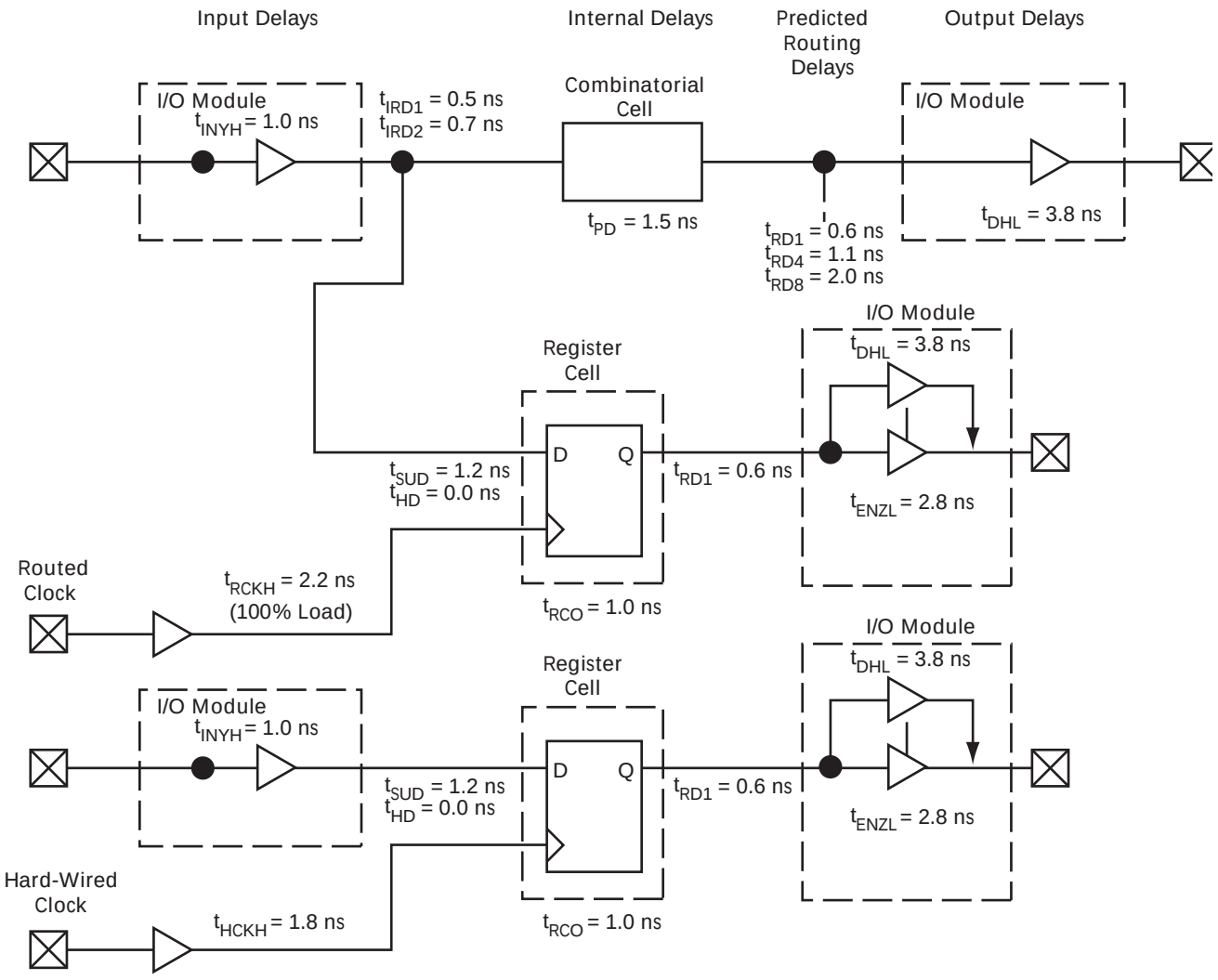
Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Thin Quad Flat Pack (TQFP)	100	12	37.5	30	°C/W
Thin Quad Flat Pack (TQFP)	144	11	32	24	°C/W
Plastic Quad Flat Pack (PQFP)[1]	208	8	30	23	°C/W
Plastic Quad Flat Pack (PQFP) with Heat Spreader[2]	208	3.8	20	17	°C/W
Fine Pitch Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.3	30	25	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3	20	15	°C/W

Note:

1. The A54SX08A PQ208 has no heat spreader.
2. The SX-A PQ208 package has a heat spreader for A54SX16A, A54SX32A, and A54SX72A.

For Power Estimator information, please go to *http://www.actel.com/products/tools/index.html*.

SX-A Timing Model*



Note: **Values shown for A54SX08A, worst-case automotive conditions at 3.3V PCI with standard place-and-route.*

Figure 1-14 • **Timing Model**

Sample Path Calculations

Hardwired Clock

External Setup $=(t_{INYH} + t_{IRD2} + t_{SUD}) - t_{HCKH}$
$=1.0+0.7+1.2-1.8=1.1ns$

Clock-to-Out (Pad-to-Pad)

$=t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
$=1.8+1.0+0.6+3.8=7.2ns$

Routed Clock

External Setup $= (t_{INYH} + t_{IRD2} + t_{SUD}) - t_{RCKH}$
$= 1.0+0.7+1.2-1.8=1.1ns$

Clock-to-Out (Pad-to-Pad)

$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$
$= 1.8+1.0+0.6+3.8=7.2ns$

Output Buffer Delays

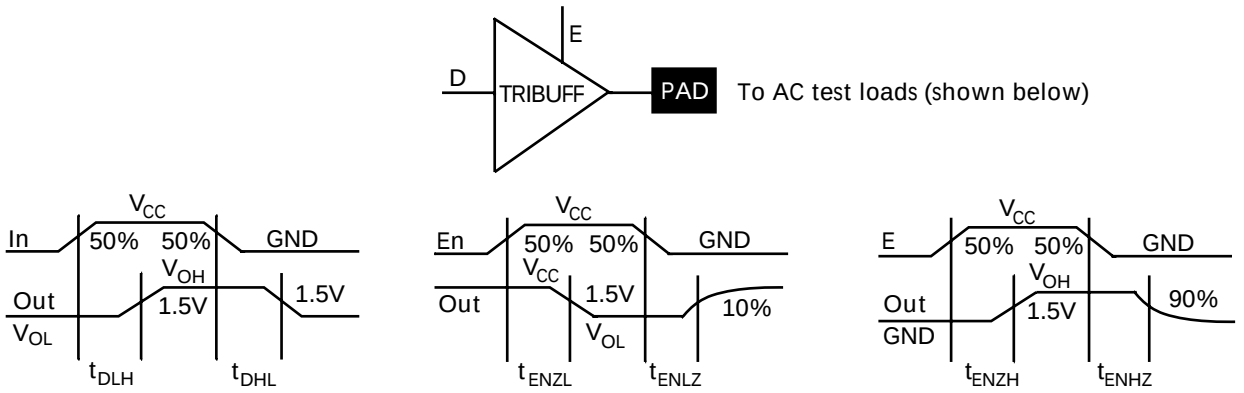


Figure 1-15 • **Output Buffer Delay**

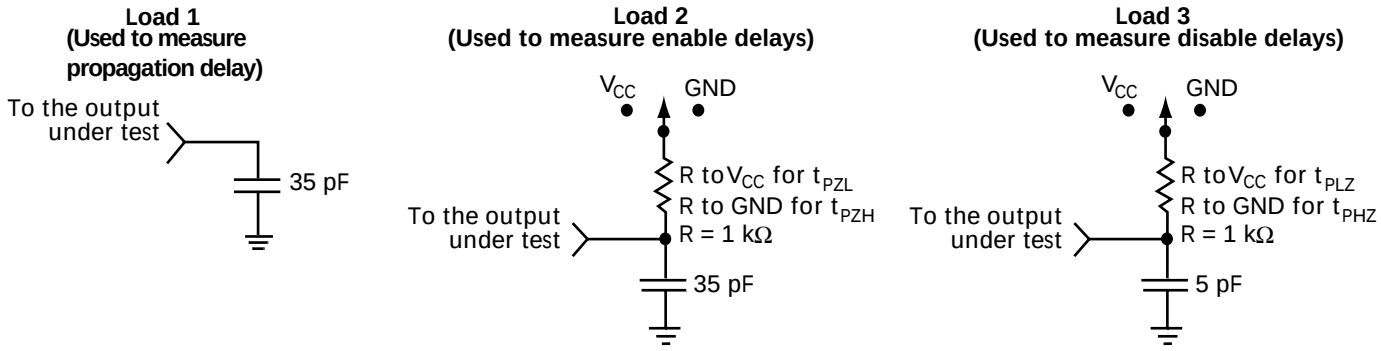


Figure 1-16 • **AC Test Loads**

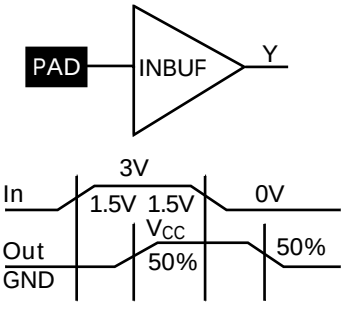


Figure 1-17 • **Input Buffer Delays**

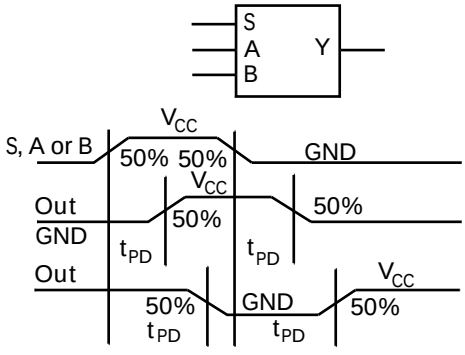


Figure 1-18 • **C-Cell Delays**

Cell Timing Characteristics

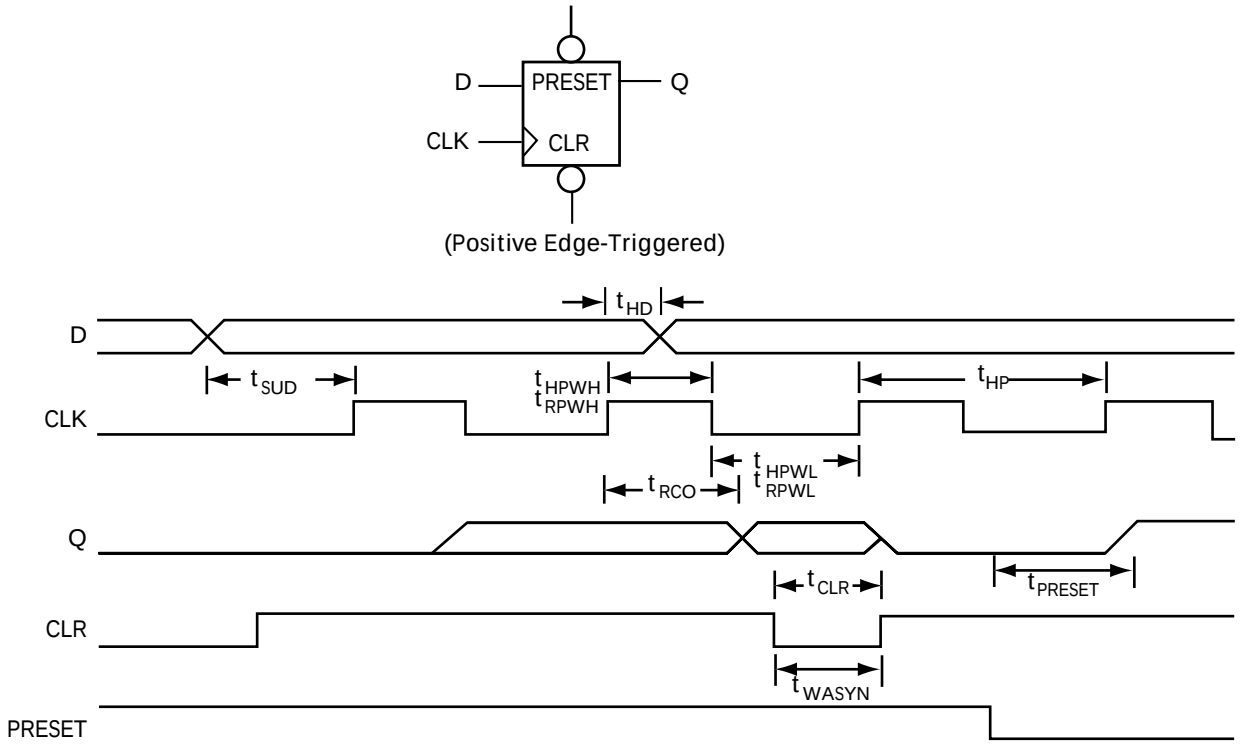


Figure 1-19 • **Cell Timing Characteristics**

Timing Characteristics

Timing characteristics for SX-A devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all SX-A family members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while 90 percent of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three to five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

SX-A devices are manufactured with a CMOS process. Therefore, device performance varies according to temperature, voltage, and process changes. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Table 1-14 • **Temperature and Voltage Derating Factors (Normalized to T_J = 125°C, V_{CCA} = 2.3V)**

V_{CCA}	Junction Temperature (T_J)						
	–55°C	**–40°C**	**0°C**	**25°C**	**70°C**	**85°C**	**125°C**
2.3V	0.7	0.70	0.77	0.78	0.88	0.91	1.00
2.5V	0.65	0.66	0.72	0.73	0.83	0.85	0.93
2.7V	0.66	0.62	0.67	0.69	0.78	0.80	0.88

Table 1-15 • **A54SX08A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]				
t_{PD}	Internal Array Module		1.5	ns
Predicted Routing Delays[2]				
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.7	ns
t_{RD3}	FO=3 Routing Delay		0.9	ns
t_{RD4}	FO=4 Routing Delay		1.1	ns
t_{RD8}	FO=8 Routing Delay		2.0	ns
t_{RD12}	FO=12 Routing Delay		2.9	ns
R-Cell Timing				
t_{RCO}	Sequential Clock-to-Q		1.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	1.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.3		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.6		ns
t_{HASYN}	Asynchronous Hold Time	0.5		ns
Input Module Propagation Delays				
t_{INYH}	Input Data Pad-to-Y HIGH		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.6	ns

Note:

1. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-15 • **A54SX08A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Input Module Predicted Routing Delays[2]				
t_{IRD1}	FO=1 Routing Delay		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.7	ns
t_{IRD3}	FO=3 Routing Delay		0.9	ns
t_{IRD4}	FO=4 Routing Delay		1.1	ns
t_{IRD8}	FO=8 Routing Delay		2.0	ns
t_{IRD12}	FO=12 Routing Delay		2.9	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		2.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.4		ns
t_{HCKSW}	Maximum Skew		0.3	ns
t_{HP}	Minimum Period	4.8		ns
f_{HMAX}	Maximum Frequency		208	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.2	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.2	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.5	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.6	ns
t_{RPWH}	Min. Pulse Width HIGH	2.4		ns
t_{RPWL}	Min. Pulse Width LOW	2.4		ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-15 • **A54SX08A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{RCKSW}	Maximum Skew (Light Load)		0.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)	1.8		ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.7	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.4		ns
t_{HCKSW}	Maximum Skew		0.3	ns
t_{HP}	Minimum Period	4.8		ns
f_{HMAX}	Maximum Frequency		208	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.3	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.1	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.5	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.2	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.6	ns
t_{RPWH}	Min. Pulse Width HIGH	2.4		ns
t_{RPWL}	Min. Pulse Width LOW	2.4		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.5	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.5	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-15 • **A54SX08A Timing Characteristics**
(Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
2.5V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		5.0	ns
t_{DHL}	Data-to-Pad HIGH to LOW		21.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		4.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		22.8	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		6.7	ns
t_{ENZH}	Enable-to-Pad, Z to H		4.1	ns
t_{ENLZ}	Enable-to-Pad, L to Z		6.7	ns
t_{ENHZ}	Enable-to-Pad, H to Z		0.064	ns
d_{TLH}	Delta LOW to HIGH		0.029	ns/pF
d_{THL}	Delta HIGH to LOW		0.108	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		5.0	ns/pF
3.3V PCI Output Module Timing[4]				
t_{DLH}	Data-to-Pad LOW to HIGH	3.8		ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF
3.3V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		5.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		17.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.3	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		31.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		5.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.5	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-15 • **A54SX08A Timing Characteristics**
(Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.092	ns/pF

Note:

1. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-16 • **A54SX16A Timing Characteristics**
(Worst-Case Automotive Conditions, VCCA = 2.3V, VCCI = 3.0V, TJ = 125°C)

		'Std' Speed		
Parameter	**Description**	**Min**	**Max.**	**Units**
C-Cell Propagation Delays[1]				
t_{PD}	Internal Array Module	1.5		ns
Predicted Routing Delays[2]				
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.7	ns
t_{RD3}	FO=3 Routing Delay		0.9	ns
t_{RD4}	FO=4 Routing Delay		1.1	ns
t_{RD8}	FO=8 Routing Delay		2.0	ns
t_{RD12}	FO=12 Routing Delay		2.9	ns
R-Cell Timing				
t_{RCO}	Sequential Clock-to-Q		1.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	1.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		ns

Note:

1. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-16 • **A54SX16A Timing Characteristics**
(Worst-Case Automotive Conditions, VCCA = 2.3V, VCCI = 3.0V, TJ = 125°C) (Continued)

		'Std' Speed		
Parameter	**Description**	**Min**	**Max.**	**Units**
t_{WASYN}	Asynchronous Pulse Width	2.3		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.6		ns
t_{HASYN}	Asynchronous Removal Time	0.5		ns
Input Module Propagation Delays				
t_{INYH}	Input Data Pad-to-Y HIGH		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.6	ns
Input Module Predicted Routing Delays[2]				
t_{IRD1}	FO=1 Routing Delay		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.7	ns
t_{IRD3}	FO=3 Routing Delay		0.9	ns
t_{IRD4}	FO=4 Routing Delay		1.1	ns
t_{IRD8}	FO=8 Routing Delay		0.9	ns
t_{IRD12}	FO=12 Routing Delay		2.9	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		2.2	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.1	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.4		ns
t_{HCKSW}	Maximum Skew		0.1	ns
t_{HP}	Minimum Period	4.8		ns
f_{HMAX}	Maximum Frequency		208	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.1	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.2	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.6	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-16 • **A54SX16A Timing Characteristics (Worst-Case Automotive Conditions, VCCA = 2.3V, VCCI = 3.0V, TJ = 125°C) (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min**	**Max.**	**Units**
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.6	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.1	ns
t_{RPWH}	Min. Pulse Width HIGH	2.4		ns
t_{RPWL}	Min. Pulse Width LOW	2.4		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		2.2	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.1	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.4		ns
t_{HPWL}	Minimum Pulse Width LOW	2.4		ns
t_{HCKSW}	Maximum Skew		0.1	ns
t_{HP}	Minimum Period	4.8		ns
f_{HMAX}	Maximum Frequency		208	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.1	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.3	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.7	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		3.0	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-16 • **A54SX16A Timing Characteristics**
(Worst-Case Automotive Conditions, VCCA = 2.3V, VCCI = 3.0V, TJ = 125°C) (Continued)

		'Std' Speed		
Parameter	**Description**	**Min**	**Max.**	**Units**
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.1	ns
t_{RPWH}	Min. Pulse Width HIGH	2.4		ns
t_{RPWL}	Min. Pulse Width LOW	2.4		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.9	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.9	ns
2.5V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		6.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		21.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.6	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		22.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		6.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		6.7	ns
d_{TLH}	Delta LOW to HIGH		0.064	ns/pF
d_{THL}	Delta HIGH to LOW		0.029	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.108	ns/pF
3.3V PCI Output Module Timing[4]				
t_{DLH}	Data-to-Pad LOW to HIGH		3.8	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF
3.3V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		5.3	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-16 • **A54SX16A Timing Characteristics**
(Worst-Case Automotive Conditions, VCCA = 2.3V, VCCI = 3.0V, TJ = 125°C) (Continued)

		'Std' Speed		
Parameter	**Description**	**Min**	**Max.**	**Units**
t_{DHL}	Data-to-Pad HIGH to LOW		4.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		17.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.3	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		31.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		5.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.092	ns/pF

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-17 • **A54SX32A Timing Characteristics**
(Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]				
t_{PD}	Internal Array Module		1.5	ns
Predicted Routing Delays[2]				
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.7	ns
t_{RD3}	FO=3 Routing Delay		0.9	ns
t_{RD4}	FO=4 Routing Delay		1.1	ns
t_{RD8}	FO=8 Routing Delay		2.0	ns
t_{RD12}	FO=12 Routing Delay		2.9	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-17 • **A54SX32A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
R-Cell Timing				
t_{RCO}	Sequential Clock-to-Q		1.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	1.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.3		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.6		ns
t_{HASYN}	Asynchronous Removal Time	0.5		ns
Input Module Propagation Delays				
t_{INYH}	Input Data Pad-to-Y HIGH		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.6	ns
Input Module Predicted Routing Delays[2]				
t_{IRD1}	FO=1 Routing Delay		0.5	ns
t_{IRD2}	FO=2 Routing Delay		0.7	ns
t_{IRD3}	FO=3 Routing Delay		0.9	ns
t_{IRD4}	FO=4 Routing Delay		1.1	ns
t_{IRD8}	FO=8 Routing Delay		2.0	ns
t_{IRD12}	FO=12 Routing Delay		2.9	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)	3.1		ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.5		ns
t_{HCKSW}	Maximum Skew		0.6	ns
t_{HP}	Minimum Period	5.0		ns
f_{HMAX}	Maximum Frequency		199	MHz

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-17 • **A54SX32A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		3.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.9	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.5		ns
t_{RPWL}	Min. Pulse Width LOW	2.5		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		2.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		2.3	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)	3.1		ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.5		ns
t_{HCKSW}	Maximum Skew		0.6	ns
t_{HP}	Minimum Period	5.0		ns
f_{HMAX}	Maximum Frequency		199	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		3.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.7	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-17 • **A54SX32A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.9	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.5		ns
t_{RPWL}	Min. Pulse Width LOW	2.5		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		2.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		2.3	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.5	0.0	ns
t_{HPWL}	Minimum Pulse Width LOW	2.5		ns
t_{HCKSW}	Maximum Skew		0.6	ns
t_{HP}	Minimum Period	5.0		ns
f_{HMAX}	Maximum Frequency		199	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		3.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.8	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.9	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-17 • **A54SX32A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		4.3	ns
t_{RPWH}	Min. Pulse Width HIGH	2.5		ns
t_{RPWL}	Min. Pulse Width LOW	2.5		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.5	ns
t_{RCKSW}	Maximum Skew (50% Load)		2.2	ns
t_{RCKSW}	Maximum Skew (100% Load)		2.3	ns
2.5V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		6.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		21.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.6	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		22.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		6.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		6.7	ns
d_{TLH}	Delta LOW to HIGH		0.064	ns/pF
d_{THL}	Delta HIGH to LOW		0.029	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.108	ns/pF
3.3V PCI Output Module Timing[4]				
t_{DLH}	Data-to-Pad LOW to HIGH		3.8	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-17 • **A54SX32A Timing Characteristics**
(Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C (Continued)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
3.3V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		5.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		17.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.3	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		31.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		5.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew			ns/pF

Note:

1. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-18 • **A54SX72A Timing Characteristics**
(Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]				
t_{PD}	Internal Array Module		1.5	ns
Predicted Routing Delays[2]				
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.6	ns
t_{RD2}	FO=2 Routing Delay		0.8	ns
t_{RD3}	FO=3 Routing Delay		1.0	ns
t_{RD4}	FO=4 Routing Delay		1.2	ns

Note:

1. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-18 • **A54SX72A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{RD8}	FO=8 Routing Delay		2.4	ns
t_{RD12}	FO=12 Routing Delay		3.4	ns
R-Cell Timing				
t_{RCO}	Sequential Clock-to-Q		1.0	ns
t_{CLR}	Asynchronous Clear-to-Q		1.2	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	1.2		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		ns
t_{WASYN}	Asynchronous Pulse Width	2.3		ns
$t_{RECASYN}$	Asynchronous Recovery Time	0.6		ns
t_{HASYN}	Asynchronous Hold Time	0.5		ns
Input Module Propagation Delays				
t_{INYH}	Input Data Pad-to-Y HIGH		1.0	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.6	ns
Input Module Predicted Routing Delays[2]				
t_{IRD1}	FO=1 Routing Delay		0.6	ns
t_{IRD2}	FO=2 Routing Delay		0.8	ns
t_{IRD3}	FO=3 Routing Delay		1.0	ns
t_{IRD4}	FO=4 Routing Delay		1.2	ns
t_{IRD8}	FO=8 Routing Delay		2.4	ns
t_{IRD12}	FO=12 Routing Delay		3.4	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		2.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.5		ns
t_{HCKSW}	Maximum Skew		1.1	ns
t_{HP}	Minimum Period	5.0		ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-18 • **A54SX72A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
f_{HMAX}	Maximum Frequency		199	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.0	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)			ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		4.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)			ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		5.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)			ns
t_{RPWH}	Min. Pulse Width HIGH		5.6	ns
t_{RPWL}	Min. Pulse Width LOW			ns
t_{RCKSW}	Maximum Skew (Light Load)		6.5	ns
t_{RCKSW}	Maximum Skew (50% Load)			ns
t_{RCKSW}	Maximum Skew (100% Load)		6.9	ns
Dedicated (Hardwired) Array Clock Networks				
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		2.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		2.2	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.5		ns
t_{HCKSW}	Maximum Skew		1.1	ns
t_{HP}	Minimum Period	5.0		ns
f_{HMAX}	Maximum Frequency		199	MHz
Routed Array Clock Networks				
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		4.0	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-18 • **A54SX72A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)			ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		4.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)			ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		5.3	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)			ns
t_{RPWH}	Min. Pulse Width HIGH		5.6	ns
t_{RPWL}	Min. Pulse Width LOW			ns
t_{RCKSW}	Maximum Skew (Light Load)		6.5	ns
t_{RCKSW}	Maximum Skew (50% Load)			ns
t_{RCKSW}	Maximum Skew (100% Load)		6.9	ns
2.5V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		6.5	ns
t_{DHL}	Data-to-Pad HIGH to LOW		5.0	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		22.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.6	ns
t_{ENZLS}	Data-to-Pad, Z to L—low slew		22.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		6.7	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		6.7	ns
d_{TLH}	Delta LOW to HIGH		0.064	ns/pF
d_{THL}	Delta HIGH to LOW		0.029	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.108	ns/pF
3.3V PCI Output Module Timing[4]				
t_{DLH}	Data-to-Pad LOW to HIGH		3.8	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.8	ns

Note:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Table 1-18 • **A54SX72A Timing Characteristics (Worst-Case Automotive Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C) (Continued)**

		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{ENZH}	Enable-to-Pad, Z to H		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		4.8	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF
3.3V LVTTL Output Module Timing[3]				
t_{DLH}	Data-to-Pad LOW to HIGH		5.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		4.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW—low slew		17.3	ns
t_{ENZL}	Enable-to-Pad, Z to L		4.3	ns
t_{ENZLS}	Enable-to-Pad, Z to L—low slew		31.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		5.5	ns
t_{ENLZ}	Enable-to-Pad, L to Z		5.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		4.8	ns
d_{TLH}	Delta LOW to HIGH		0.050	ns/pF
d_{THL}	Delta HIGH to LOW		0.019	ns/pF
d_{THLS}	Delta HIGH to LOW—low slew		0.092	ns/pF

Note:

1. For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Delays based on 35 pF loading.
4. Delays based on 10 pF loading and 25Ω resistance.

Pin Description

CLKA/B **Clock A and B**

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard LVTTL or 3.3V PCI specifications. The clock input is buffered prior to clocking the R-cells. If not used, these pins must be set LOW or HIGH on the board except A54SX72A. In A54SX72A these clocks can be configured as user I/O.

QCLKA/B/C/D, I/O **Quadrant Clock A, B, C, and D**

These four pins are the quadrant clock inputs and are only for A54SX72A with A, B, C and D corresponding to bottom-left, bottom-right, top-left and top-right quadrants, respectively. They are clock inputs for clock distribution networks. Input levels are compatible with standard LVTTL and 3.3V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used as a clock it will behave as a regular I/O.

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (Hardwired) Array Clock**

This pin is the clock input for sequential modules. Input levels are compatible with LVTTL or 3.3V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board and must not be left floating.

I/O **Input/Output**

The I/O pin functions as an input, output, tristate or bidirectional buffer. Based on certain configurations, input and output levels are compatible with LVTTL or 3.3V PCI specifications. Unused I/O pins are automatically tristated by the Designer software.

NC **No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O **Probe A/B**
PRB, I/O

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK, I/O **Test Clock**

Test clock input for diagnostic probe and device programming. In flexible mode, TCK becomes active when the TMS pin is set LOW (refer to Table 1-5 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDI, I/O **Test Data Input**

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 1-5 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O **Test Data Output**

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 1-5 on page 1-9). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state. When Silicon Explorer II is being used, TDO will act as an output when the "checksum" command is run. It will return to user IO when "checksum" is complete.

TMS **Test Mode Select**

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 1-5 on page 1-9). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O **Boundary Scan Reset Pin**

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the "Reserve JTAG Reset Pin" is not selected in Designer.

V_{CCI} **Supply Voltage**

Supply voltage for I/Os. See "Recommended Operating Conditions" on page 1-12. All V_{CCI} power pins in the device should be connected.

V_{CCA} **Supply Voltage**

Supply voltage for Array. See "Recommended Operating Conditions" on page 1-12. All V_{CCA} power pins in the device should be connected.

Package Pin Assignments

208-Pin PQFP (Top View)

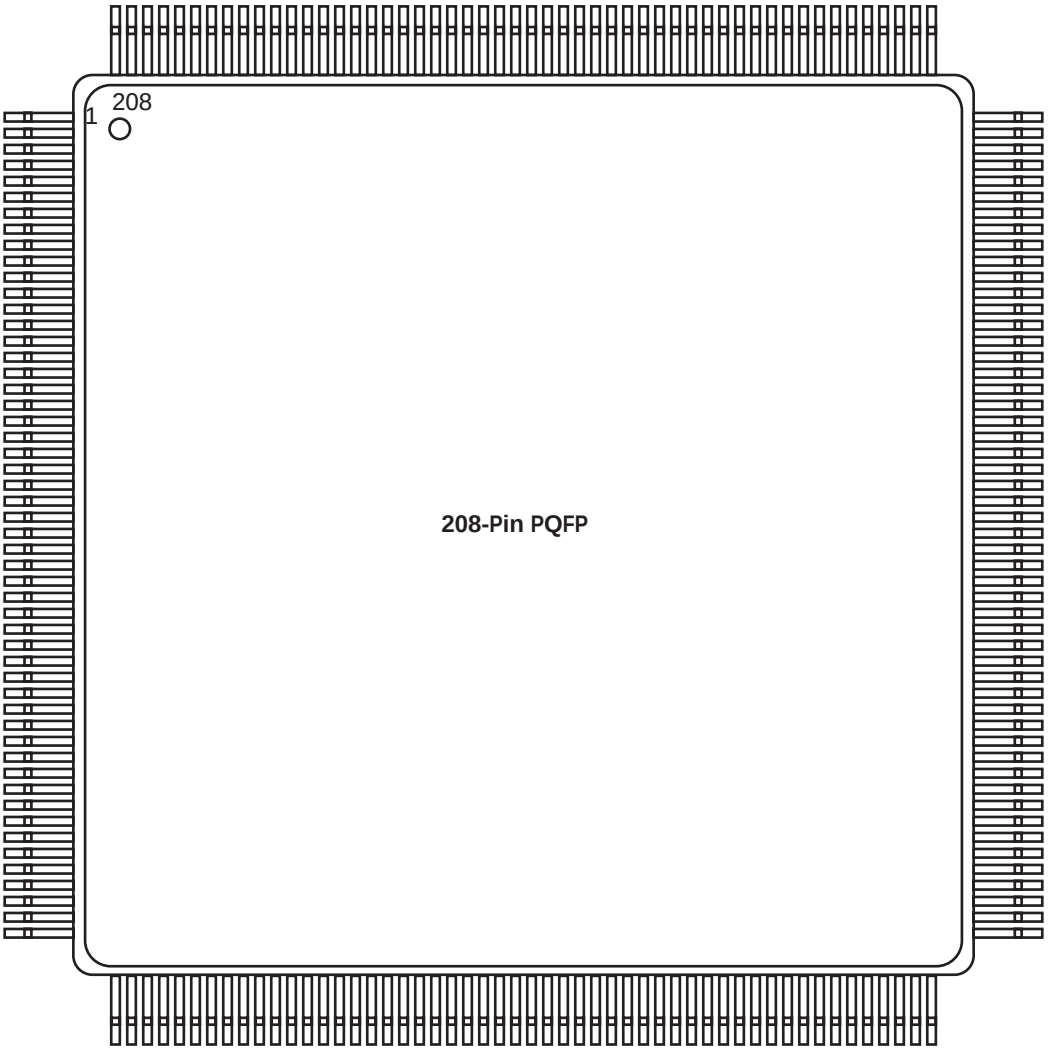


Figure 2-1 • **208-Pin PQFP**

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
1	GND	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O	I/O
4	NC	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	NC	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	TMS	TMS	TMS	TMS
12	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
13	I/O	I/O	I/O	I/O
14	NC	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	I/O	I/O	I/O	I/O
17	NC	I/O	I/O	I/O
18	I/O	I/O	I/O	GND
19	I/O	I/O	I/O	V_{CCA}
20	NC	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	I/O	I/O	I/O	I/O
23	NC	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	NC	NC	NC	I/O
26	GND	GND	GND	GND
27	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
28	GND	GND	GND	GND
29	I/O	I/O	I/O	I/O
30	TRST, I/O	TRST, I/O	TRST, I/O	TRST, I/O
31	NC	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
36	I/O	I/O	I/O	I/O
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	NC	I/O	I/O	I/O
40	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	NC	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	I/O	I/O	I/O	I/O
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
61	NC	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O
65	I/O	I/O	NC	I/O
66	I/O	I/O	I/O	I/O
67	NC	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	NC	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
71	I/O	I/O	I/O	I/O
72	I/O	I/O	I/O	I/O
73	NC	I/O	I/O	I/O
74	I/O	I/O	I/O	QCLKA, I/O
75	NC	I/O	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O	PRB,I/O
77	GND	GND	GND	GND
78	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
79	GND	GND	GND	GND
80	NC	NC	NC	NC
81	I/O	I/O	I/O	I/O
82	HCLK	HCLK	HCLK	HCLK
83	I/O	I/O	I/O	V_{CCI}
84	I/O	I/O	I/O	QCLKB, I/O
85	NC	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	NC	I/O	I/O	I/O
89	I/O	I/O	I/O	I/O
90	I/O	I/O	I/O	I/O
91	NC	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	NC	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	NC	I/O	I/O	I/O
98	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	I/O	I/O	I/O	I/O
102	I/O	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O	I/O
105	GND	GND	GND	GND

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
106	NC	I/O	I/O	I/O
107	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	I/O
109	I/O	I/O	I/O	I/O
110	I/O	I/O	I/O	I/O
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
116	NC	I/O	I/O	GND
117	I/O	I/O	I/O	V_{CCA}
118	I/O	I/O	I/O	I/O
119	NC	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	NC	I/O	I/O	I/O
123	I/O	I/O	I/O	I/O
124	I/O	I/O	I/O	I/O
125	NC	I/O	I/O	I/O
126	I/O	I/O	I/O	I/O
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	GND	GND	GND	GND
130	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
131	GND	GND	GND	GND
132	NC	NC	NC	I/O
133	I/O	I/O	I/O	I/O
134	I/O	I/O	I/O	I/O
135	NC	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	NC	I/O	I/O	I/O
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
141	NC	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O
143	NC	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
146	GND	GND	GND	GND
147	I/O	I/O	I/O	I/O
148	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	NC	I/O	I/O	I/O
156	NC	I/O	I/O	I/O
157	GND	GND	GND	GND
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	I/O	I/O	I/O	I/O
163	I/O	I/O	I/O	I/O
164	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	NC	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	NC	I/O	I/O	I/O
171	I/O	I/O	I/O	I/O
172	I/O	I/O	I/O	I/O
173	NC	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O

208-Pin PQFP				
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function	A54SX72A Function
176	NC	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	I/O	I/O	I/O	QCLKD, I/O
179	I/O	I/O	I/O	I/O
180	CLKA	CLKA	CLKA	CLKA, I/O
181	CLKB	CLKB	CLKB	CLKB, I/O
182	NC	NC	NC	NC
183	GND	GND	GND	GND
184	V_{CCA}	V_{CCA}	V_{CCA}	V_{CCA}
185	GND	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O	V_{CCI}
188	I/O	I/O	I/O	I/O
189	NC	I/O	I/O	I/O
190	I/O	I/O	I/O	QCLKC, I/O
191	I/O	I/O	I/O	I/O
192	NC	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	NC	I/O	I/O	I/O
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	NC	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	V_{CCI}	V_{CCI}	V_{CCI}	V_{CCI}
202	NC	I/O	I/O	I/O
203	NC	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	NC	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O	TCK, I/O

100-Pin TQFP (Top View)

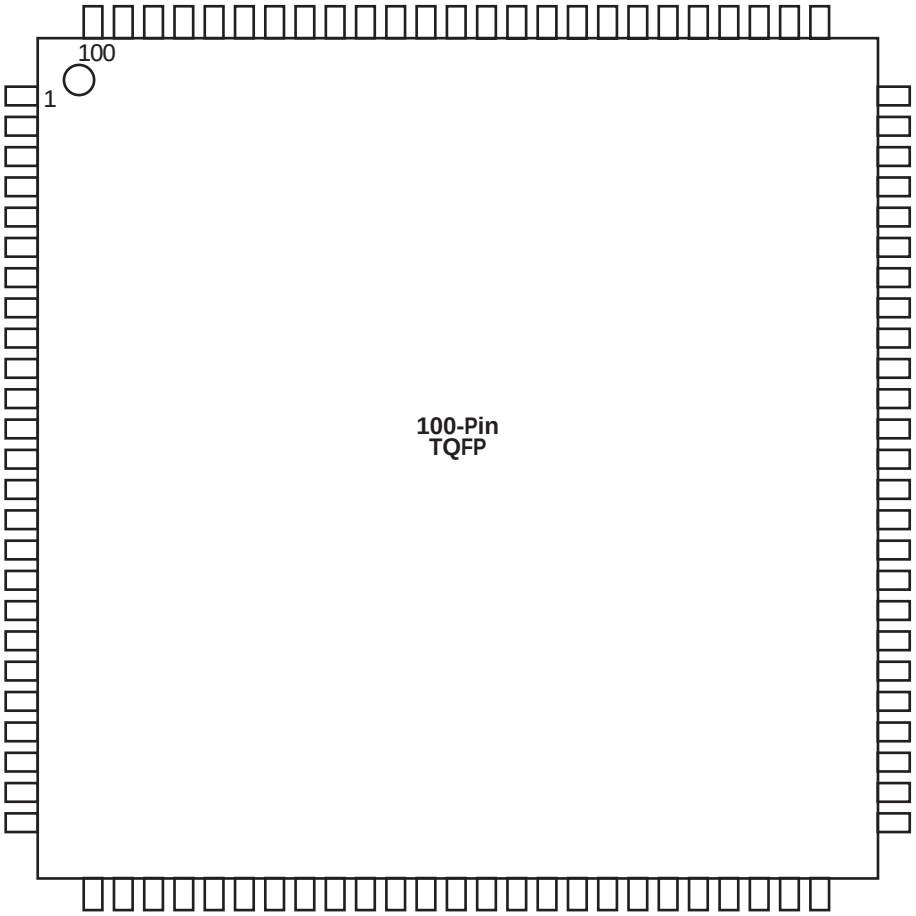


Figure 2-2 • **100-Pin TQFP**

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	TMS	TMS	TMS
8	V_{CCI}	V_{CCI}	V_{CCI}
9	GND	GND	GND
10	I/O	I/O	I/O
11	I/O	I/O	I/O
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	TRST, I/O	TRST, I/O	TRST, I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	V_{CCI}	V_{CCI}	V_{CCI}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	PRB, I/O	PRB, I/O	PRB, I/O
35	V_{CCA}	V_{CCA}	V_{CCA}

100-TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
36	GND	GND	GND
37	NC	NC	NC
38	I/O	I/O	I/O
39	HCLK	HCLK	HCLK
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	TDO, I/O	TDO, I/O	TDO, I/O
50	I/O	I/O	I/O
51	GND	GND	GND
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	V_{CCA}	V_{CCA}	V_{CCA}
58	V_{CCI}	V_{CCI}	V_{CCI}
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	V_{CCA}	V_{CCA}	V_{CCA}
68	GND	GND	GND
69	GND	GND	GND
70	I/O	I/O	I/O

100-TQFP			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	I/O	I/O	I/O
80	I/O	I/O	I/O
81	I/O	I/O	I/O
82	V_{CCI}	V_{CCI}	V_{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	CLKA	CLKA	CLKA
88	CLKB	CLKB	CLKB
89	NC	NC	NC
90	V_{CCA}	V_{CCA}	V_{CCA}
91	GND	GND	GND
92	PRA, I/O	PRA, I/O	PRA, I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	I/O	I/O	I/O
99	I/O	I/O	I/O
100	TCK, I/O	TCK, I/O	TCK, I/O

144-Pin TQFP (Top View)

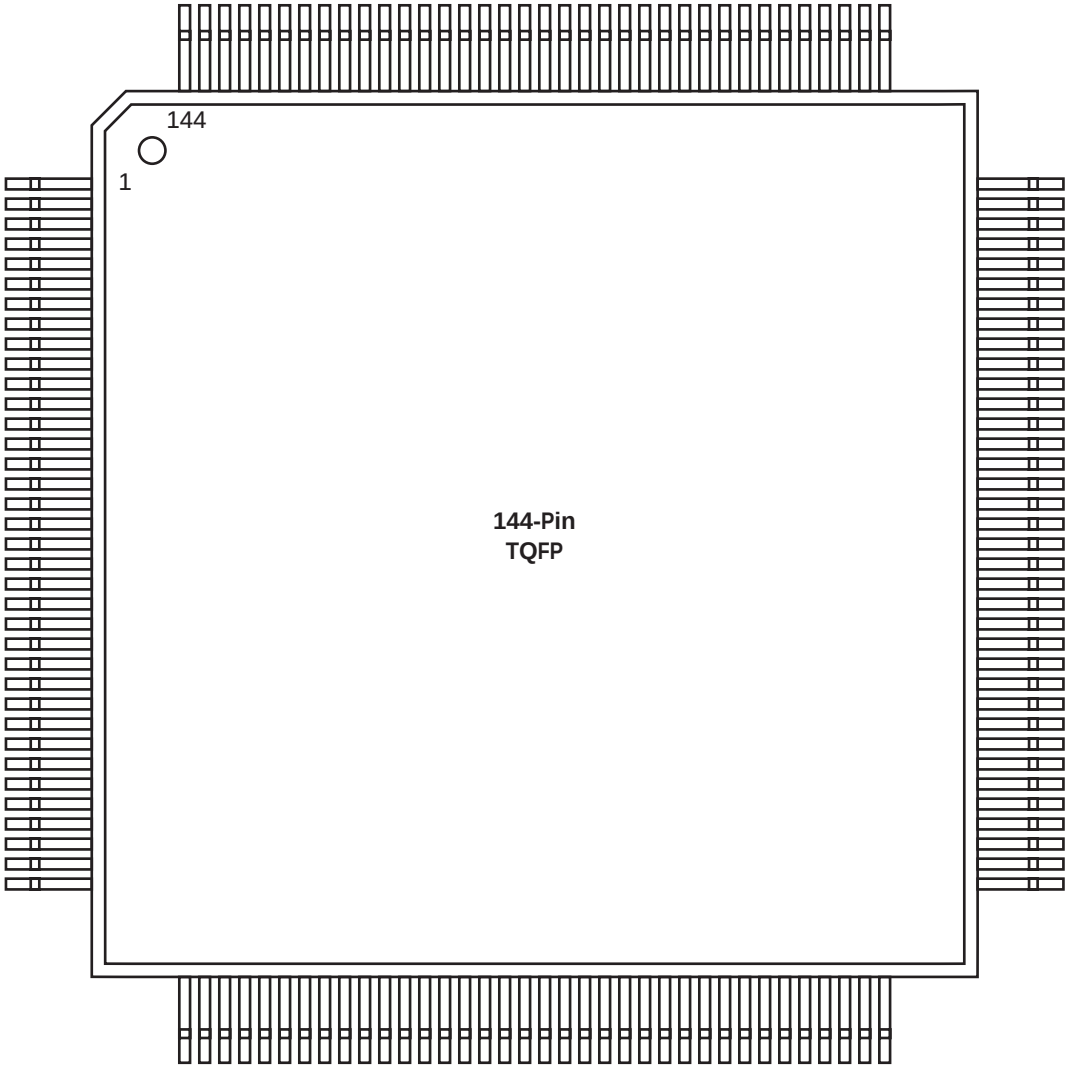


Figure 2-3 • **144-Pin TQFP**

144-Pin TQFP			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V_{CCI}	V_{CCI}	V_{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	NC	NC	NC
20	V_{CCA}	V_{CCA}	V_{CCA}
21	I/O	I/O	I/O
22	TRST, I/O	TRST, I/O	TRST, I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V_{CCI}	V_{CCI}	V_{CCI}
30	V_{CCA}	V_{CCA}	V_{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND

144-Pin TQFP			
Pin Number	**A54SX08A Function**	**A54SX16A Function**	**A54SX32A Function**
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V_{CCI}	V_{CCI}	V_{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V_{CCA}	V_{CCA}	V_{CCA}
57	GND	GND	GND
58	NC	NC	NC
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V_{CCI}	V_{CCI}	V_{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V_{CCA}	V_{CCA}	V_{CCA}
80	V_{CCI}	V_{CCI}	V_{CCI}
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V_{CCA}	V_{CCA}	V_{CCA}
90	NC	NC	NC
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V_{CCA}	V_{CCA}	V_{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V_{CCI}	V_{CCI}	V_{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O

144-Pin TQFP			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V_{CCI}	V_{CCI}	V_{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	NC	NC	NC
128	GND	GND	GND
129	V_{CCA}	V_{CCA}	V_{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V_{CCI}	V_{CCI}	V_{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

144-Pin FBGA (Top View)

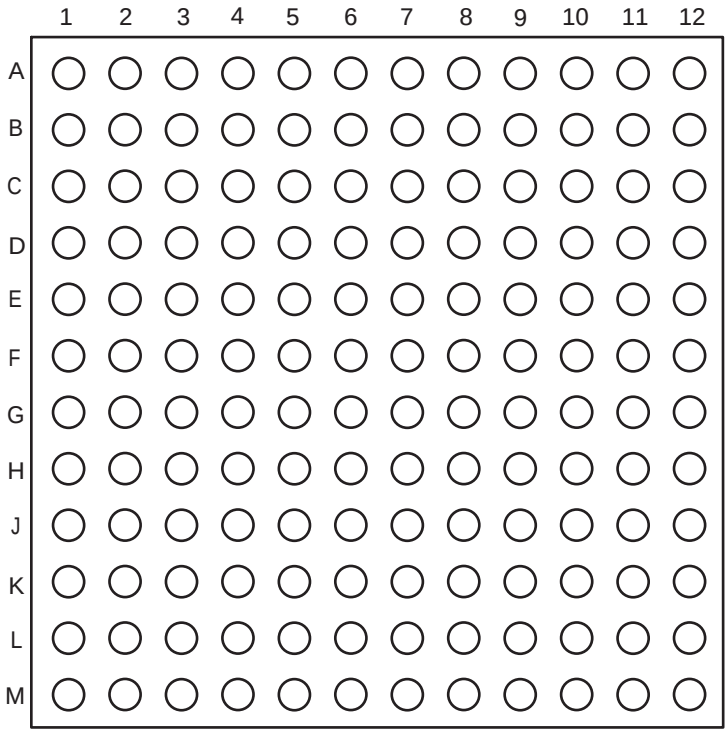


Figure 2-4 • **144-Pin FBGA**

144-Pin FGBA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
A1	I/O	I/O	I/O
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	V_{CCA}	V_{CCA}	V_{CCA}
A6	GND	GND	GND
A7	CLKA	CLKA	CLKA
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	CLKB	CLKB	CLKB
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	GND	GND	GND
B12	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	TCK, I/O	TCK, I/O	TCK, I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	PRA, I/O	PRA, I/O	PRA, I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O

144-Pin FGBA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
D1	I/O	I/O	I/O
D2	V_{CCI}	V_{CCI}	V_{CCI}
D3	TDI, I/O	TDI, I/O	TDI, I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	TMS	TMS	TMS
E6	V_{CCI}	V_{CCI}	V_{CCI}
E7	V_{CCI}	V_{CCI}	V_{CCI}
E8	V_{CCI}	V_{CCI}	V_{CCI}
E9	V_{CCA}	V_{CCA}	V_{CCA}
E10	I/O	I/O	I/O
E11	GND	GND	GND
E12	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	NC	NC	NC
F4	I/O	I/O	I/O
F5	GND	GND	GND
F6	GND	GND	GND
F7	GND	GND	GND
F8	V_{CCI}	V_{CCI}	V_{CCI}
F9	I/O	I/O	I/O
F10	GND	GND	GND
F11	I/O	I/O	I/O
F12	I/O	I/O	I/O

144-Pin FGBA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
G1	I/O	I/O	I/O
G2	GND	GND	GND
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	V_{CCI}	V_{CCI}	V_{CCI}
G9	I/O	I/O	I/O
G10	I/O	I/O	I/O
G11	I/O	I/O	I/O
G12	I/O	I/O	I/O
H1	TRST, I/O	TRST, I/O	TRST, I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V_{CCA}	V_{CCA}	V_{CCA}
H6	VCCA	VCCA	VCCA
H7	V_{CCI}	V_{CCI}	V_{CCI}
H8	V_{CCI}	V_{CCI}	V_{CCI}
H9	V_{CCA}	V_{CCA}	V_{CCA}
H10	I/O	I/O	I/O
H11	I/O	I/O	I/O
H12	NC	NC	NC
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	PRB, I/O	PRB, I/O	PRB, I/O
J7	I/O	I/O	I/O
J8	I/O	I/O	I/O
J9	I/O	I/O	I/O
J10	I/O	I/O	I/O
J11	I/O	I/O	I/O
J12	V_{CCA}	V_{CCA}	V_{CCA}

144-Pin FGBA			
Pin Number	A54SX08A Function	A54SX16A Function	A54SX32A Function
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K6	I/O	I/O	I/O
K7	GND	GND	GND
K8	I/O	I/O	I/O
K9	I/O	I/O	I/O
K10	GND	GND	GND
K11	I/O	I/O	I/O
K12	I/O	I/O	I/O
L1	GND	GND	GND
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	HCLK	HCLK	HCLK
L8	I/O	I/O	I/O
L9	I/O	I/O	I/O
L10	I/O	I/O	I/O
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	V_{CCA}	V_{CCA}	V_{CCA}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	TDO, I/O	TDO, I/O	TDO, I/O
M12	I/O	I/O	I/O

256-Pin FBGA (Top View)

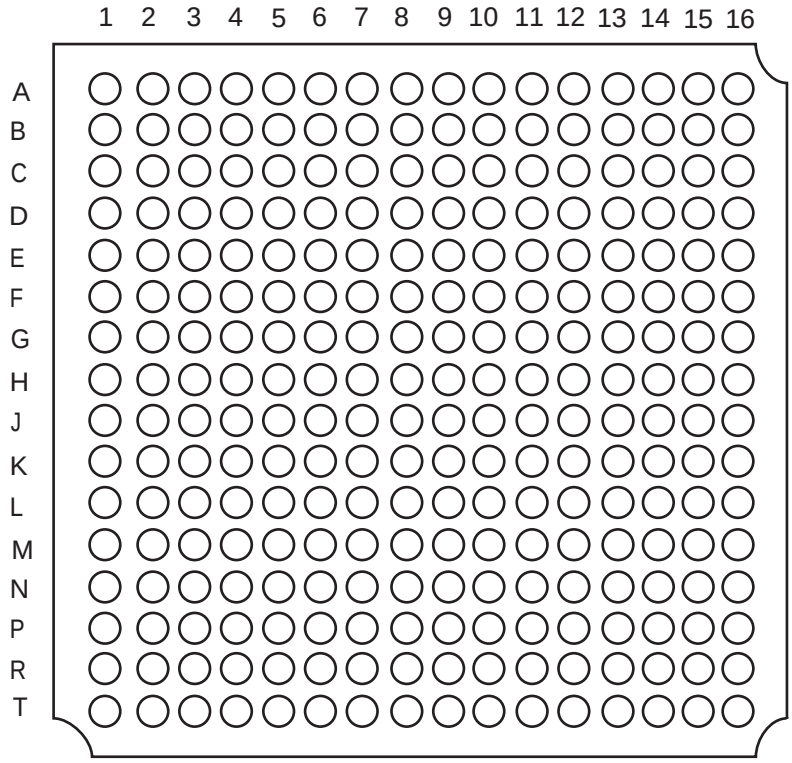


Figure 2-5 • **256-Pin FBGA**

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
A1	GND	GND	GND
A2	TCK, I/O	TCK, I/O	TCK, I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	I/O	I/O	I/O
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	CLKB	CLKB	CLKB, I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	I/O	I/O	I/O
A15	GND	GND	GND
A16	GND	GND	GND
B1	I/O	I/O	I/O
B2	GND	GND	GND
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	NC	I/O	I/O
B7	I/O	I/O	I/O
B8	V_{CCA}	V_{CCA}	V_{CCA}
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	NC	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	GND	GND	GND
B16	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	TDI, I/O	TDI, I/O	TDI, I/O
C3	GND	GND	GND

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
C4	I/O	I/O	I/O
C5	NC	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	CLKA	CLKA	CLKA, I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	PRA, I/O	PRA, I/O	PRA, I/O
D9	I/O	I/O	QCLKD, I/O
D10	I/O	I/O	I/O
D11	NC	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	I/O	I/O	I/O
E6	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
E7	I/O	I/O	QCLKC, I/O
E8	I/O	I/O	I/O
E9	I/O	I/O	I/O
E10	I/O	I/O	I/O
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	NC	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	TMS	TMS	TMS
F5	I/O	I/O	I/O
F6	I/O	I/O	I/O
F7	V_{CCI}	V_{CCI}	V_{CCI}
F8	V_{CCI}	V_{CCI}	V_{CCI}
F9	V_{CCI}	V_{CCI}	V_{CCI}
F10	V_{CCI}	V_{CCI}	V_{CCI}
F11	I/O	I/O	I/O
F12	V_{CCA}	V_{CCA}	V_{CCA}
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	NC	I/O	I/O
G4	I/O	I/O	I/O
G5	I/O	I/O	I/O
G6	V_{CCI}	V_{CCI}	V_{CCI}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND

256-Pin FBGA			
Pin Number	A54SX16A Function	A54SX32A Function	A54SX72A Function
G10	GND	GND	GND
G11	V_{CCI}	V_{CCI}	V_{CCI}
G12	I/O	I/O	I/O
G13	GND	GND	GND
G14	NC	I/O	I/O
G15	V_{CCA}	V_{CCA}	V_{CCA}
G16	I/O	I/O	I/O
H1	I/O	I/O	I/O
H2	I/O	I/O	I/O
H3	V_{CCA}	V_{CCA}	V_{CCA}
H4	TRST, I/O	TRST, I/O	TRST, I/O
H5	I/O	I/O	I/O
H6	V_{CCI}	V_{CCI}	V_{CCI}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V_{CCI}	V_{CCI}	V_{CCI}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	NC	I/O	I/O
J1	NC	I/O	I/O
J2	NC	I/O	I/O
J3	NC	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V_{CCI}	V_{CCI}	V_{CCI}
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V_{CCI}	V_{CCI}	V_{CCI}
J12	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	I/O	I/O	I/O
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	NC	I/O	I/O
K4	V_{CCA}	V_{CCA}	V_{CCA}
K5	I/O	I/O	I/O
K6	V_{CCI}	V_{CCI}	V_{CCI}
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V_{CCI}	V_{CCI}	V_{CCI}
K12	I/O	I/O	I/O
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	NC	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L6	I/O	I/O	I/O
L7	V_{CCI}	V_{CCI}	V_{CCI}
L8	V_{CCI}	V_{CCI}	V_{CCI}
L9	V_{CCI}	V_{CCI}	V_{CCI}
L10	V_{CCI}	V_{CCI}	V_{CCI}
L11	I/O	I/O	I/O
L12	I/O	I/O	I/O
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
L16	NC	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	I/O	I/O	I/O
M7	I/O	I/O	QCLKA, I/O
M8	PRB, I/O	PRB, I/O	PRB, I/O
M9	I/O	I/O	I/O
M10	I/O	I/O	I/O
M11	I/O	I/O	I/O
M12	NC	I/O	I/O
M13	I/O	I/O	I/O
M14	NC	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	I/O	I/O	I/O
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	GND	GND	GND

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	NC	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	NC	I/O	I/O
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	V_{CCA}	V_{CCA}	V_{CCA}
P14	I/O	I/O	I/O
P15	I/O	I/O	I/O
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	GND	GND	GND
R3	I/O	I/O	I/O
R4	NC	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	HCLK	HCLK	HCLK
R10	I/O	I/O	QCLKB, I/O
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	I/O	I/O	I/O
R15	GND	GND	GND
R16	GND	GND	GND
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	NC	I/O	I/O
T5	I/O	I/O	I/O

256-Pin FBGA			
Pin Number	**A54SX16A Function**	**A54SX32A Function**	**A54SX72A Function**
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	V_{CCA}	V_{CCA}	V_{CCA}
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	NC	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TDO, I/O	TDO, I/O	TDO, I/O
T16	GND	GND	GND

484-Pin FBGA (Top View)

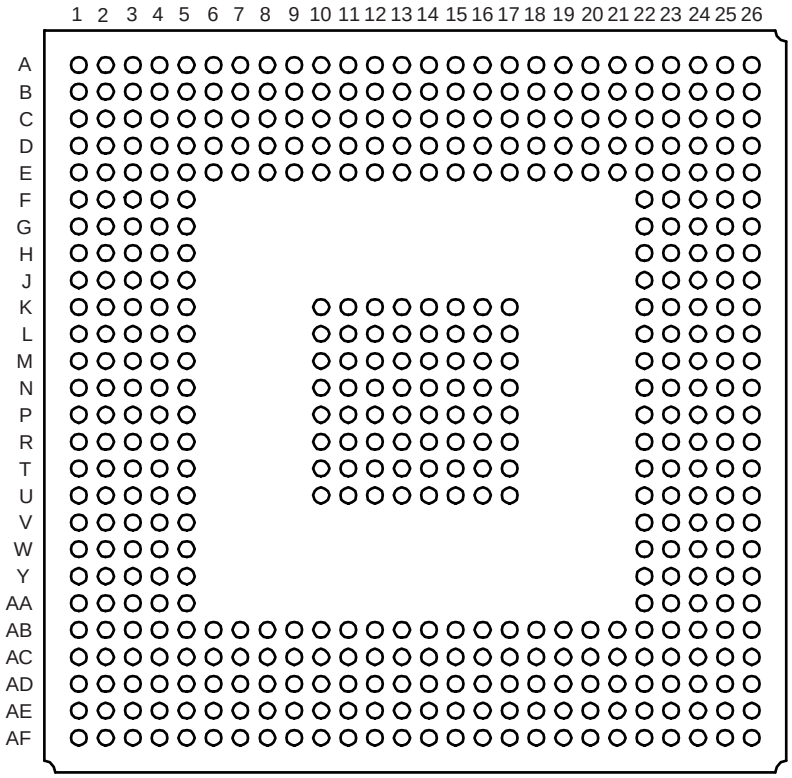


Figure 2-6 • **484-Pin FBGA**

484-Pin FBGA	
Pin Number	**A54SX72A Function**
A1	NC
A2	NC
A3	I/O
A4	I/O
A5	I/O
A6	I/O
A7	I/O
A8	I/O
A9	I/O
A10	I/O
A11	I/O
A12	I/O
A13	I/O
A14	NC
A15	I/O
A16	I/O
A17	I/O
A18	I/O
A19	I/O
A20	I/O
A21	I/O
A22	I/O
A23	I/O
A24	I/O
A25	NC
A26	NC
AA1	I/O
AA2	I/O
AA3	V_{CCA}
AA4	I/O
AA5	I/O
AA22	I/O
AA23	I/O
AA24	I/O
AA25	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
AA26	I/O
AB1	NC
AB2	V_{CCI}
AB3	I/O
AB4	I/O
AB5	I/O
AB6	I/O
AB7	I/O
AB8	I/O
AB9	I/O
AB10	I/O
AB11	I/O
AB12	PRB, I/O
AB13	V_{CCA}
AB14	I/O
AB15	I/O
AB16	I/O
AB17	I/O
AB18	I/O
AB19	I/O
AB20	TDO, I/O
AB21	GND
AB22	I/O
AB23	I/O
AB24	I/O
AB25	I/O
AB26	I/O
AC1	I/O
AC2	I/O
AC3	I/O
AC4	I/O
AC5	V_{CCI}
AC6	I/O
AC7	V_{CCI}
AC8	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
AC9	I/O
AC10	I/O
AC11	I/O
AC12	QCLKA, I/O
AC13	I/O
AC14	I/O
AC15	I/O
AC16	I/O
AC17	I/O
AC18	I/O
AC19	I/O
AC20	V_{CCI}
AC21	I/O
AC22	I/O
AC23	I/O
AC24	I/O
AC25	I/O
AC26	I/O
AD1	I/O
AD2	I/O
AD3	GND
AD4	I/O
AD5	I/O
AD6	I/O
AD7	I/O
AD8	I/O
AD9	V_{CCI}
AD10	I/O
AD11	I/O
AD12	I/O
AD13	V_{CCI}
AD14	I/O
AD15	I/O
AD16	I/O
AD17	V_{CCI}

484-Pin FBGA	
Pin Number	**A54SX72A Function**
AD18	I/O
AD19	I/O
AD20	I/O
AD21	I/O
AD22	I/O
AD23	V_{CCI}
AD24	I/O
AD25	I/O
AD26	I/O
AE1	NC
AE2	I/O
AE3	I/O
AE4	I/O
AE5	I/O
AE6	I/O
AE7	I/O
AE8	I/O
AE9	I/O
AE10	I/O
AE11	I/O
AE12	I/O
AE13	I/O
AE14	I/O
AE15	I/O
AE16	I/O
AE17	I/O
AE18	I/O
AE19	I/O
AE20	I/O
AE21	I/O
AE22	I/O
AE23	I/O
AE24	I/O
AE25	NC
AE26	NC

484-Pin FBGA	
Pin Number	**A54SX72A Function**
AF1	NC
AF2	NC
AF3	I/O
AF4	I/O
AF5	I/O
AF6	I/O
AF7	I/O
AF8	I/O
AF9	I/O
AF10	I/O
AF11	I/O
AF12	NC
AF13	HCLK
AF14	QCLKB, I/O
AF15	I/O
AF16	I/O
AF17	I/O
AF18	I/O
AF19	I/O
AF20	I/O
AF21	I/O
AF22	I/O
AF23	I/O
AF24	I/O
AF25	NC
AF26	NC
B1	NC
B2	NC
B3	I/O
B4	I/O
B5	I/O
B6	I/O
B7	I/O
B8	I/O
B9	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
B10	I/O
B11	I/O
B12	I/O
B13	V_{CCI}
B14	CLKA, I/O
B15	I/O
B16	I/O
B17	I/O
B18	V_{CCI}
B19	I/O
B20	I/O
B21	I/O
B22	I/O
B23	I/O
B24	I/O
B25	I/O
B26	NC
C1	I/O
C2	I/O
C3	I/O
C4	I/O
C5	I/O
C6	V_{CCI}
C7	I/O
C8	I/O
C9	V_{CCI}
C10	I/O
C11	I/O
C12	I/O
C13	PRA, I/O
C14	I/O
C15	QCLKD, I/O
C16	I/O
C17	I/O
C18	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
C19	I/O
C20	V_{CCI}
C21	I/O
C22	I/O
C23	I/O
C24	I/O
C25	I/O
C26	I/O
D1	I/O
D2	TMS
D3	I/O
D4	V_{CCI}
D5	I/O
D6	TCK, I/O
D7	I/O
D8	I/O
D9	I/O
D10	I/O
D11	I/O
D12	QCLKC, I/O
D13	I/O
D14	I/O
D15	I/O
D16	I/O
D17	I/O
D18	I/O
D19	I/O
D20	I/O
D21	V_{CCI}
D22	GND
D23	I/O
D24	I/O
D25	I/O
D26	I/O
E1	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
E2	I/O
E3	I/O
E4	I/O
E5	GND
E6	TDI, IO
E7	I/O
E8	I/O
E9	I/O
E10	I/O
E11	I/O
E12	I/O
E13	V_{CCA}
E14	CLKB, I/O
E15	I/O
E16	I/O
E17	I/O
E18	I/O
E19	I/O
E20	I/O
E21	I/O
E22	I/O
E23	I/O
E24	I/O
E25	V_{CCI}
E26	GND
F1	V_{CCI}
F2	I/O
F3	I/O
F4	I/O
F5	I/O
F22	I/O
F23	I/O
F24	I/O
F25	I/O
F26	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
G1	I/O
G2	I/O
G3	I/O
G4	I/O
G5	I/O
G22	I/O
G23	V_{CCA}
G24	I/O
G25	I/O
G26	I/O
H1	I/O
H2	I/O
H3	I/O
H4	I/O
H5	I/O
H22	I/O
H23	I/O
H24	I/O
H25	I/O
H26	I/O
J1	I/O
J2	I/O
J3	I/O
J4	I/O
J5	I/O
J22	I/O
J23	I/O
J24	I/O
J25	V_{CCI}
J26	I/O
K1	I/O
K2	V_{CCI}
K3	I/O
K4	I/O
K5	V_{CCA}

484-Pin FBGA	
Pin Number	**A54SX72A Function**
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K22	I/O
K23	I/O
K24	NC
K25	I/O
K26	I/O
L1	I/O
L2	I/O
L3	I/O
L4	I/O
L5	I/O
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND
L17	GND
L22	I/O
L23	I/O
L24	I/O
L25	I/O
L26	I/O
M1	NC
M2	I/O
M3	I/O
M4	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
M5	I/O
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M22	I/O
M23	I/O
M24	I/O
M25	I/O
M26	I/O
N1	I/O
N2	V_{CCI}
N3	I/O
N4	I/O
N5	I/O
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N22	V_{CCA}
N23	I/O
N24	I/O
N25	I/O
N26	NC
P1	I/O
P2	I/O
P3	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
P4	I/O
P5	V_{CCA}
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P22	I/O
P23	I/O
P24	V_{CCI}
P25	I/O
P26	I/O
R1	I/O
R2	I/O
R3	I/O
R4	I/O
R5	TRST, I/O
R10	GND
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R22	I/O
R23	I/O
R24	I/O
R25	I/O
R26	I/O
T1	I/O
T2	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
T3	I/O
T4	I/O
T5	I/O
T10	GND
T11	GND
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T22	I/O
T23	I/O
T24	I/O
T25	I/O
T26	I/O
U1	I/O
U2	VCCI
U3	I/O
U4	I/O
U5	I/O
U10	GND
U11	GND
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U22	I/O
U23	I/O
U24	I/O
U25	V_{CCI}
U26	I/O
V1	I/O

484-Pin FBGA	
Pin Number	**A54SX72A Function**
V2	I/O
V3	I/O
V4	I/O
V5	I/O
V22	V_{CCA}
V23	I/O
V24	I/O
V25	I/O
V26	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W5	I/O
W22	I/O
W23	V_{CCA}
W24	I/O
W25	I/O
W26	I/O
Y1	I/O
Y2	I/O
Y3	I/O
Y4	I/O
Y5	I/O
Y22	I/O
Y23	I/O
Y24	V_{CCI}
Y25	I/O
Y26	I/O

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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