

GILA EVT1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
?		?	?	?	?

11/21/03

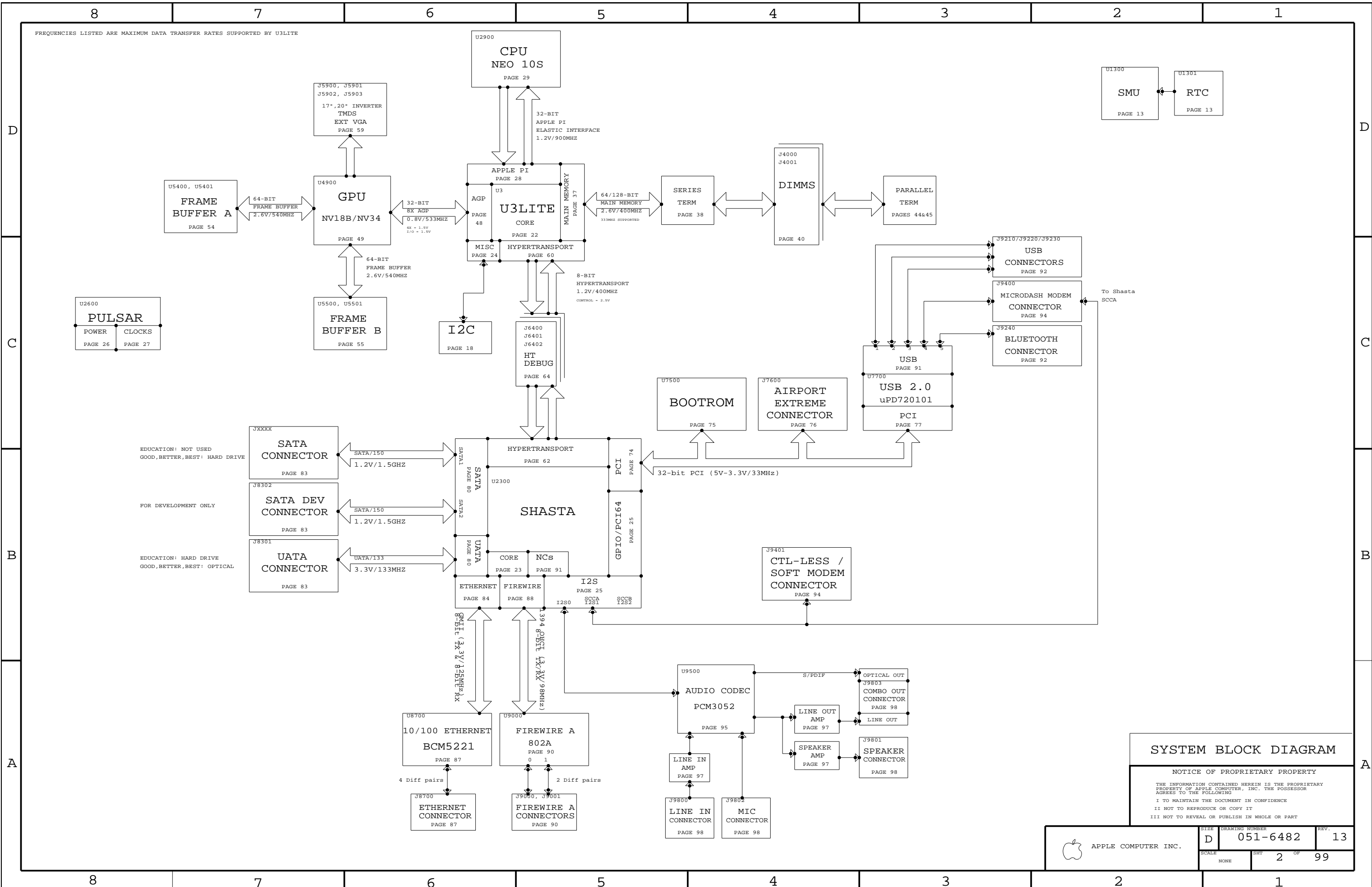
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77*	56	USB2 PCI	
80*	57	SHASTA DISK	
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84*	59	SHASTA ETHERNET	
87	60	ETHERNET PHY & CONNECTORS	ETHERNET
88*	61	SHASTA FIREWIRE	
90	62	FIREWIRE A PHY & CONNECTORS	FIREWIRE
91*	63	USB HOST INTERFACE	
92	64	USB DEVICE INTERFACE	USB
94	65	MODEM CONNECTOR	MODEM
95*	66	AUDIO CODEC, LINE IN, MIC IN	
96*	67	HEADPHONE / LINE OUT	
97*	68	SPEAKER AMP	AUDIO
98*	69	AUDIO CONNECTORS	
99*	70	AUDIO POWER SUPPLIES	

* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

<p style="font-size: 0.8em;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: 0.7em;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: 0.6em;">THIRD ANGLE PROJECTION</p> </div>	<p style="font-weight: bold; font-size: 1.1em;">METRIC</p>	<p style="text-align: right; font-weight: bold; font-size: 1.1em;">Apple Computer Inc.</p> <hr/> <p style="font-size: 0.7em;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: 0.6em;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: 0.5em;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <hr/> <p style="text-align: center; font-weight: bold; font-size: 1.1em;">SCH, MLB, GILA</p> <hr/> <p style="text-align: right;">DRAWING NUMBER 051-6482 REV. 13</p> <p style="text-align: right; font-size: 0.8em;">SHT 1 OF 99</p>
WRAPPER <input checked="" type="checkbox"/> DESIGN CR <input checked="" type="checkbox"/> ENG APPD <input checked="" type="checkbox"/> MFG APPD <input checked="" type="checkbox"/> QA APPD <input checked="" type="checkbox"/> DESIGNER <input checked="" type="checkbox"/> RELEASE <input checked="" type="checkbox"/> SCALE NONE <input checked="" type="checkbox"/>	MATERIAL/FINISH NOTED AS APPLICABLE SIZE D	

FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE



SYSTEM BLOCK DIAGRAM

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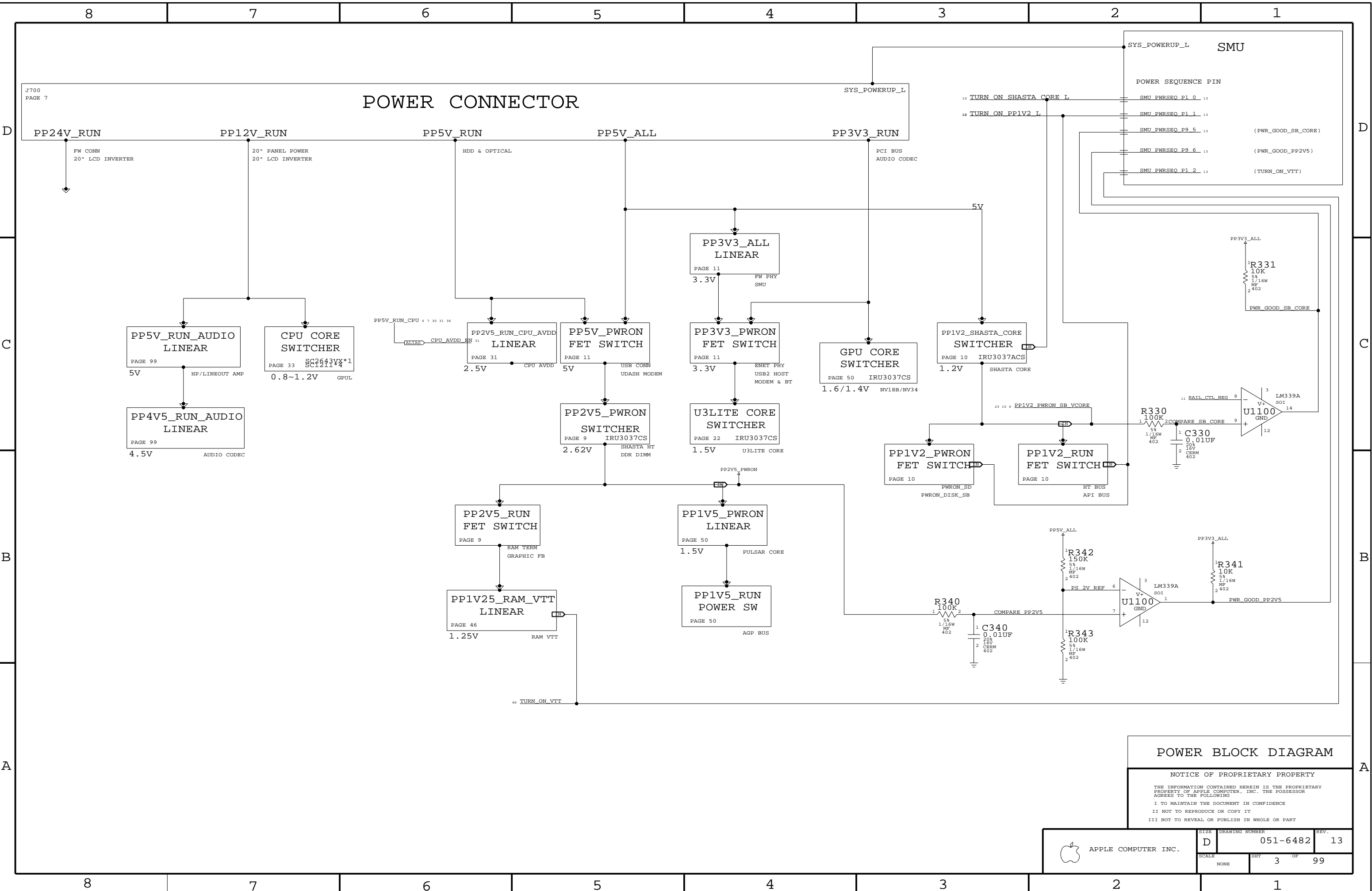
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NONE			



POWER BLOCK DIAGRAM

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NONE	3	99	

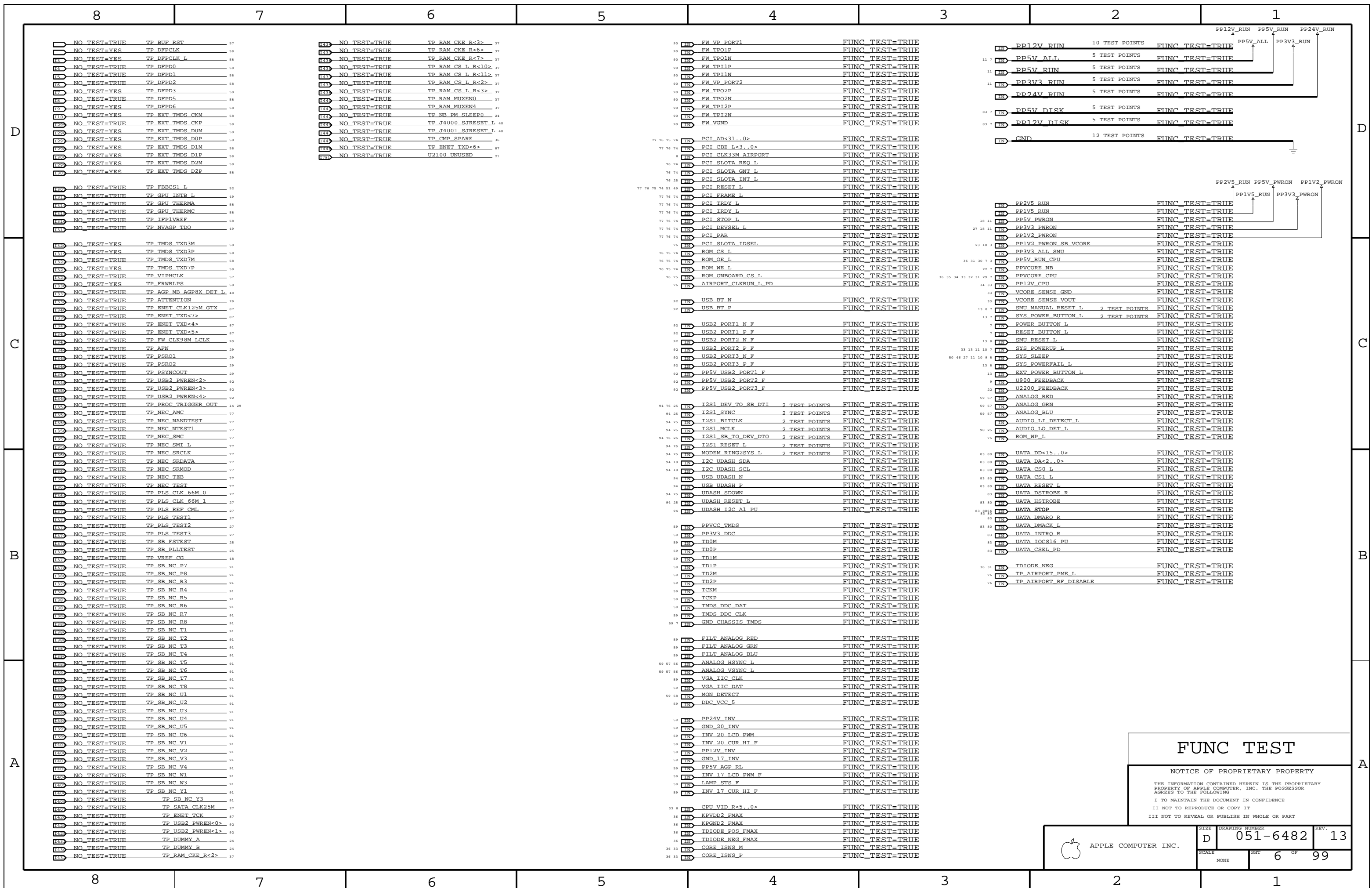
	8	7	6	5	4	3	2	1
	DATE DESCRIPTION							
	10/08/03	PROTO RELEASE (REV 09)						
	10/13/03	CHANGED ALL 4 NB AVDDS TO PP1V5_PWRON_NB_AVDD RAIL TERMINATION FOR VSP CLOCK NOW TRACKS PP1V2_HT RAIL TERMINATION FOR NB CLOCK NOW TRACKS PP1V2_EI_NB RAIL TERMINATION FOR CPU CLOCK NOW TRACKS PP1V2_EI_CPU RAIL NO STUFFED R1303 BECAUSE WHITE LED IS ACTIVE HIGH ADDED 5 PULLDOWNS FOR CPU VID SIGNALS UNCONNECTED THERMAL PAD FOR U9600 HEADPHONE AMP CHECKIN 09001	11/19/03	STUFFING CHANGES FOR ETHERNET RESET CHANGED XW3302 TO LAYER 6 SHORT POWER BUTTON CONNECTOR SYMBOL UPDATED UPDATED CRITICAL LIST CHANGE Y5700 TO 4 PIN CRYSTAL CHECKIN 12005				
	10/14/03	ADDED 4 SMT NUTS U3600 PIN 6 TO PP5V_RUN CHECKIN 09002	11/20/03	CHANGED R2700 TO 220HM AND NOSTUFFED CPU VID SET TO 1.475V J1400 CHANGED TO NOSTUFF CHANGED HALF OF DIMM AND VTT DECOUPLING TO 1UF EVT1 RELEASE (REV 13)				
	10/15/03	SWAPPED EI_CPU_TO_NB_AD17 WITH EI_CPU_TO_NB_AD24 ON J1400 BOM CHANGES FOR R2910, R5727, R9139, R9810 MAIN PROTO RELEASE (REV 10)						
	11/03/03	REPINNED J9240 BLUETOOTH CONNECTOR MANY MIN_NECK_WIDTH UPDATES DC-DC UPDATES ON PAGES 9,10,22,33,34,50 NEW CONNECTORS FOR MODEM AND PATA ADDED GAP FILLER CHANGED PART NUMBER OF NV18B MOVED SERIES TERM FOR PULSAR CLOCKS TO LOGIC ANALYZER PAGE ADDED NET_SPACING_TYPE=PROC_DIFF TO TDIODE_POS, TDIODE_NEG, KPVDD2, AND KPGND2 CHANGED PULSAR 2.2UF CAPS TO 10% MASTER PAGE SYNC CHECKIN 10001						
	11/04/03	NEW AIRPORT CONNECTOR ADDED LEDS FOR 5V ALL RAIL AND PANEL POWER CHANGED DS870X TO LED870X TO FOLLOW CONVENTION REPLACED POWER CONNECTOR MASTER PAGE SYNC RELEASE REV 11						
	11/10/03	J8301 PATA CONNECTOR ROTATED 180 DEGREES MIN_LINE_WIDTH AND MIN_NECK_WIDTH UPDATES THROUGHOUT ADDED EMI-SPRING AND TIED TO GND_CHASSIS_MODEM UPDATED CRYSTAL CONSTRAINTS FIREWIRE NET NAME CHANGES TO MATCH NAMING CONVENTION CHANGED Q1001 TO NTD60N02R CHANGED PULSAR SERIES TERM R2707, R2719, R2701, R2761, R2779 TO 0 OHM CHANGED ZH700 AND ZH701 TO HOL-315R138 CHANGED 20* INVERTER TO 518-0141 CHANGED U3LITE P/N TO V1.1 MASTER PAGE SYNC CHECKIN 11001						
	11/11/03	PLL-LOCK LED CHANGED TO GREEN SMU PART# UPDATED DC/DC NET NAME FIXES ON PAGES 9,10,22 ADDED SERIAL SIGNALS TO AIRPORT CARD FOR NEW MARTY CARD PULSAR SERIES TERM - CHANGED R2705,R2711,R2702 TO 0 OHM. R2770 -> 20 OHM CHANGED SHASTA P/N TO V1.1 UPDATED POWER SEQUENCING TO MATCH SMU PINOUT 1.4 NO_TEST UPDATES ADDED 6 OUTPUT CAPS (124-0322) TO CPU VCORE VREG MASTER PAGE SYNC CHECKIN 11002 - EVT DESIGN REVIEW						
	11/13/03	CHANGED CRYSTAL Y5700 TO 197S0026 LED3002, LED3600, AND LED800 CHANGED TO D3002, D3610, AND D810 P/N 378S0042 CPU POWER SUPPLY FETS - VISHAY USED ON SAMSUNG BOMS AND ON SEMI ON HYNIX BOMS CHANGED INPUT CAPS TO 124-0323 INPUT AND OUTPUT CERM CAPS MARKED AS CRITICAL NEW LARGER CAP FOR VTT VREG. C4609 CHANGED TO 128S0022. C4608 NOSTUFFED BOMOPTIONS AND SCHEMATIC CLEANUP TO AGP (BUSY, STOP, TYPEDET, GCDET) CHANGED 20* INVERTER DECOUPLING TO TWO 1UF 1210 CAPS ADDED MORE POWER AND GROUND SHORTS FOR AUDIO ADDED NET_SPACING_TYPE=PROC_DIFF TO DIFF PAIRS THAT DIDN'T HAVE IT MASTER PAGE SYNC RELEASE REV 12						
	11/14/03	CHANGED PCI_CLK33M_SB_EXT NET NAME ON PAGE 27 FOR REUSE. ALIAS ADDED ON PAGE 8 ADDED ECSET FOR PLS_EXTCLK NET. DROPPED PROP DELAY FROM OTHER CRYSTALS ALIASED PP5V_AUDIO TO PP5V_RUN RAIL ADDED CIRCUIT SO 5V RAIL TO 17* INVERTER COMES UP AFTER 12V R2742 CHANGED TO 806 OHM MASTER PAGE SYNC CHECKIN 12001						
	11/15/03	CHANGED J8303 TO 5 PIN CONNECTOR CHANGED MICRodash MODEM HEIGHT AND CHANGED TO DEVELOPMENT BOM OPTION						
	11/17/03	PIN SWAPPED L5908 FOR ROUTING STUFFED TMS INDUCTORS AND NOSTUFFED 0 OHM RESISTORS CHANGED MODEM STANDOFFS TO 862-0035 AND ADDED ELECTRICAL CONNECTIONS ADDED TWO MORE SMT NUTS FOR CPU HEATSINK CHANGED LED700,701,702,5900,8301,8700,8701,8702 AND D3001 TO 378S0045 MASTER PAGE SYNC CHECKIN 12002						
	11/17/03	NO_TEST, FUNC_TEST UPDATES CHECKIN 12003						
	11/18/03	CHASSIS MODEM NO LONGER TIES TO REST OF CHASSIS ADDED CAPS TO GROUND FOR CPU HEATSINK SMT NUTS CHANGED CRYSTAL FILTERING FOR PULSAR MOVED RAM_CKE SIGNALS TO 62 OHM VTT PARALLEL TERM WITH 4.7K PULL-DOWN ADDED POWER SEQUENCING FOR VTT VREG MASTER PAGE SYNC CHECKIN 12004						
	8	7	6	5	4	3	2	1

REVISION HISTORY

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FUNC TEST

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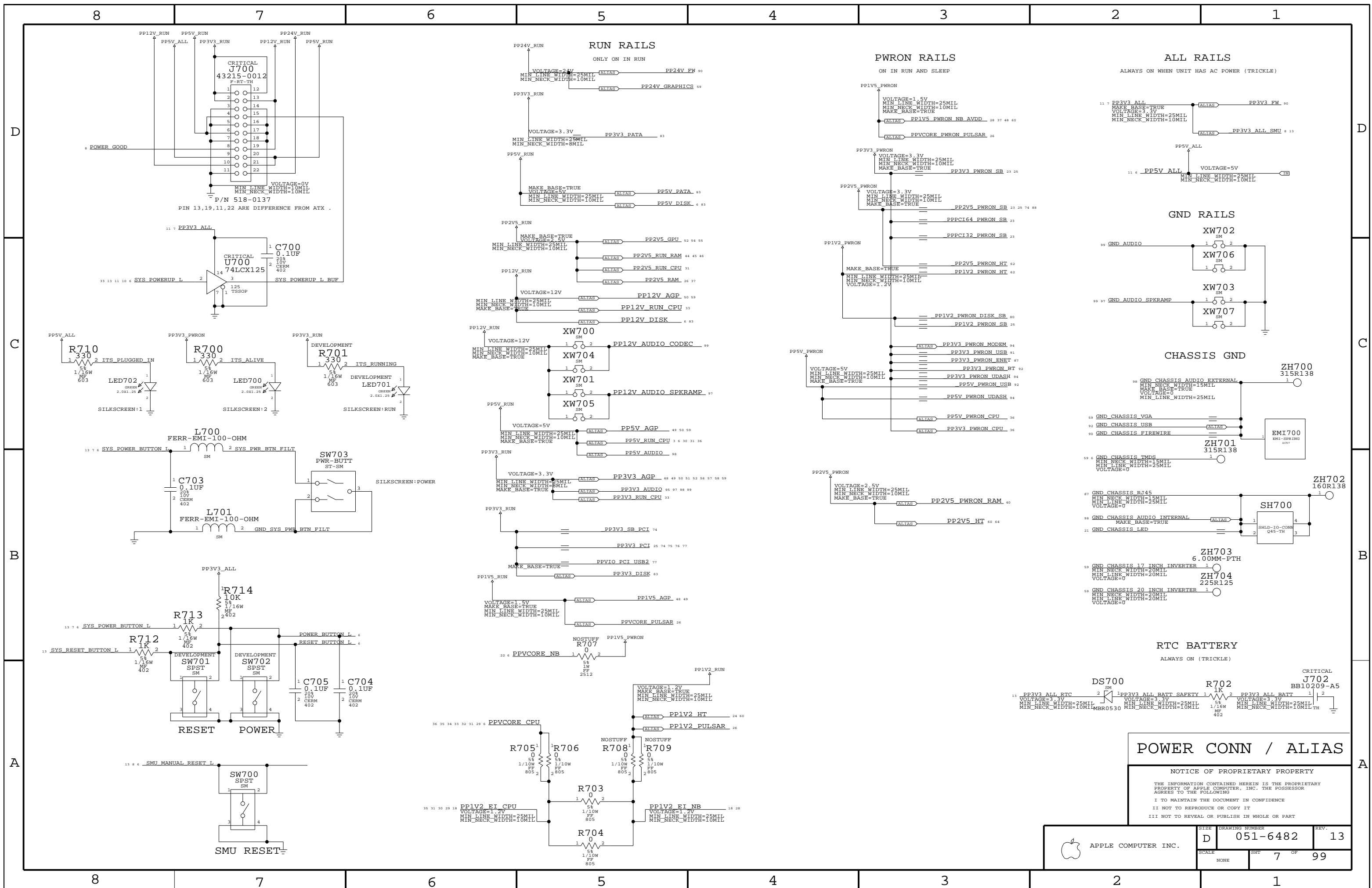
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POWER CONN / ALIAS

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	NONE	7 OF 99	13

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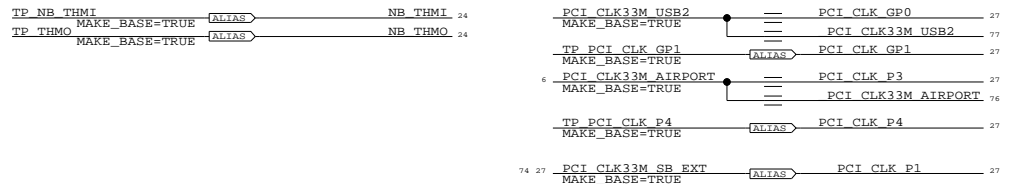
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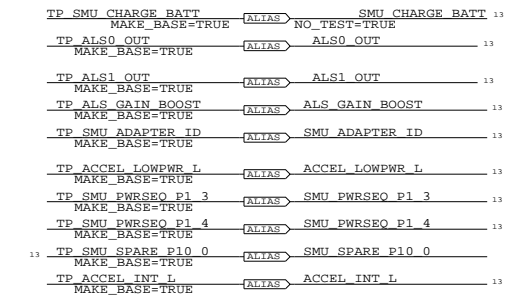
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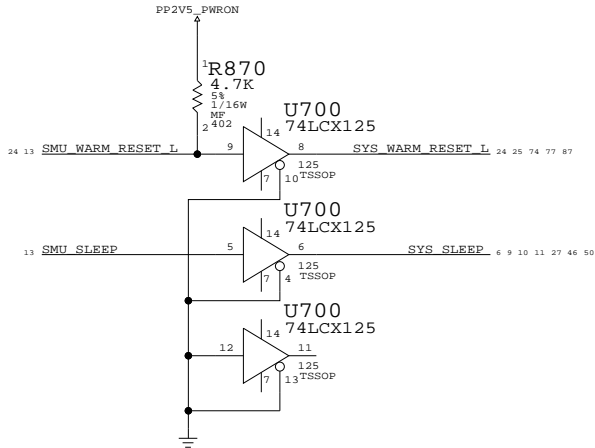
PCI CLOCKS



SMU



PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2784	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV2,1.8GHZ,70C	1.8GHZ	1.15V	45W	?	U2900	NEO_REV2_1_8GHZ
337S2785	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV2,2.0GHZ,70C	2.0GHZ	1.15V	65W	?	U2900	NEO_REV2_2_0GHZ
337S2786	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV3,1.8GHZ,70C	1.8GHZ	1.15V	45W	?	U2900	NEO_REV3_1_8GHZ
337S2787	1	PROCESSOR	CBGA-576-1MM	IC,MPU,NEO,10S,REV3,2.0GHZ,70C	2.0GHZ	1.15V	65W	?	U2900	NEO_REV3_2_0GHZ



MISC PARTS

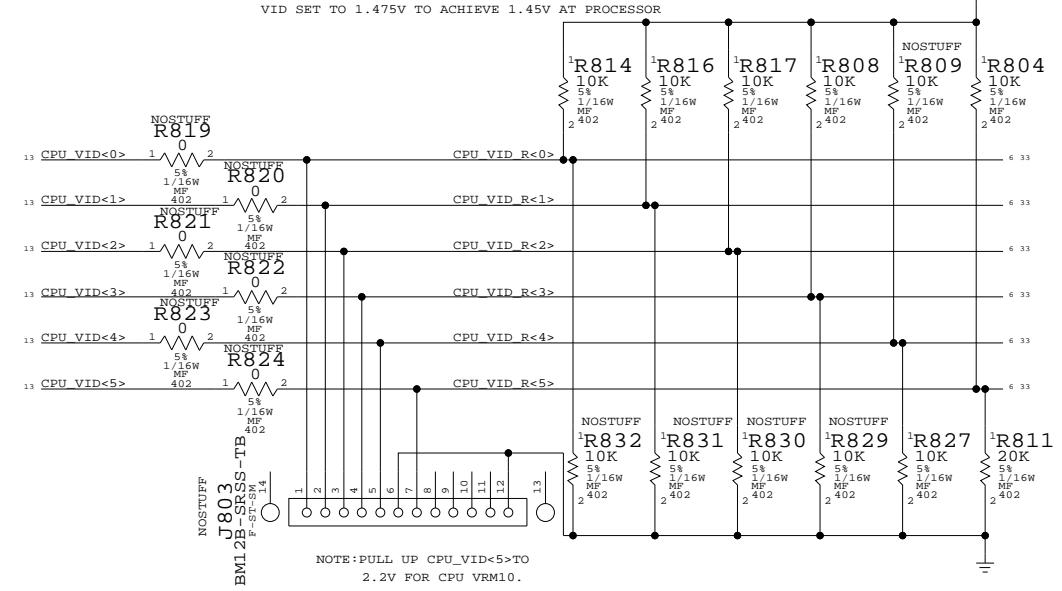
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
820-1540	1	PCB,FAB,MLB	MLB1	
825-2029	1	LBL,SER #,INP DEV	LBL1	
051-6482	1	PCB,SCHEM,MLB	SCH1	
341T1366	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT700	
875-1614	1	GAP FILLER	GAP2900	
341T1395	1	PURCH ASSY, SMU BIG	UI300	
875-1752	1	GPU GAP PAD	PAD4900	
452-0678	6	CPU HEATSINK SCREW	SRW800,SRW801,SRW802	SRW803,SRW804,SRW805
870-1177	6	CPU HEATSINK SPRING	SPR800,SPR801,SPR802	SPR803,SPR804,SPR805
730-0291	1	CPU HEATSINK	HS2900	

NEED TO ADD THERMAL GREASE TO MLB BOM

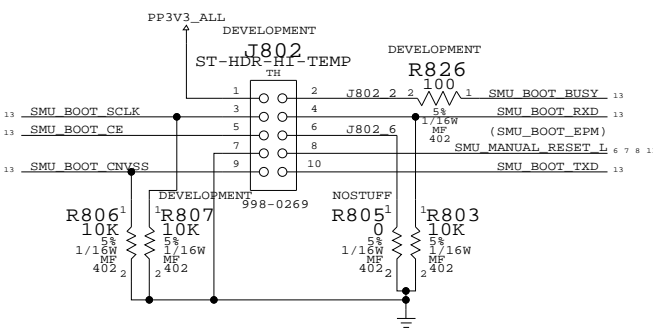
ALTERNATE FOR SERIAL NUMBER LABEL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
825-2808	825-2029	COMMON	LBL1	BAR CODE LABEL

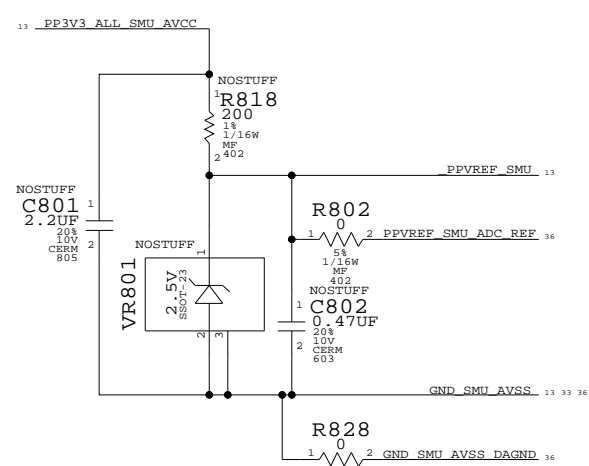
CPU VID<0:5>



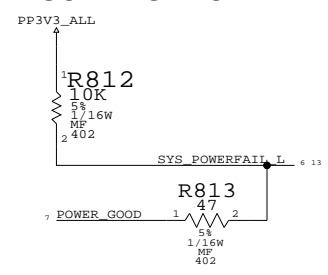
DOWNLOAD CONNECTOR



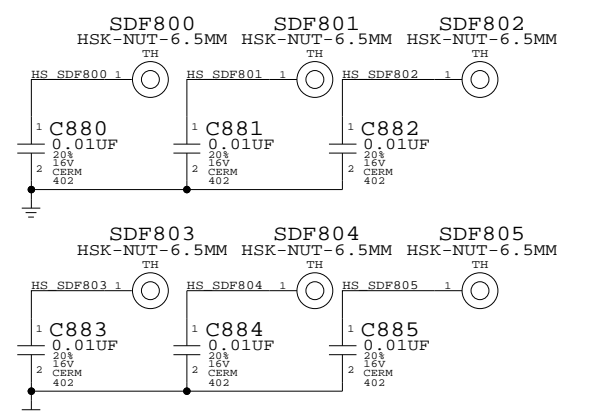
SMU ANALOG VREF



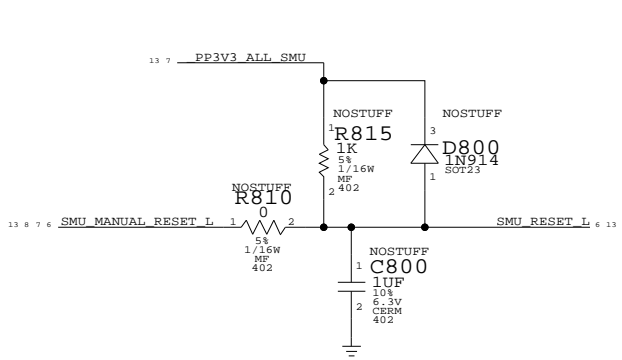
POWER_FAIL_L CONNECTION



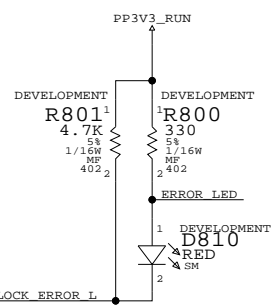
CPU HEATSINK SMT NUTS



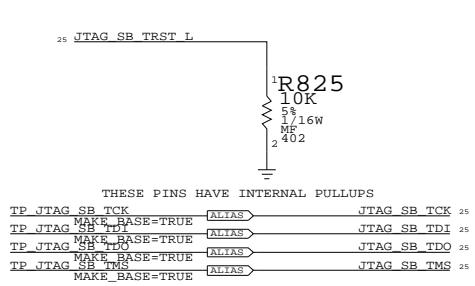
CHEAPER SMU RESET



PULSAR ERROR_L LED



SHASTA JTAG PULL DOWN



SIGNAL ALIAS

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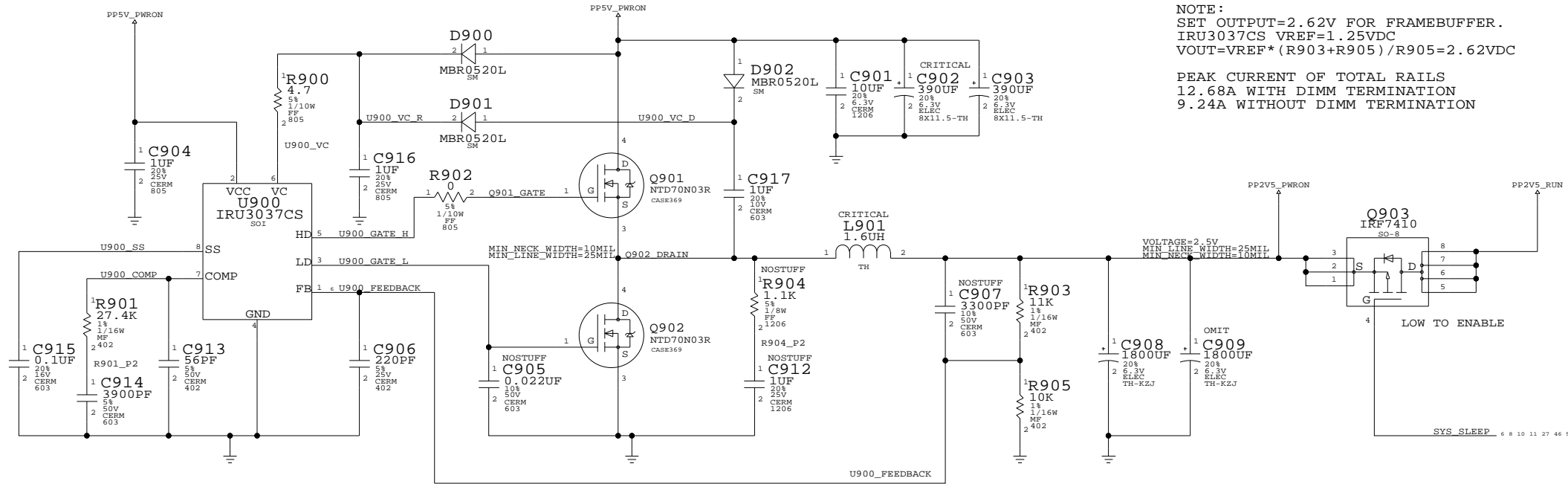
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2.5V VOLTAGE REGULATOR



NOTE:
 SET OUTPUT=2.62V FOR FRAMEBUFFER.
 IRU3037CS VREF=1.25VDC
 $V_{OUT} = V_{REF} * (R_{903} + R_{905}) / R_{905} = 2.62VDC$

PEAK CURRENT OF TOTAL RAILS
 12.68A WITH DIMM TERMINATION
 9.24A WITHOUT DIMM TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
124-0324	1	CAP,AL ELEC,1500UF,6.3V	C909	17_INCH_LCD
124-0322	1	CAP,AL ELEC,1800UF,6.3V	C909	20_INCH_LCD

2.5V VREG

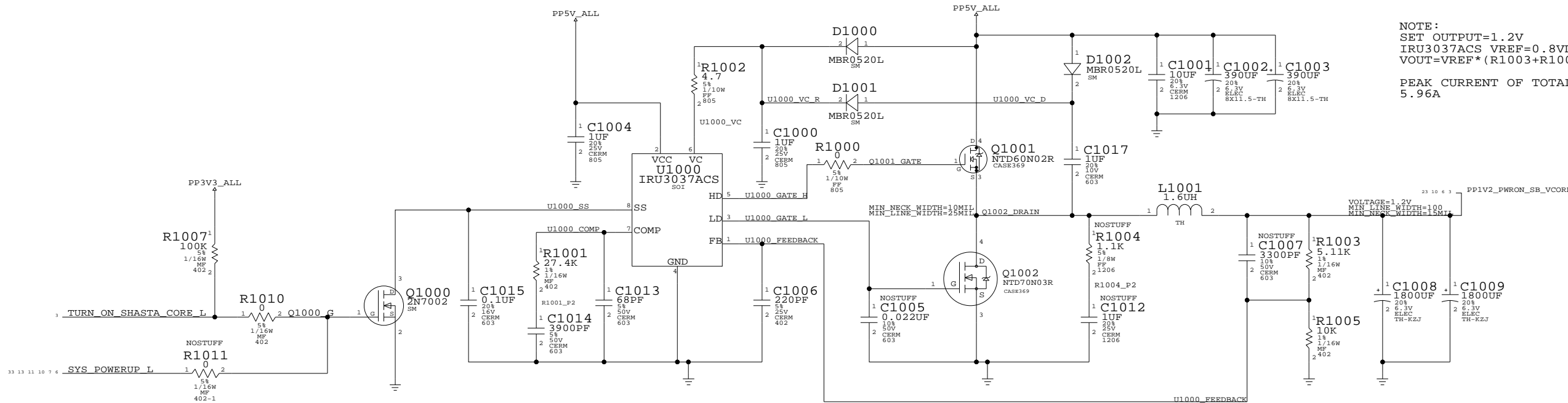
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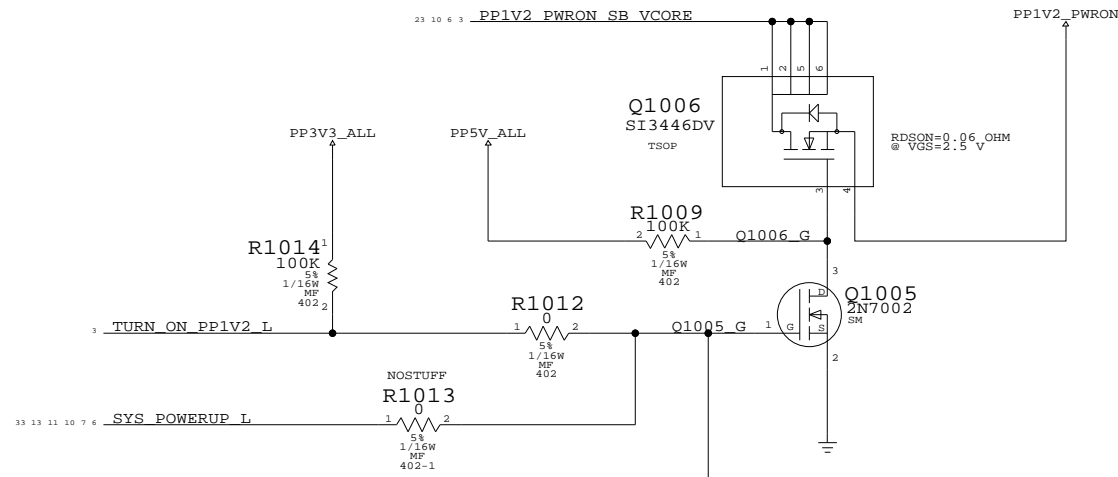
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SCALE		SHT	OF
NONE		9	99

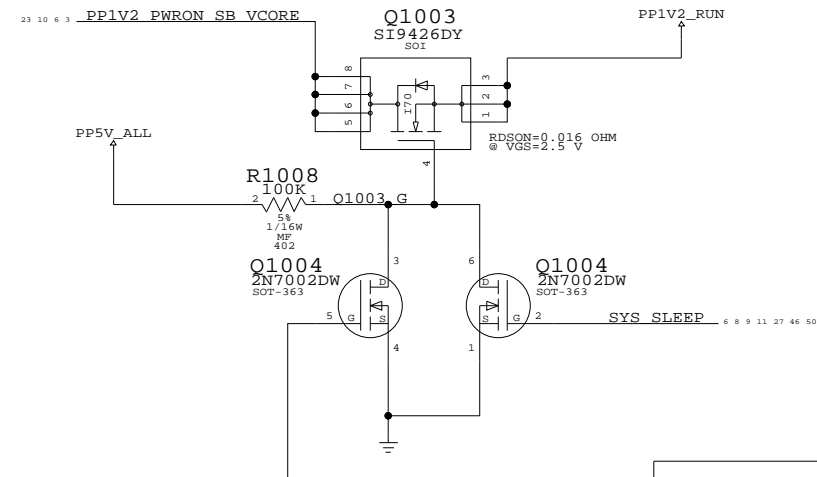
SHASTA CORE VOLTAGE REGULATOR



PP1V2_PWRON FET SWITCH
PEAK CURRENT 0.6A



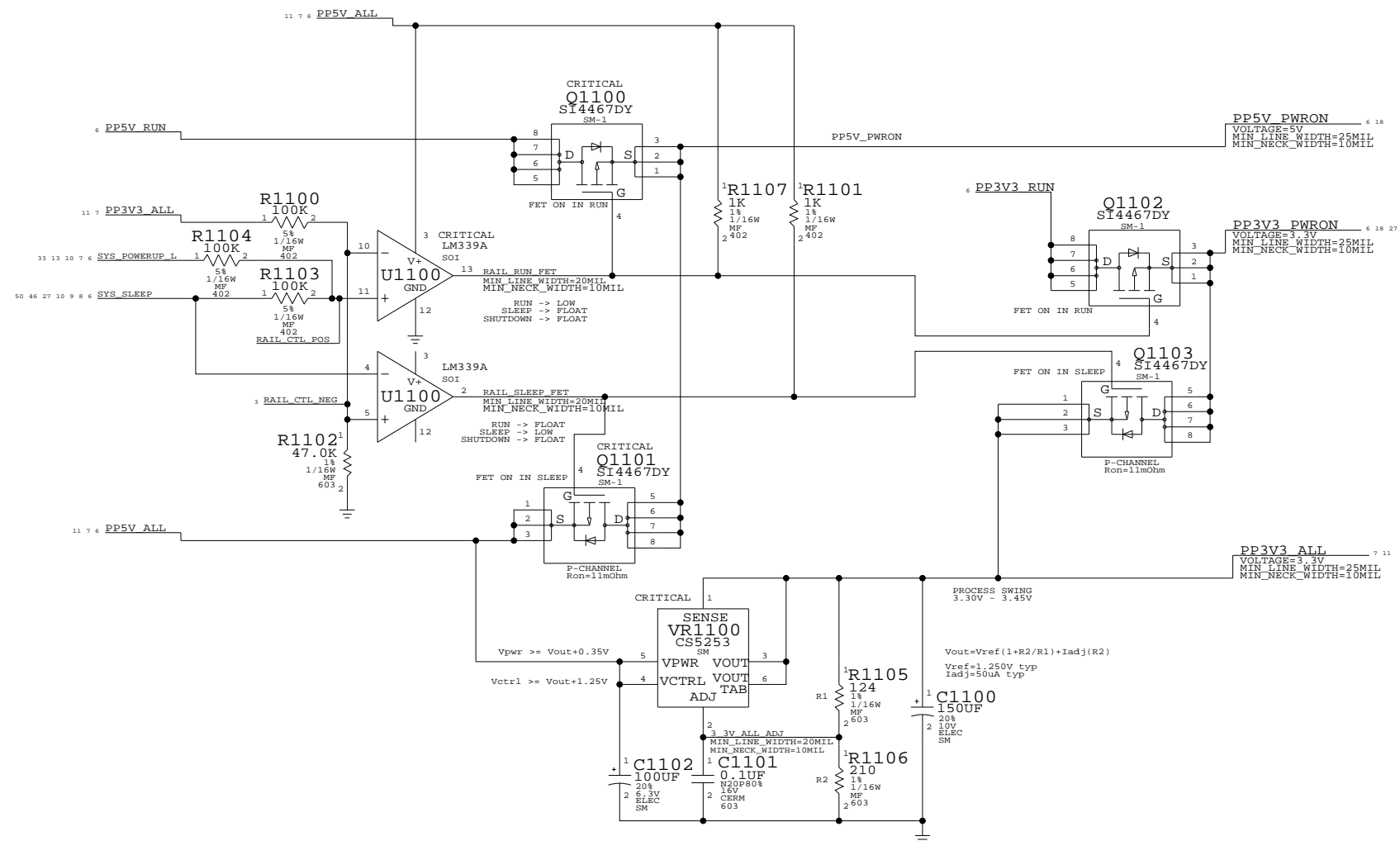
PP1V2_RUN FET SWITCH
PEAK CURRENT 4.43A



1.2V VREG

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5V & 3.3V VREGS

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NONE	11		99

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	15 MIL SPACING	SMU_CLK10M_XIN
	15 MIL SPACING	SMU_CLK10M_XOUT
	15 MIL SPACING	SMU_CLK10M_XOUT_R
RTC_CLK32K_XTAL	15 MIL SPACING	RTC_CLK32K_X1
	15 MIL SPACING	RTC_CLK32K_X2

Page Notes

Power aliases required by this page:
 - _PP3V3_ALL_SMU
 - _PP3V3_ALL_RTC
 - _PP3V3_PWRON_SMU
 - _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

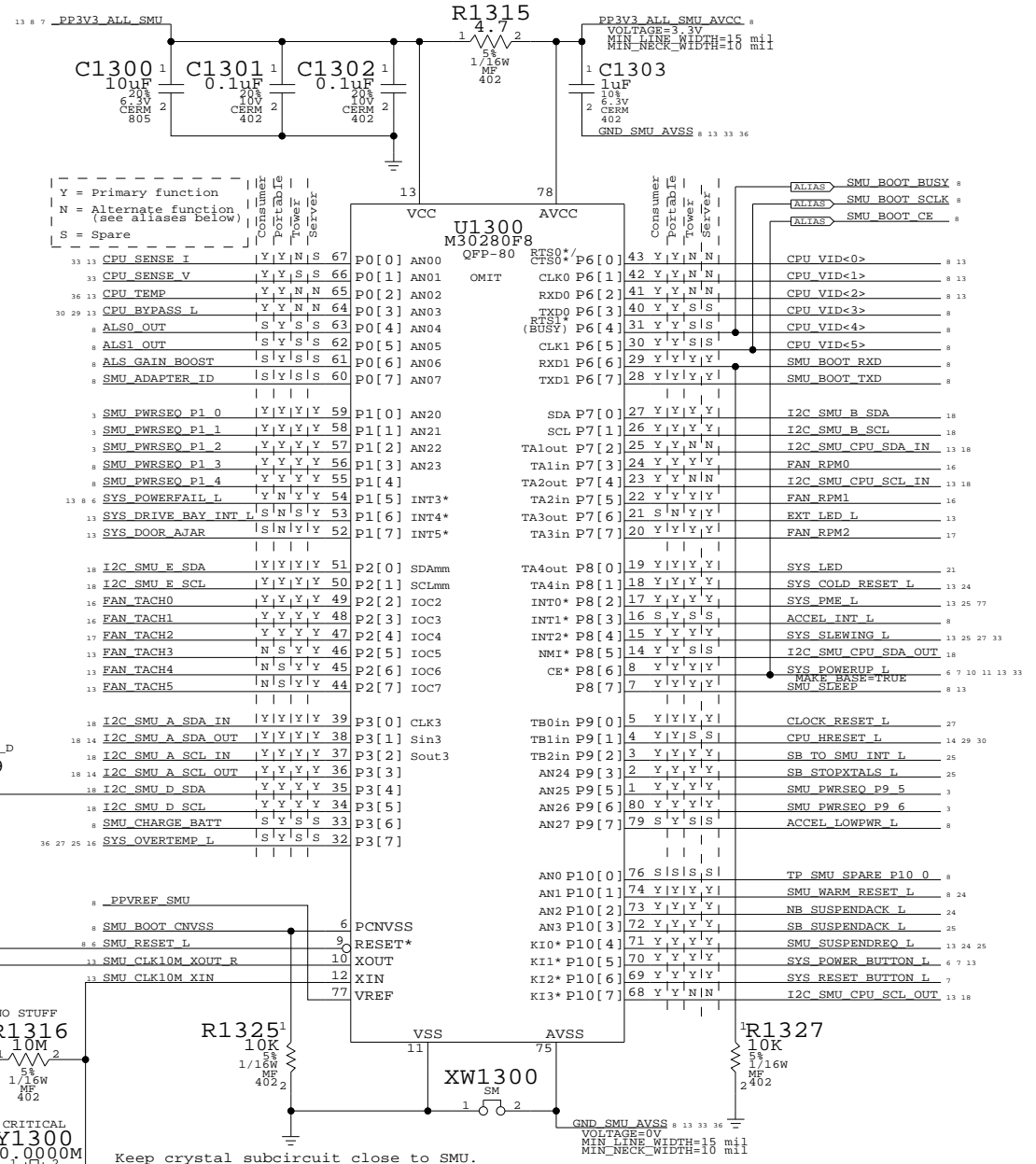
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

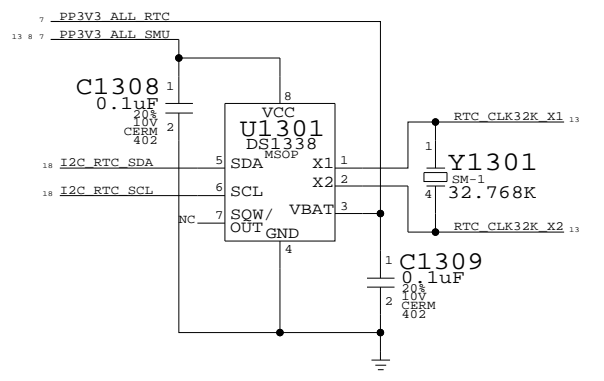
NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.4.

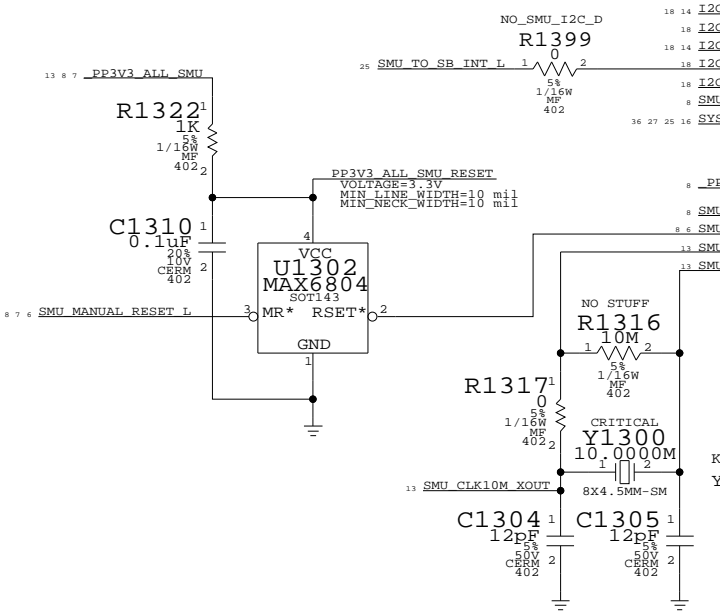
System Management Unit



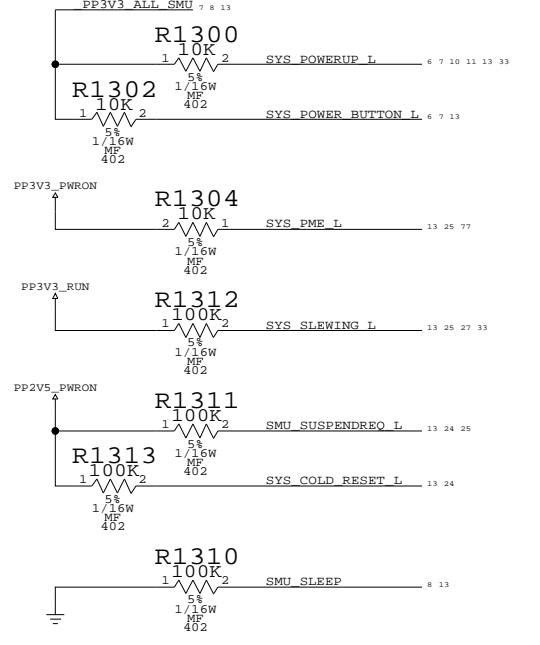
Real Time Clock



Undervoltage Reset Circuit



SMU Pull-ups / pull-down



Alternate Functions

Consumer		Portable		Tower & Server	
Port		Port		Port	
13 FAN TACH3	2.5 [ALIAS] SYS_LED_RED	13 SYS POWERFAIL L	1.5 [ALIAS] SMU_ACIN	33 CPU_SENSE_I	0.0 [ALIAS] SYS_SLOT_PWR
13 FAN TACH4	2.6 [ALIAS] SYS_LED_GREEN	13 SYS_DRIVE_BAY_INT L	1.6 [ALIAS] SMU_BATT_DET L	36 CPU_TEMP	0.2 [ALIAS] FAN_TACH6
13 FAN TACH5	2.7 [ALIAS] SYS_LED_BLUE	13 SYS_DOOR_AJAR	1.7 [ALIAS] SYS_LID_OPEN	30 29 13 CPU_BYPASS L	0.3 [ALIAS] FAN_TACH7
		13 EXT_LED L	7.6 [ALIAS] SYS_KBDLED	13 CPU_VID<0>	6.0 [ALIAS] FAN_RPM3
				13 CPU_VID<1>	6.1 [ALIAS] FAN_RPM4
				13 CPU_VID<2>	6.2 [ALIAS] FAN_RPM5
				13 I2C_SMU_CPU_SDA_IN	7.2 [ALIAS] FAN_PWM6
				18 13 I2C_SMU_CPU_SCL_IN	7.4 [ALIAS] FAN_PWM7
				18 13 I2C_SMU_CPU_SCL_OUT 10.7	[ALIAS] EXT_POWER_BUTTON L

System Management Unit

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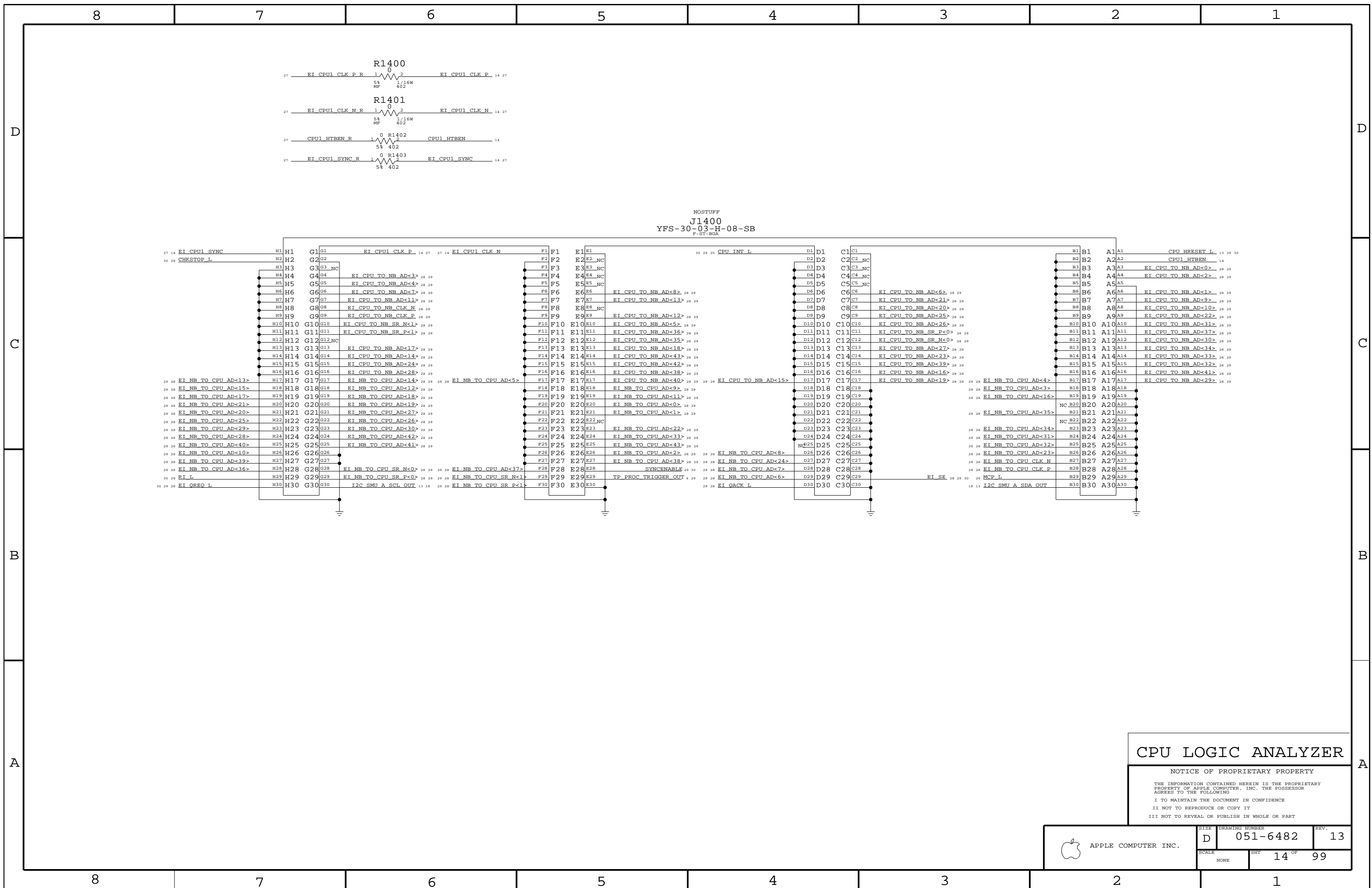
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	SHEET	OF	
	13	99	



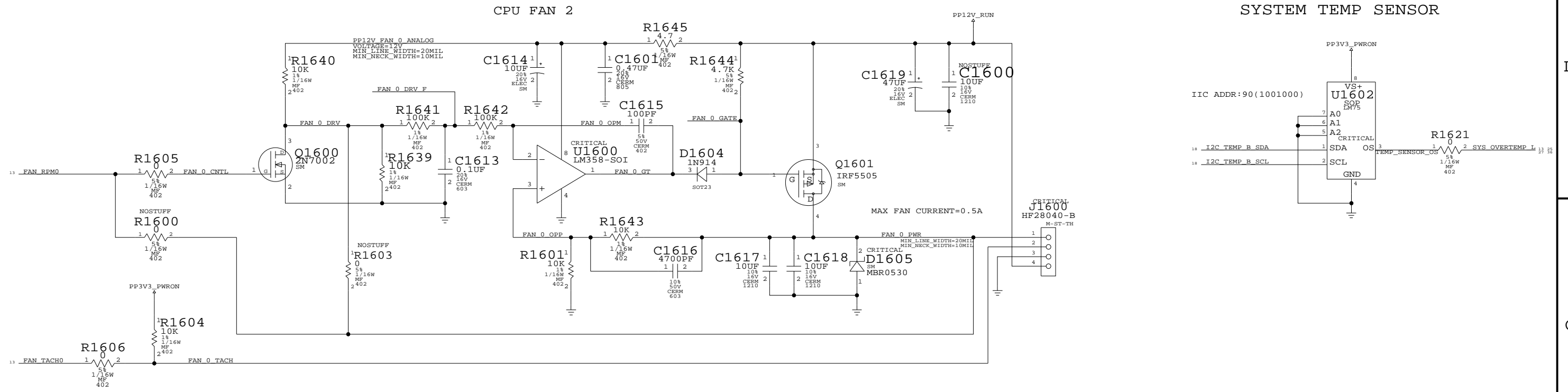
CPU LOGIC ANALYZER

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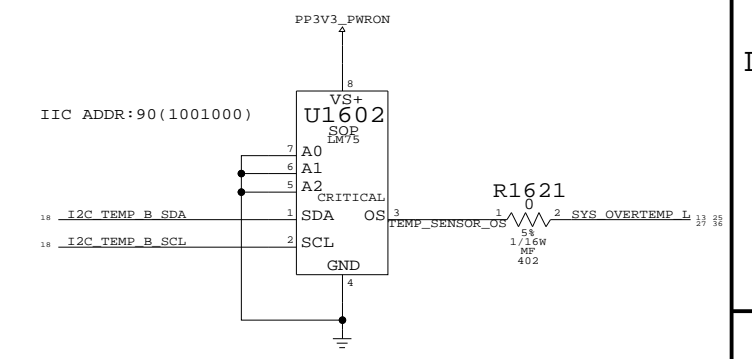
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	SCALE NONE	SHEET 14 OF 99	

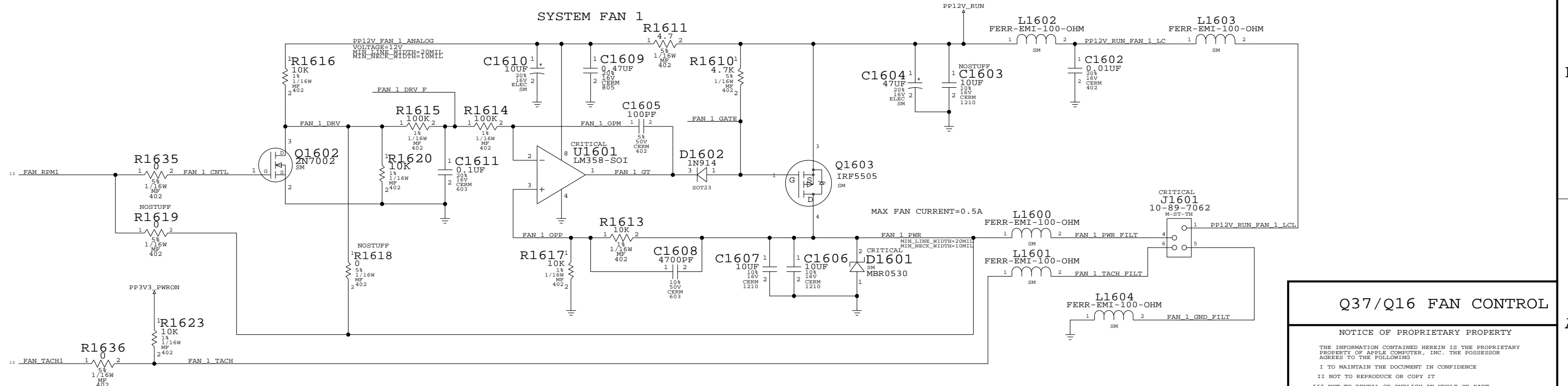
FAN 0 - Q37 STYLE CPU FAN CONTROL CIRCUIT



SYSTEM TEMP SENSOR



FAN 1 - Q37 STYLE CPU FAN CONTROL CIRCUIT



Q37/Q16 FAN CONTROL

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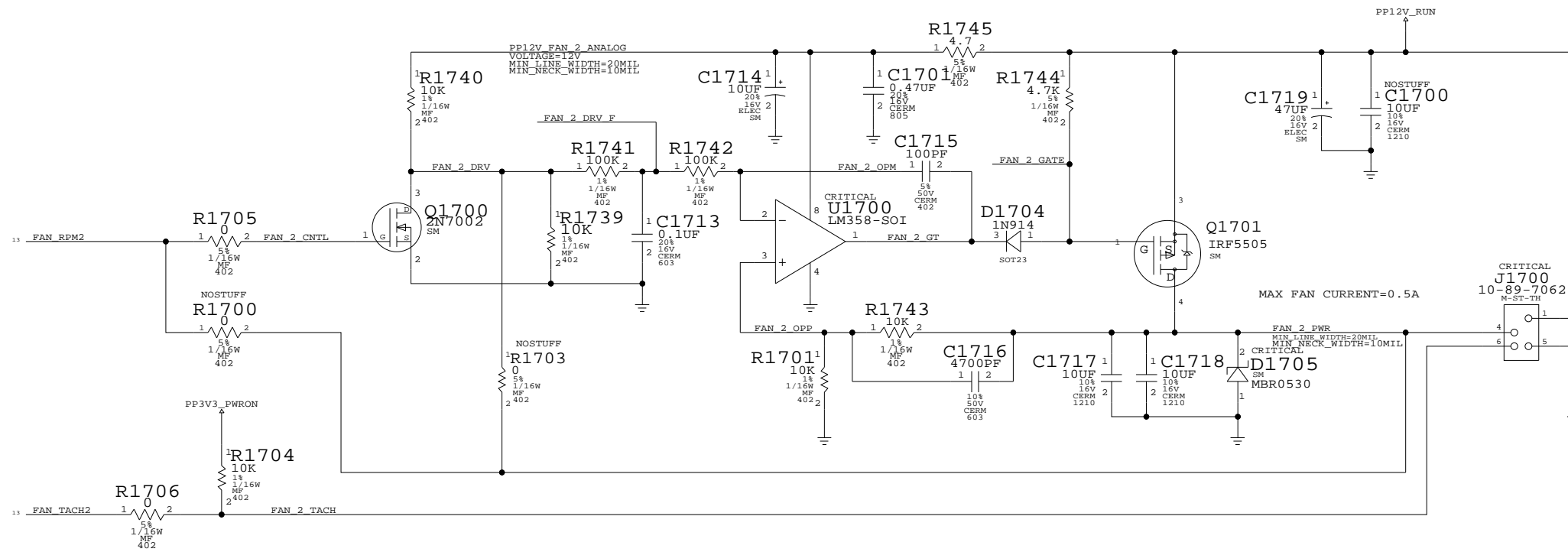
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		16	99

FAN 2 - Q37 STYLE SYSTEM FAN CONTROL CIRCUIT



CPU FAN CONNECTOR

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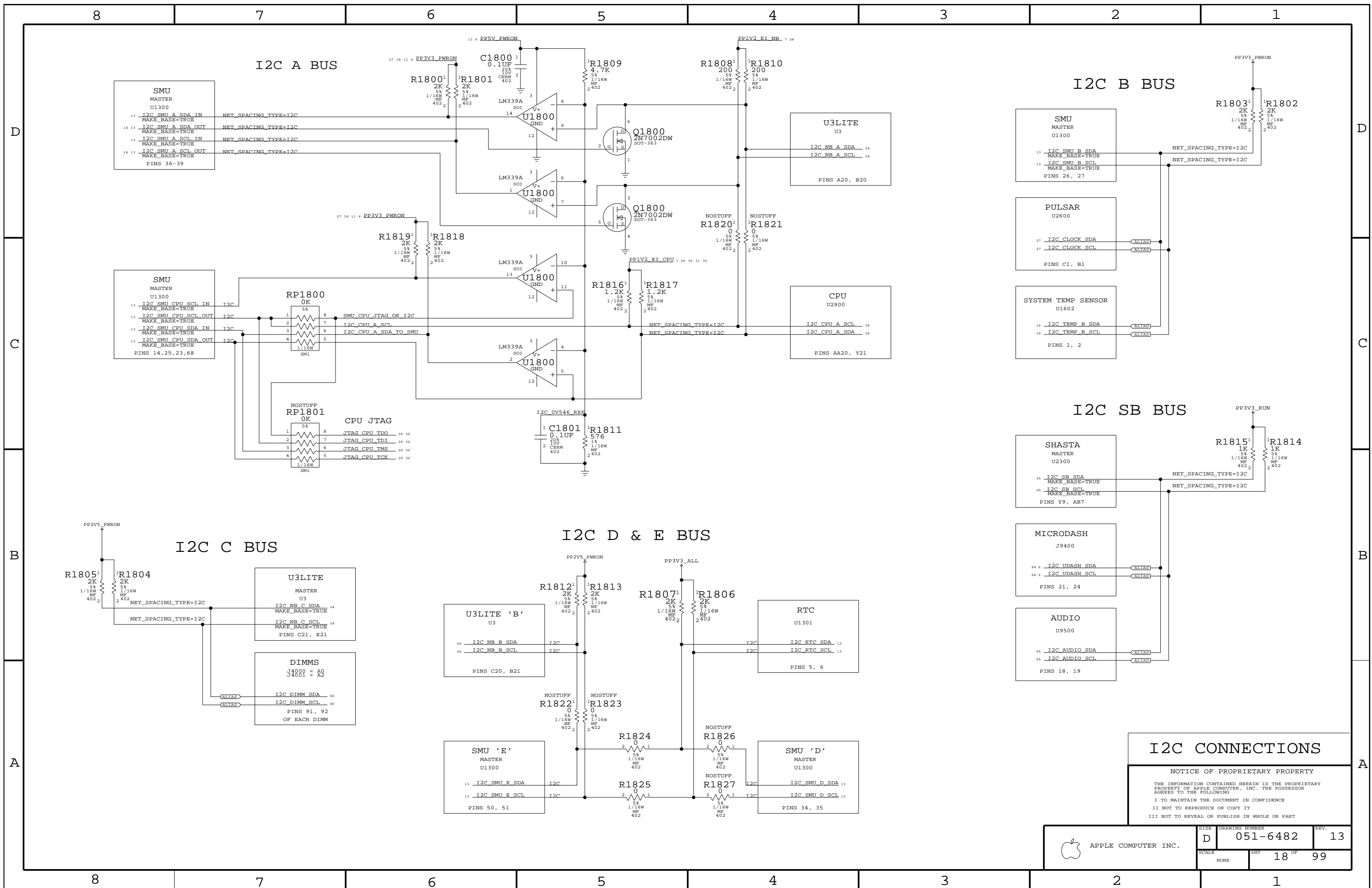
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NONE		17 OF 99	



I2C CONNECTIONS

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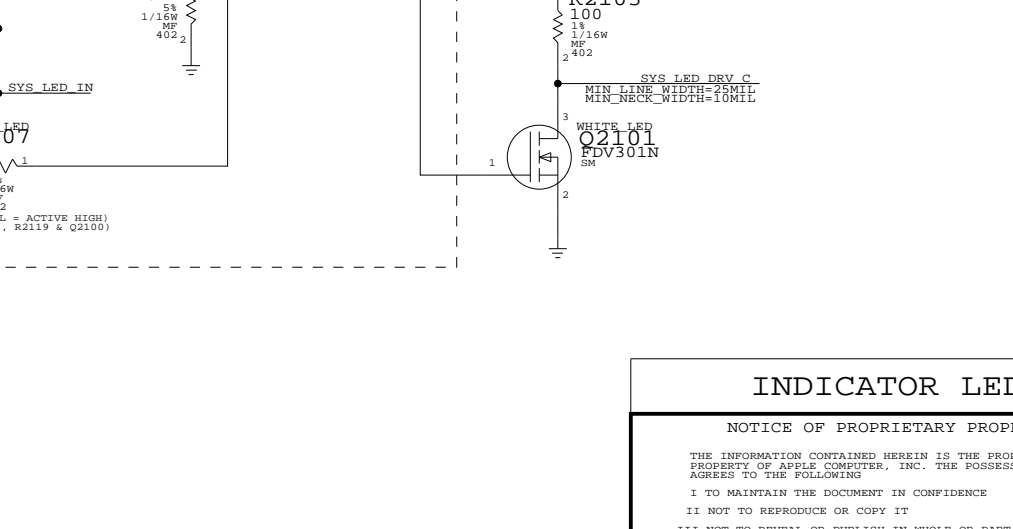
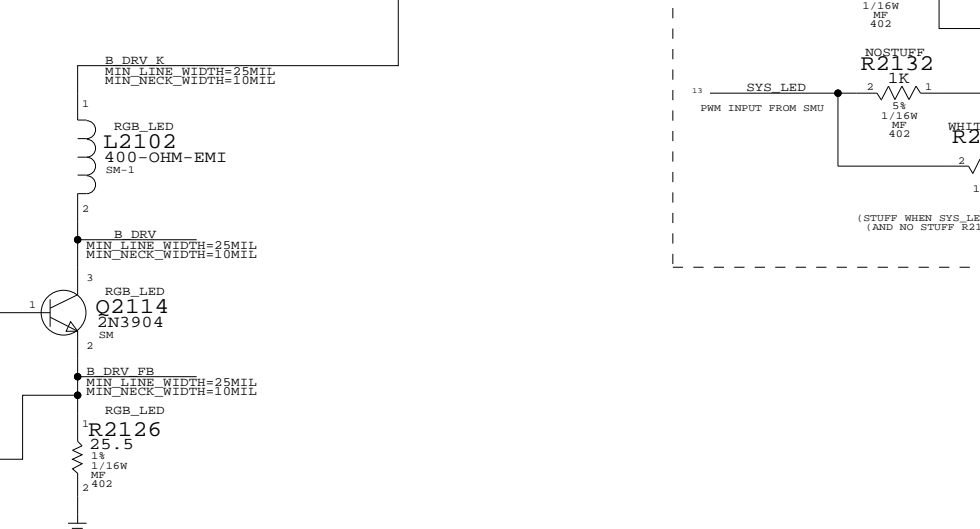
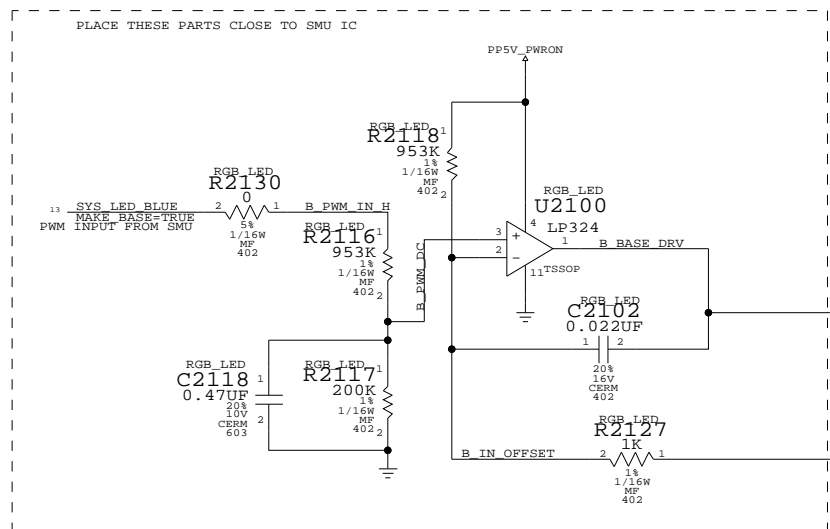
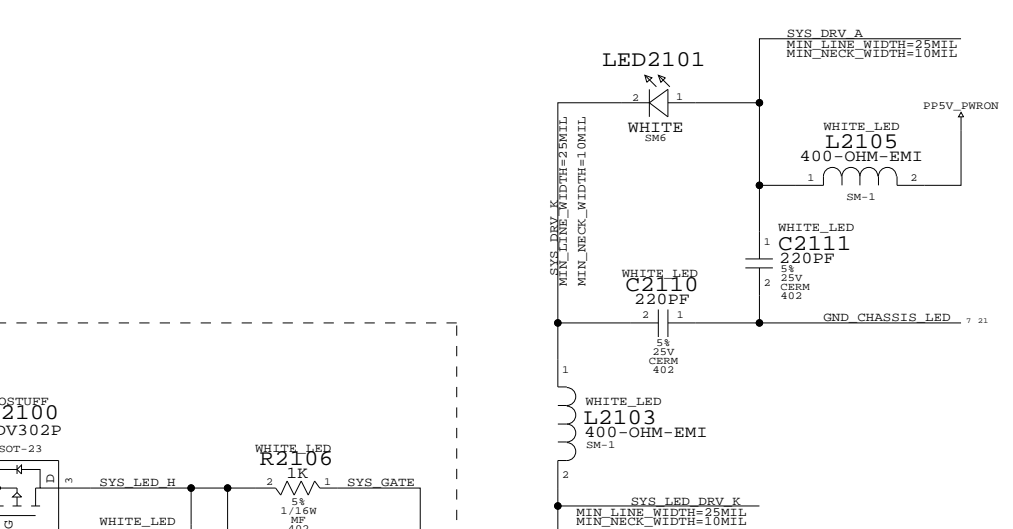
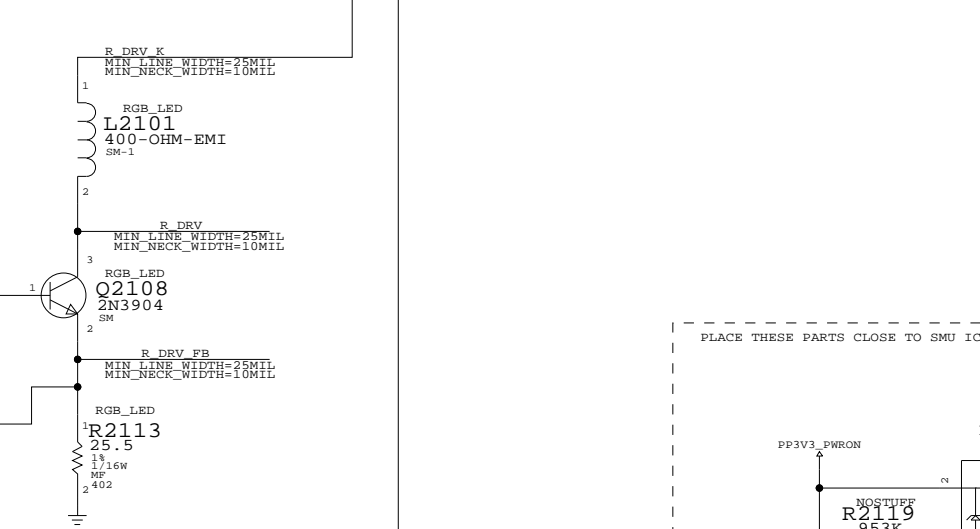
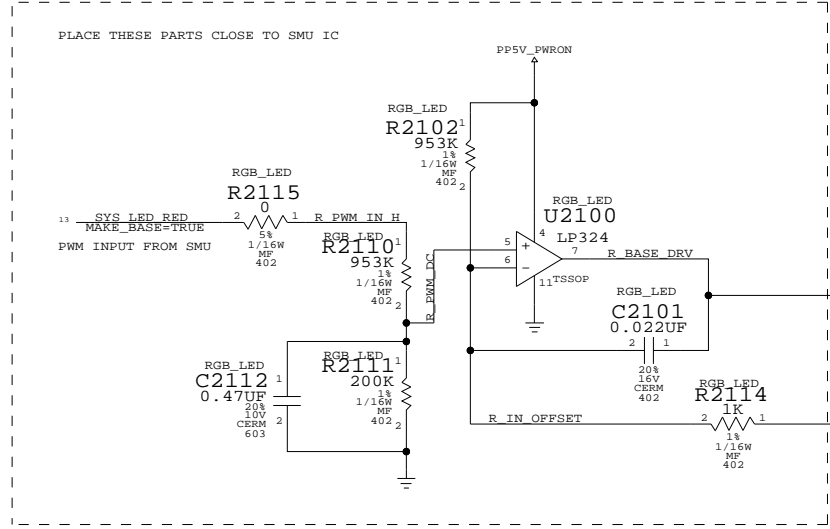
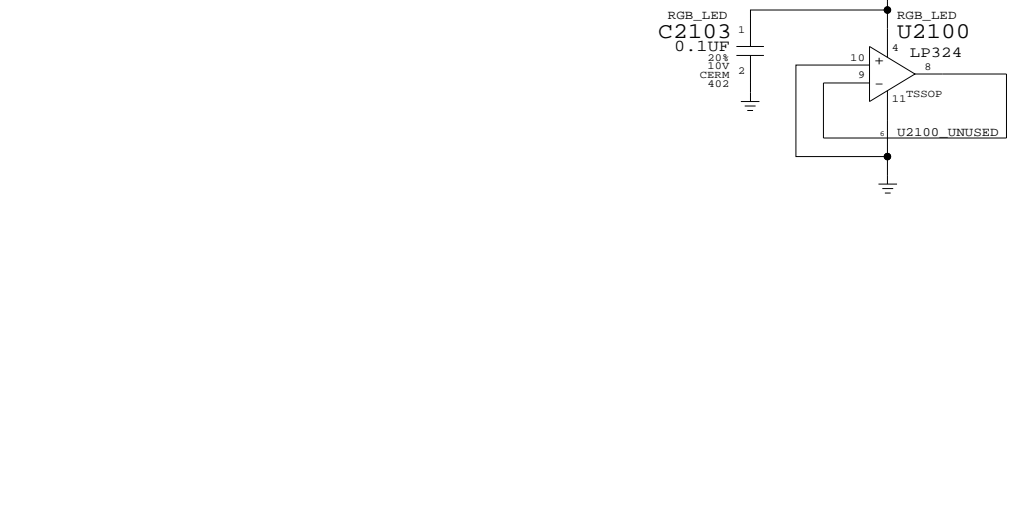
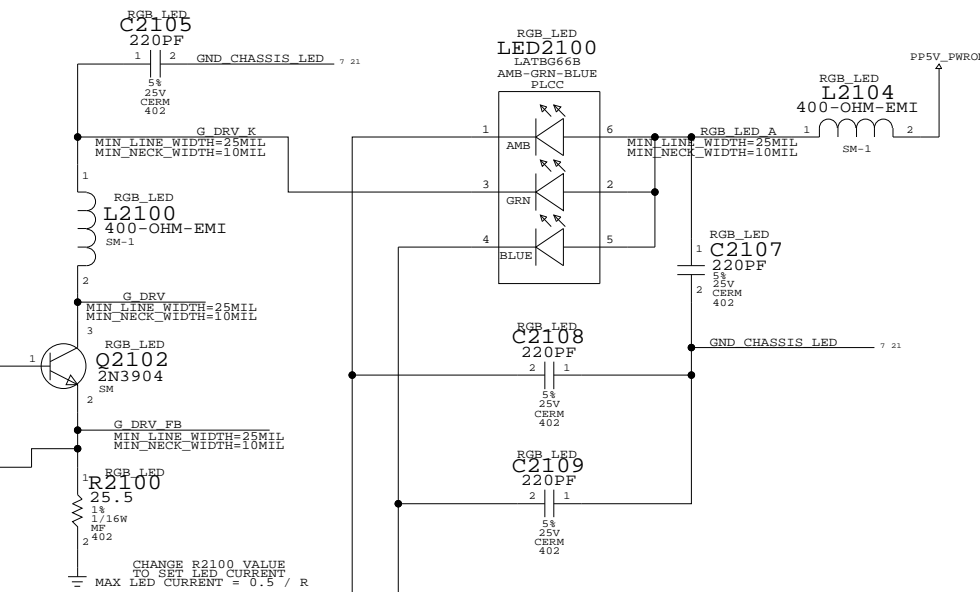
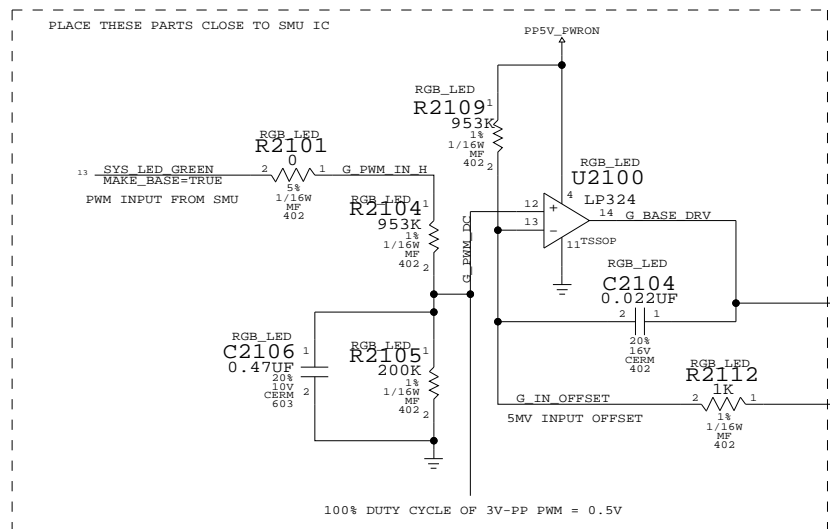
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NONE			

TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS



INDICATOR LED

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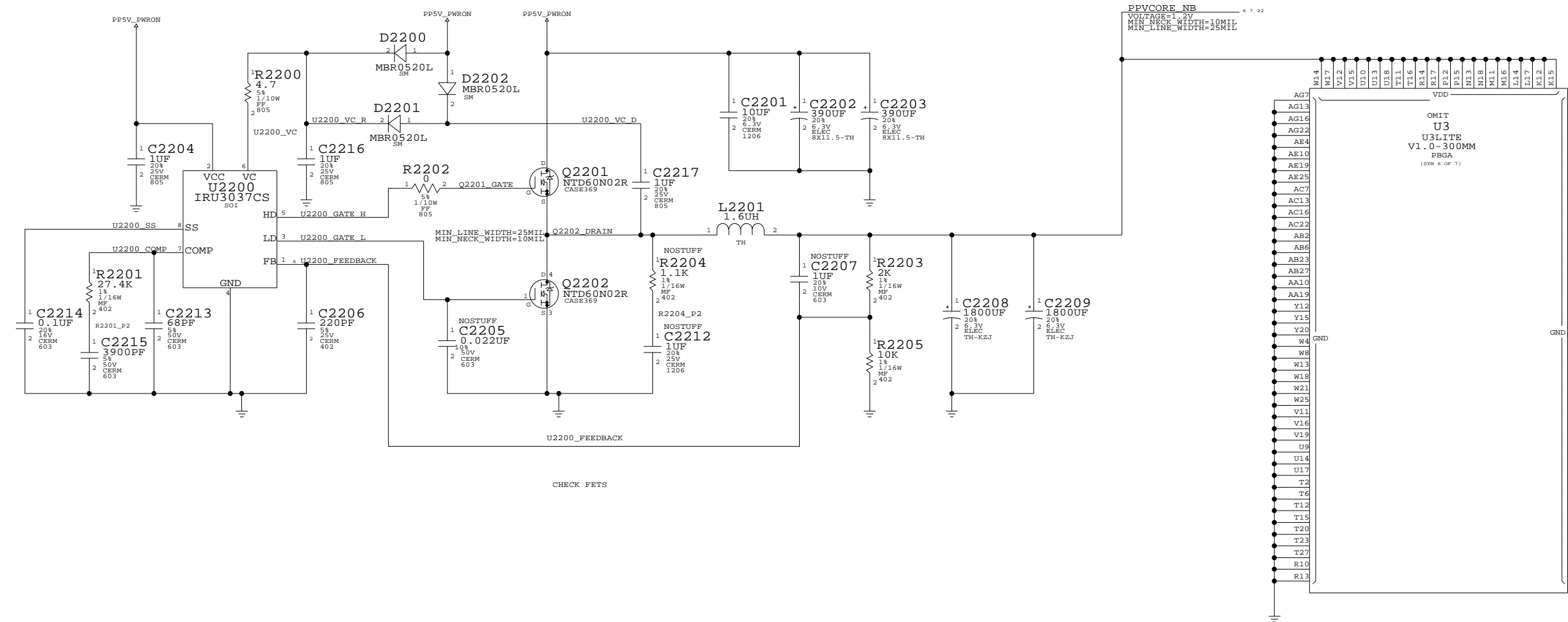
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NONE	21		

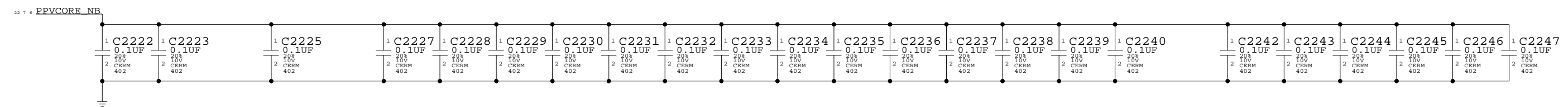
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0284	1	IC,U3LITE,V1.1,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L,V1.1,200MM,PBGA

NOTE:
 SET OUTPUT=1.5VDC FOR U3LITE CORE
 IRU3037CS VREF=1.25VDC
 $V_{OUT} = V_{REF} * (R_{2203} + R_{2205}) / R_{2205} = 1.5VDC$
 7.73A OF PEAK CURRENT DRAW ON PCORE_NB



CHECK FETS



U3LITE CORE POWER

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	D	051-6482	13
SCALE	NONE	SHT	22 OF 99

VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
3.3V	25MIL	10MIL	PPPCI64_PWRON_SB 7 23
3.3V	25MIL	10MIL	PPPCI32_PWRON_SB 7 23
3.3V	25MIL	10MIL	PP3V3_PWRON_SB 7 23 25
2.5V	25MIL	10MIL	PP2V5_PWRON_SB 7 23 25 74 88
1.2V	100	15MIL	PP1V2_PWRON_SB_VCORE 1 6 10 23

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
34380283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

Page Notes

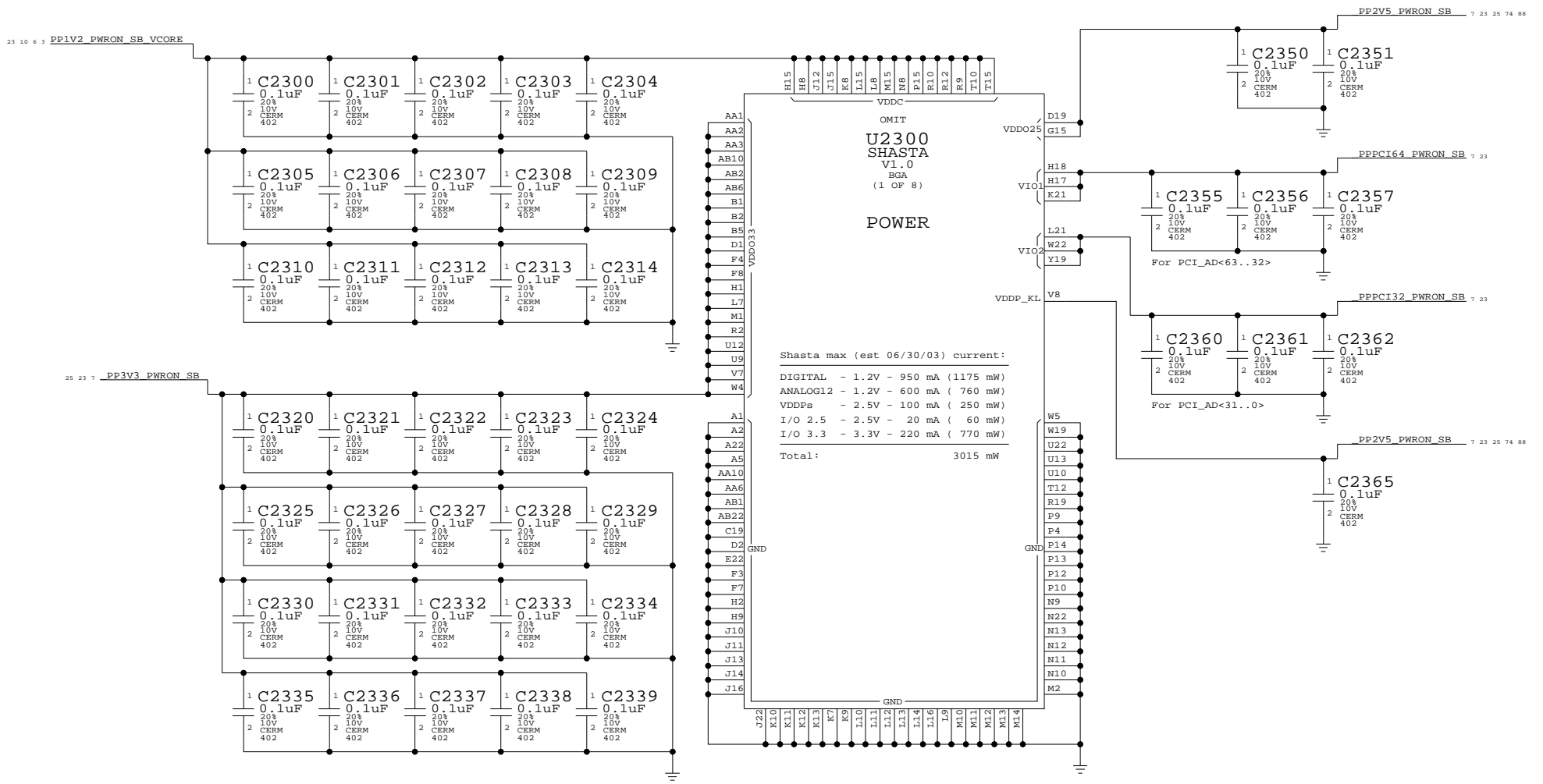
Power aliases required by this page:
 - _PPPCI64_PWRON_SB (to 5V or 3.3V)
 - _PPPCI32_PWRON_SB (to 5V or 3.3V)
 - _PP3V3_PWRON_SB
 - _PP2V5_PWRON_SB

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
 - (NONE)

Power Sequencing:
 Must power Shasta VCore rail before any other Shasta supplies.

neoBorg Implementation
 Master power enable signal (from PMU) connects directly to SBVCORE supply (SBVCORE_RUN). Supply asserts PGOOD (SBVCORE_PGOOD) when ready, which acts as the power enable signal for the rest of the neoBorg components.

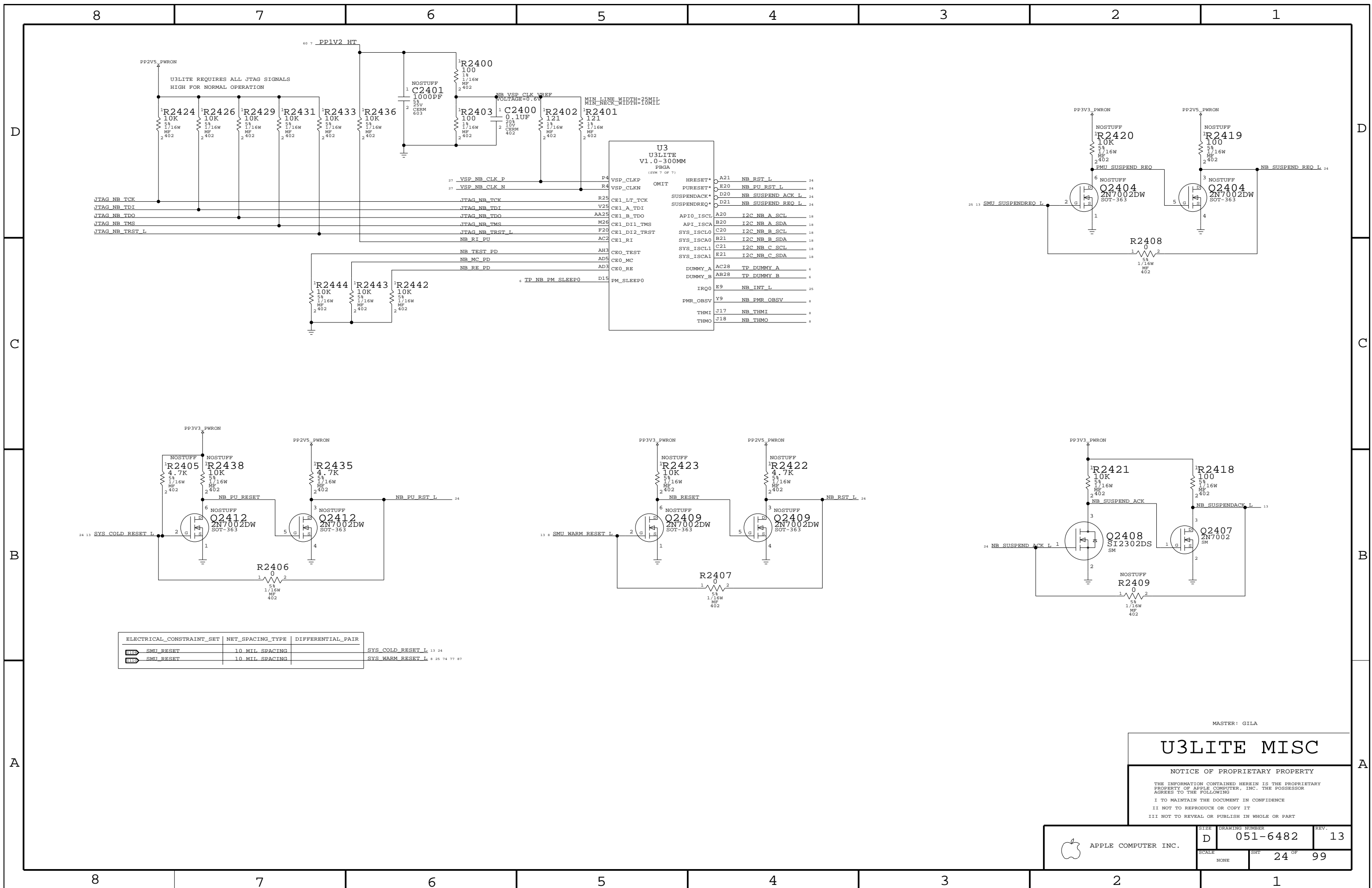


Shasta Core

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_RESET	10 MIL SPACING	SYS_COLD_RESET_L 13 24
SMU_RESET	10 MIL SPACING	SYS_WARM_RESET_L 13 25 74 87

MASTER: GILA

U3LITE MISC

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	D	051-6482	13
SCALE	SHT	24 OF 99	
NONE			

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		I2S0_DEV_TO_SB_DTI
I2S0_TO_DEV		I2S0_SB_TO_DEV_DTO
I2S0_TO_DEV		I2S0_MCLK
I2S0_BIDIR		I2S0_BITCLK
I2S0_BIDIR		I2S0_SYNC
I2S1_TO_SB		I2S1_DEV_TO_SB_DTI
I2S1_TO_DEV		I2S1_SB_TO_DEV_DTO
I2S1_TO_DEV		I2S1_MCLK
I2S1_BIDIR		I2S1_BITCLK
I2S1_BIDIR		I2S1_SYNC
I2S2_TO_SB		I2S2_DEV_TO_SB_DTI
I2S2_TO_DEV		I2S2_SB_TO_DEV_DTO
I2S2_TO_DEV		I2S2_MCLK
I2S2_BIDIR		I2S2_BITCLK
I2S2_BIDIR		I2S2_SYNC
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALI
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALO
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALO_R
SB_CLK25M_ATA	15 MIL SPACING	SB_CLK25M_ATA

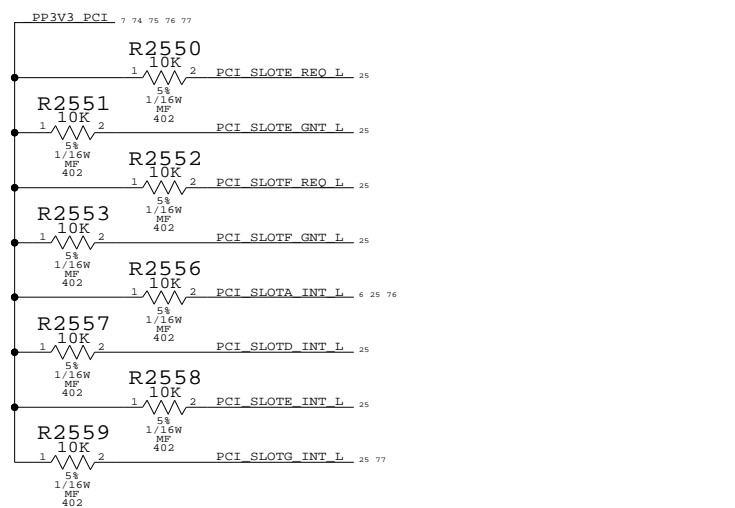
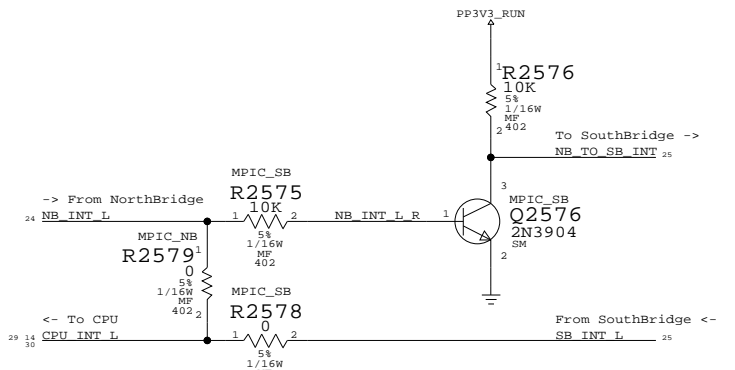
Page Notes

Power aliases required by this page:
 - PP3V3_PCI
 - PP3V3_PWRON_SB
 - PP2V5_PWRON_SB
 - PP1V2_PWRON_SB

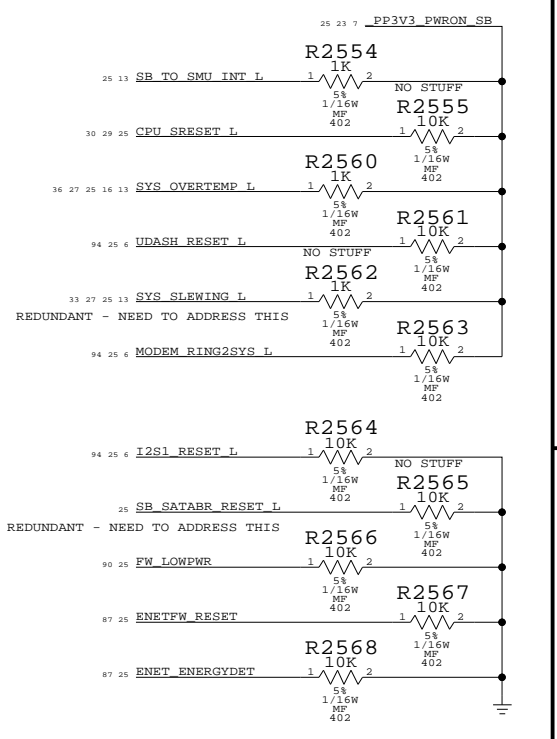
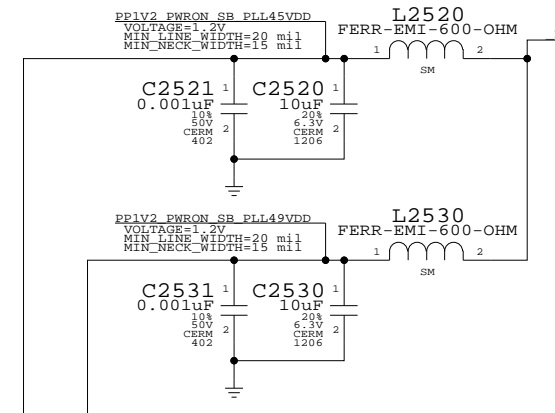
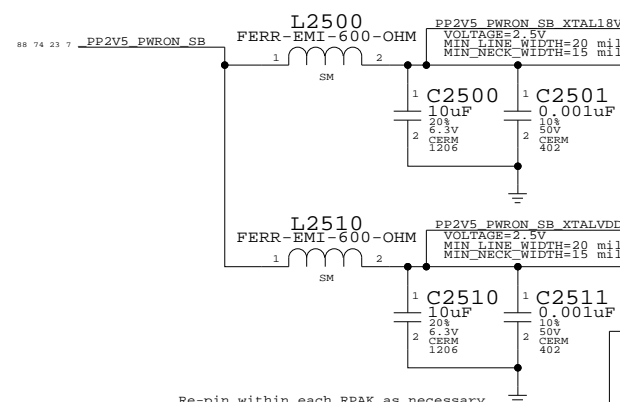
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - PCI_64BIT
 Configures Shasta for 64-bit PCI
 NOTE: XGC required for Shasta GPIOs

NorthBridge / SouthBridge MPIC Routing

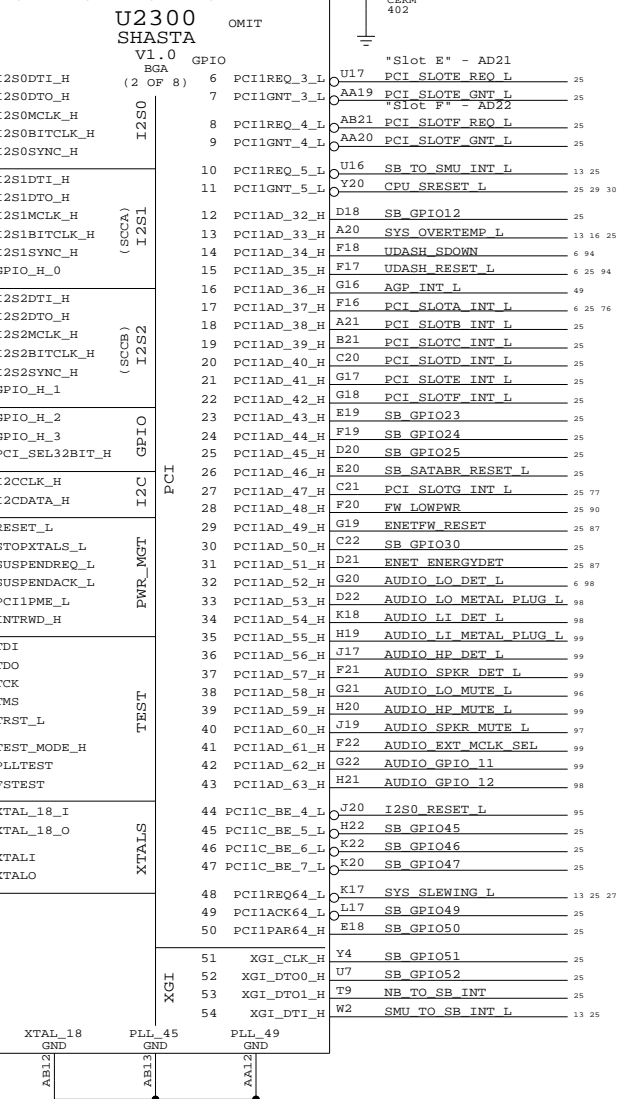


PCI 32-bit select
 1 = 32-bit PCI & GPIOs
 0 = 64-bit PCI & XGC
 (Internal pull-up)



Re-pin within each RPAK as necessary
DO NOT swap between RPAKs

PP2V5_PWRON_SB	PP2V5_PWRON_SB_XTAL18VDD	PP2V5_PWRON_SB_XTAL18VDD	PP2V5_PWRON_SB_XTAL18VDD	PP2V5_PWRON_SB_XTAL18VDD	PP2V5_PWRON_SB_XTAL18VDD
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9
10	10	10	10	10	10
11	11	11	11	11	11
12	12	12	12	12	12
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14	14	14	14	14	14
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50	50	50	50	50	50
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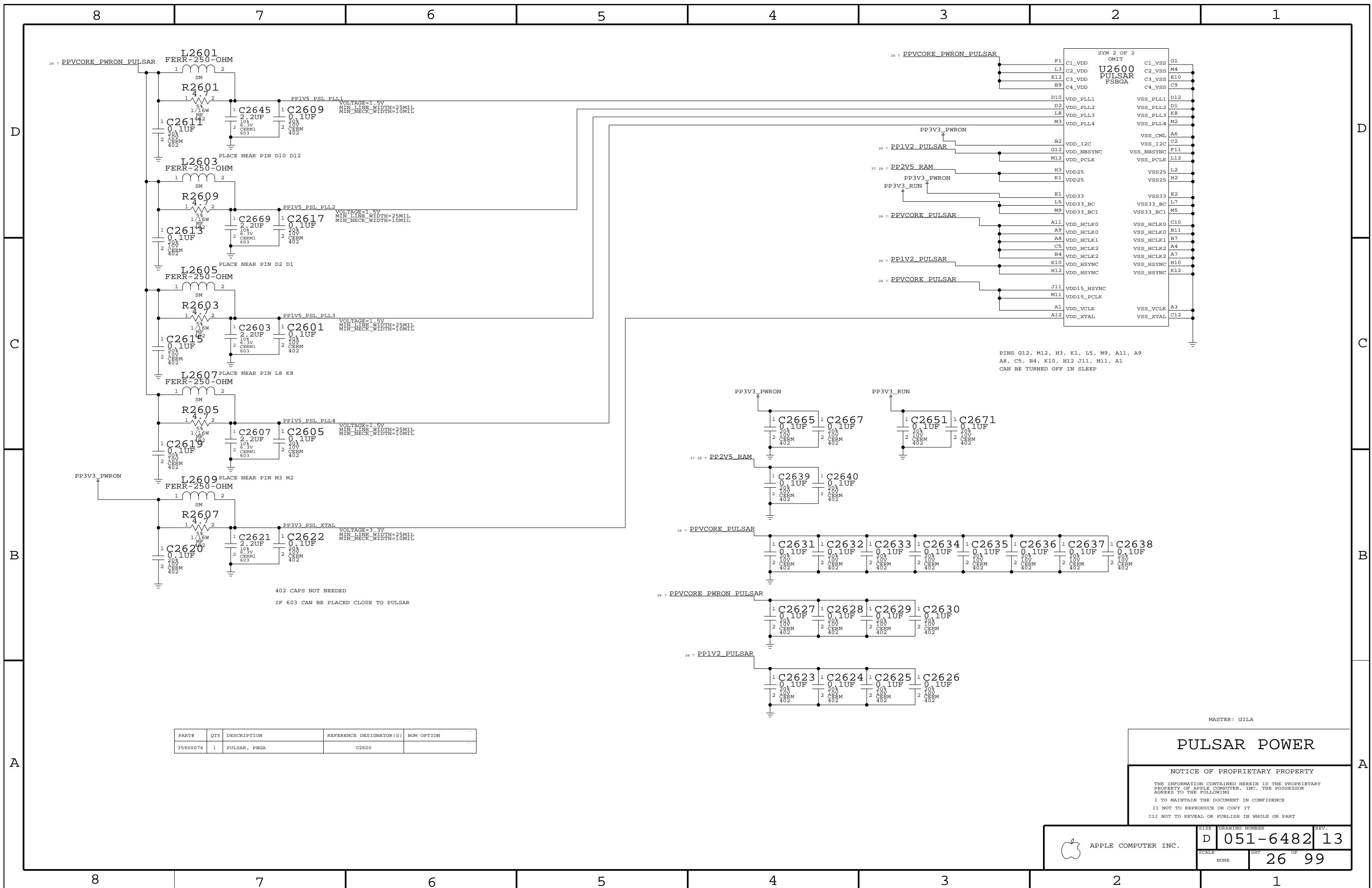


AUDIO GPIOs
 NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

Master: Link

Shasta Serial / Misc

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PINS G12, M12, H3, K1, L5, M9, A11, A9, A8, C5, B4, K10, H12, J11, M11, A1 CAN BE TURNED OFF IN SLEEP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, FBGA	U2600	

402 CAPS NOT NEEDED
IF 603 CAN BE PLACED CLOSE TO PULSAR

MASTER: GILA

PULSAR POWER

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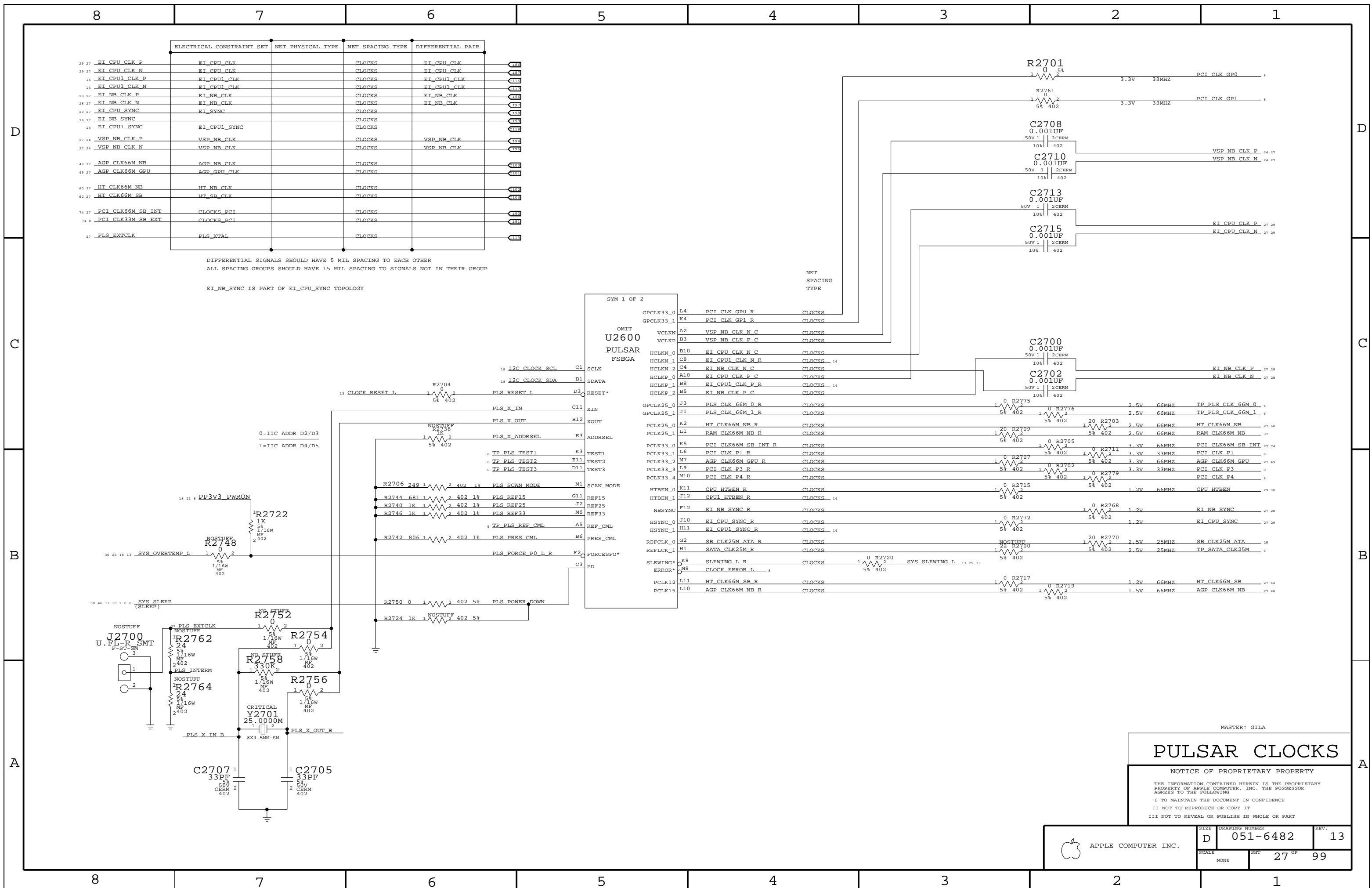
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SCALE		SHEET	
NONE		26 OF 99	



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
29 27	EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
29 27	EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
14	EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
14	EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
28 27	EI_NB_CLK_P	EI_NB_CLK	CLOCKS	EI_NB_CLK
28 27	EI_NB_CLK_N	EI_NB_CLK	CLOCKS	EI_NB_CLK
29 27	EI_CPU_SYNC	EI_SYNC	CLOCKS	
28 27	EI_NB_SYNC		CLOCKS	
14	EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS	
27 24	VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
27 24	VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
48 27	AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS	
49 27	AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS	
60 27	HT_CLK66M_NB	HT_NB_CLK	CLOCKS	
62 27	HT_CLK66M_SB	HT_SB_CLK	CLOCKS	
74 27	PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS	
74 8	PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS	
27	PLS_EXTCLK	PLS_XTAL	CLOCKS	

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
 ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

SYM 1 OF 2

OMIT
U2600
 PULSAR
 FSBGA

GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS
GPCLK25_0	J3	PLS_CLK_66M_0_R	CLOCKS
GPCLK25_1	J1	PLS_CLK_66M_1_R	CLOCKS
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS
REFLCK_1	H1	SATA_CLK25M_R	CLOCKS
SLEWING+ ERROR+	K9 M8	SLEWING_L_R CLOCK_ERROR_L	CLOCKS
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS

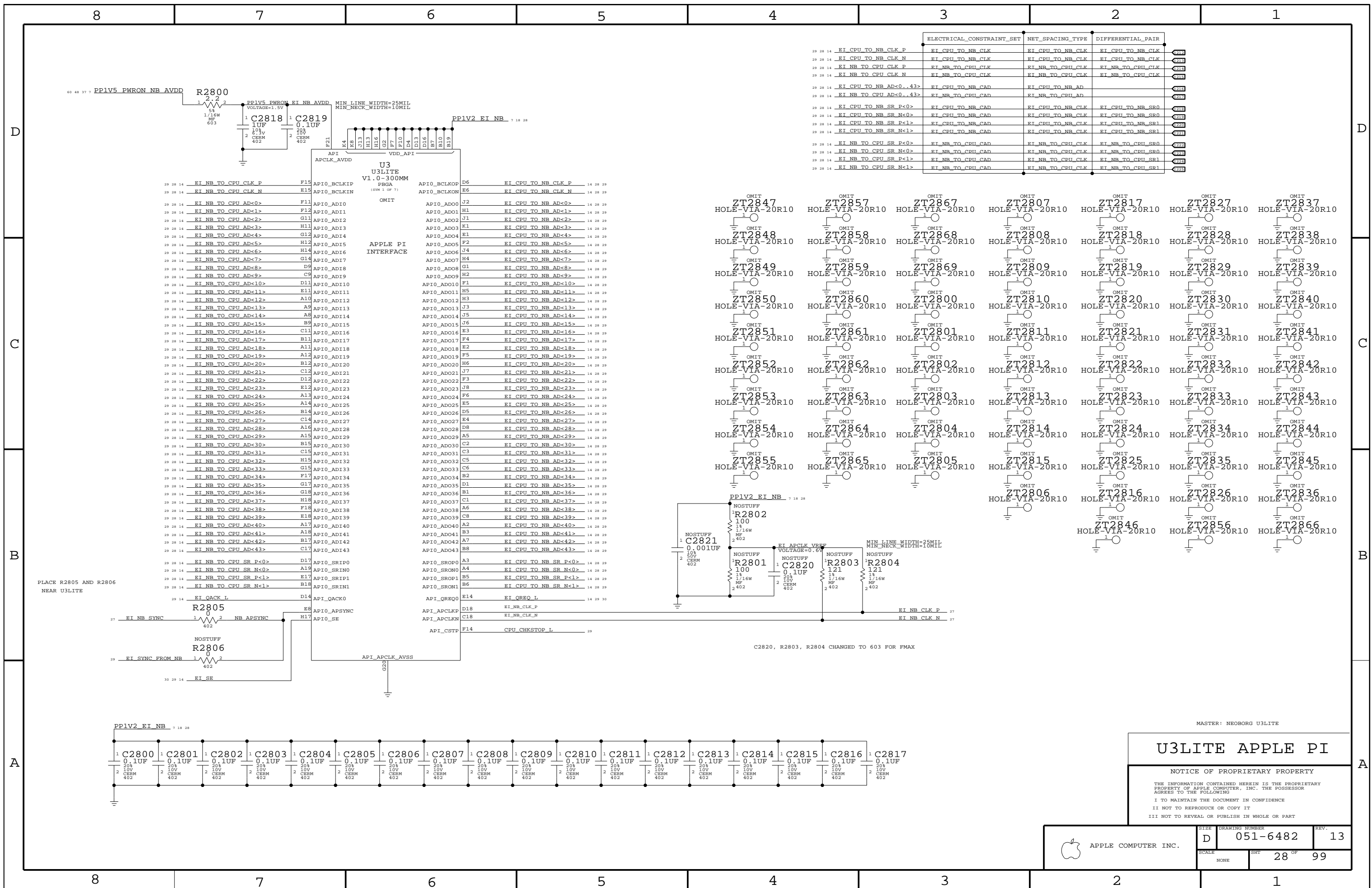
MASTER: GILA

PULSAR CLOCKS

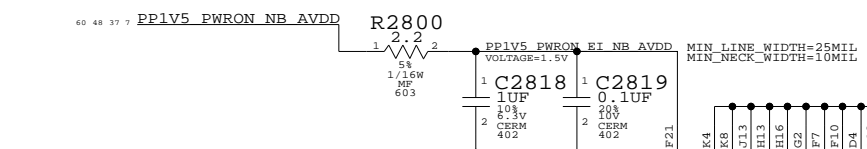
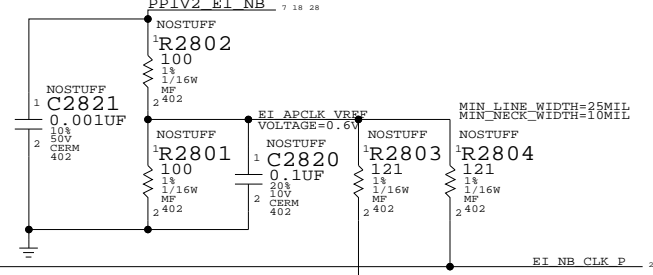
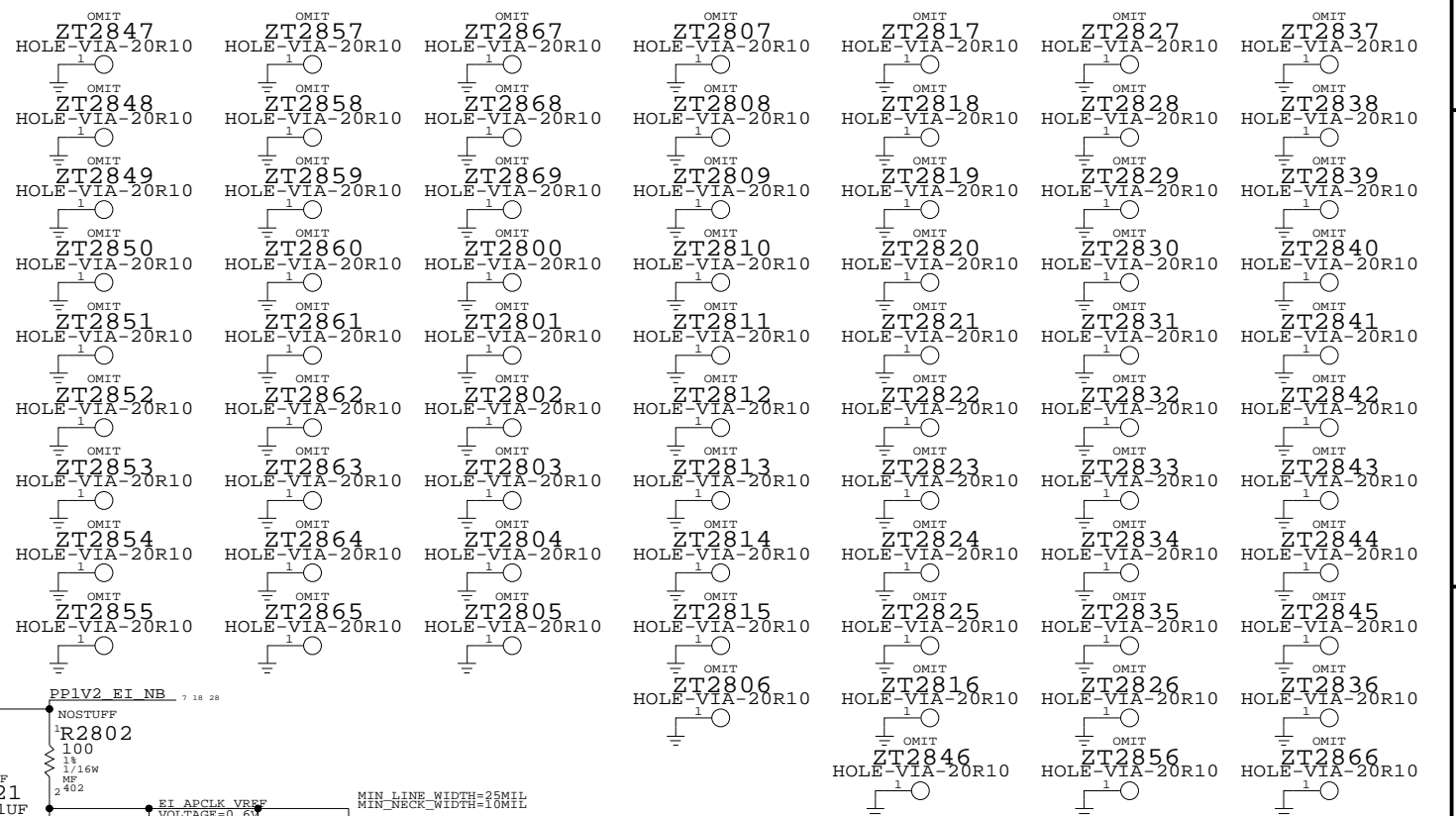
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	D	051-6482	13
SCALE	SHT	27 OF 99	
NONE			



	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
29 28 14	EI CPU TO NB CLK P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	Q290
29 28 14	EI CPU TO NB CLK N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	Q291
29 28 14	EI NB TO CPU CLK P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	Q292
29 28 14	EI NB TO CPU CLK N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	Q293
29 28 14	EI CPU TO NB AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD	Q294
29 28 14	EI NB TO CPU AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD	Q295
29 28 14	EI CPU TO NB SR P<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	Q296
29 28 14	EI CPU TO NB SR N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	Q297
29 28 14	EI CPU TO NB SR P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	Q298
29 28 14	EI CPU TO NB SR N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	Q299
29 28 14	EI NB TO CPU SR P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	Q300
29 28 14	EI NB TO CPU SR N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	Q301
29 28 14	EI NB TO CPU SR P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	Q302
29 28 14	EI NB TO CPU SR N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	Q303



PLACE R2805 AND R2806 NEAR U3LITE

C2820, R2803, R2804 CHANGED TO 603 FOR FMAX

MASTER: NEOBORG U3LITE

U3LITE APPLE PI

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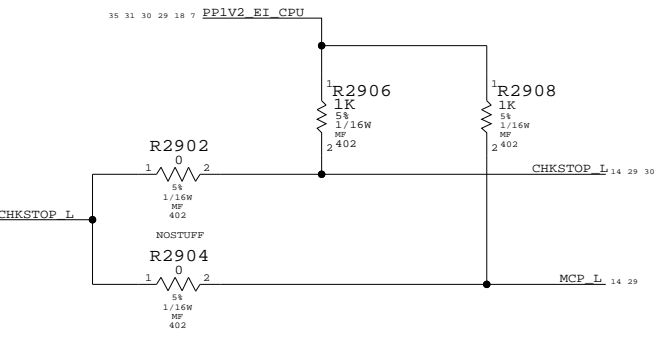
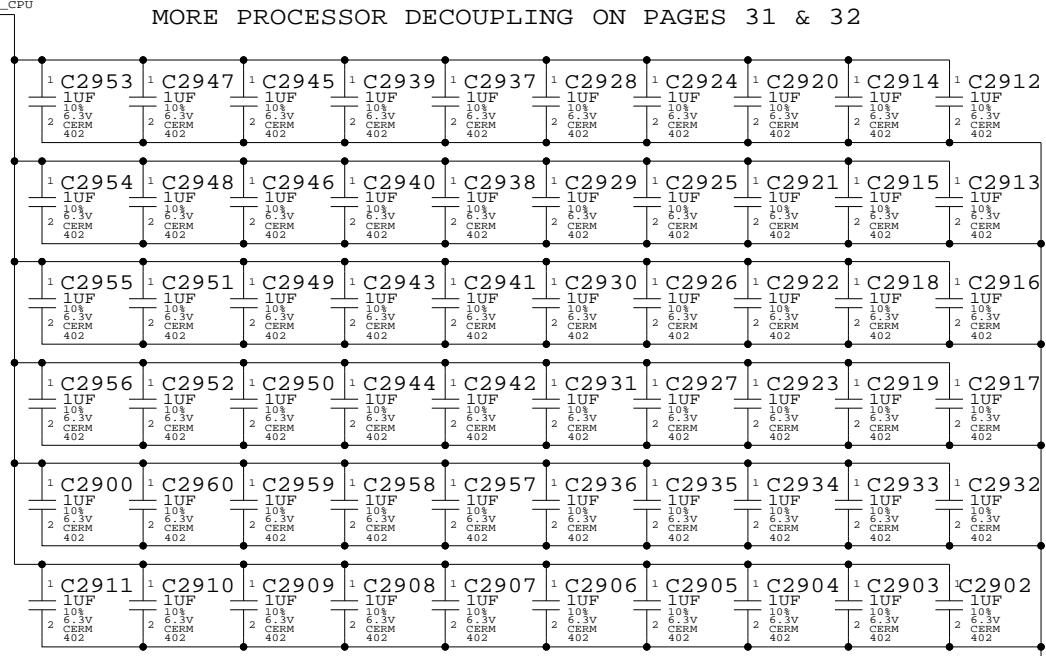
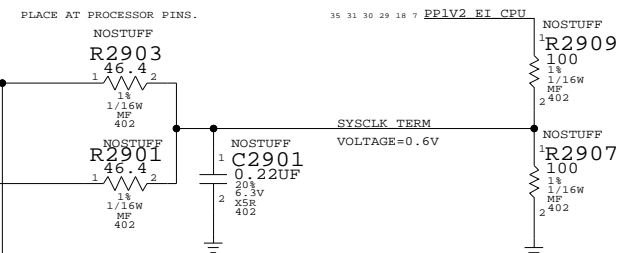
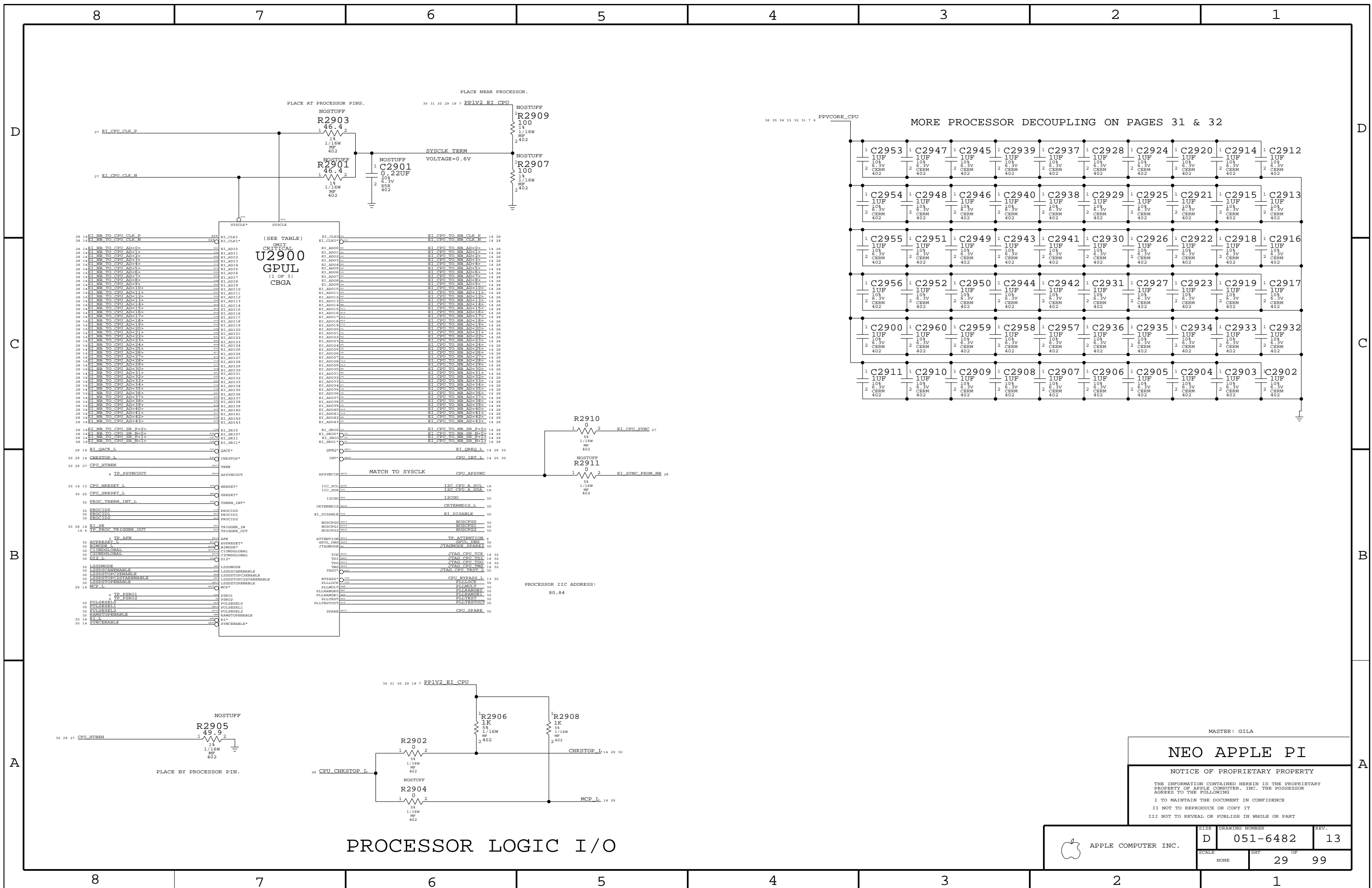
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SCALE	SHEET	28 OF 99	
NONE			



MASTER: GILA

NEO APPLE PI

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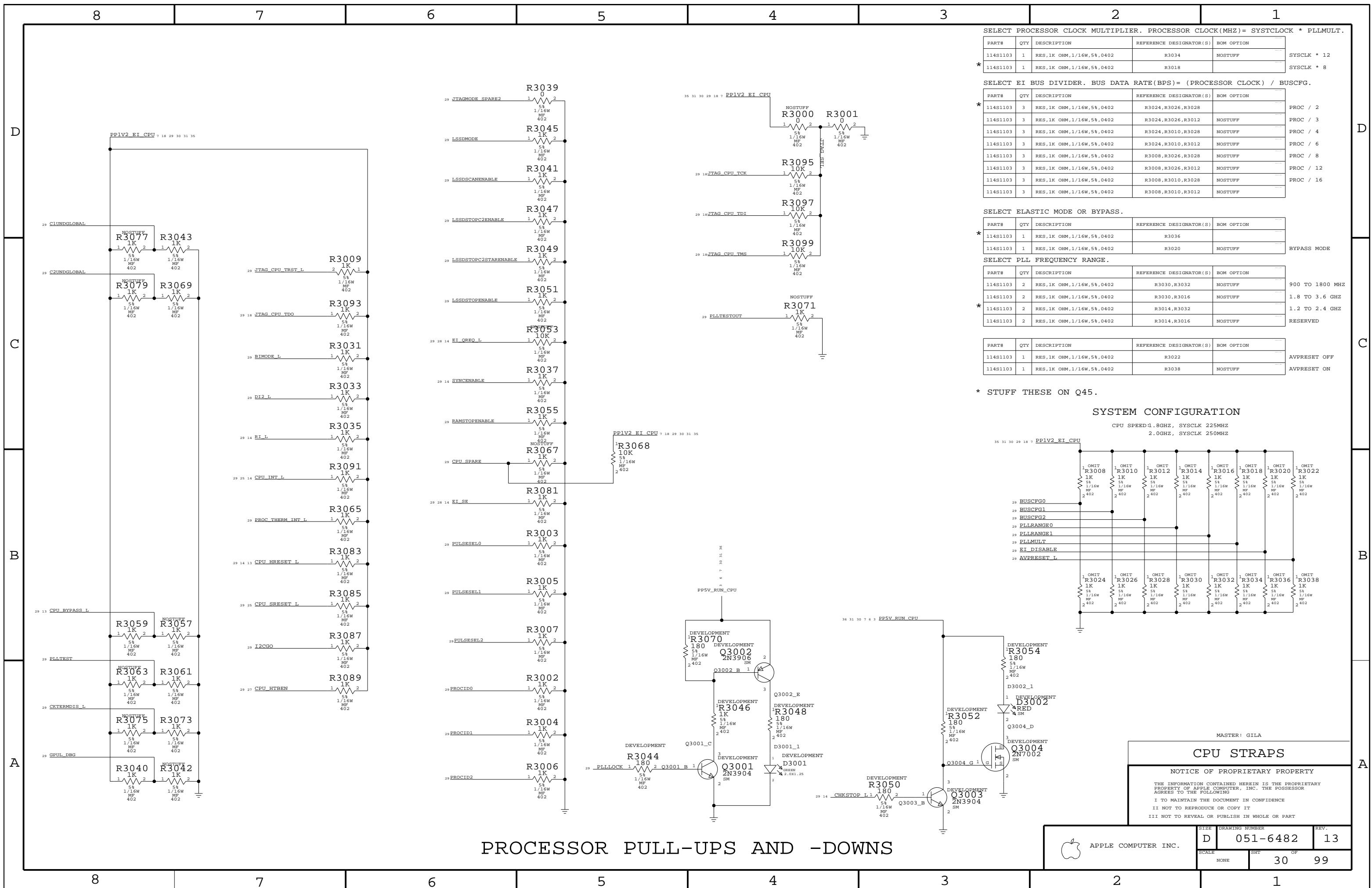
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SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE	SHT	OF
NONE	29	99

PROCESSOR LOGIC I/O

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	13
SCALE	SHT	OF
NONE	29	99



SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	NOSTUFF	SYSCLK * 12
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	NOSTUFF	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	NOSTUFF	PROC / 2
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	NOSTUFF	PROC / 3
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	PROC / 12
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16

SELECT ELASTIC MODE OR BYPASS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036	NOSTUFF	BYPASS MODE
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

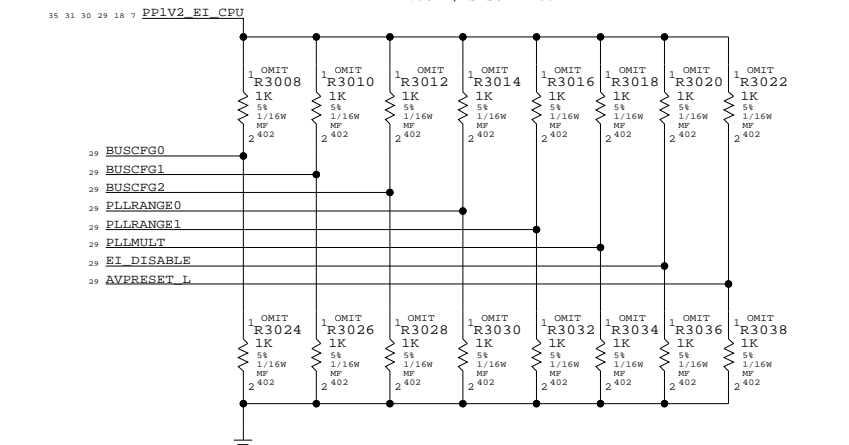
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	NOSTUFF	900 TO 1800 MHZ
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	NOSTUFF	1.8 TO 3.6 GHZ
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	NOSTUFF	1.2 TO 2.4 GHZ
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022	NOSTUFF	AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION

CPU SPEED 1.8GHZ, SYSCLK 225MHZ
2.0GHZ, SYSCLK 250MHZ



MASTER: GILA

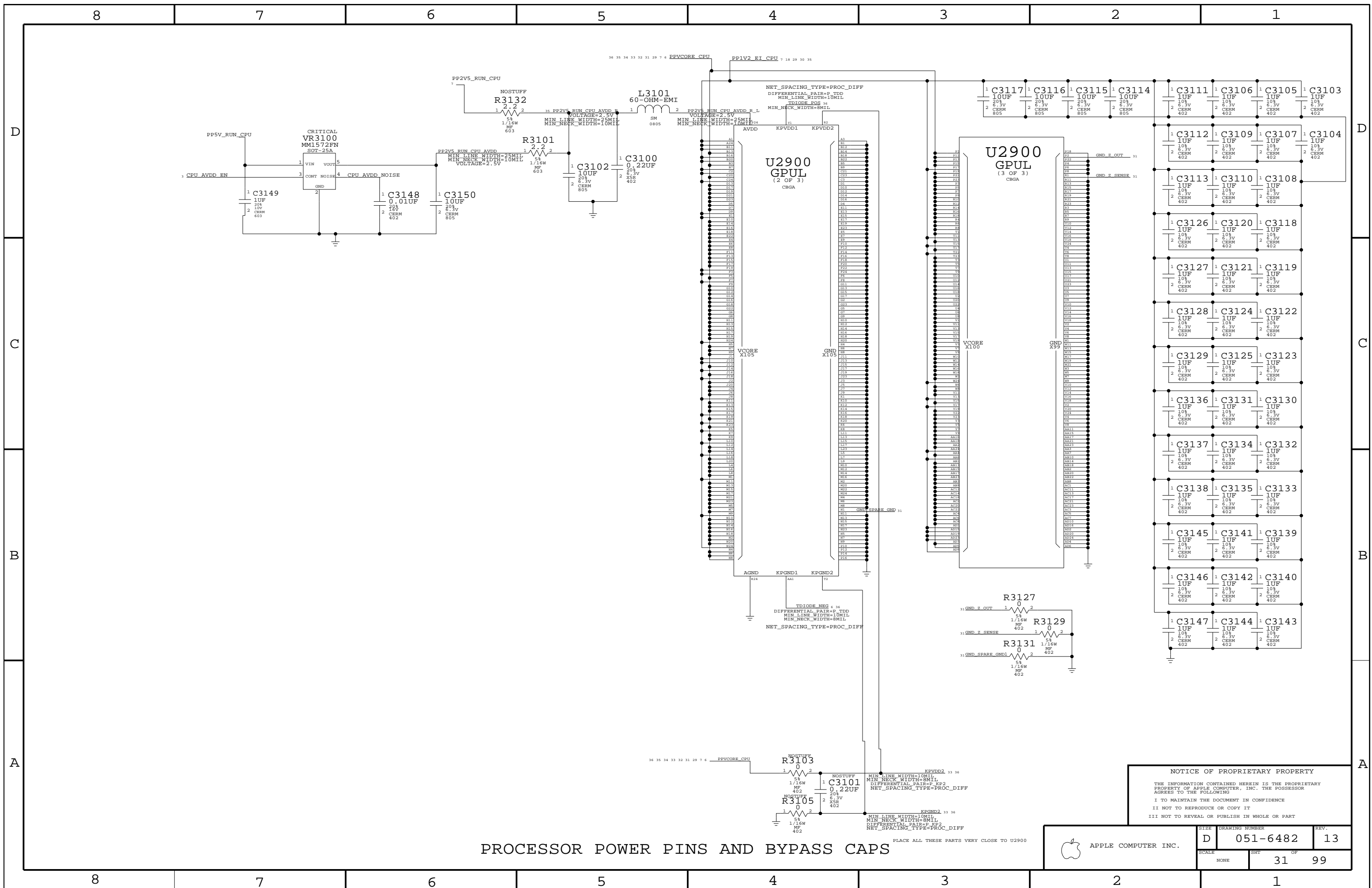
CPU STRAPS

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SCALE	NONE	SHT	OF
		30	99

PROCESSOR PULL-UPS AND -DOWNS



PROCESSOR POWER PINS AND BYPASS CAPS

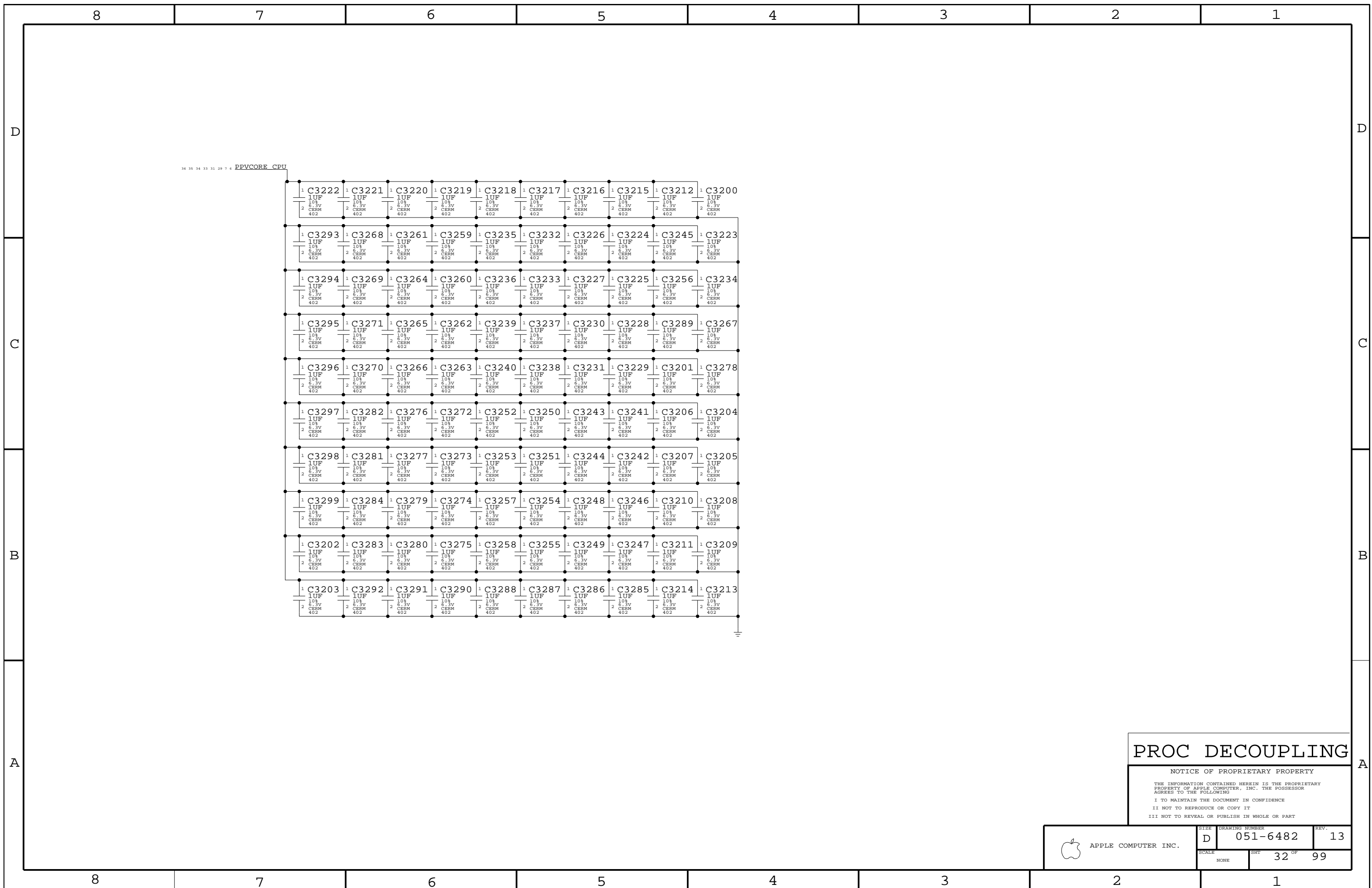
PLACE ALL THESE PARTS VERY CLOSE TO U2900

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DRAWING NUMBER	051-6482	REV.	13
	SCALE	NONE	SHT
OF		31	
OF		99	



APPLE COMPUTER INC.



PROC DECOUPLING


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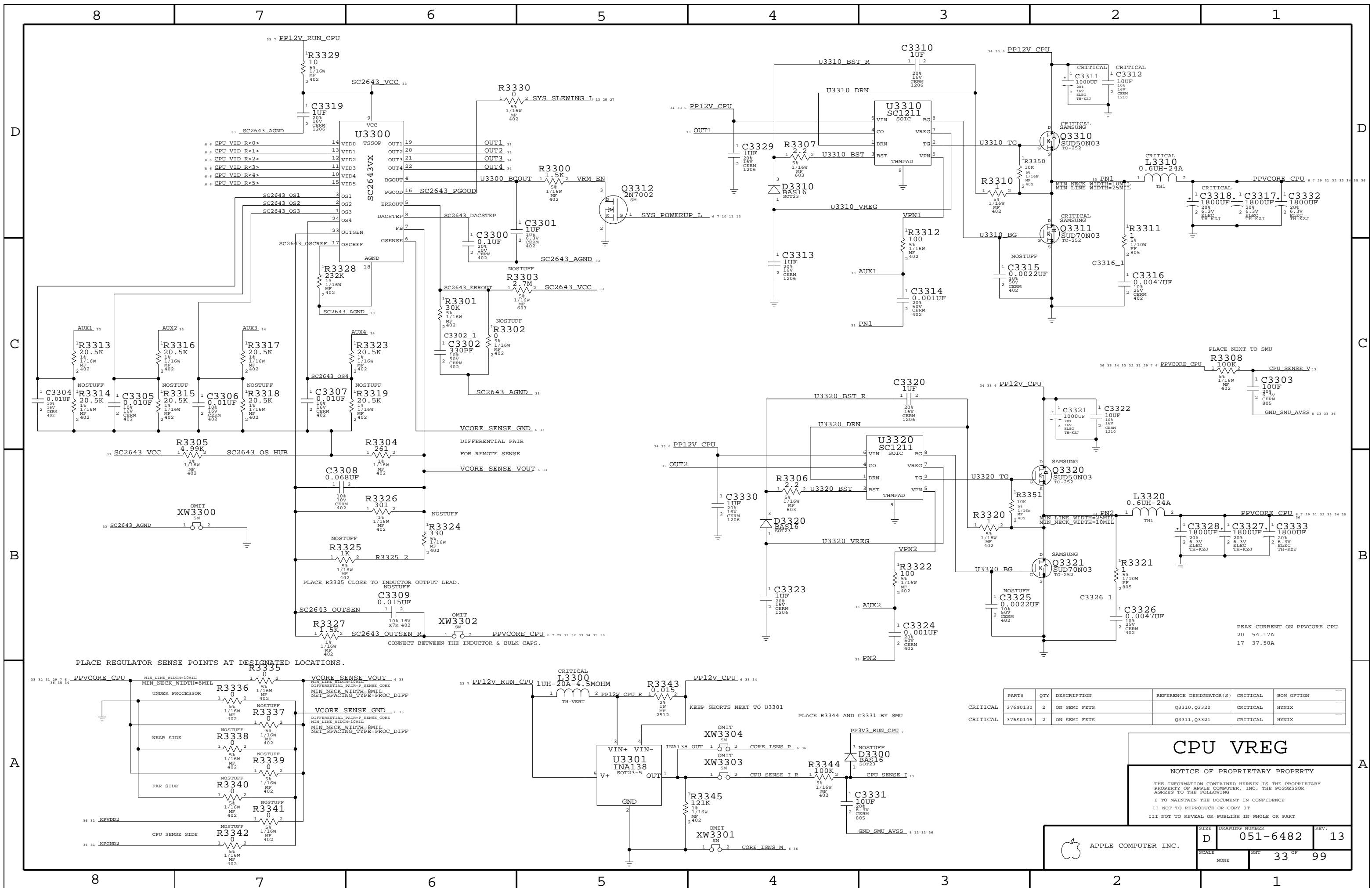
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	D	051-6482	13
SCALE	SHT	OF	
NONE	32	99	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
37680130	2	ON SEMI FETS	Q3310, Q3320	CRITICAL	HYNIX
37680146	2	ON SEMI FETS	Q3311, Q3321	CRITICAL	HYNIX

CPU VREG

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	D	051-6482	13
SCALE	NONE	SHT	33 OF 99

PEAK CURRENT ON PPVCORE_CPU
 20 54.17A
 17 37.50A

PLACE REGULATOR SENSE POINTS AT DESIGNATED LOCATIONS.

PLACE R3325 CLOSE TO INDUCTOR OUTPUT LEAD.

CONNECT BETWEEN THE INDUCTOR & BULK CAPS.

KEEP SHORTS NEXT TO U3301

PLACE R3344 AND C3331 BY SMU

MIN LINE WIDTH=10MIL
 MIN_NECK_WIDTH=5MIL
 NET_SPACING_TYPE=PROC_DIFF

MIN LINE WIDTH=10MIL
 MIN_NECK_WIDTH=5MIL
 NET_SPACING_TYPE=PROC_DIFF

MIN LINE WIDTH=10MIL
 MIN_NECK_WIDTH=5MIL
 NET_SPACING_TYPE=PROC_DIFF

MIN LINE WIDTH=10MIL
 MIN_NECK_WIDTH=5MIL
 NET_SPACING_TYPE=PROC_DIFF

MIN LINE WIDTH=10MIL
 MIN_NECK_WIDTH=5MIL
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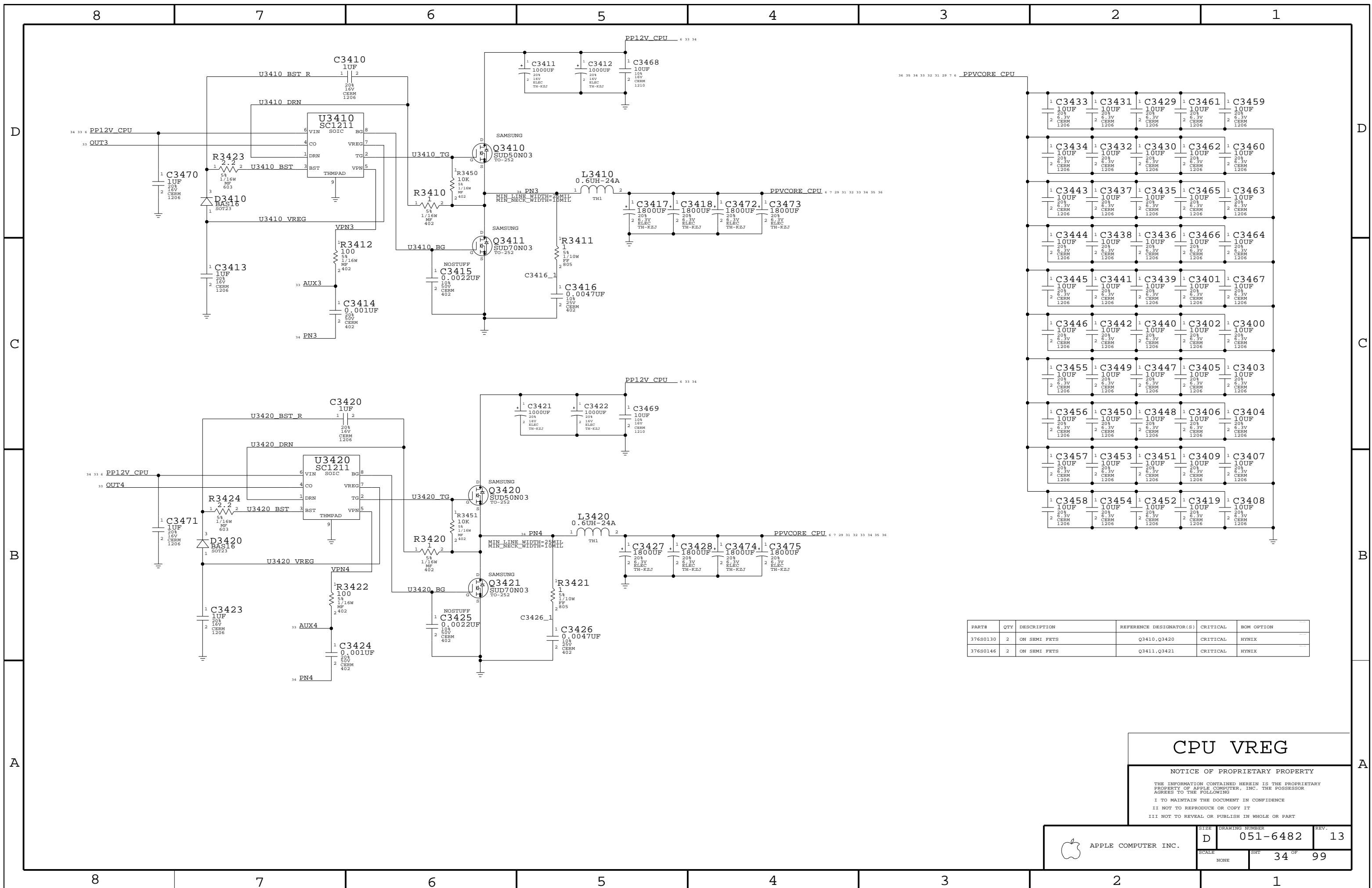
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MIN LINE WIDTH=10MIL
 MIN_NECK_WIDTH=5MIL
 NET_SPACING_TYPE=PROC_DIFF

MIN LINE WIDTH=10MIL
 MIN_NECK_WIDTH=5MIL
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 MIN_NECK_WIDTH=5MIL
 NET_SPACING_TYPE=PROC_DIFF



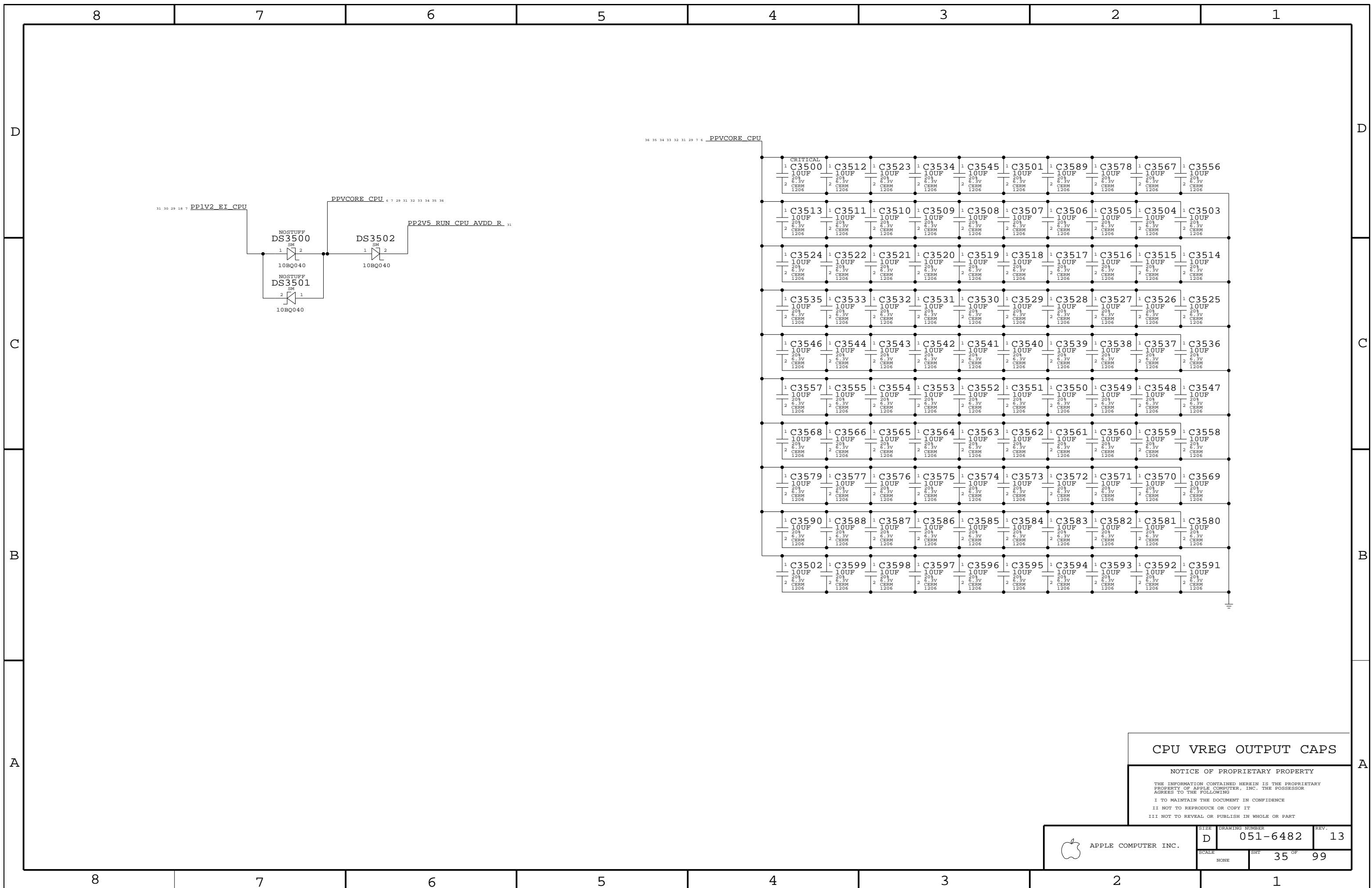
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0130	2	ON SEMI FETS	Q3410, Q3420	CRITICAL	HYNIX
376S0146	2	ON SEMI FETS	Q3411, Q3421	CRITICAL	HYNIX

CPU VREG

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	SCALE NONE	SHEET 34 OF 99	



CPU VREG OUTPUT CAPS

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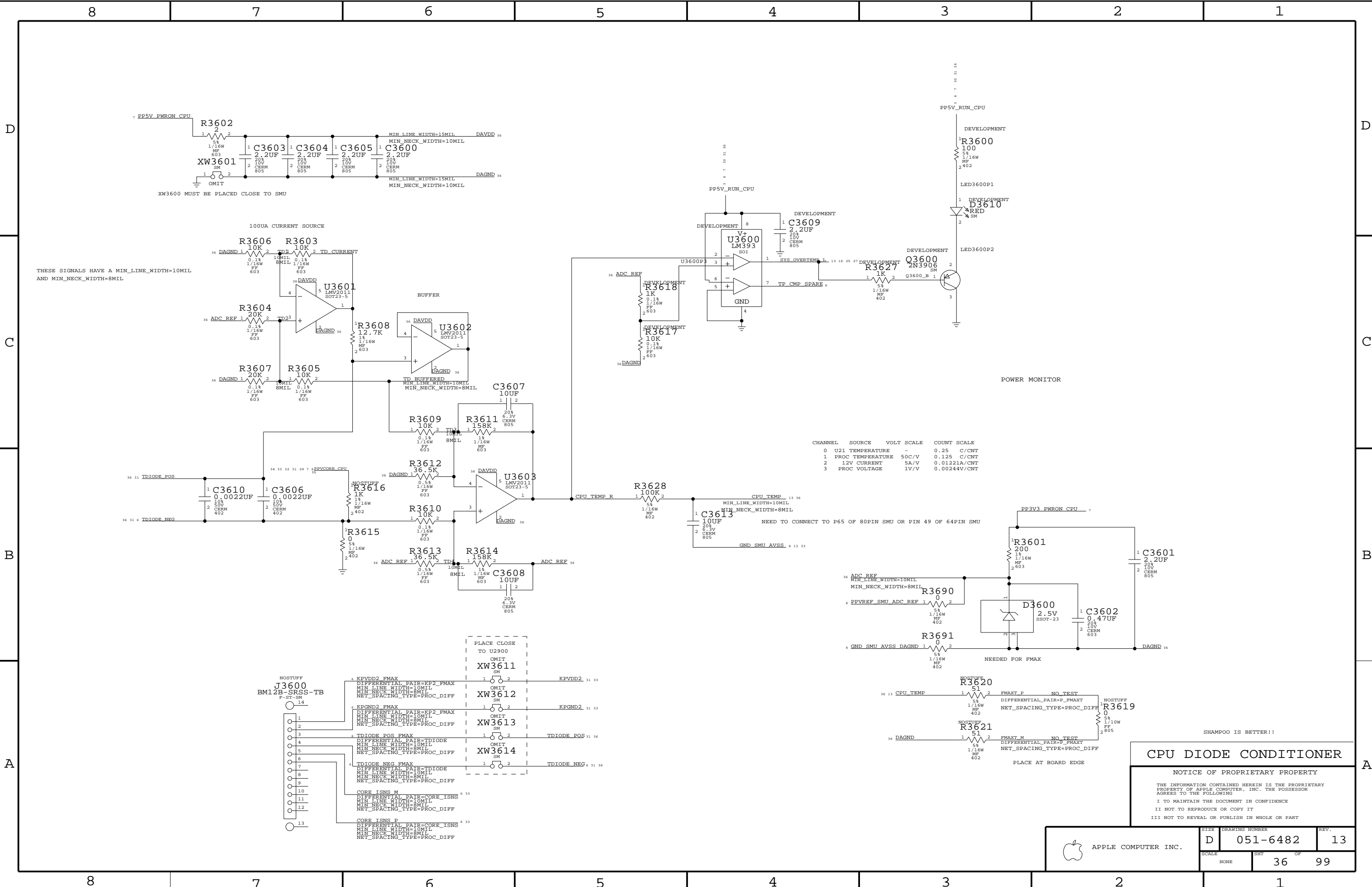
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	SCALE NONE	SHEET 35 OF 99	



THESE SIGNALS HAVE A MIN_LINE_WIDTH=10MIL AND MIN_NECK_WIDTH=8MIL

CHANNEL	SOURCE	VOLT SCALE	COUNT SCALE
0	U21 TEMPERATURE	-	0.25 C/CNT
1	PROC TEMPERATURE	50C/V	0.125 C/CNT
2	12V CURRENT	5A/V	0.01221A/CNT
3	PROC VOLTAGE	1V/V	0.00244V/CNT

CPU DIODE CONDITIONER

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SCALE	NONE	SHT	OF
		36	99

8

7

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3

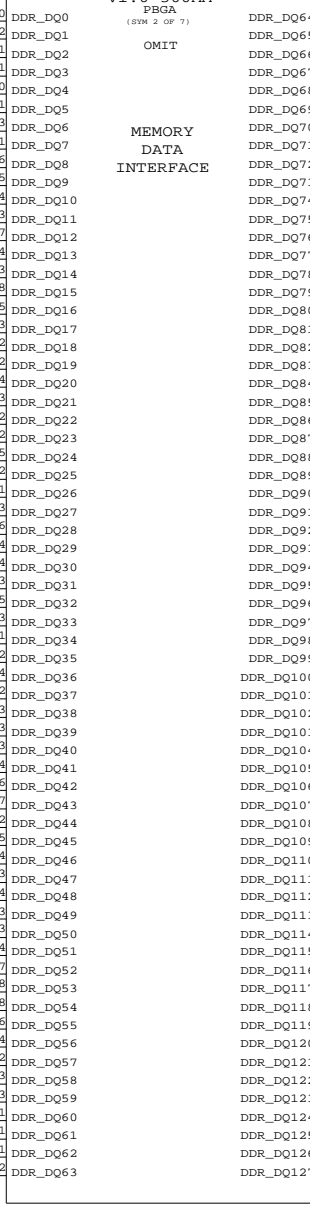
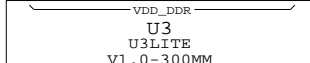
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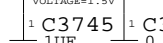
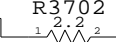
U3LITE'S MAIN MEMORY INTERFACE CAN BE TURNED OFF IN SLEEP

U3TWIN DO NOT HAVE MASKS

PP2V5_RAM

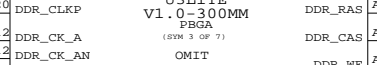
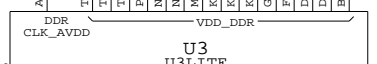
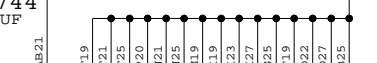


PP1V5_PWRON NB AVDD



MIN LINE WIDTH=25MIL MIN NECK WIDTH=10MIL

PP2V5_RAM



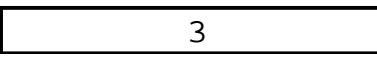
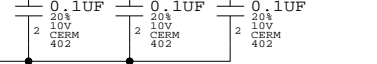
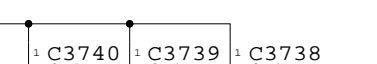
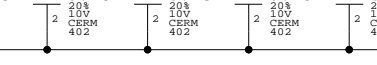
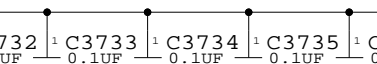
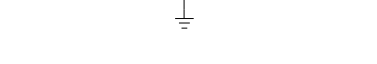
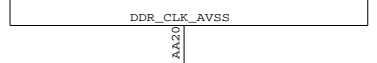
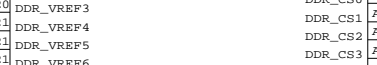
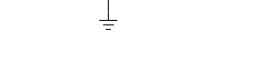
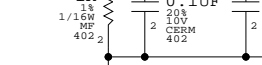
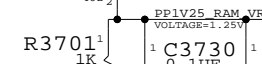
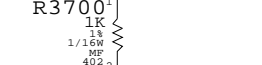
CLK<A..C> GO TO J4000

CLK<D..F> GO TO J4001

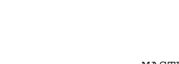
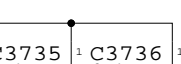
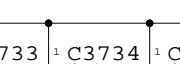
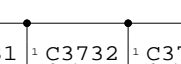
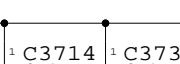
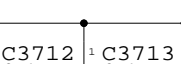
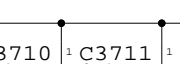
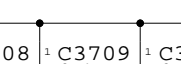
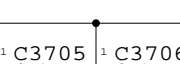
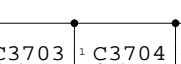
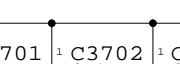
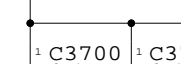
CKE<1..0> GO TO J4000

CKE<5..4> GO TO J4001

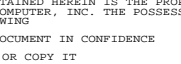
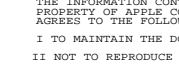
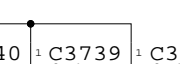
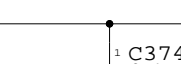
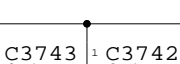
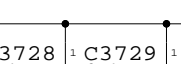
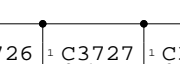
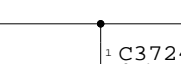
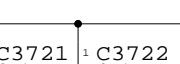
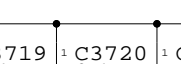
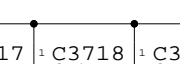
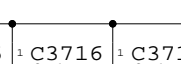
PP2V5_RAM



PP2V5_RAM



PP2V5_RAM



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MASTER: NEOBORG U3LITE

U3LITE MEMORY

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	NONE	D 051-6482	13
		SHEET	37 OF 99

ALL R PACKS ARE 15 OHM 1/16W 5%

ELECTRICAL_CONSTRAINT_SET NET_PHYSICAL_TYPE NET_SPACING_TYPE DIFFERENTIAL_PAIR

Table of component values for RAM DO R<2> through RAM DO R<62>, including part numbers like RP3836 and values like 15, 8, 7, 6, 5.

Table of component values for RAM DO R<68> through RAM DO R<127>, including part numbers like RP3818 and values like 15, 7, 6, 5, 4, 3, 2.

Table of component values for RAM CLK A P R through RAM WE L, including part numbers like RP3818 and values like 15, 7, 6, 5, 4, 3, 2, 1.

Table titled 'THE FOLLOWING IS A SWAPPABLE GROUP' for RAM_CKE R<4> through RAM_CS L R<0>, including part numbers like RP3841 and values like 15, 6, 5, 4, 3, 2, 1.

Table titled 'THE FOLLOWING ARE 0402 5% RESISTORS' for RAM_CLK A P R through RAM_CLK F N R, including part numbers like R3816 and values like 15, 2, 1.

Table titled 'THE FOLLOWING IS A SWAPPABLE GROUP' for RAM A R<11> through RAM A R<3>, including part numbers like RP3832 and values like 15, 6, 5, 4, 3, 2, 1.

Table of component values for RAM_DQS R<0> through RAM_DQS R<15>, including part numbers like R3800 and values like 15, 2, 1.

Table of component values for RAM_CAS L R through RAM A R<8>, including part numbers like RP3804 and values like 15, 8, 7, 6, 5, 4, 3, 2, 1.

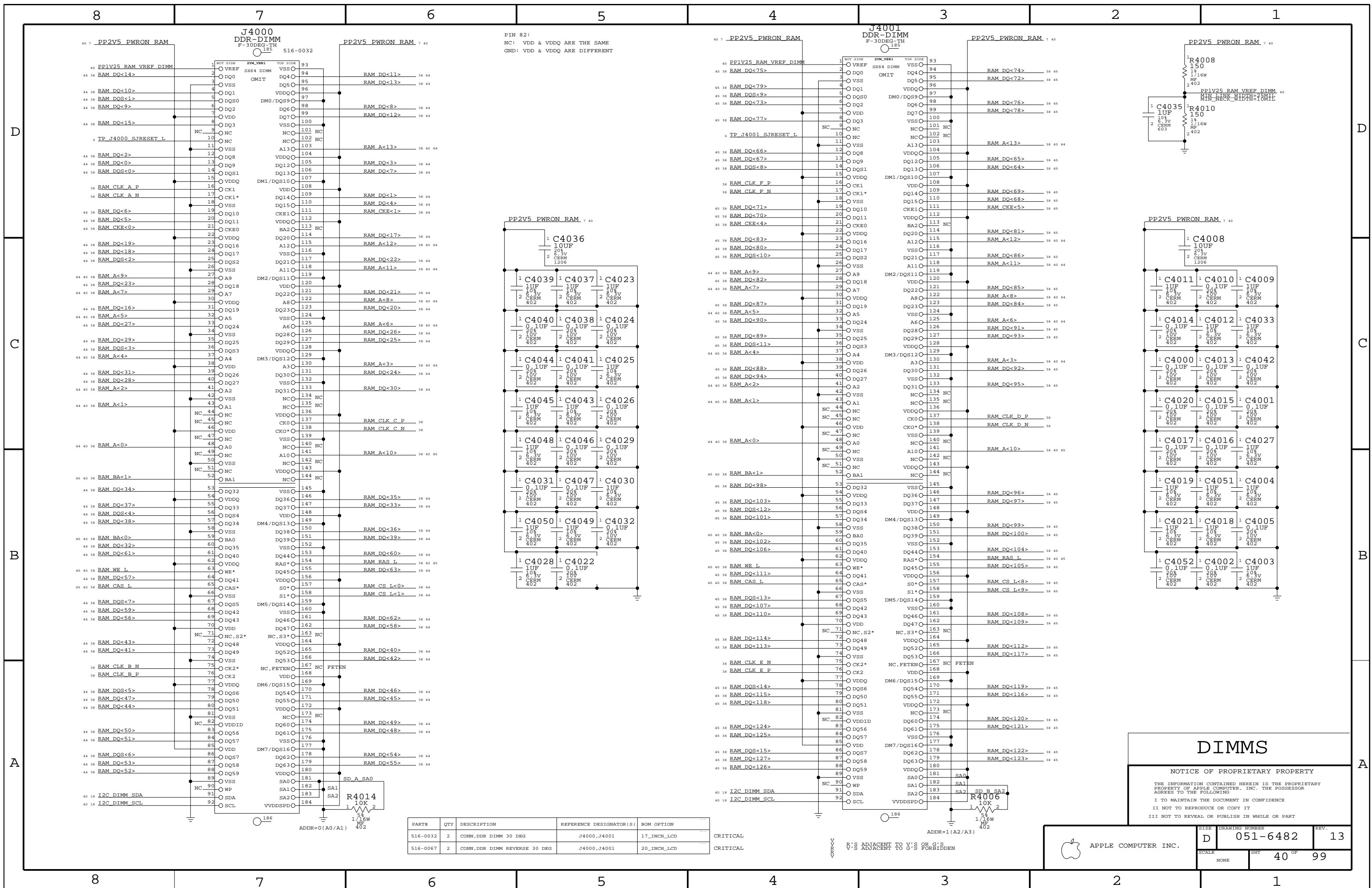
RAM_CLK PRIMARY SPACING SET TO 5MIL
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERANCE = 20PS = 2.82MM
RAM_CAD SPACING IS 10MIL

SERIES TERM

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APPLE COMPUTER INC. DRAWING NUMBER 051-6482 REV. 13
SCALE NONE SHEET 38 OF 99



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
516-0032	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD
516-0067	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD

DIMMS

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APPLE COMPUTER INC.	SCALE	SHEET	REV.
	NONE	40 OF 99	13

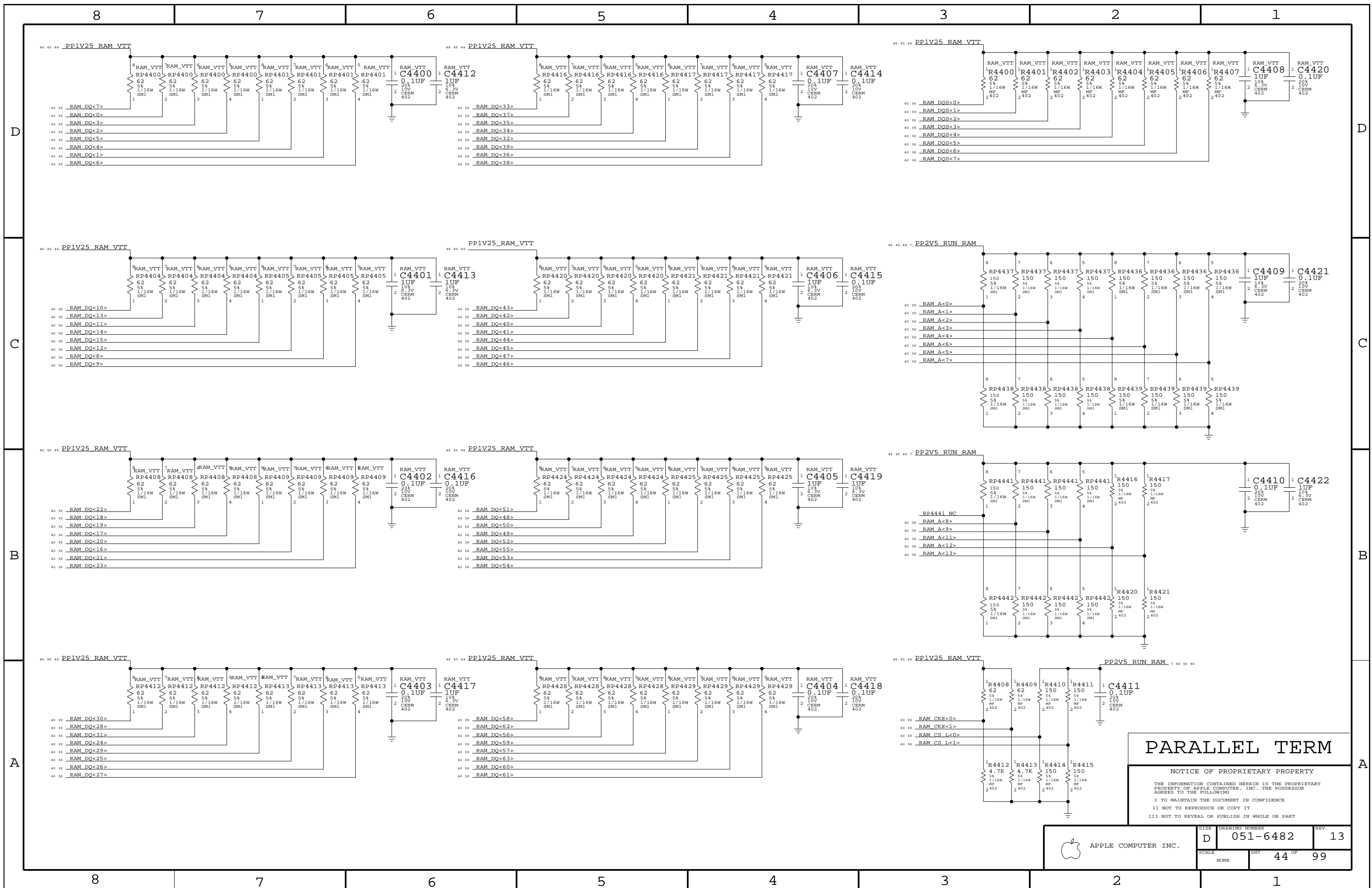
CRITICAL

CRITICAL

V'S ADJACENT TO V'S OR G'S
 G'S ADJACENT TO G'S OR S'S FORBIDDEN

ADDR=1(A2/A3)

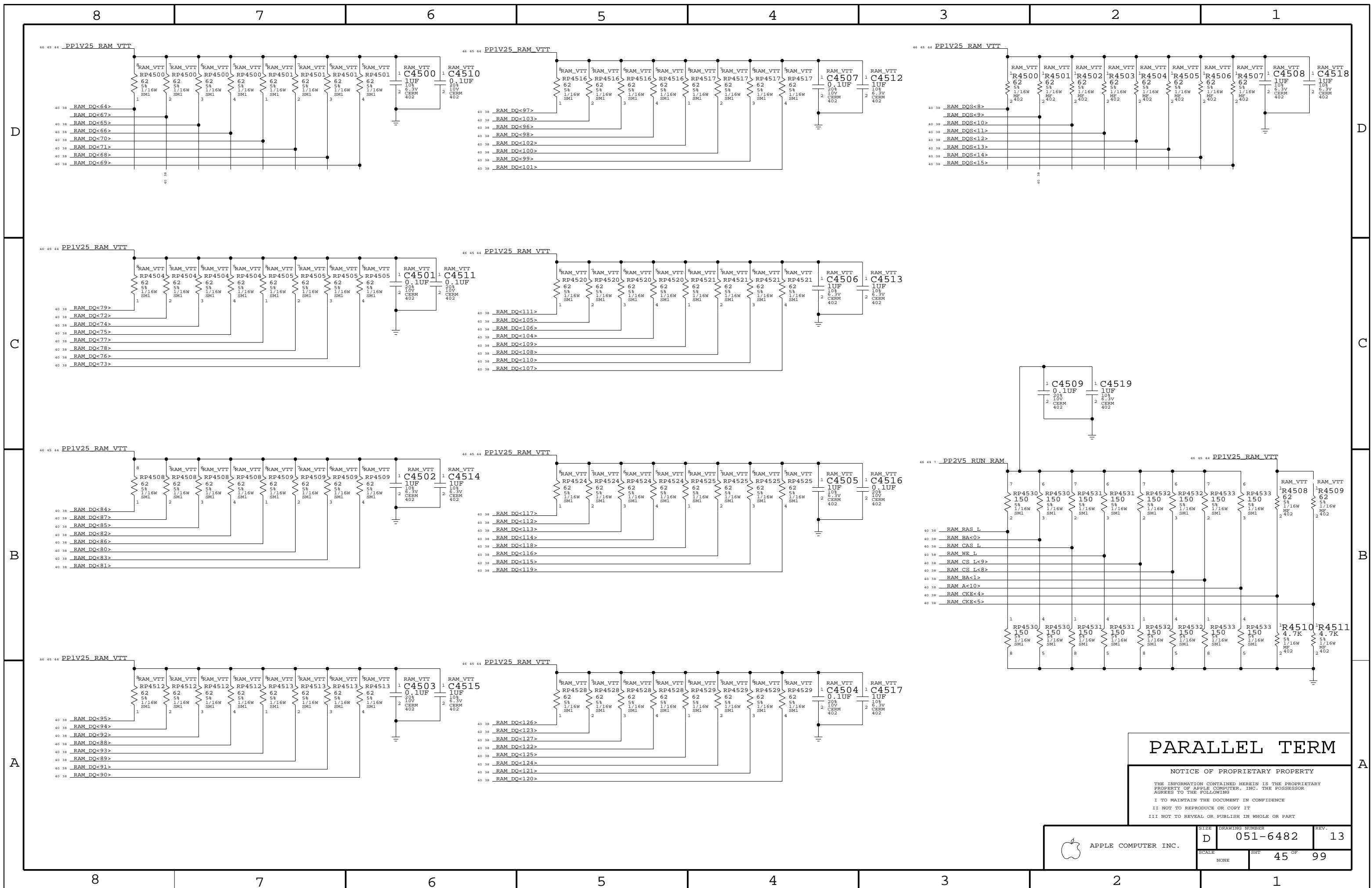
ADDR=0(A0/A1)



PARALLEL TERM

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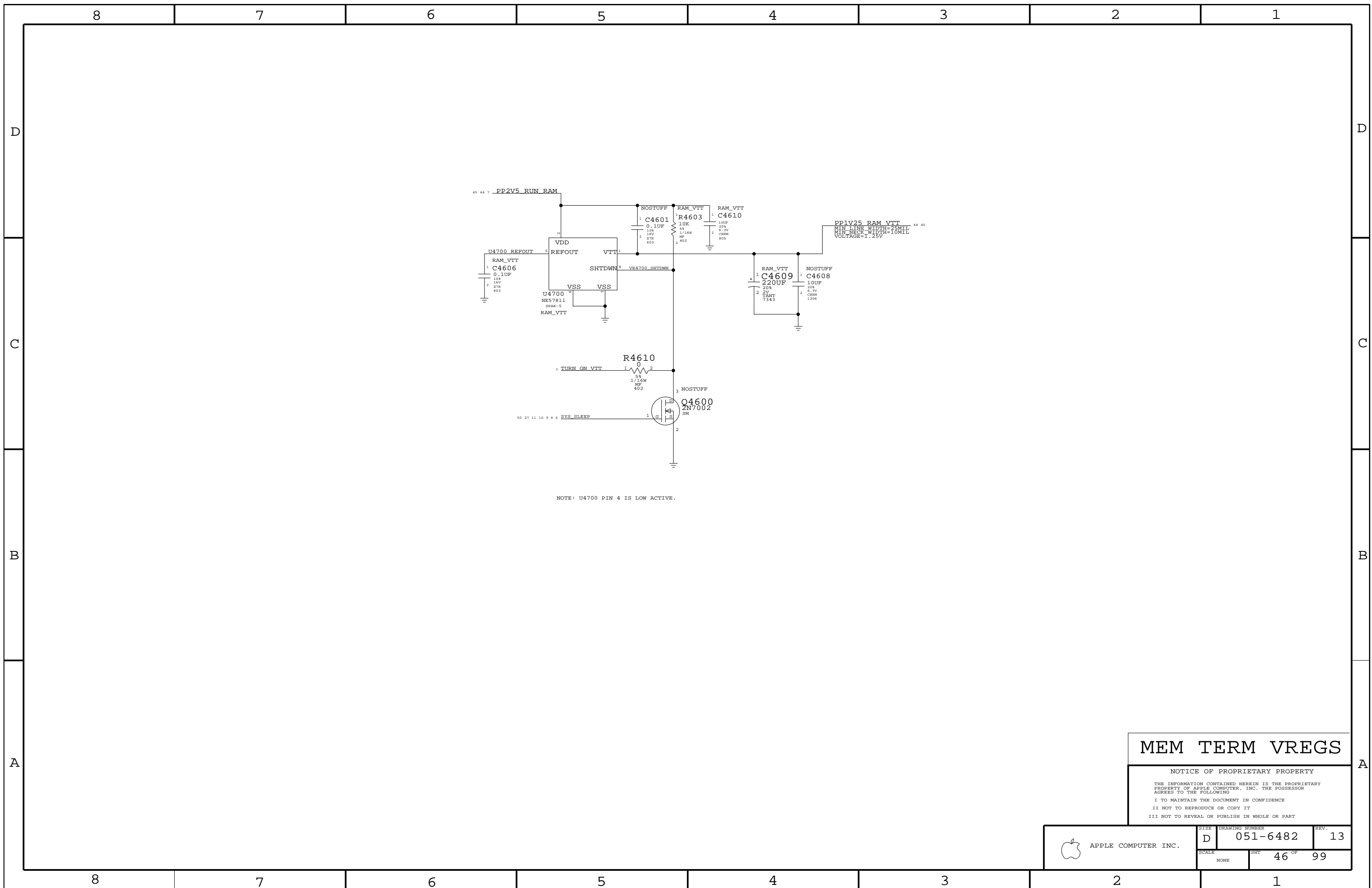
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. 13
	SCALE NONE	SHEET 44 OF 99	



PARALLEL TERM

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	SCALE NONE	SHEET 45 OF 99	



MEM TERM VREGS

NOTICE OF PROPRIETARY PROPERTY

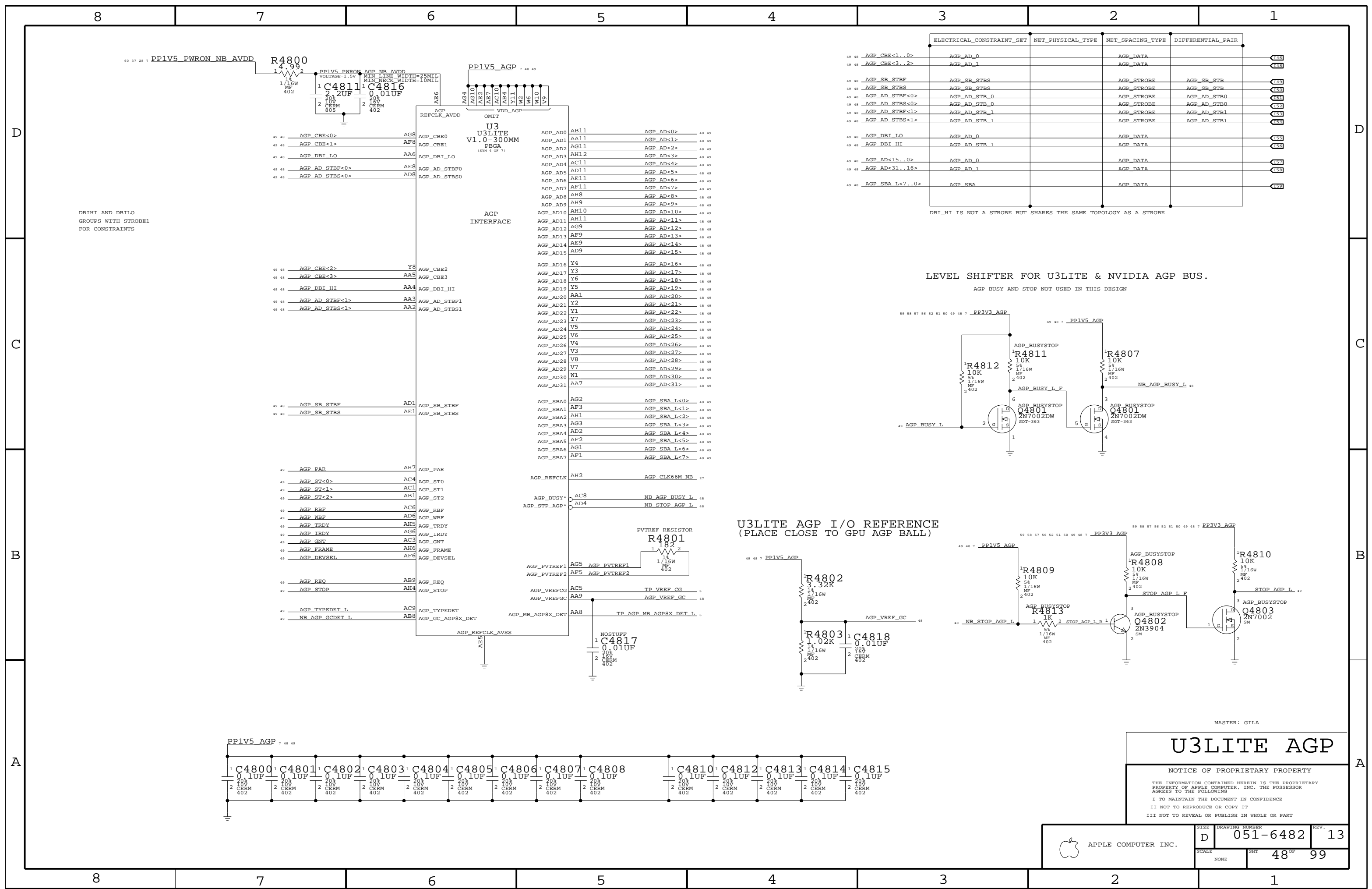
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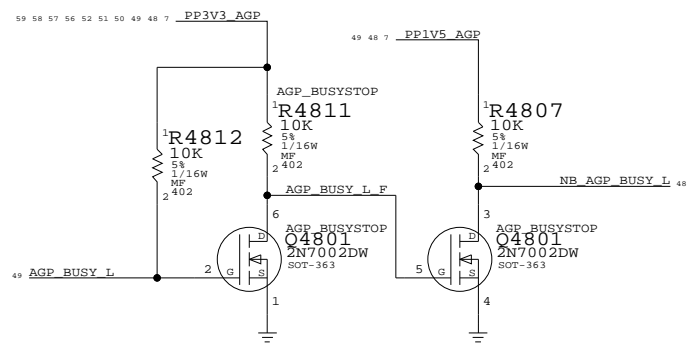
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. 13
	SCALE NONE	SHEET 46	OF 99



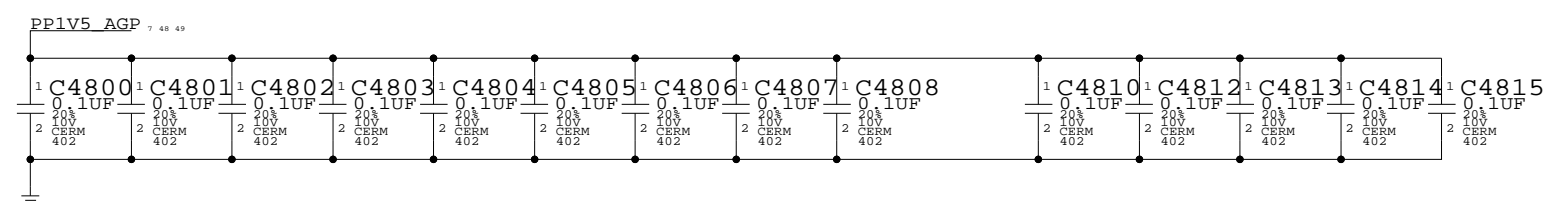
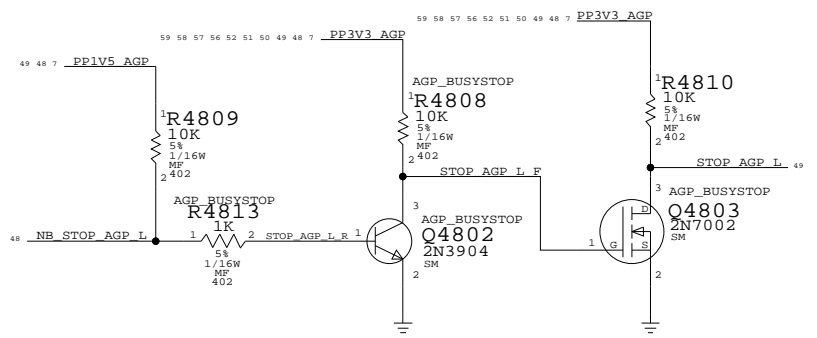
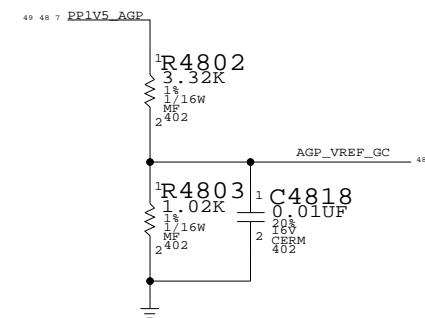
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
AGP_CBE<1..0>	AGP_AD_0	AGP_DATA	486
AGP_CBE<3..2>	AGP_AD_1	AGP_DATA	488
AGP_SB_STBF	AGP_SB_STBS	AGP_STROBE	489
AGP_SB_STBS	AGP_SB_STBS	AGP_STROBE	490
AGP_AD_STBF<0>	AGP_AD_STB_0	AGP_STROBE	491
AGP_AD_STBS<0>	AGP_AD_STB_0	AGP_STROBE	492
AGP_AD_STBF<1>	AGP_AD_STB_1	AGP_STROBE	493
AGP_AD_STBS<1>	AGP_AD_STB_1	AGP_STROBE	494
AGP_DBI_LO	AGP_AD_0	AGP_DATA	495
AGP_DBI_HI	AGP_AD_STB_1	AGP_DATA	496
AGP_AD<15..0>	AGP_AD_0	AGP_DATA	497
AGP_AD<31..16>	AGP_AD_1	AGP_DATA	498
AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA	499

DBI_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE

LEVEL SHIFTER FOR U3LITE & NVIDIA AGP BUS.
AGP BUSY AND STOP NOT USED IN THIS DESIGN



U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)



MASTER: GILA

U3LITE AGP

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	SHT	48 OF 99	
NONE			

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0155	1	IC,NV18B,GRAPHIC CTRL	U4900	NV18B
338S0113	1	IC,NV34,GRAPHIC CTRL	U4900	NV34

NVIDIA RECOMMENDS A WIDER RANGE OF CAP VALUES, EMC LIKES ONE VALUE

AGP AD<0>	AJ28	PCIAD0
AGP AD<1>	AK28	PCIAD1
AGP AD<2>	AH27	PCIAD2
AGP AD<3>	AK27	PCIAD3
AGP AD<4>	AJ27	PCIAD4
AGP AD<5>	AH26	PCIAD5
AGP AD<6>	AJ26	PCIAD6
AGP AD<7>	AH25	PCIAD7
AGP AD<8>	AH23	PCIAD8
AGP AD<9>	AJ23	PCIAD9
AGP AD<10>	AH22	PCIAD10
AGP AD<11>	AJ22	PCIAD11
AGP AD<12>	AJ21	PCIAD12
AGP AD<13>	AK21	PCIAD13
AGP AD<14>	AH20	PCIAD14
AGP AD<15>	AJ20	PCIAD15
AGP AD<16>	AG26	PCIAD16
AGP AD<17>	AE24	PCIAD17
AGP AD<18>	AG25	PCIAD18
AGP AD<19>	AG24	PCIAD19
AGP AD<20>	AF24	PCIAD20
AGP AD<21>	AG23	PCIAD21
AGP AD<22>	AE22	PCIAD22
AGP AD<23>	AF22	PCIAD23
AGP AD<24>	AE21	PCIAD24
AGP AD<25>	AG20	PCIAD25
AGP AD<26>	AG19	PCIAD26
AGP AD<27>	AF19	PCIAD27
AGP AD<28>	AE19	PCIAD28
AGP AD<29>	AF18	PCIAD29
AGP AD<30>	AG18	PCIAD30
AGP AD<31>	AE18	PCIAD31

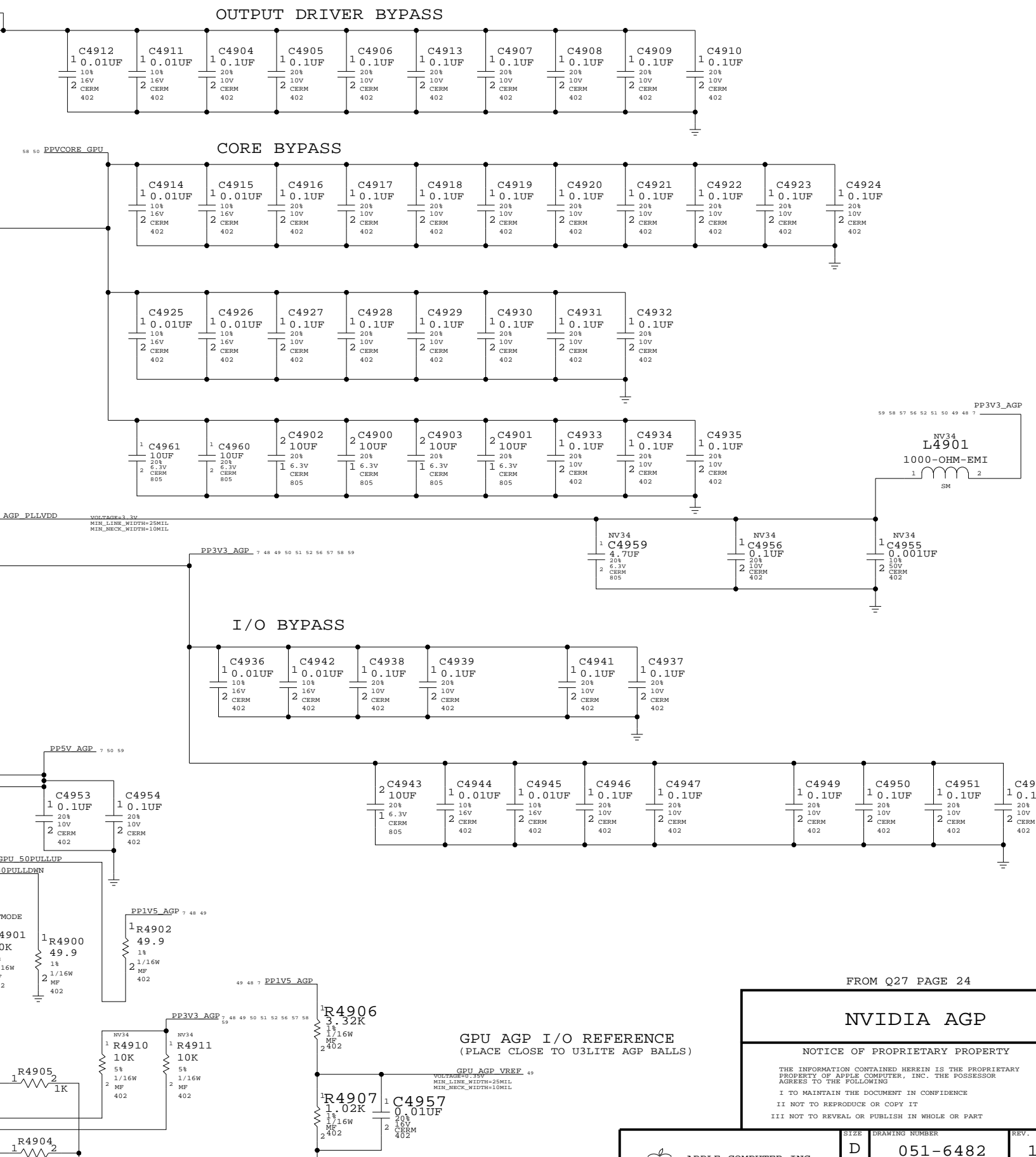
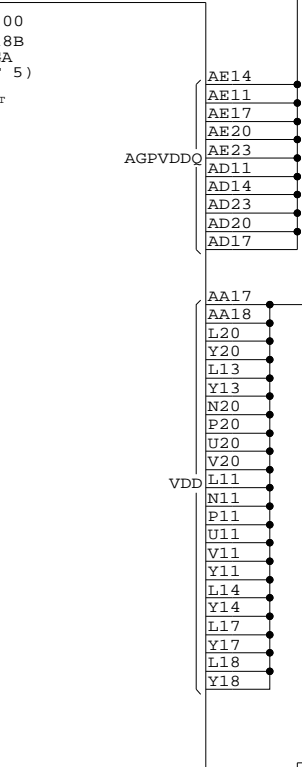
AGP CBE<0>	AJ24	PCIC0/BE0*	C0*/BE0
AGP CBE<1>	AH19	PCIC1/BE1*	C1*/BE1
AGP CBE<2>	AF25	PCIC2/BE2*	C2*/BE2
AGP CBE<3>	AG22	PCIC3/BE3*	C3*/BE3

AGP AD STBF<0>	AK24	AGPADSTBF0	ADSTBF0
AGP AD STBS<0>	AJ25	AGPADSTBS0*	ADSTBS0
AGP AD STBF<1>	AG21	AGPADSTBF1	ADSTBF1
AGP AD STBS<1>	AF21	AGPADSTBS1*	ADSTBS1

AGP SBA L<0>	AJ11	AGPSBA0	SBA0*
AGP SBA L<1>	AH11	AGPSBA1	SBA1*
AGP SBA L<2>	AJ12	AGPSBA2	SBA2*
AGP SBA L<3>	AH12	AGPSBA3	SBA3*
AGP SBA L<4>	AJ14	AGPSBA4	SBA4*
AGP SBA L<5>	AH14	AGPSBA5	SBA5*
AGP SBA L<6>	AJ15	AGPSBA6	SBA6*
AGP SBA L<7>	AH15	AGPSBA7	SBA7*

GPU MBDT L	AF16	<RESRVD>	MBDET*
AGP BUSY L	AF12	AGPBUSY*	BUSY*
STOP_AGP L	AG11	AGPSTOP*	STOP*
GPU_AGP_VREF	AK29	AGPVREF	AGPVREF

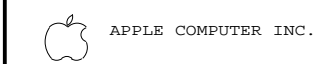
AGP VERSION SELECT	(LOW = AGP V3.X)	(HIGH = AGP V2.X)
TP_GPU<0>	AK30	
TP_GPU<1>	AK31	
TP_GPU<2>	R7	
TP_GPU<3>	R7	
TP_GPU<4>	L1	



FROM Q27 PAGE 24
NVIDIA AGP

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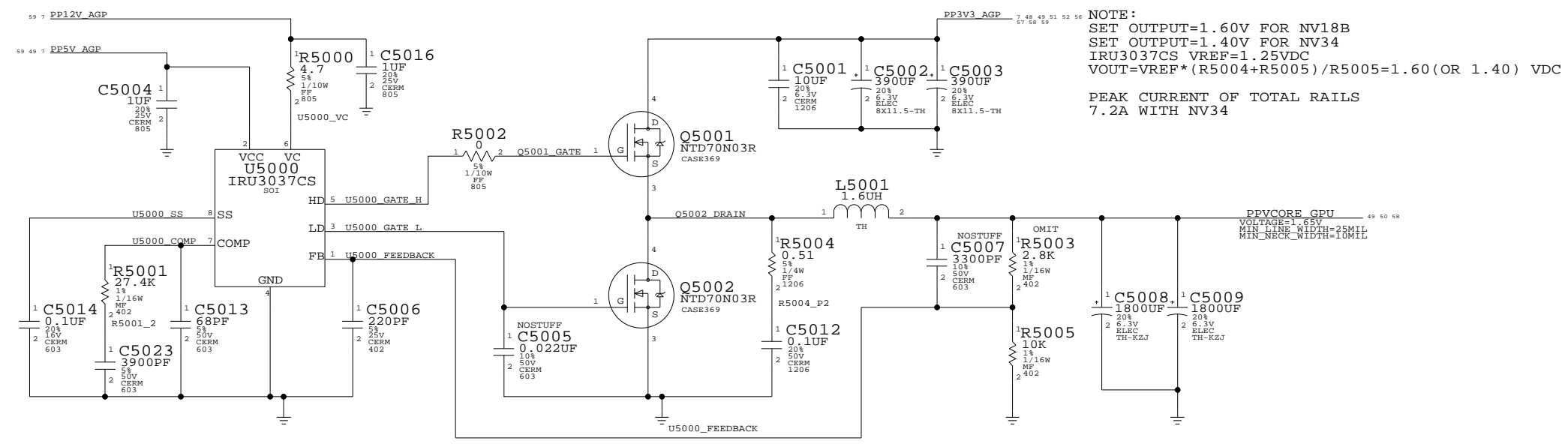
SCALE	DRAWING NUMBER	REV.
NONE	D 051-6482	13
	SHEET	OF
	49	99



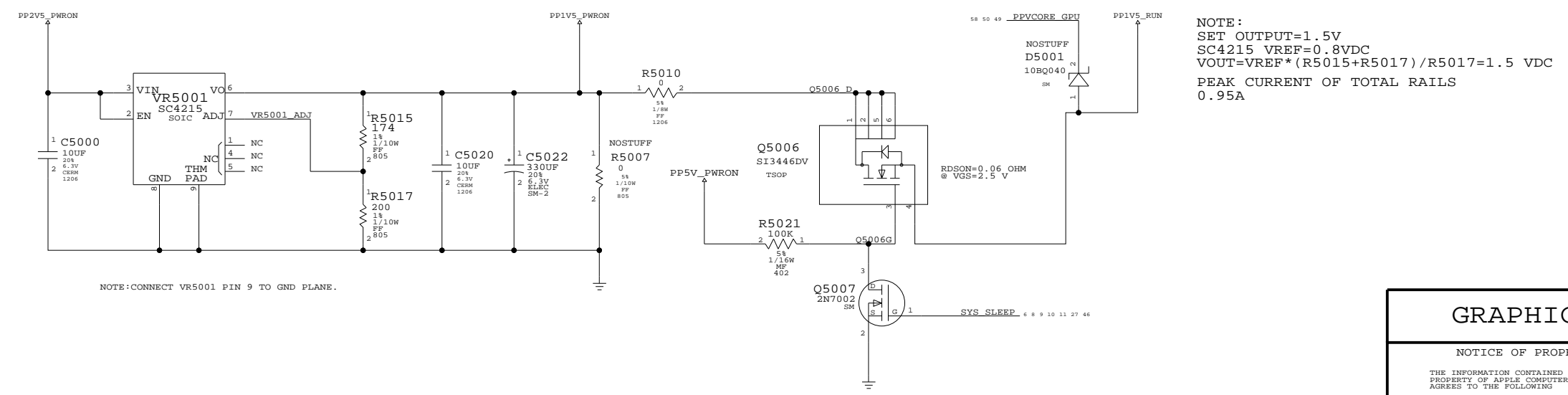
BOUNDARY SCAN AVAILABLE ONLY ON NV3X SERIES

PPVOCRE_GPU	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
1.60VDC	114S2803	1	RES,2.8K OHM,1/16W,1%,0402	R5003	NV18B
1.40VDC	114S1213	1	RES,1.21K OHM,1/16W,1%,0402	R5003	NV34

GPU VCORE VREG



AGP 1.5V VREG



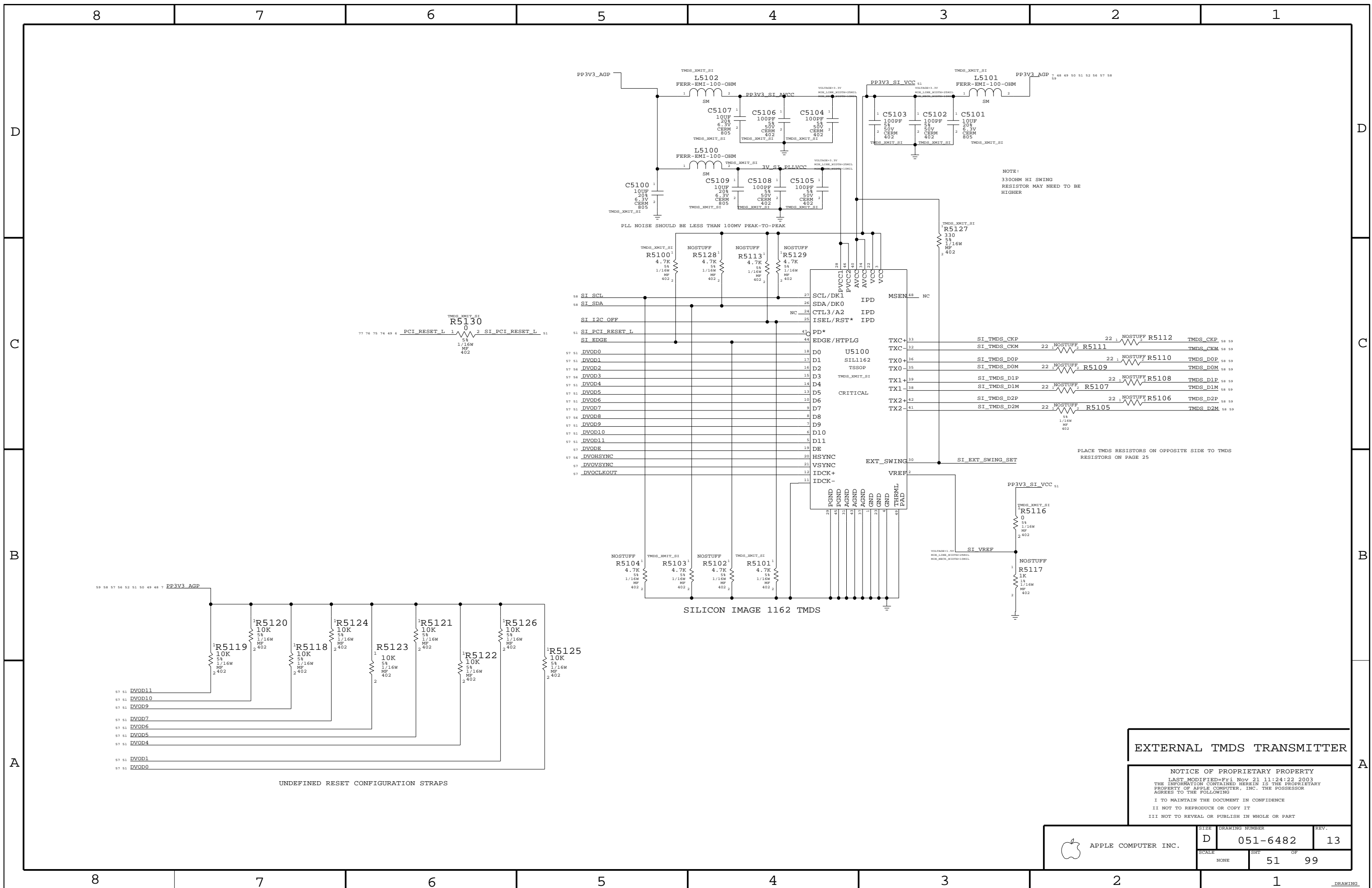
GRAPHICS VREGS

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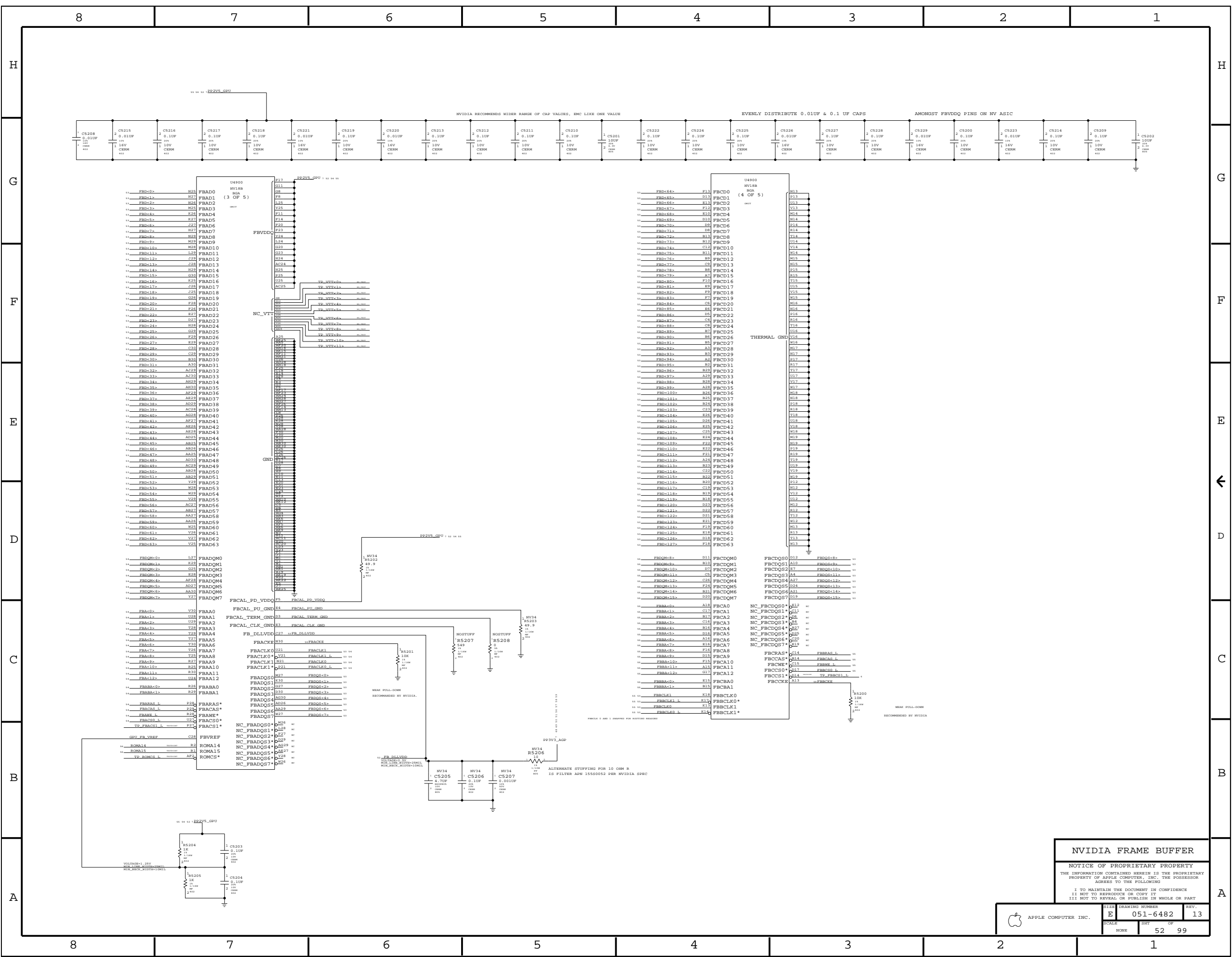
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	NONE	SHT	OF
		50	99



EXTERNAL TMSD TRANSMITTER

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SCALE	NONE	SHT	OF
		51	99



NVIDIA FRAME BUFFER

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SCALE	None	DRAWING NUMBER	051-6482	REV.	13
SHEET	52	OF	99		



APPLE COMPUTER INC.

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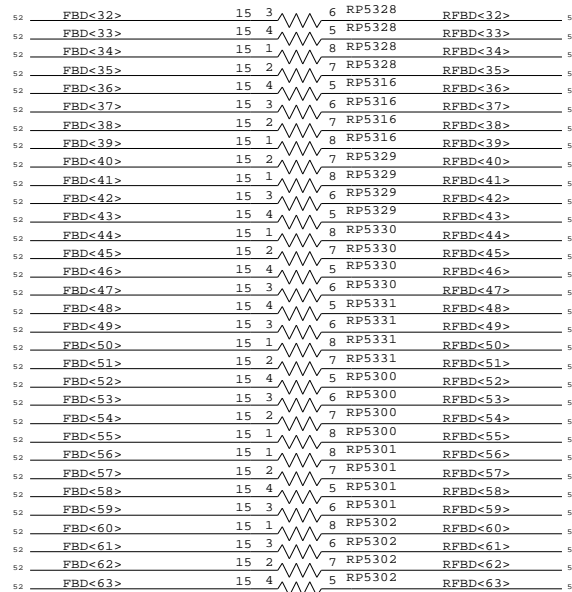
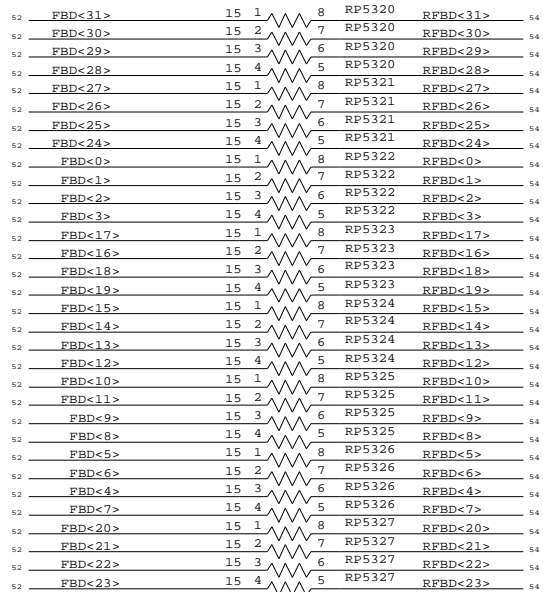
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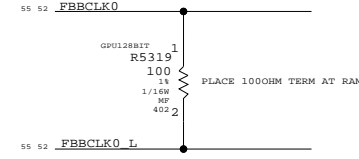
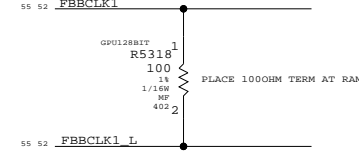
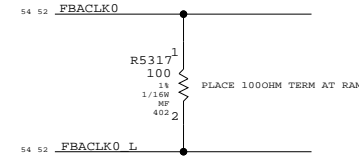
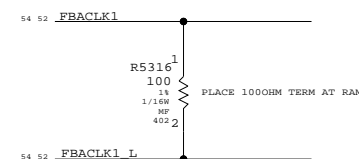
2

1

PLACE R'S CLOSE TO MEMORY



PLACE R'S CLOSE TO GPU



D

D

C

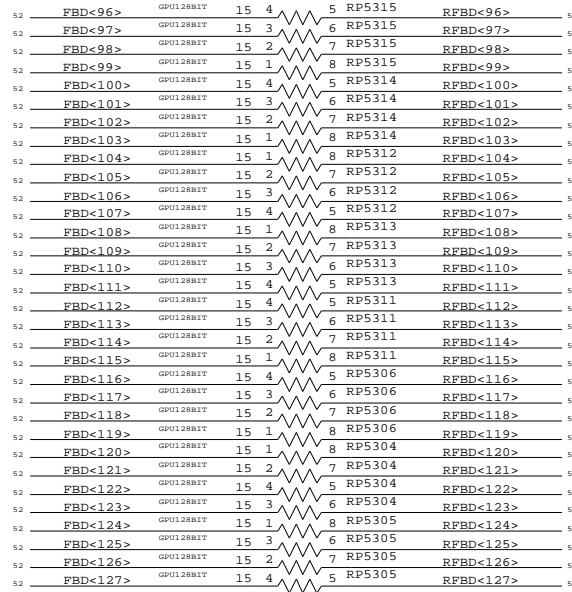
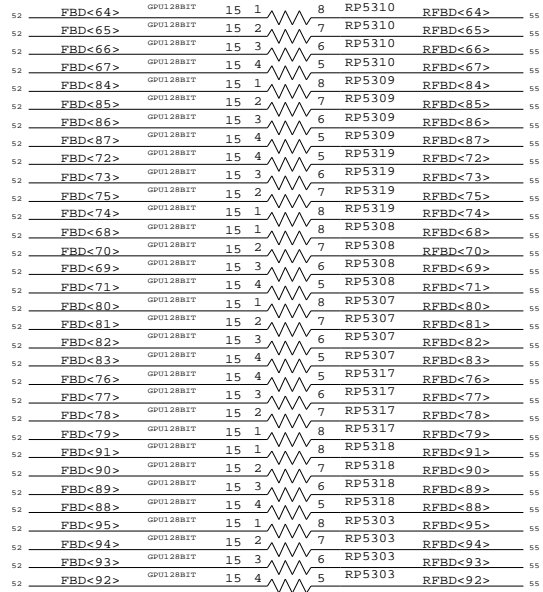
C

B

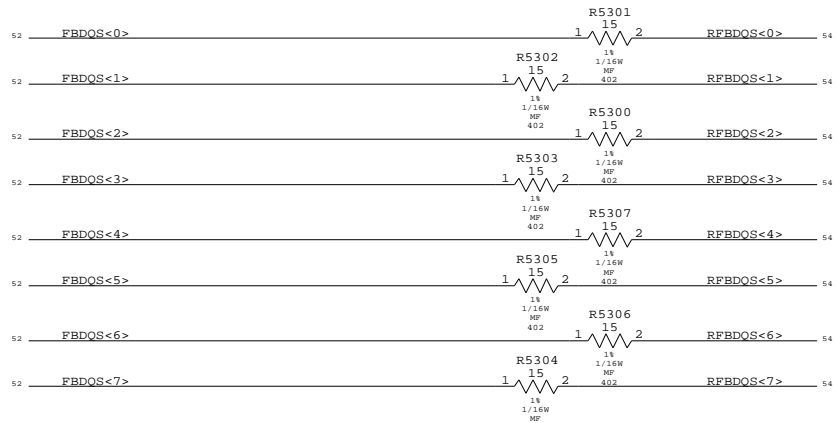
B

A

A



PLACE THESE R CLOSE TO SGRAM



PLACE THESE R CLOSE TO SGRAM



FROM Q27 PAGE 26

FB TERMINATION

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SCALE	NONE	SHT	OF
		53	99

8

7

6

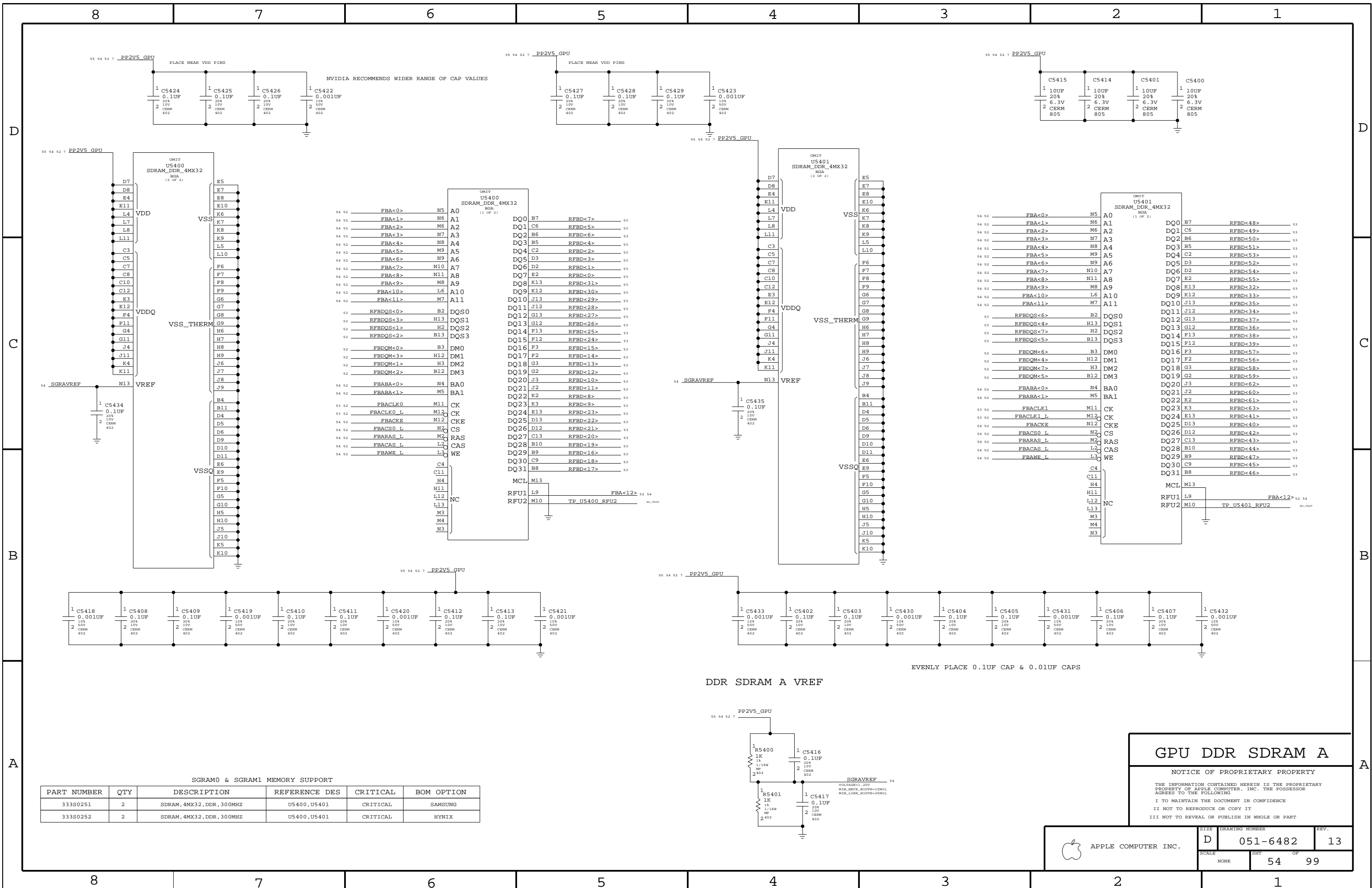
5

4

3

2

1



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B

A

SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U5400, U5401	CRITICAL	SAMSUNG
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U5400, U5401	CRITICAL	HYNIX

GPU DDR SDRAM A

NOTICE OF PROPRIETARY PROPERTY

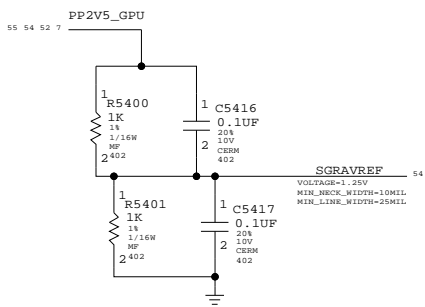
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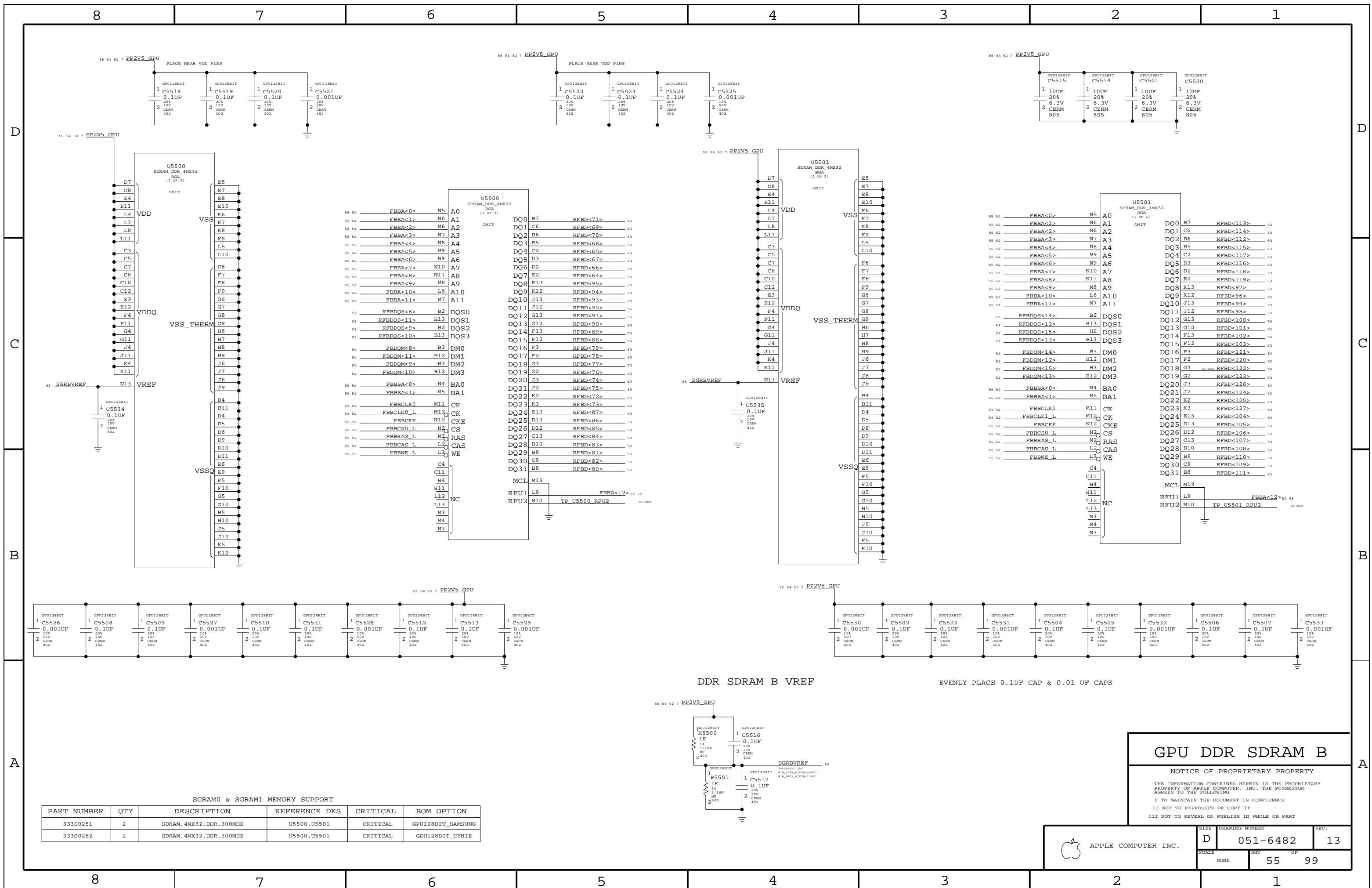
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SCALE NONE	SHEET 54	DRAWING NUMBER 051-6482	REV. 13
			APPLE COMPUTER INC.

EVENLY PLACE 0.1UF CAP & 0.01UF CAPS

DDR SDRAM A VREF





D

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A

D

C

B

A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33380251	2	SDRAM, 4MX32, DDR, 300MHZ	U5500, U5501	CRITICAL	GPU128BIT_SAMSUNG
33380252	2	SDRAM, 4MX32, DDR, 300MHZ	U5500, U5501	CRITICAL	GPU128BIT_HYNIX

GPU DDR SDRAM B

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APPLE COMPUTER INC.

SCALE: NONE

SIZE: D

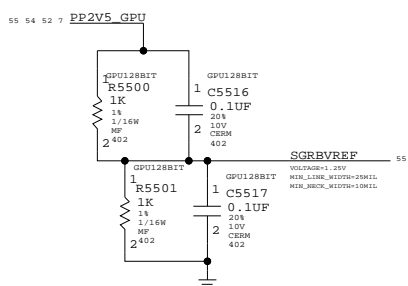
DRAWING NUMBER: 051-6482

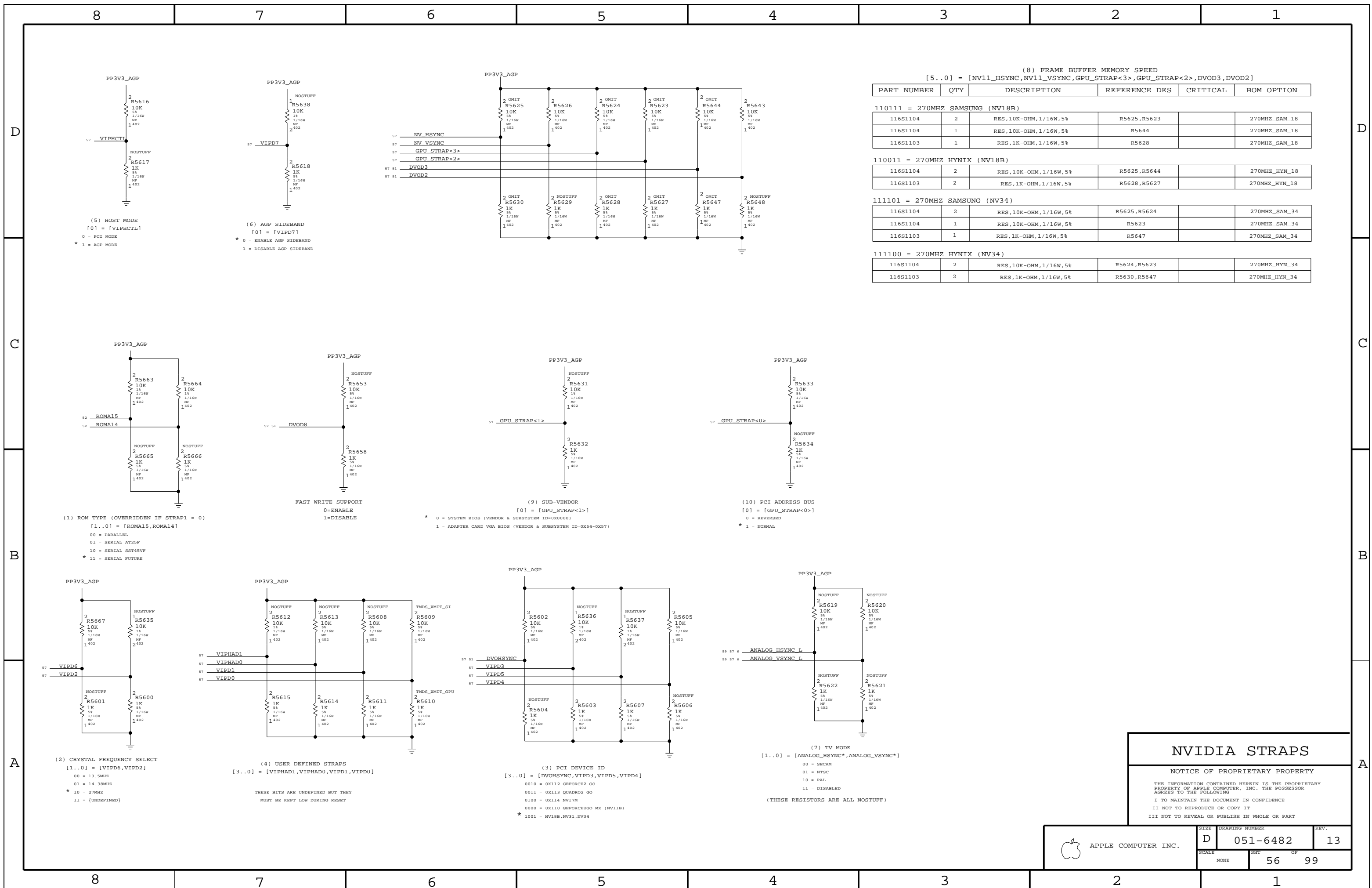
SHEET: 55 OF 99

REV: 13

DDR SDRAM B VREF

EVENLY PLACE 0.1UF CAP & 0.01 UF CAPS





(8) FRAME BUFFER MEMORY SPEED
[5..0] = [NV11_HSYNC, NV11_VSYNC, GPU_STRAP<3>, GPU_STRAP<2>, DVOD3, DVOD2]

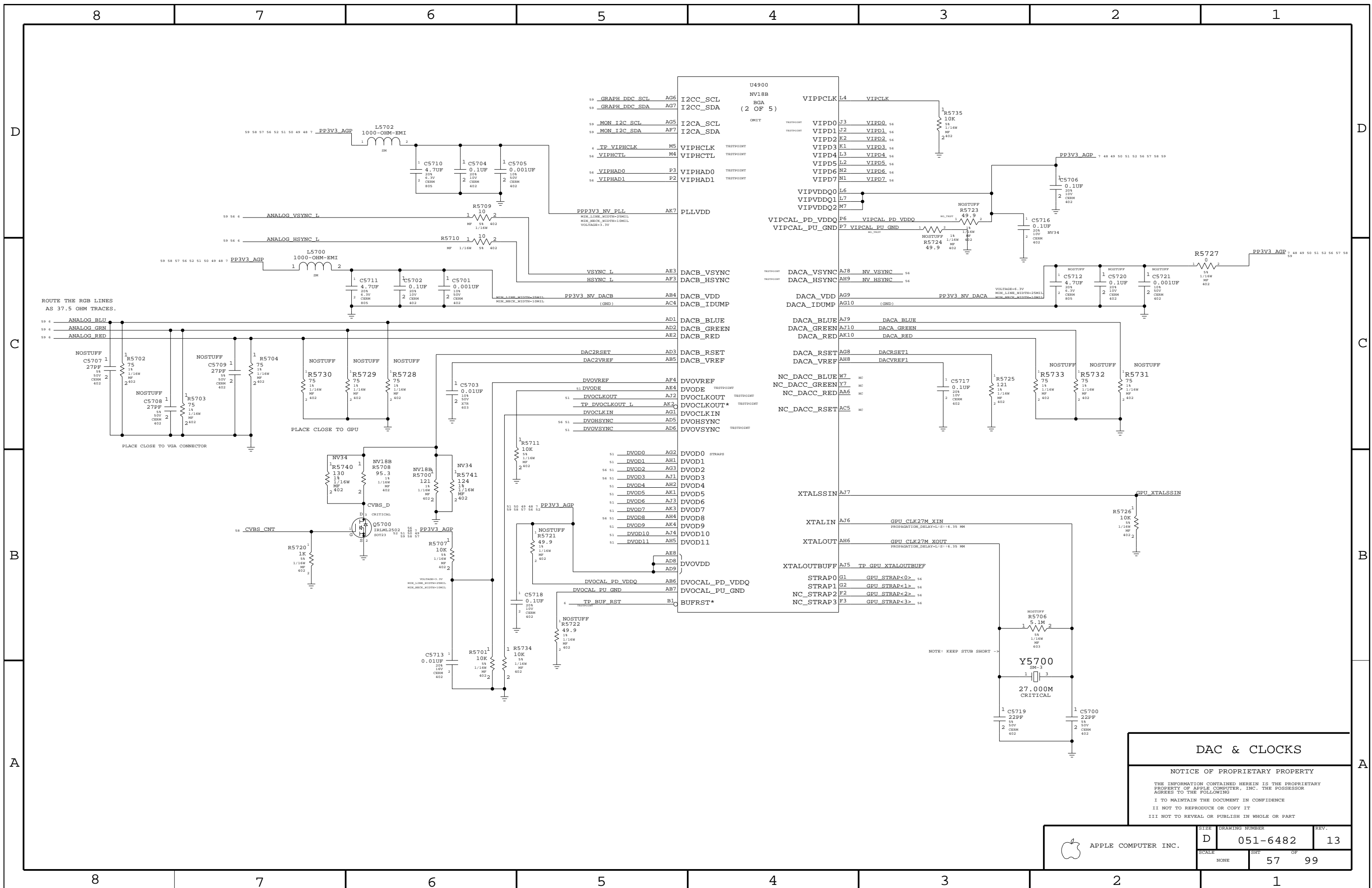
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
110111 = 270MHZ SAMSUNG (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5623		270MHZ_SAM_18
116S1104	1	RES,10K-OHM,1/16W,5%	R5644		270MHZ_SAM_18
116S1103	1	RES,1K-OHM,1/16W,5%	R5628		270MHZ_SAM_18
110011 = 270MHZ HYNIX (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5644		270MHZ_HYN_18
116S1103	2	RES,1K-OHM,1/16W,5%	R5628,R5627		270MHZ_HYN_18
111101 = 270MHZ SAMSUNG (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5624		270MHZ_SAM_34
116S1104	1	RES,10K-OHM,1/16W,5%	R5623		270MHZ_SAM_34
116S1103	1	RES,1K-OHM,1/16W,5%	R5647		270MHZ_SAM_34
111100 = 270MHZ HYNIX (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5624,R5623		270MHZ_HYN_34
116S1103	2	RES,1K-OHM,1/16W,5%	R5630,R5647		270MHZ_HYN_34

NVIDIA STRAPS

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ROUTE THE RGB LINES AS 37.5 OHM TRACES.

PLACE CLOSE TO GPU

PLACE CLOSE TO VGA CONNECTOR

NOTE: KEEP STUB SHORT ->

DAC & CLOCKS

NOTICE OF PROPRIETARY PROPERTY

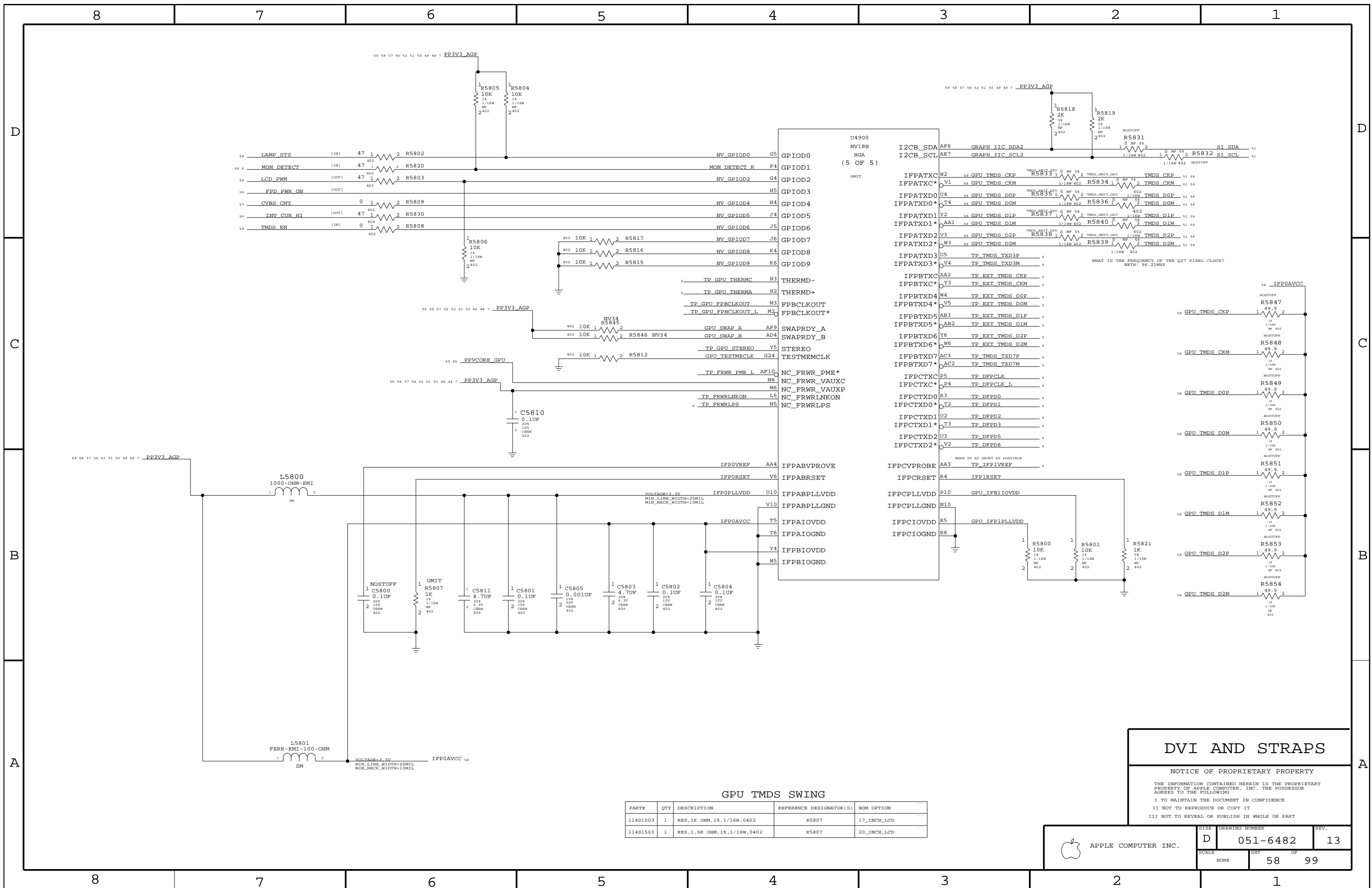
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	NONE	SHT	OF
		57	99



GPU TMS SWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1003	1	RES,1K OHM,1%,1/16W,0402	R5807	17_INCH_LCD
114S1503	1	RES,1.5K OHM,1%,1/16W,0402	R5807	20_INCH_LCD

DVI AND STRAPS

NOTICE OF PROPRIETARY PROPERTY

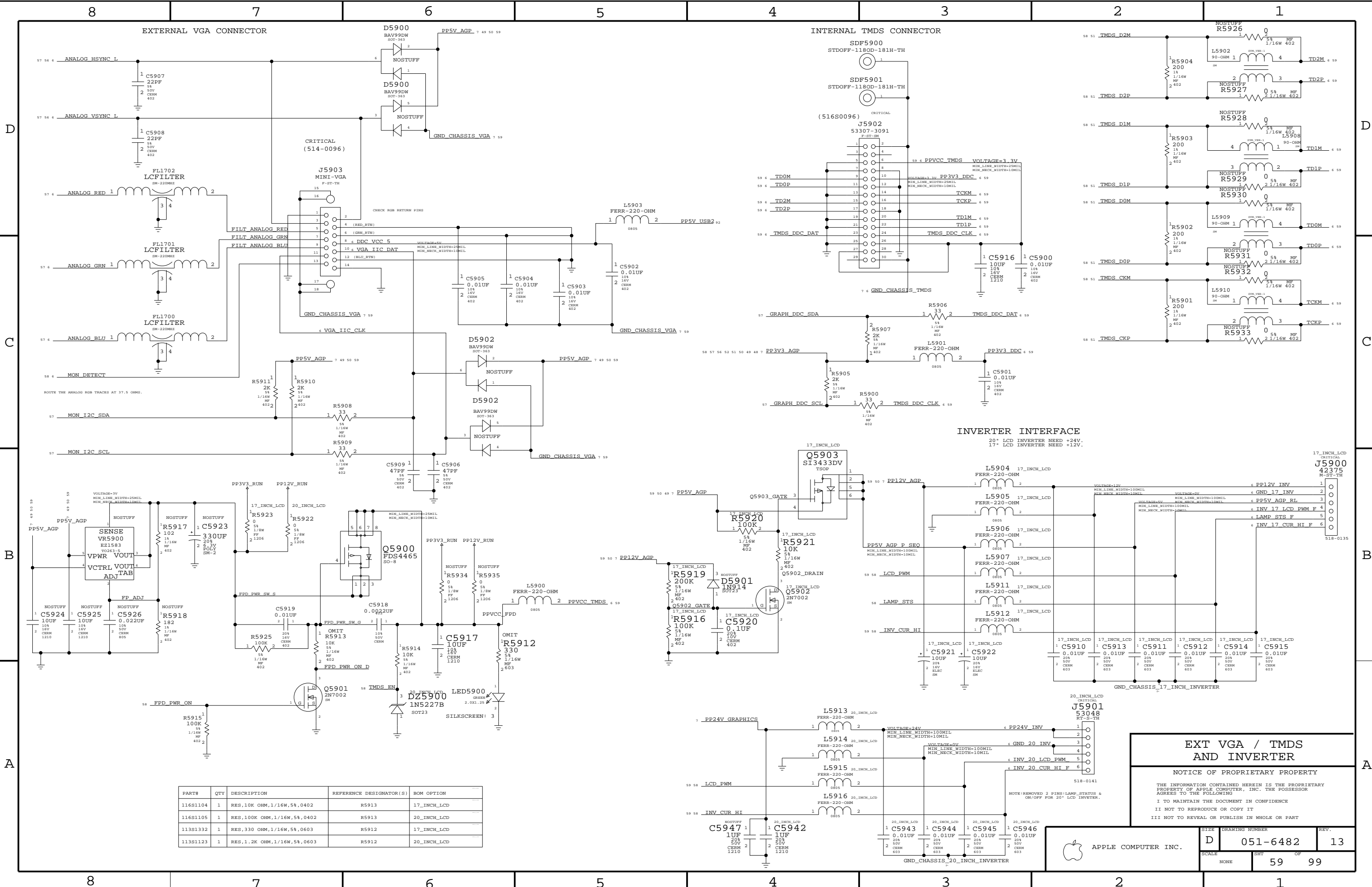
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	SCALE: NONE	SHEET: 58	OF: 99



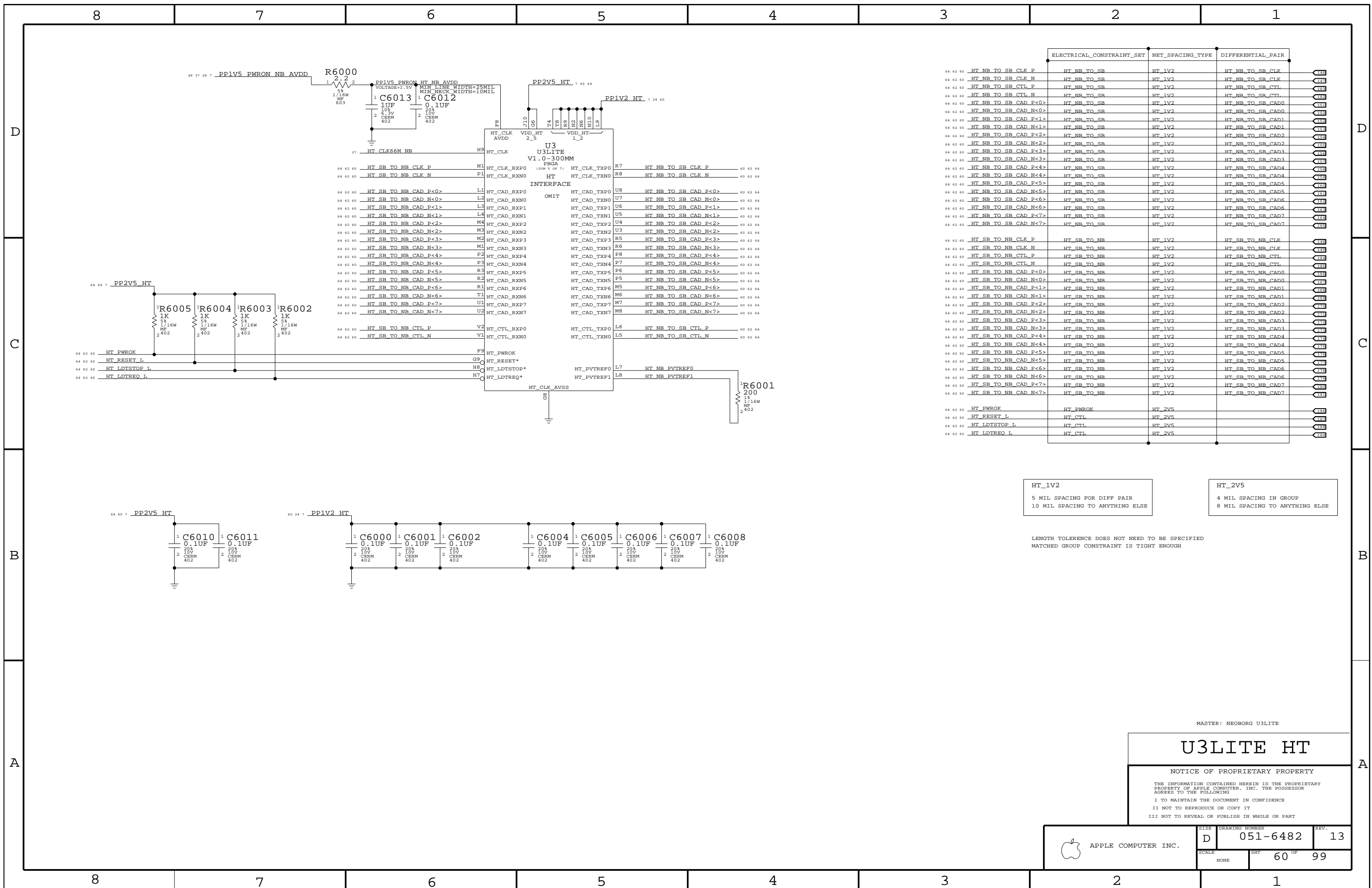
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES, 10K OHM, 1/16W, 5%, 0402	R5913	17_INCH_LCD
116S1105	1	RES, 100K OHM, 1/16W, 5%, 0402	R5913	20_INCH_LCD
113S1332	1	RES, 330 OHM, 1/16W, 5%, 0603	R5912	17_INCH_LCD
113S1123	1	RES, 1.2K OHM, 1/16W, 5%, 0603	R5912	20_INCH_LCD

EXT VGA / TMD5 AND INVERTER

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	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6482	13
SHEET		OF	
59		99	



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_1V2
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HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_1V2
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HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_1V2
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_1V2
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_1V2
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_1V2
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_1V2
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HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_1V2
HT_PWROK	HT_PWROK	HT_2V5
HT_RESET_L	HT_CTL	HT_2V5
HT_LDTSTOP_L	HT_CTL	HT_2V5
HT_LDTREQ_L	HT_CTL	HT_2V5

HT_1V2
5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5
4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERANCE DOES NOT NEED TO BE SPECIFIED
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: NEOBORG U3LITE

U3LITE HT

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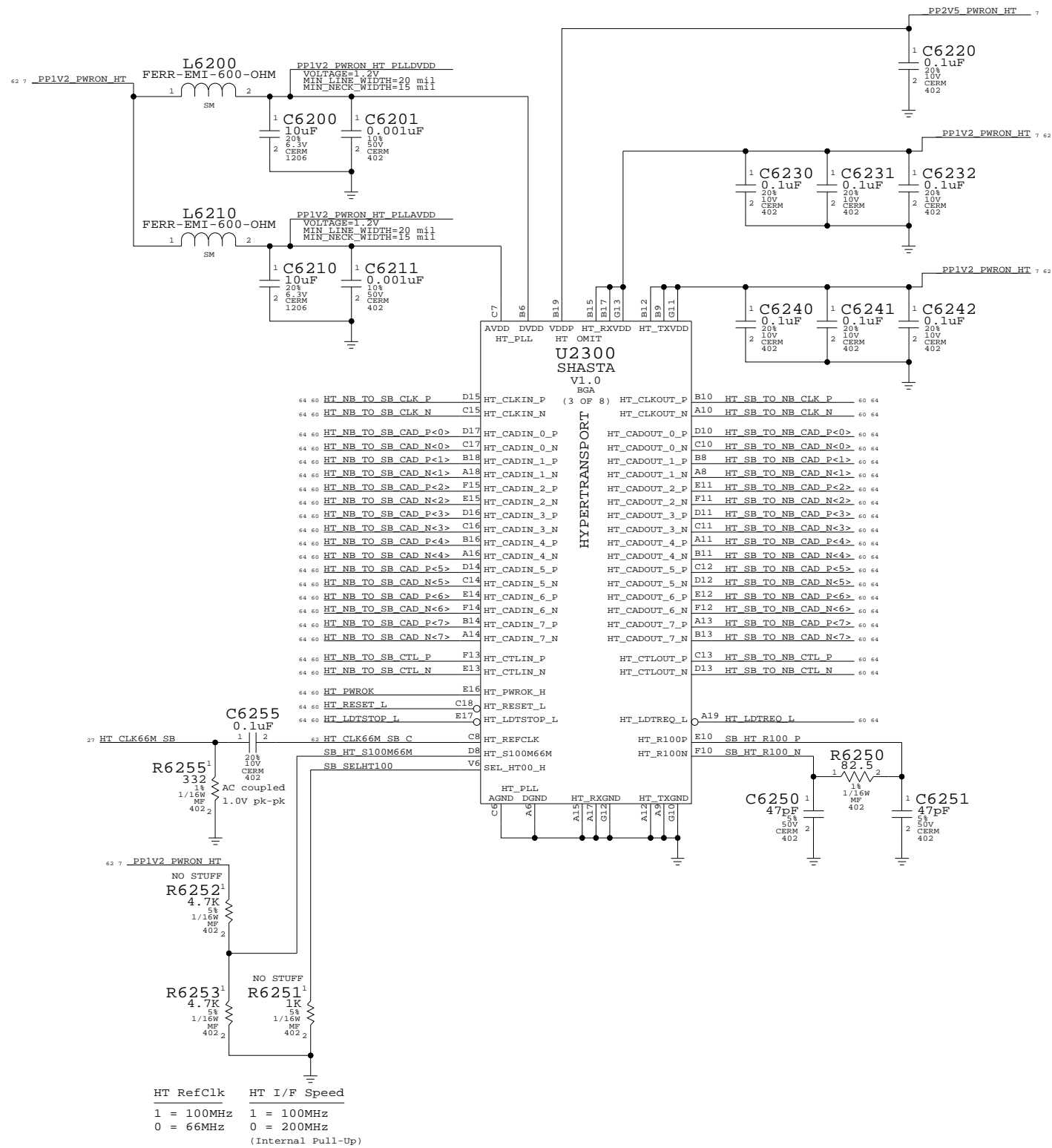
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	SHT	OF	
NONE	60	99	

Page Notes

Power aliases required by this page:
 - _PP2V5_PWRON_HT
 - _PP1V2_PWRON_HT

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Master: Fizzy

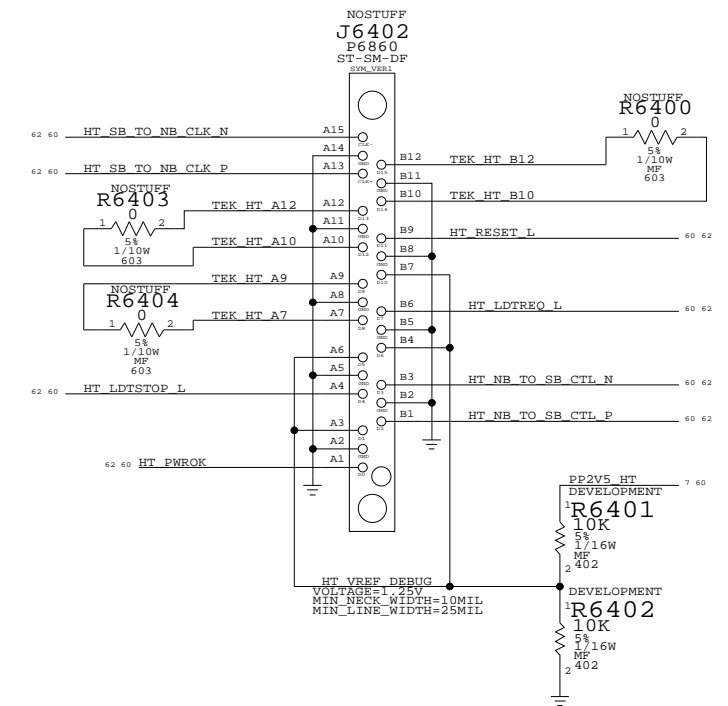
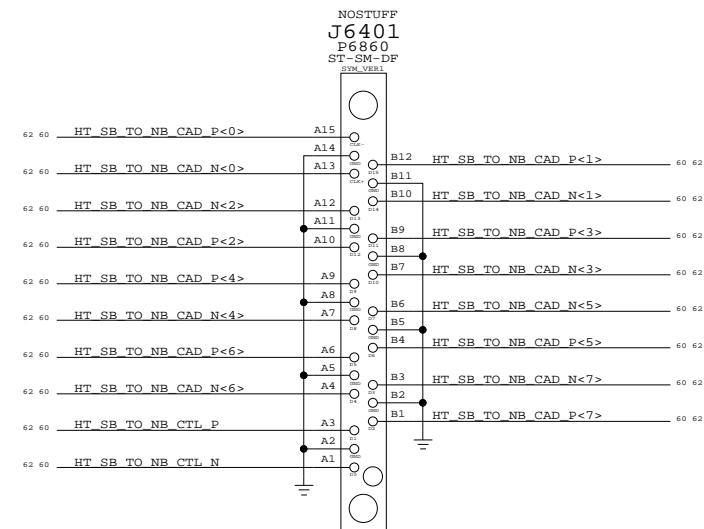
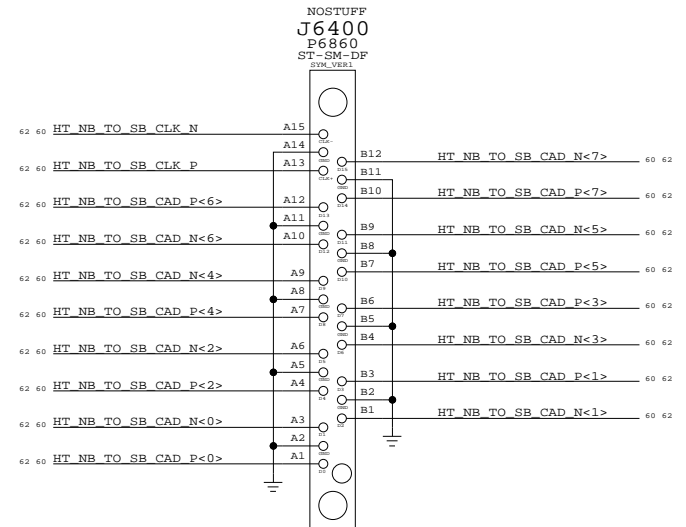
Shasta HyperTransport

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SAME CONNECTORS & PINOUT AS
Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2



MASTER: GILA

HT DEBUG CONN

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. 13
	SCALE NONE	SHEETS 64 OF 99	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_AD		PCI_AD<31..28>
PCI_AD27		PCI_AD<27>
PCI_AD		PCI_AD<26..24>
PCI_AD23		PCI_AD<23>
PCI_AD22		PCI_AD<22>
PCI_AD21		PCI_AD<21>
PCI_AD20		PCI_AD<20>
PCI_AD		PCI_AD<19..18>
PCI_AD17		PCI_AD<17>
PCI_AD		PCI_AD<16..0>
PCI		PCI_CBE_L<3..0>
PCI		PCI_PAR
PCI_CTL		PCI_DEVSEL_L
PCI_CTL		PCI_FRAME_L
PCI_CTL		PCI_IRDY_L
PCI_CTL		PCI_TRDY_L
PCI_CTL		PCI_STOP_L

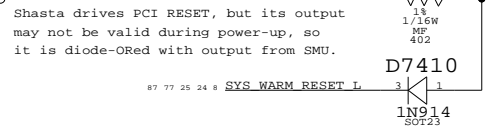
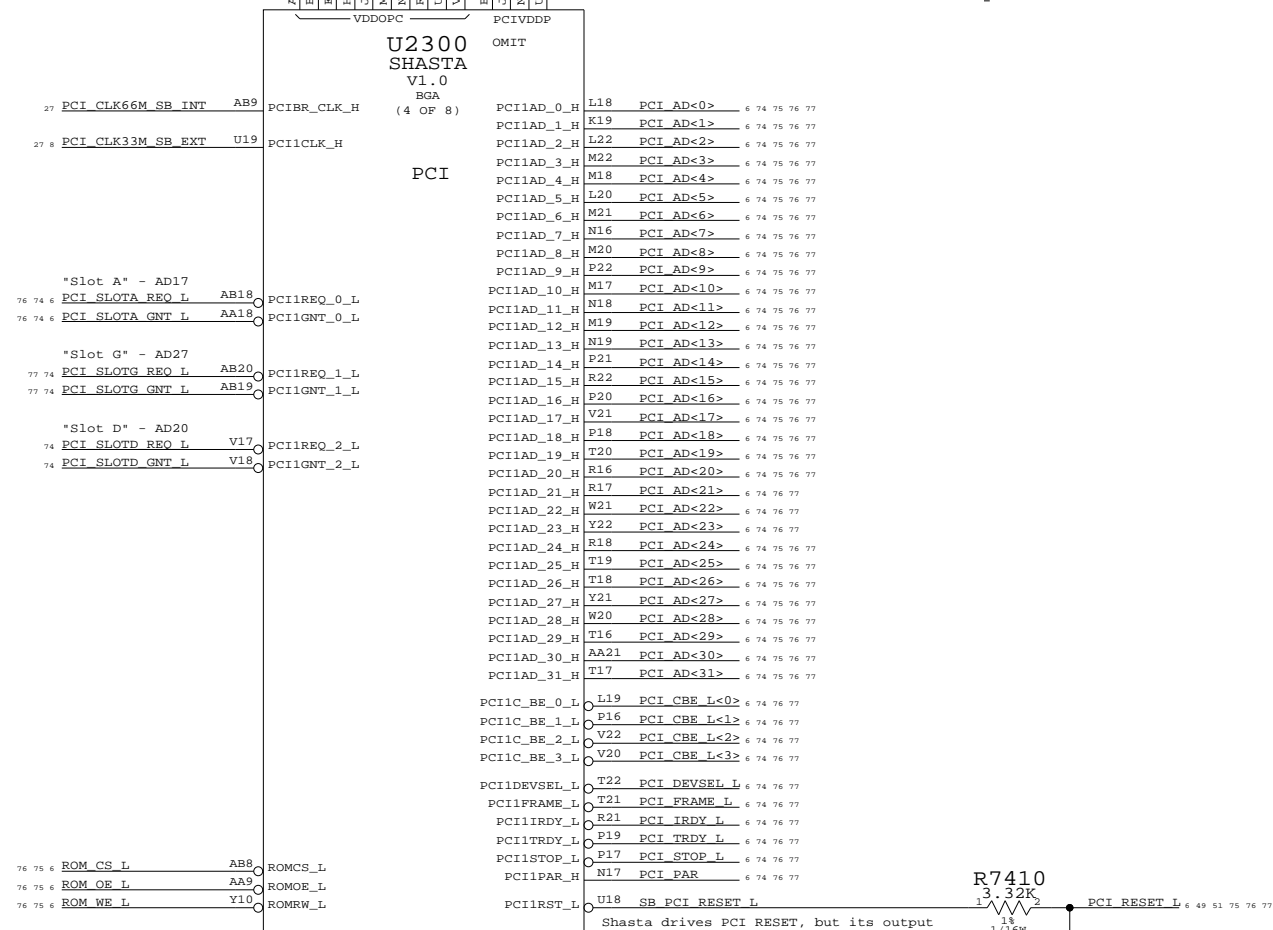
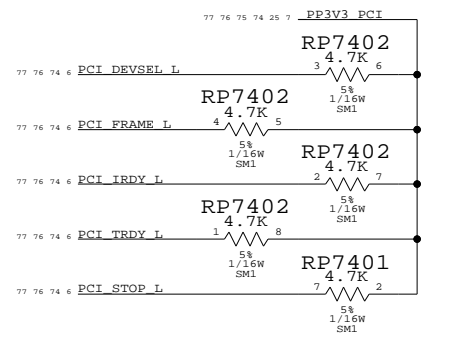
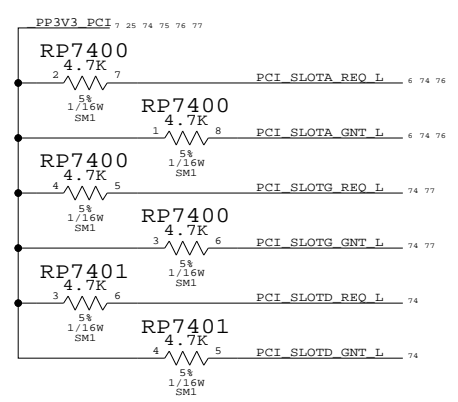
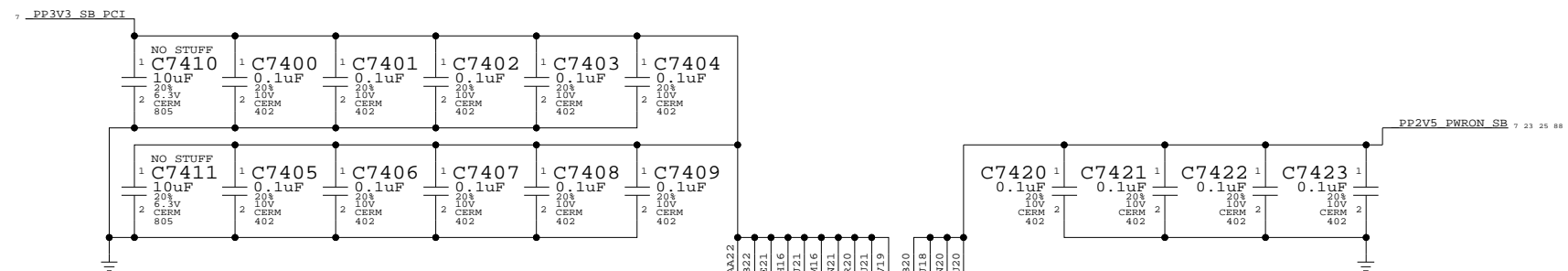
Page Notes

Power aliases required by this page:
 - _PP3V3_PCI
 - _PP3V3_SB_PCI (can be _PP3V3_PCI)
 - _PP2V5_PWRON_SB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD11 - PCI0 (0x106B/0x0053)
 AD11 - PCI1 (0x106B/0x0054)
 AD11 - PCI2 (0x106B/0x0055)
 AD23 - KeyLargo (0x106B/0x004F, PCI1)
 AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
 AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
 AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
 AD31 - Ethernet (0x106B/0x0051, PCI0)



Shasta PCI Interface

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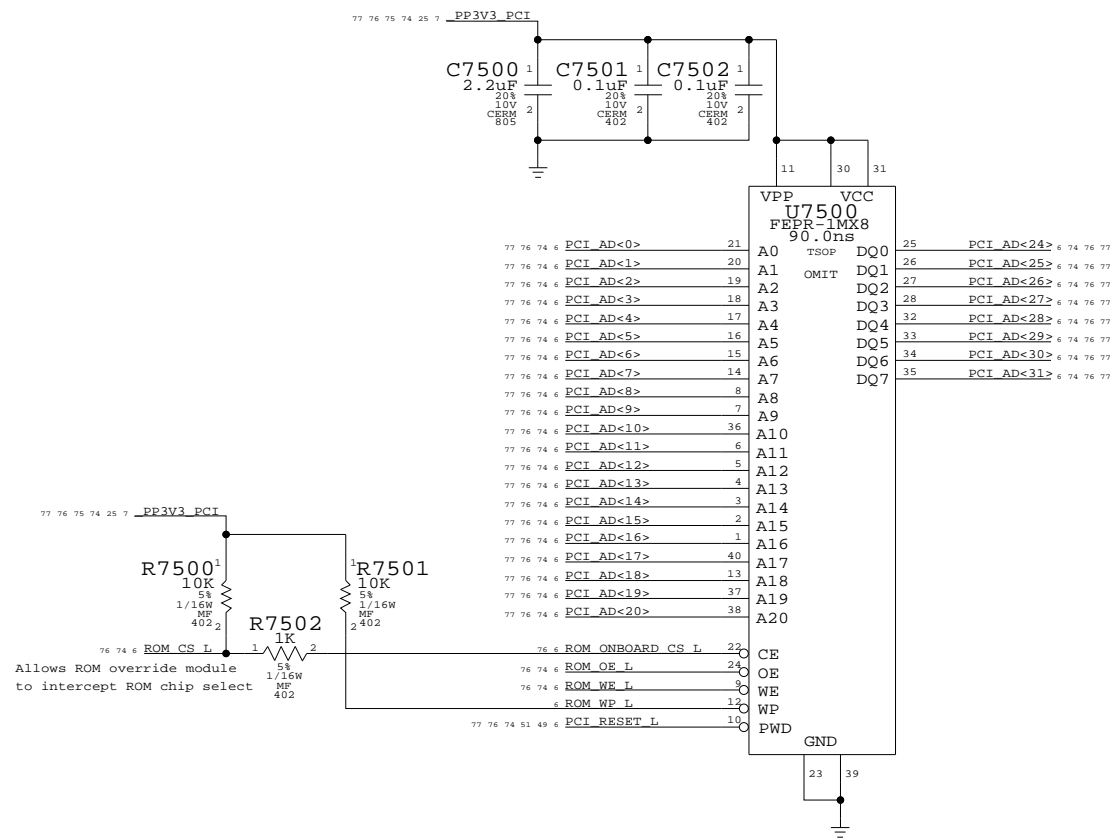
Page Notes

Power aliases required by this page:
 - _PP3V3_PCI

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



Master: Fizzy

BootROM

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DRAWING
 TITLE=FIZZY
 ABBREV=DRAWING
 LAST_MODIFIED=Fri Nov 21 11:24:32 2003

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	SHT		OF
NONE	75		99

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	PCI_CLK33M_AIRPORT

Page Notes

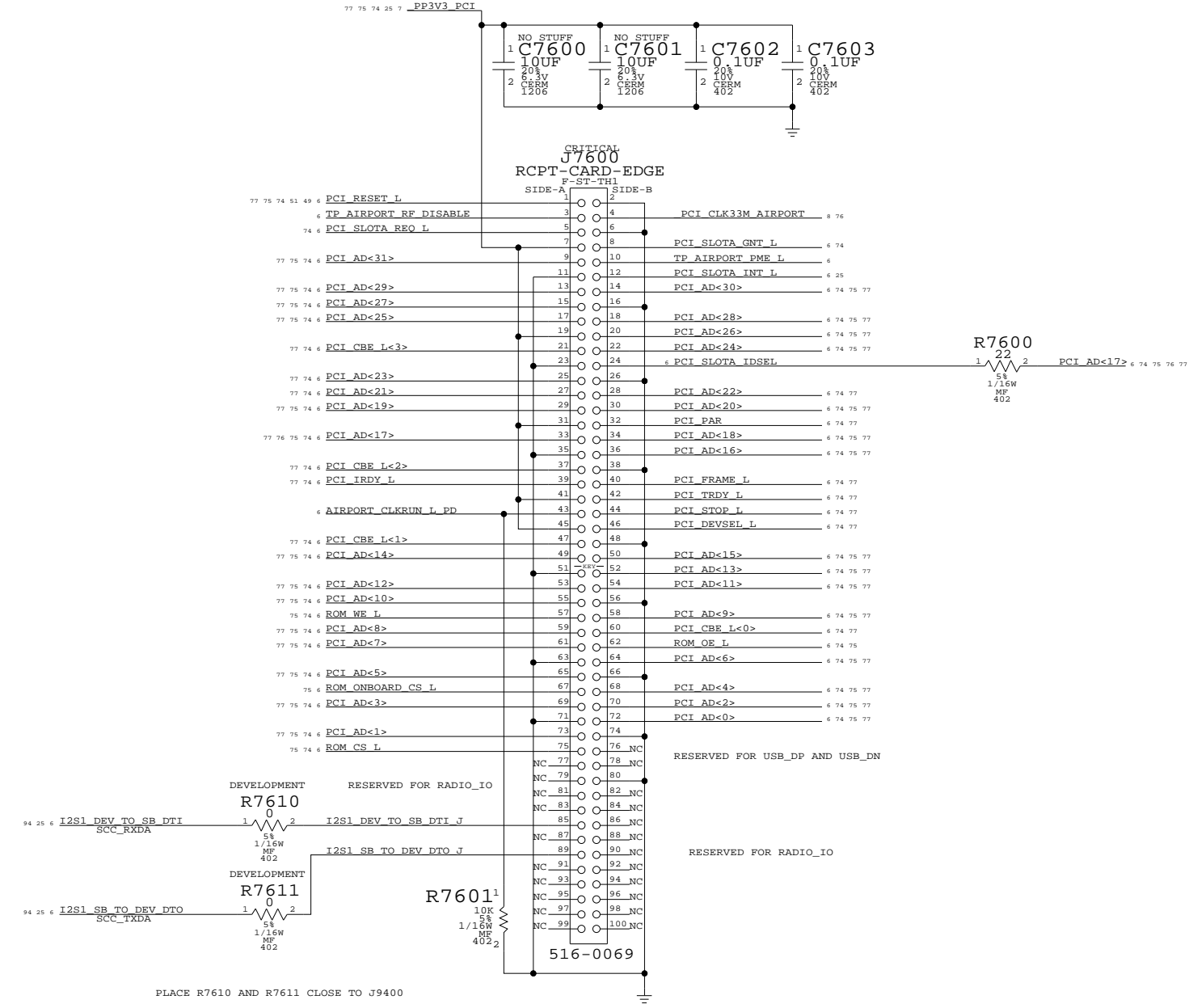
Power aliases required by this page:
 - _PP3V3_PCI

Signal aliases required by this page:
 - _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



AirPort Extreme

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	PCI_CLK33M_USB2

Page Notes

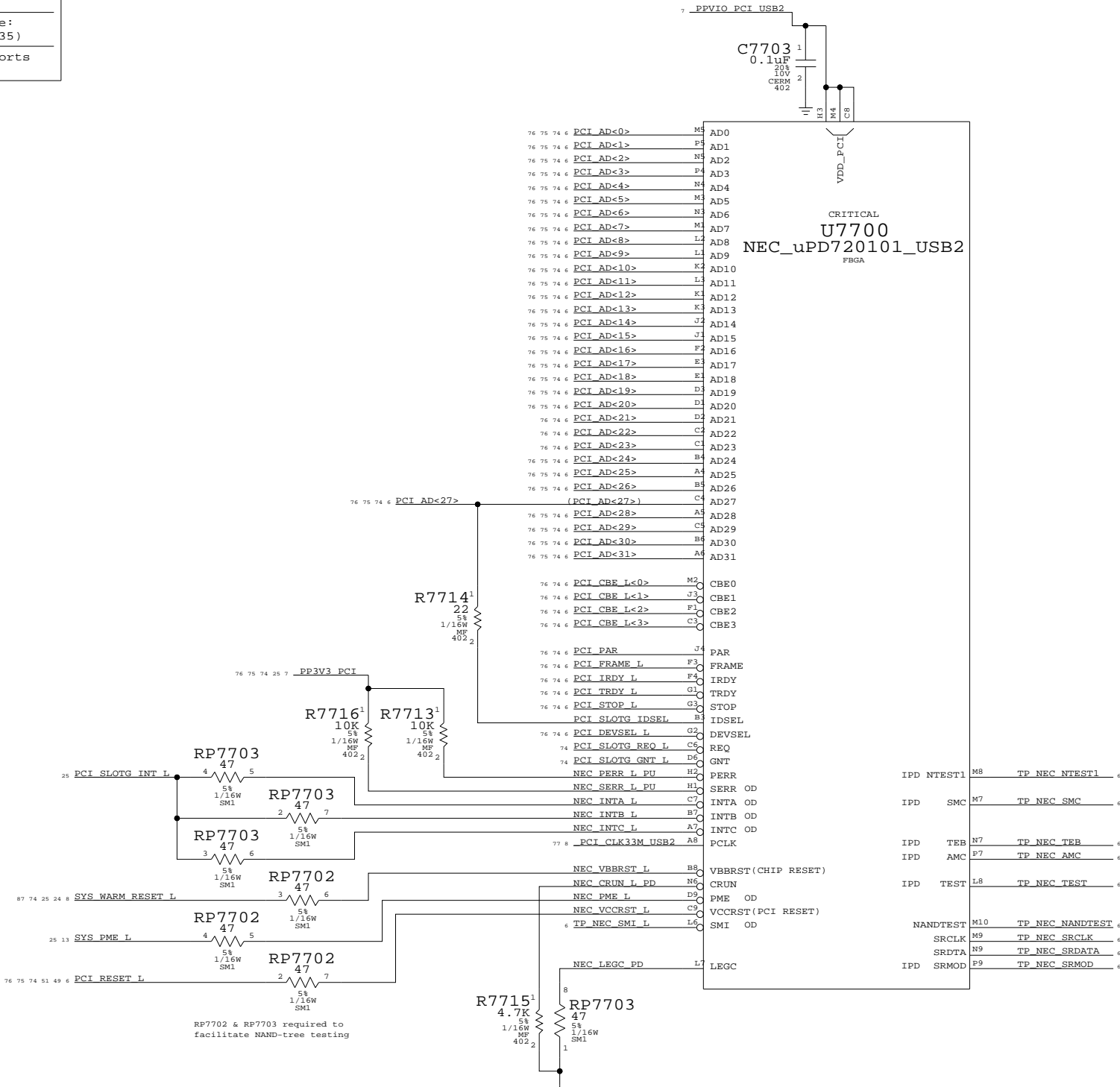
Power aliases required by this page:
 - _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
 - _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



RP7702 & RP7703 required to facilitate NAND-tree testing

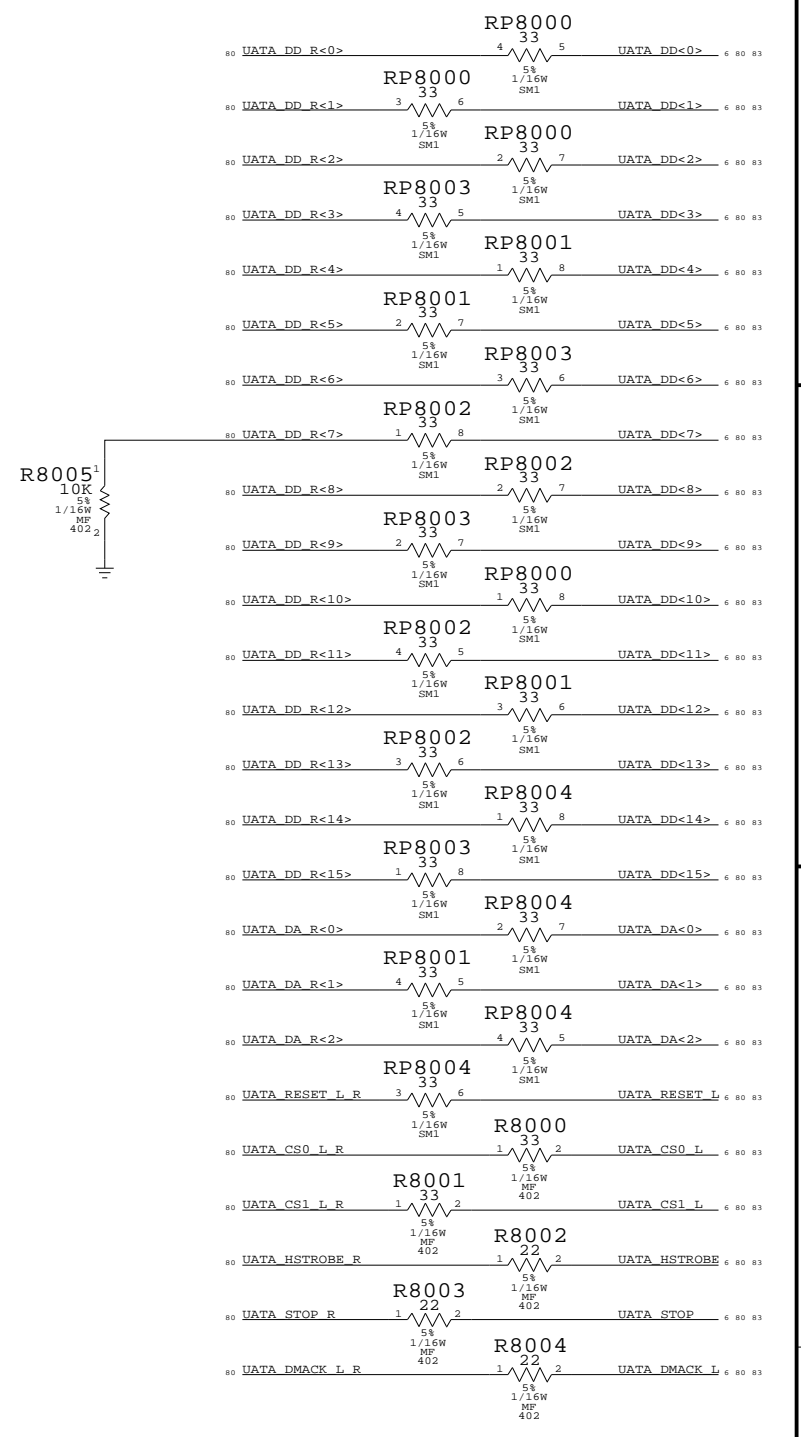
Master: Fizzy
USB 2.0 PCI Interface

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	NONE	SHT	77 OF 99

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD		UATA_DD<15..8>	
UATA_DD7		UATA_DD<7>	
UATA_DD		UATA_DD<6..0>	
UATA_HOST		UATA_DA<2..0>	
UATA_HOST		UATA_CS0_L	
UATA_HOST		UATA_CS1_L	
UATA_HOST		UATA_HSTROBE	
UATA_HOST		UATA_STOP	
UATA_HOST_R		UATA_DMACK_L	
UATA_HOST_R		UATA_RESET_L	
UATA_DEV_R_C		UATA_DSTROBE	
UATA_DEV_R		UATA_DMARQ	
UATA_DEV_R		UATA_INTRO	

UATA Termination



Page Notes

Power aliases required by this page:
 - _PPIV2_PWRON_DISK

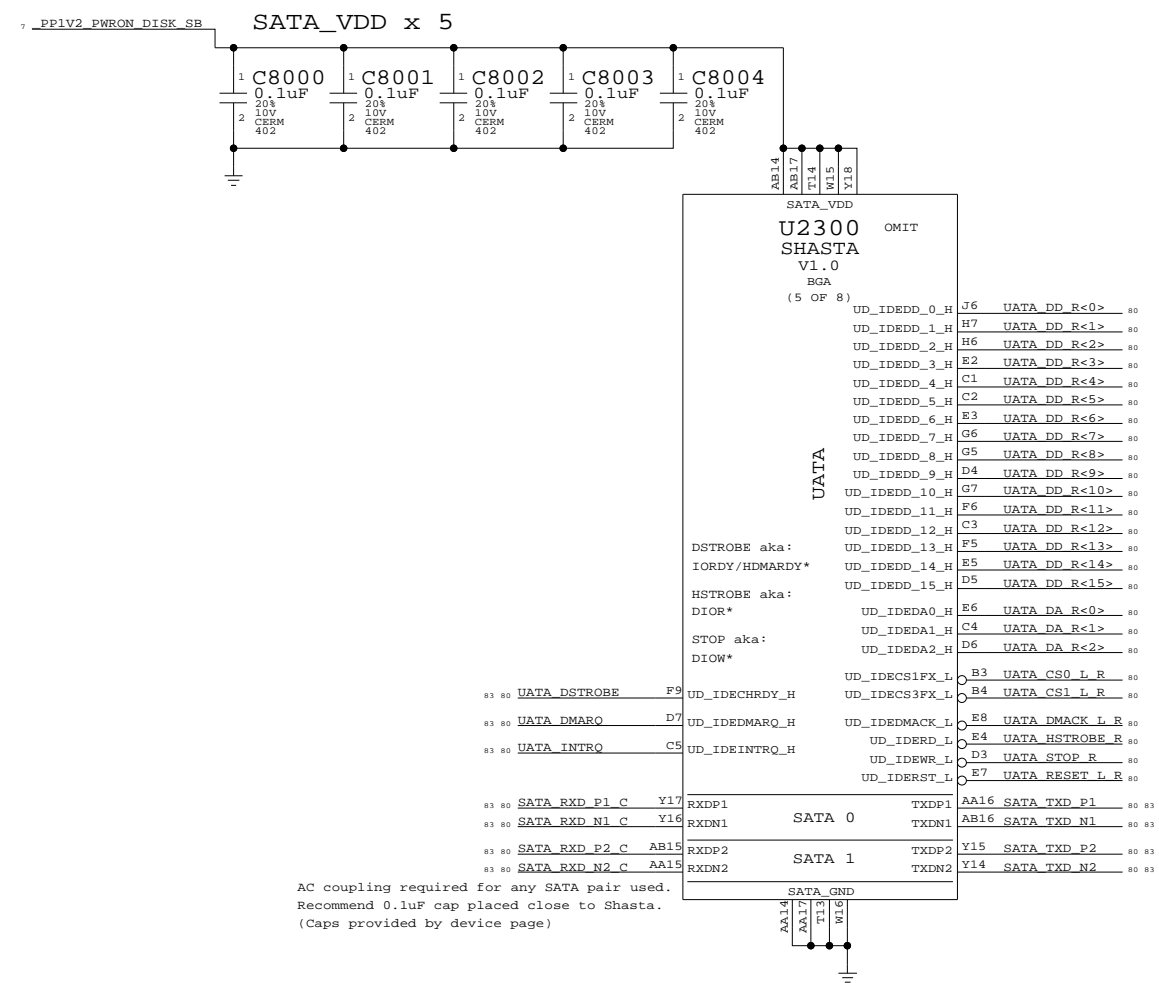
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Net Spacing Type: SATA

Line To Line: 15 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 10 mils outer
 Primary Max Sep: 9 mils inner
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.



AC coupling required for any SATA pair used.
 Recommend 0.1uF cap placed close to Shasta.
 (Caps provided by device page)

Master: Link

Shasta Disk

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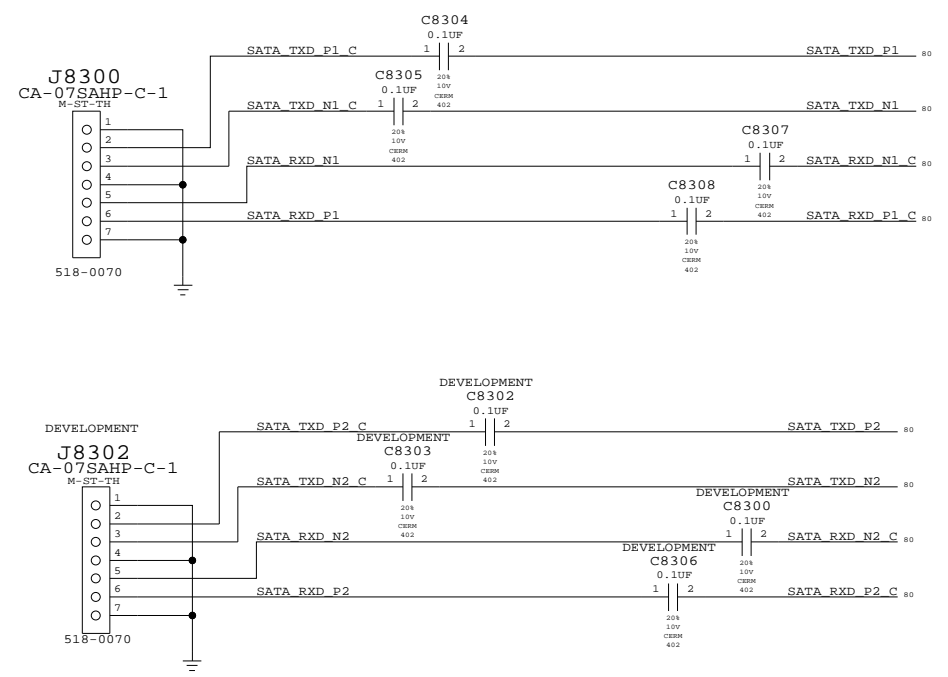
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

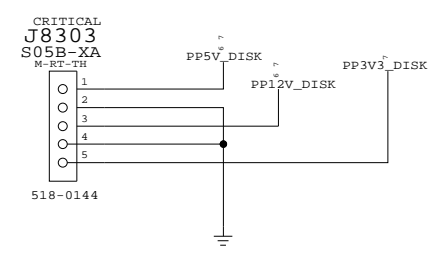
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	SHT		OF
NONE	80		99

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
83 80 6 UATA_DD<15..8>		UATA_DD		
83 80 6 UATA_DD<7>		UATA_DD7		
83 80 6 UATA_DD<6..0>		UATA_DD		
83 80 6 UATA_DA<2..0>		UATA_HOST		
83 80 6 UATA_CS0_L		UATA_HOST		
83 80 6 UATA_CS1_L		UATA_HOST		
83 80 6 UATA_HSTROBE		UATA_HOST		
83 80 6 UATA_STOP		UATA_HOST		
83 80 6 UATA_DMACK_L		UATA_HOST_R		
83 80 6 UATA_RESET_L		UATA_HOST_R		
83 80 6 UATA_DSTROBE		UATA_DEV_R_C		
83 80 6 UATA_DMARQ		UATA_DEV_R		
83 80 6 UATA_INTRO		UATA_DEV_R		

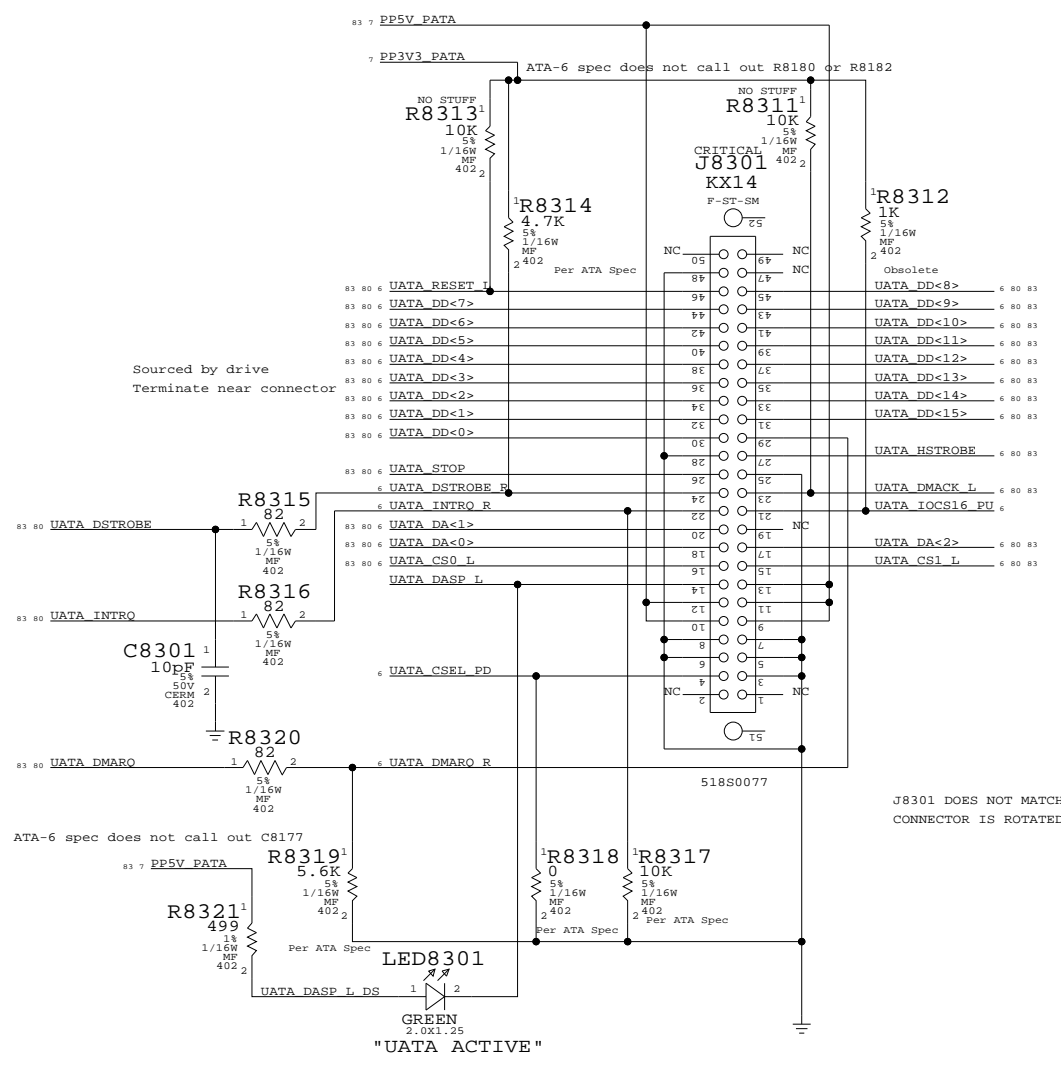
SATA CONNECTORS



HD POWER



PATA CONNECTOR



DISK CONNECTORS

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	D	051-6482	13
SCALE	NONE	SHT	OF
		83	99

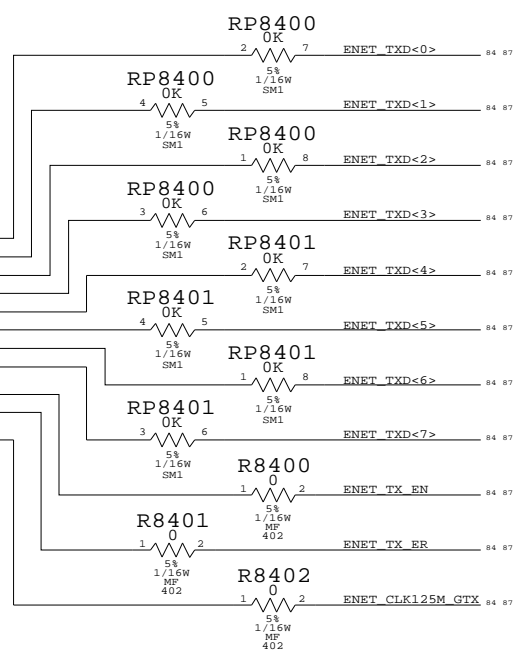
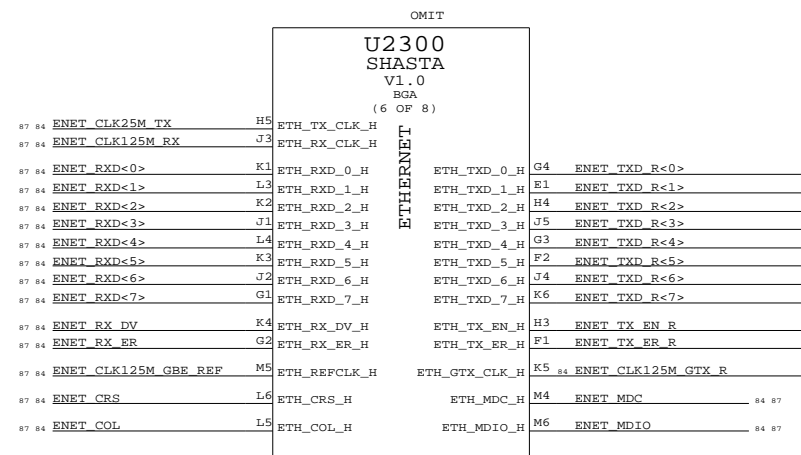
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_RX_CLK	10 MIL	ENET_CLK25M_TX
ENET_RX_CLK	10 MIL	ENET_CLK125M_RX
ENET_GBE_REF	15 MIL SPACING	ENET_CLK125M_GBE_REF
ENET_TX_CLK	15 MIL SPACING	ENET_CLK125M_GTX
	15 MIL SPACING	ENET_CLK125M_GTX_R
ENET_RX		ENET_RXD<7..0>
ENET_RX_CTL		ENET_RX_DV
ENET_RX_CTL		ENET_RX_ER
ENET_TX		ENET_TXD<7..0>
ENET_TX_CTL		ENET_TX_EN
ENET_TX_CTL		ENET_TX_ER
ENET_RX_CTL		ENET_CR_S
ENET_RX_CTL		ENET_COL
ENET_MDC		ENET_MDC
ENET_MDIO		ENET_MDIO

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Master: Link

Shasta Ethernet

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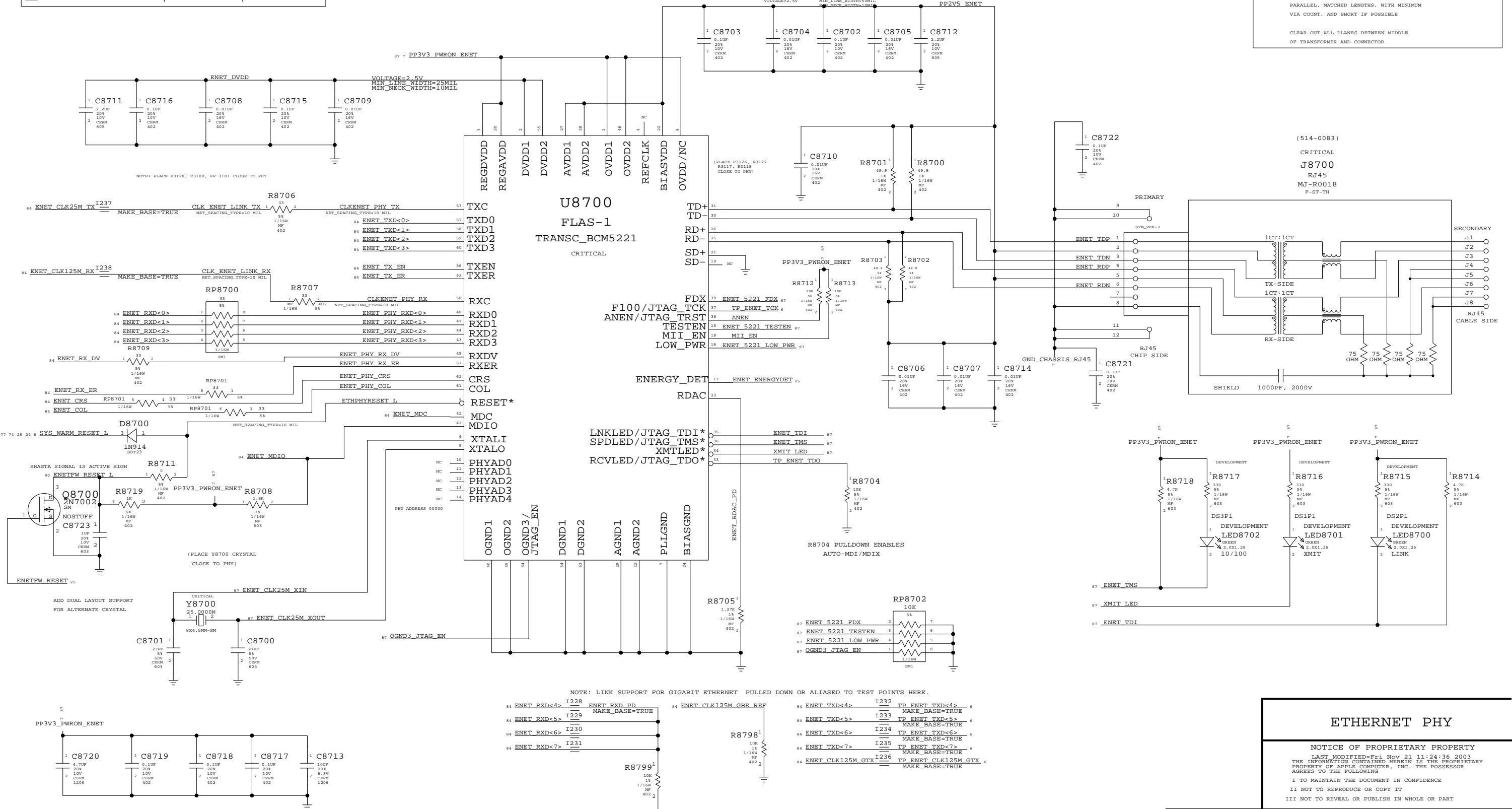
ETHERNET ROUTING PRIORITY:
 1. DECOUPLING CAPS
 2. TX TERMINATION - LOCATE NEAR PHY
 3. RX TERMINATION - LOCATE NEAR PHY

ROUTE TD OVER 2.5V PLANE (BOTTOM LAYER) ONLY
 ROUTE RD OVER GROUND PLANE (TOP LAYER) ONLY

ALL DIFFERENTIAL SIGNALS SHOULD BE CLOSE,
 PARALLEL, MATCHED LENGTHS, WITH MINIMUM
 VIA COUNT, AND SHORT IF POSSIBLE

CLEAR OUT ALL PLANES BETWEEN MIDDLE
 OF TRANSFORMER AND CONNECTOR

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDP_87
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDN_87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDP_87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDN_87
ENET_XTAL	15 MIL SPACING		ENET_CLK25M_XIN_87
	15 MIL SPACING		ENET_CLK25M_XOUT_87



ETHERNET PHY

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KEEP ALL CAPS CLOSE TO TRANSCIVER ON THIS PAGE

NOTE: LINK SUPPORT FOR GIGABIT ETHERNET PULLED DOWN OR ALIASED TO TEST POINTS HERE.

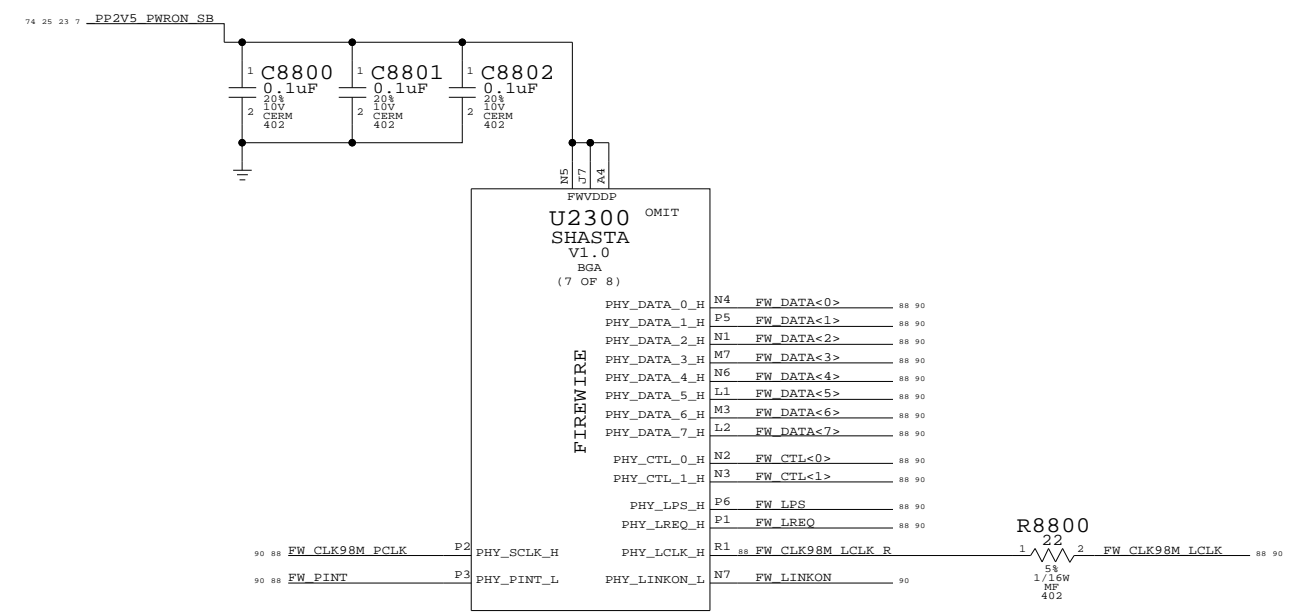
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW		FW_DATA<7..0>
FW		FW_CTL<1..0>
FW_LPS		FW_LPS
FW_LREQ		FW_LREQ
FW_PINT		FW_PINT
FW_LCLK	15 MIL SPACING	FW_CLK98M_LCLK
FW_PCLK	15 MIL SPACING	FW_CLK98M_PCLK
	15 MIL SPACING	FW_CLK98M_LCLK_R

Page Notes

Power aliases required by this page:
 - _PP2V5_PWRON_SB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



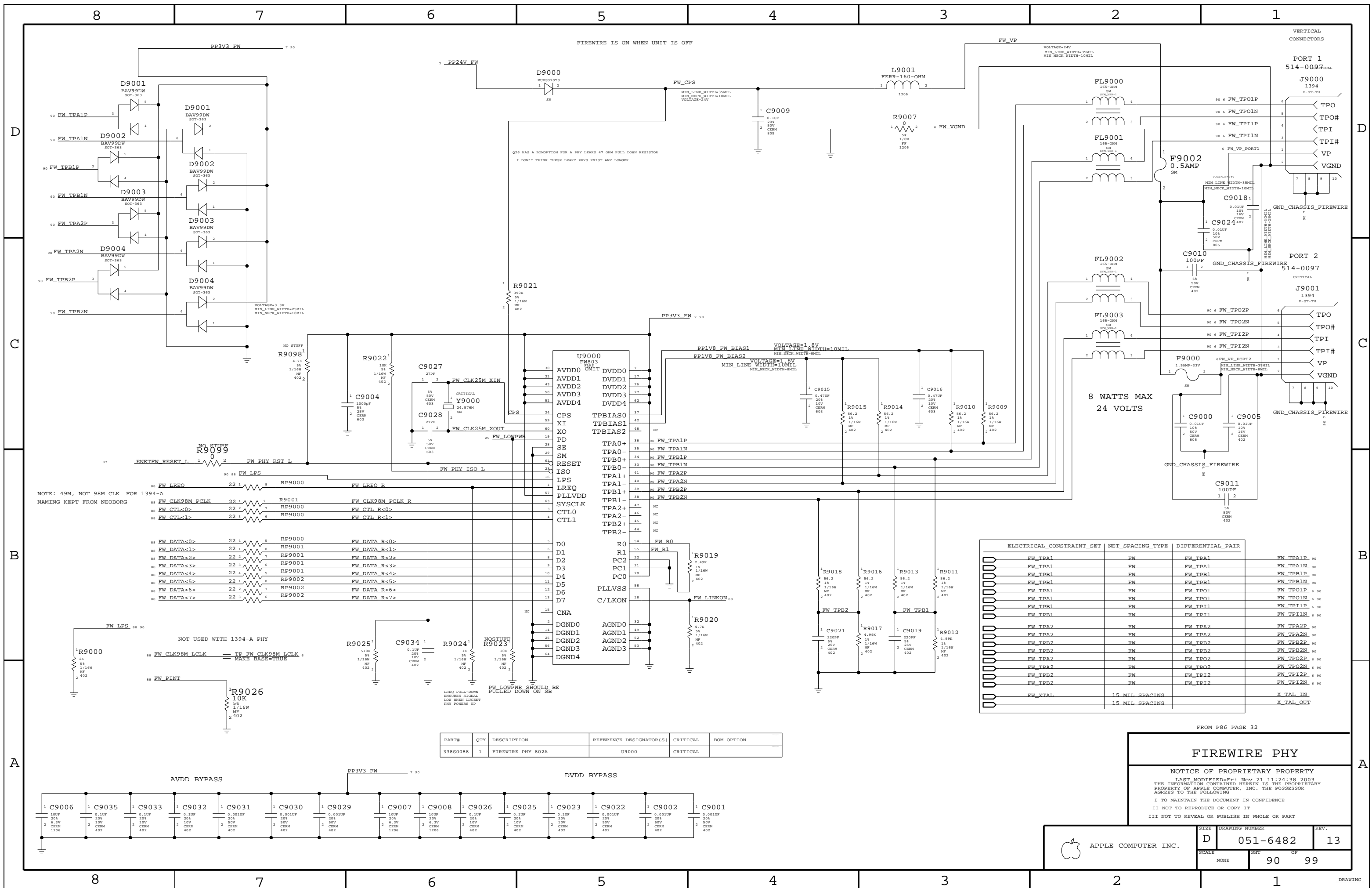
Master: Link

Shasta FireWire

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_DRAWING
 TITLE=FIZZY
 ABBREV=DRAWING
 LAST_MODIFIED=Fri Nov 21 11:24:36 2003

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE		SHT	OF
NONE		88	99



NOTE: 49M, NOT 98M CLK FOR 1394-A NAMING KEPT FROM NEOBORG

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW_TPA1	FW	FW_TPA1
FW_TPA1	FW	FW_TPA1
FW_TPB1	FW	FW_TPB1
FW_TPB1	FW	FW_TPB1
FW_TPA1	FW	FW_TPA1
FW_TPB1	FW	FW_TPB1
FW_TPA1	FW	FW_TPA1
FW_TPB1	FW	FW_TPB1
FW_TPA2	FW	FW_TPA2
FW_TPA2	FW	FW_TPA2
FW_TPB2	FW	FW_TPB2
FW_TPB2	FW	FW_TPB2
FW_TPA2	FW	FW_TPA2
FW_TPB2	FW	FW_TPB2
FW_TPA1	15 MIL SPACING	X TAL IN
FW_TPA1	15 MIL SPACING	X TAL OUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0088	1	FIREWIRE PHY 802A	U9000	CRITICAL	

FROM P86 PAGE 32

FIREWIRE PHY

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APPLE COMPUTER INC.

SCALE: NONE

DRAWING NUMBER: **D 051-6482**

SHEET: 90 OF 99

REV: 13

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2_0	USB2 P<0>
USB2_0	USB2	USB2_0	USB2 N<0>
USB2_1	USB2	USB2_1	USB2 P<1>
USB2_1	USB2	USB2_1	USB2 N<1>
USB2_2	USB2	USB2_2	USB2 P<2>
USB2_2	USB2	USB2_2	USB2 N<2>
USB2_3	USB2	USB2_3	USB2 P<3>
USB2_3	USB2	USB2_3	USB2 N<3>
USB2_4	USB2	USB2_4	USB2 P<4>
USB2_4	USB2	USB2_4	USB2 N<4>
USB2_NEC_XTAL	15 MIL SPACING		NEC_CLK30M_XT1
	15 MIL SPACING		NEC_CLK30M_XT2
	15 MIL SPACING		NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
 - _PP3V3_PWRON_USB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

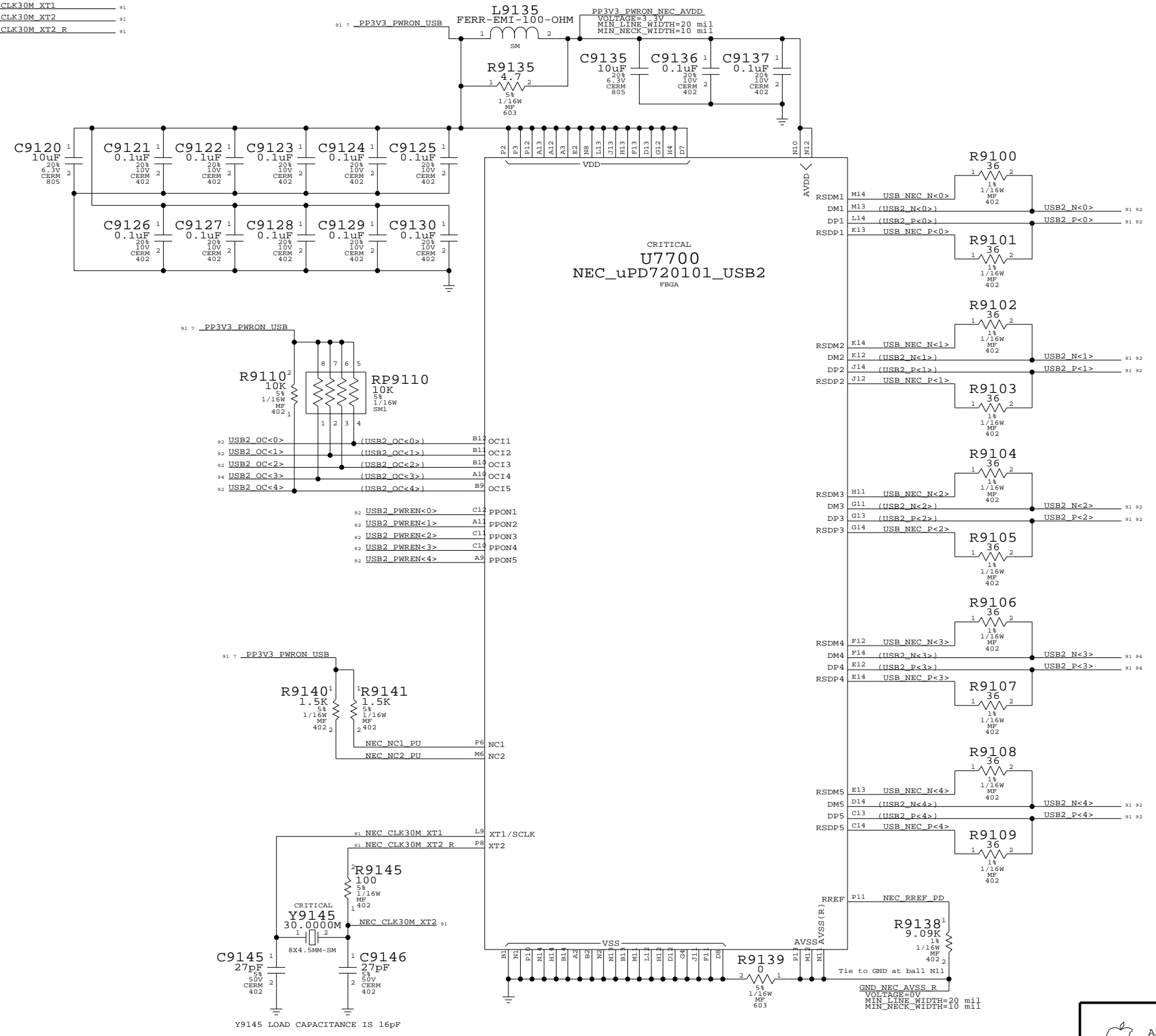
Net Spacing Type: USB2

Line To Line: 19.5 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300 SHASTA
 V1.0
 BGA
 (8 OF 8)
 OMIT

NC0	P7	TP_SB_NC_P7
NC1	P8	TP_SB_NC_P8
NC2	R3	TP_SB_NC_R3
NC3	R4	TP_SB_NC_R4
NC4	R5	TP_SB_NC_R5
NC5	R6	TP_SB_NC_R6
NC6	R7	TP_SB_NC_R7
NC7	R8	TP_SB_NC_R8
NC8	T1	TP_SB_NC_T1
NC9	T2	TP_SB_NC_T2
NC10	T3	TP_SB_NC_T3
NC11	T4	TP_SB_NC_T4
NC12	T5	TP_SB_NC_T5
NC13	T6	TP_SB_NC_T6
NC14	T7	TP_SB_NC_T7
NC15	T8	TP_SB_NC_T8
NC16	U1	TP_SB_NC_U1
NC17	U2	TP_SB_NC_U2
NC18	U3	TP_SB_NC_U3
NC19	U4	TP_SB_NC_U4
NC20	U5	TP_SB_NC_U5
NC21	U6	TP_SB_NC_U6
NC22	V1	TP_SB_NC_V1
NC23	V2	TP_SB_NC_V2
NC24	V3	TP_SB_NC_V3
NC25	V4	TP_SB_NC_V4
NC26	W1	TP_SB_NC_W1
NC27	W3	TP_SB_NC_W3
NC28	Y1	TP_SB_NC_Y1
NC29	Y3	TP_SB_NC_Y3



Master: Fizzy

USB Host Interfaces

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PROVIDED	USB2	USB2_PORT1_F
BY	USB2	USB2_PORT1_F
USB	USB2	USB2_PORT2_F
CONTROLLER	USB2	USB2_PORT2_F
	USB2	USB2_PORT3_F
	USB2	USB2_PORT3_F

Page Notes

Power aliases required by this page:
 - _PP5V_PWRON_USB
 - _PP5V_PWRON_UDASH
 - _PP3V3_PWRON_UDASH
 - _PP3V3_PWRON_BT

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

91 USB2_PWREN<0> <ALIAS> TP_USB2_PWREN<0> MAKE_BASE=TRUE

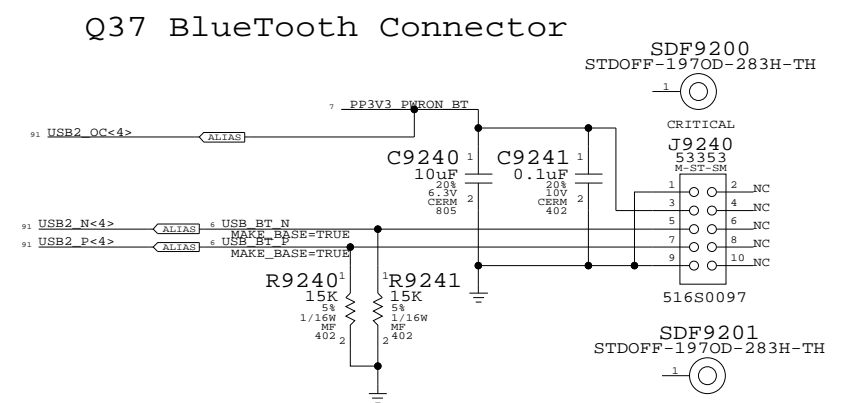
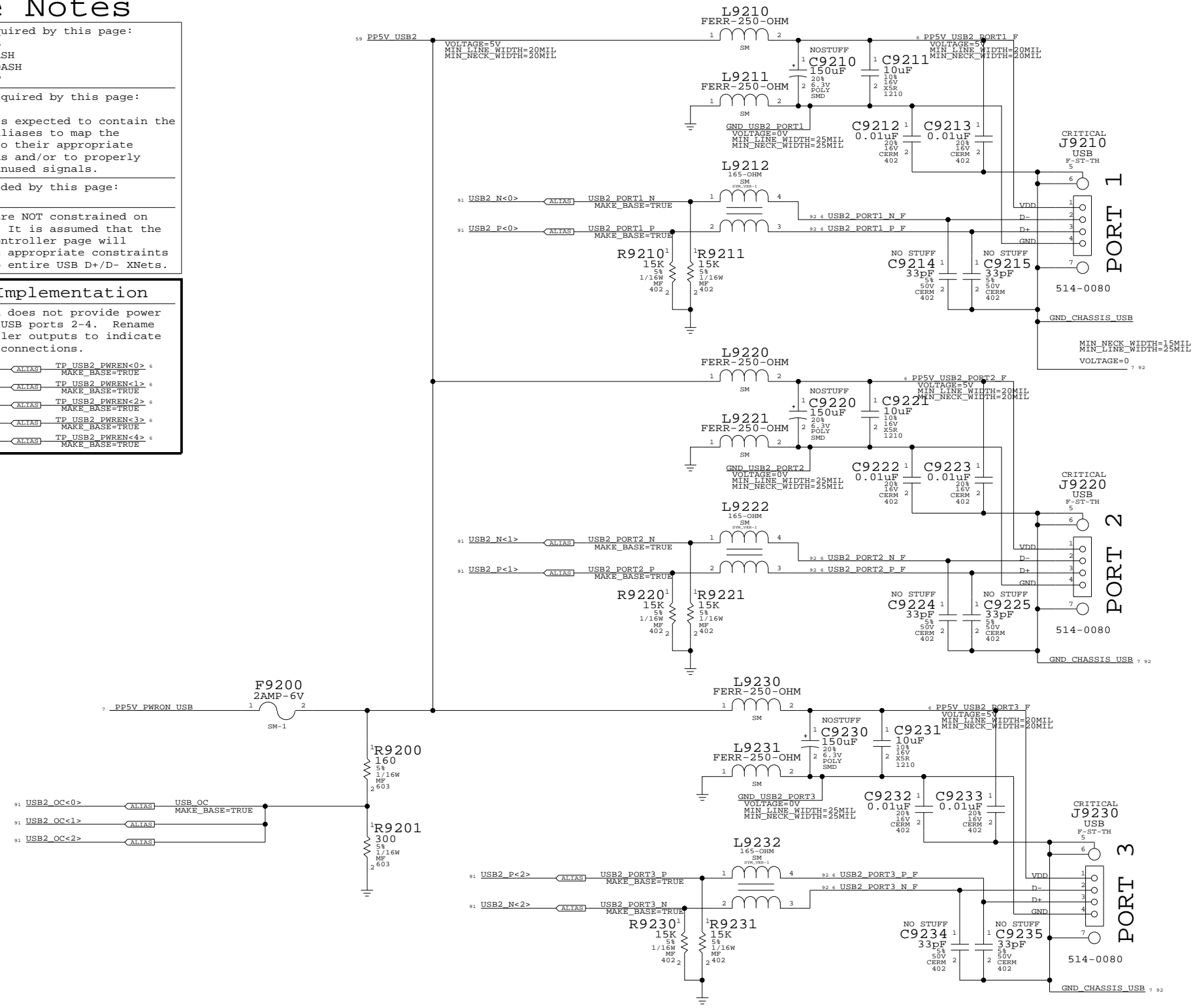
91 USB2_PWREN<1> <ALIAS> TP_USB2_PWREN<1> MAKE_BASE=TRUE

91 USB2_PWREN<2> <ALIAS> TP_USB2_PWREN<2> MAKE_BASE=TRUE

91 USB2_PWREN<3> <ALIAS> TP_USB2_PWREN<3> MAKE_BASE=TRUE

91 USB2_PWREN<4> <ALIAS> TP_USB2_PWREN<4> MAKE_BASE=TRUE

External USB Ports



USB Device Interfaces

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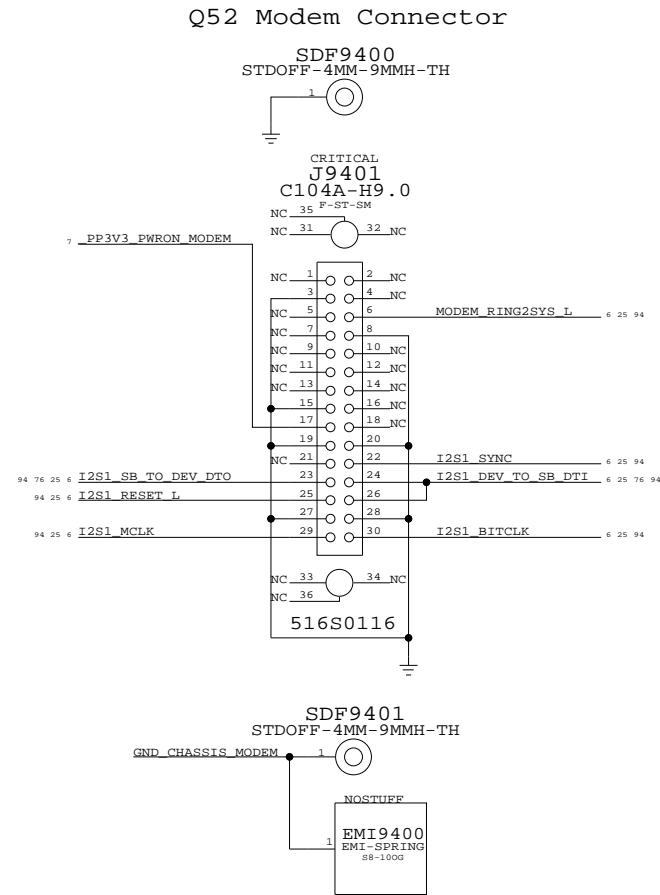
Page Notes

Power aliases required by this page:
 - _PP3V3_PWRON_MODEM
 Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

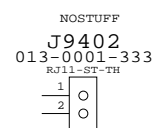
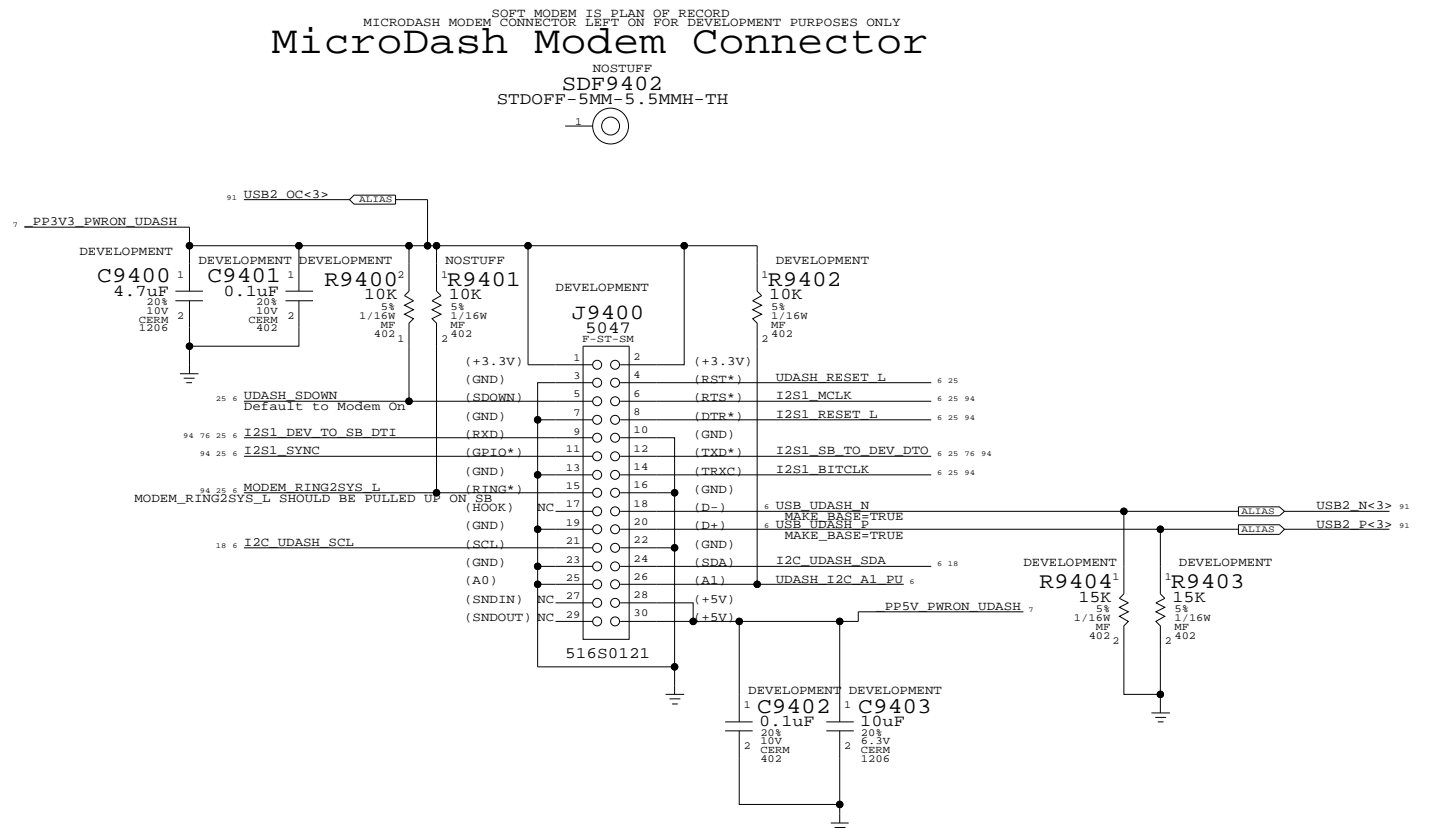
NEED TO PICK A MODEM TO STUFF FOR EVT
 AND THE CORRESPONDING STANDOFF



From Intel Mobile Audio/Modem
 Daughter Card Specification
 Rev 1.0, February 22, 1999

- | | |
|----------------------|---------------------|
| 1 - MONO_OUT/PC_BEEP | 2 - AUDIO_PWRON |
| 3 - GND | 4 - MONO_PHONE |
| 5 - AUX_A_RIGHT | 6 - RESERVED |
| 7 - AUX_A_LEFT | 8 - GND |
| 9 - CD_GND | 10 - 5Vmain |
| 11 - CD_RIGHT | 12 - RESERVED |
| 13 - CD_LEFT | 14 - RESERVED |
| 15 - GND | 16 - PRIMARY_DN |
| 17 - 3.3Vaux | 18 - 5Vd |
| 19 - GND | 20 - GND |
| 21 - 3.3Vmain | 22 - AC97_SYNC |
| 23 - AC97_SDATA_OUT | 24 - AC97_SDATA_INB |
| 25 - AC97_RESET# | 26 - AC97_SDATA_INA |
| 27 - GND | 28 - GND |
| 29 - AC97_MSTRCLK | 30 - AC97_BITCLK |

MicroDash Modem Connector



Modem Interface

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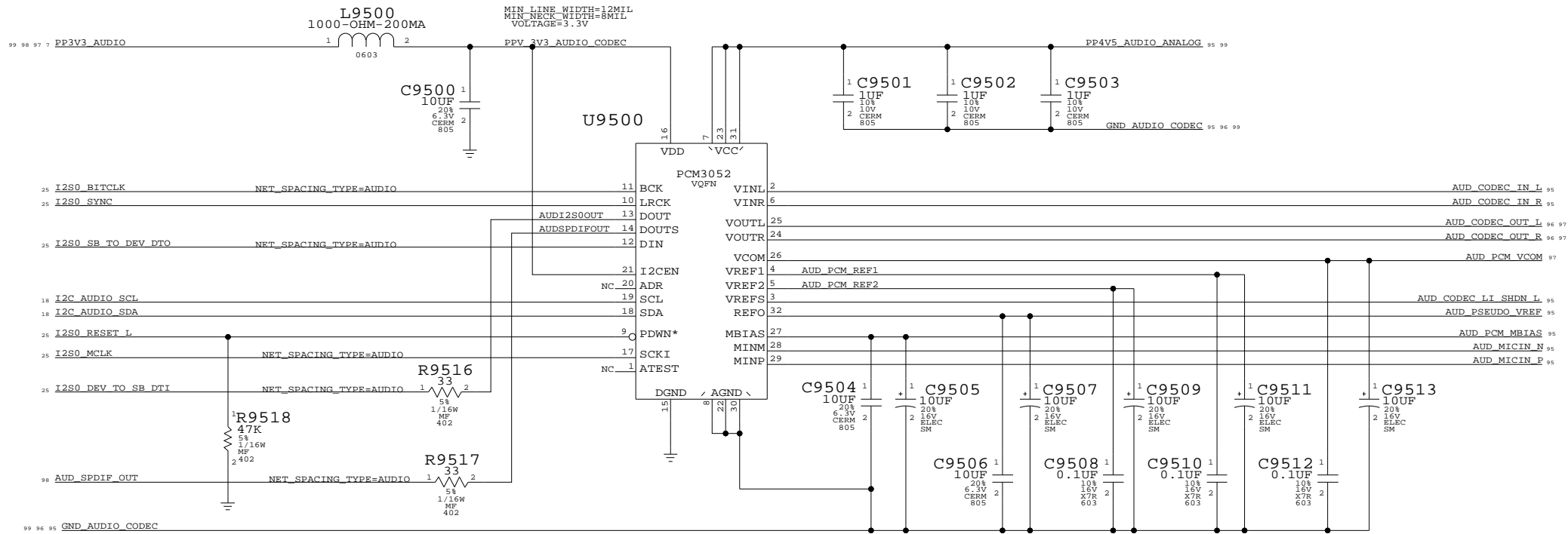
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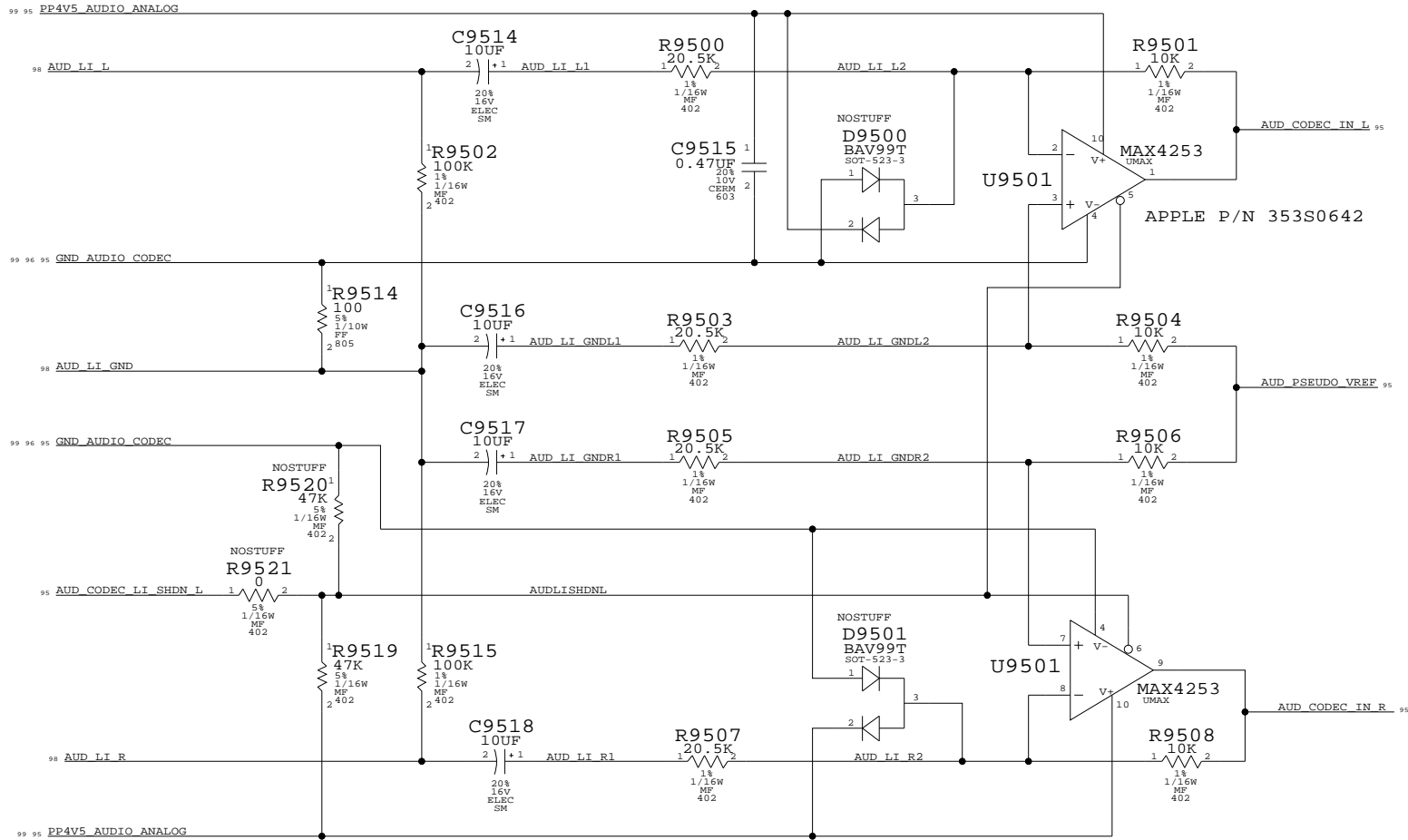
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	SHT	OF	
NONE	94	99	

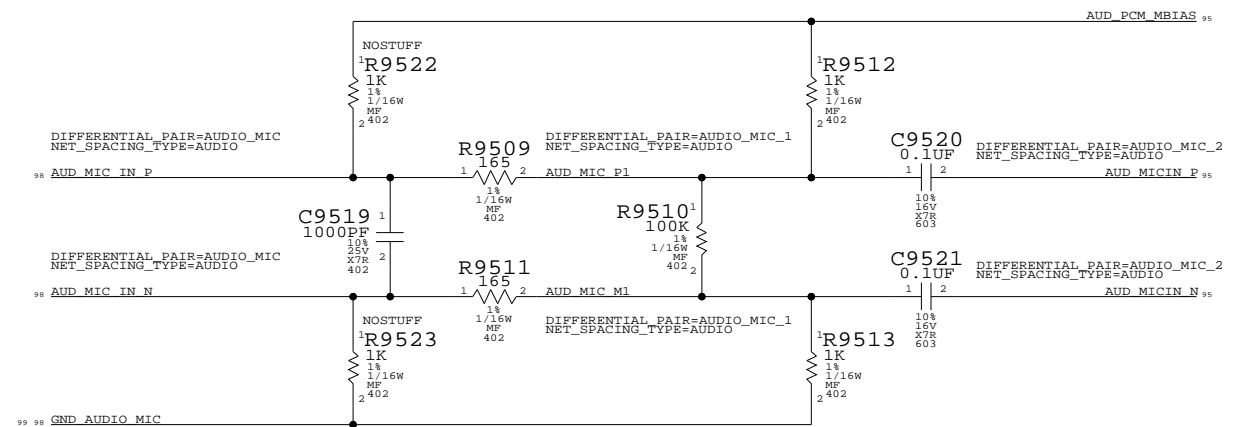
AUDIO CODEC
APPLE P/N 353S0655



LINE IN PSEUDO-DIFFERENTIAL AMP
AV = 0.49



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: CODEC, LINE INPUT

NOTICE OF PROPRIETARY PROPERTY

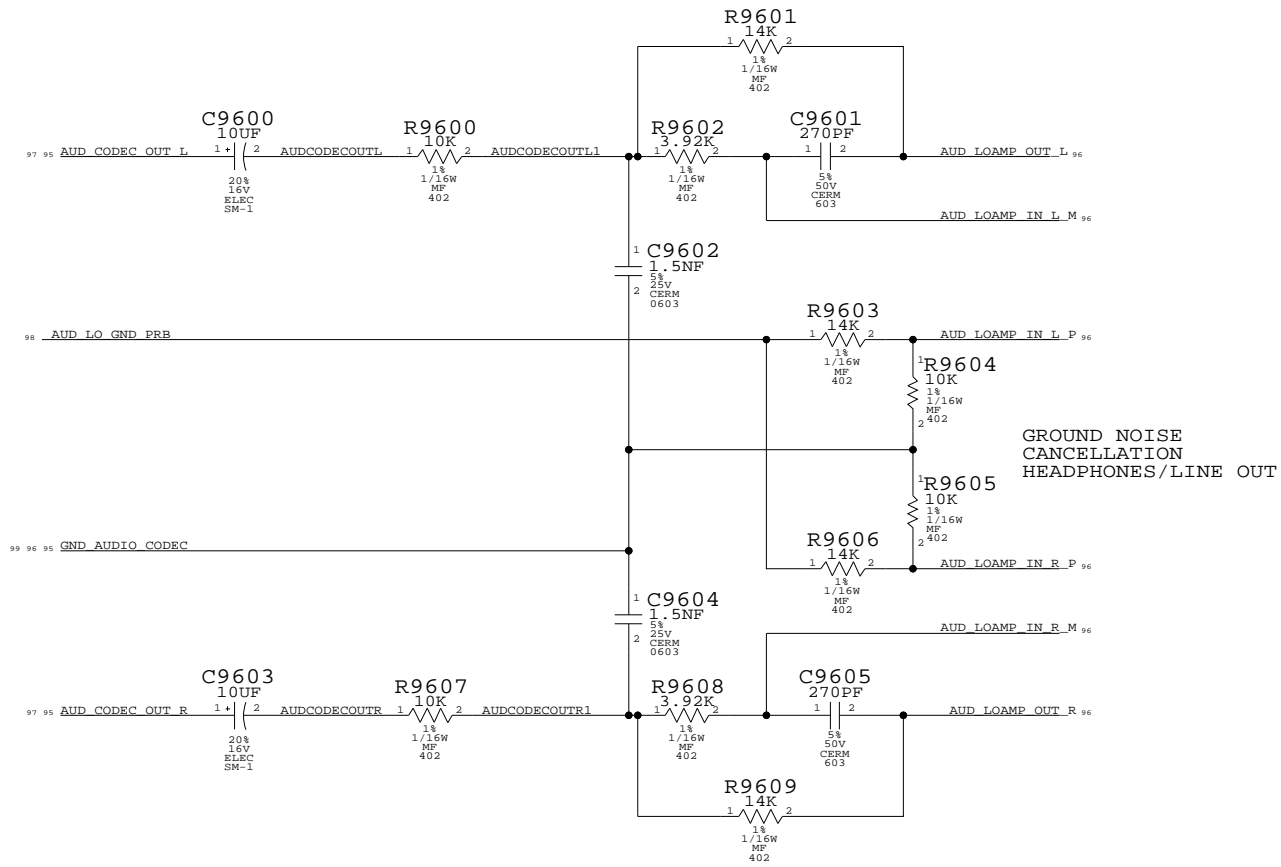
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	NONE	SHT	OF
		95	99

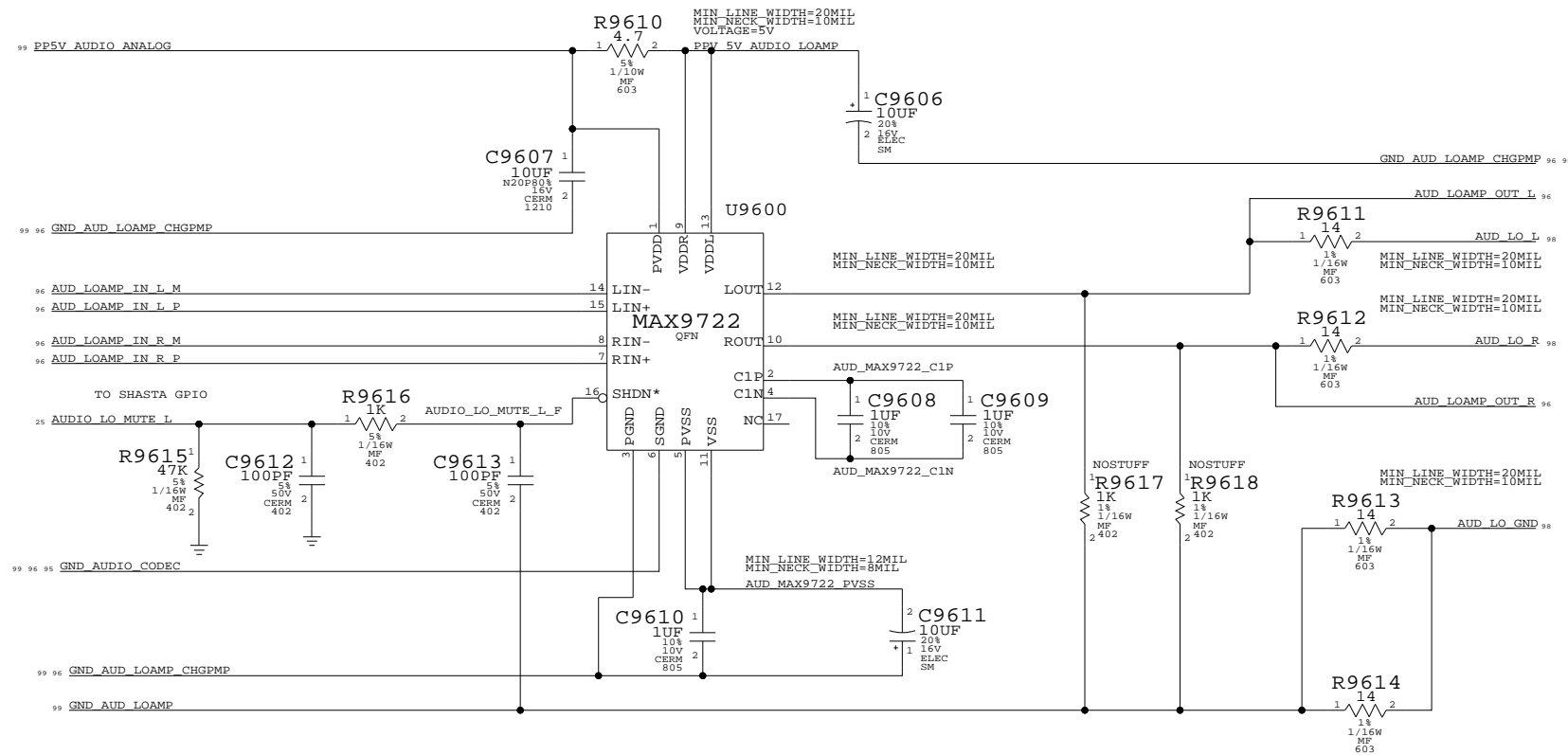
CODEC OUTPUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



HEADPHONES/LINE OUT AMP

APPLE P/N 353S0697



AUDIO:HEADPHONES / LINE OUT

NOTICE OF PROPRIETARY PROPERTY

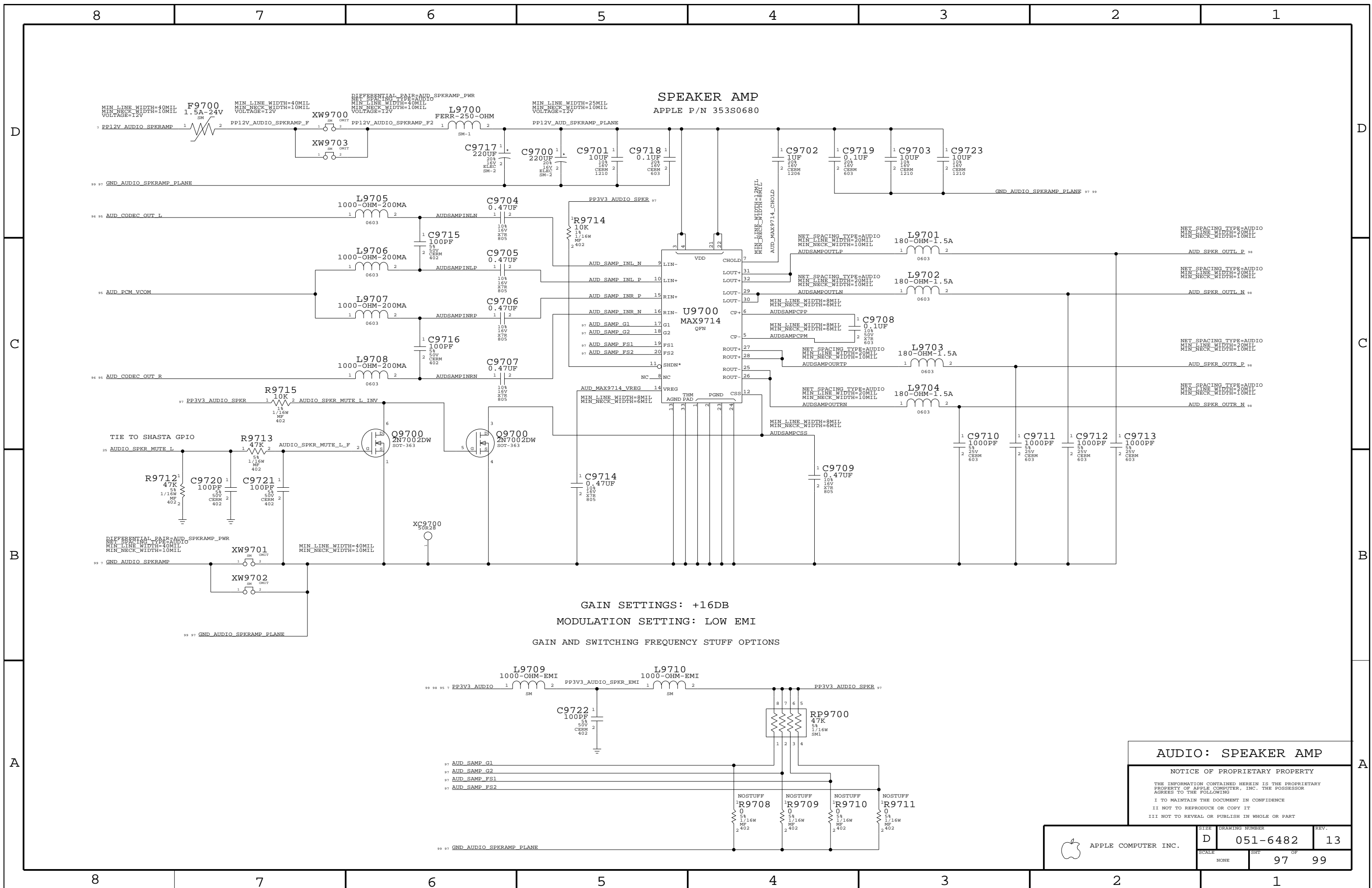
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	SHT	OF	
NONE	96	99	



SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +16DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP

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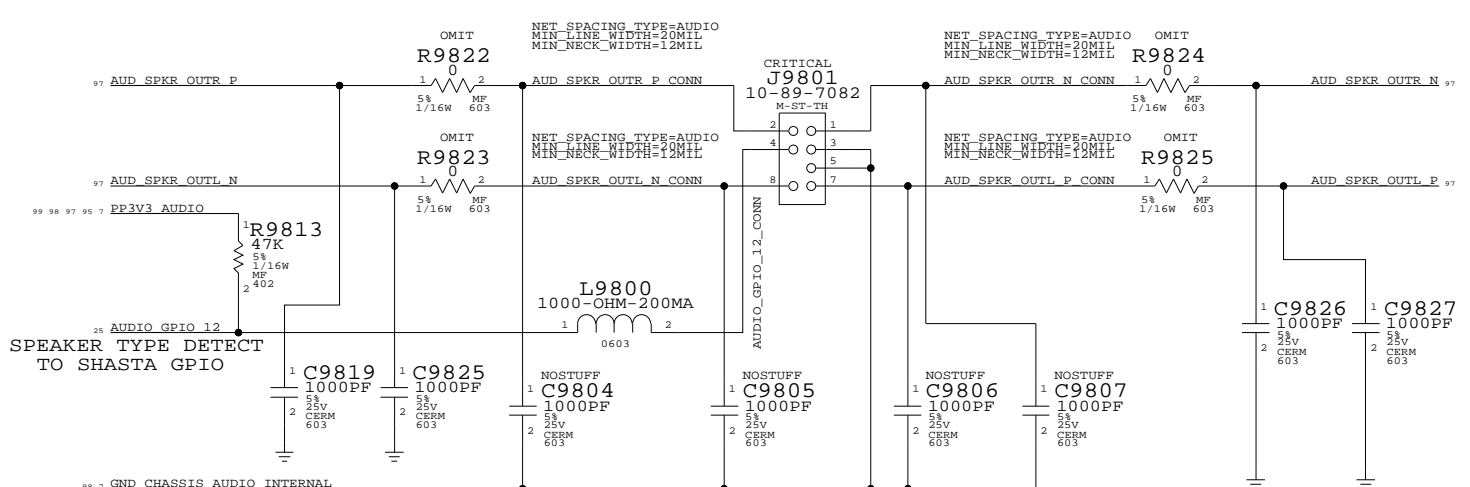
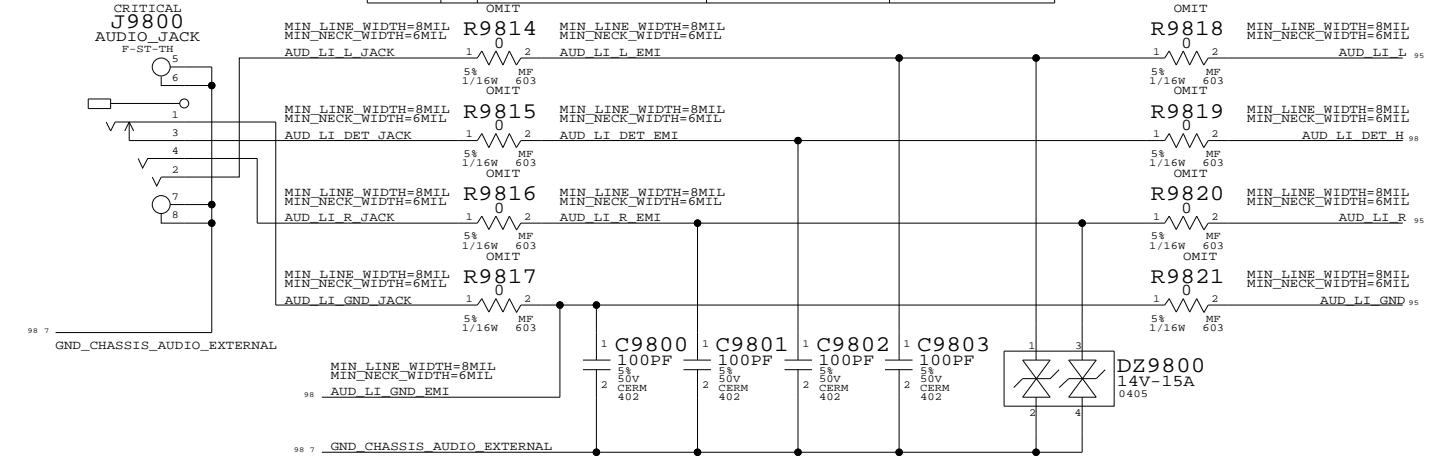
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	13
SCALE	NONE	SHT	OF
		97	99

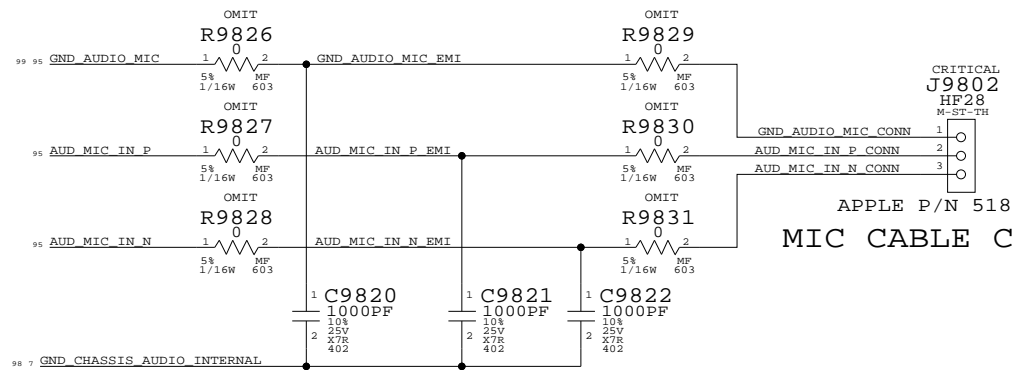
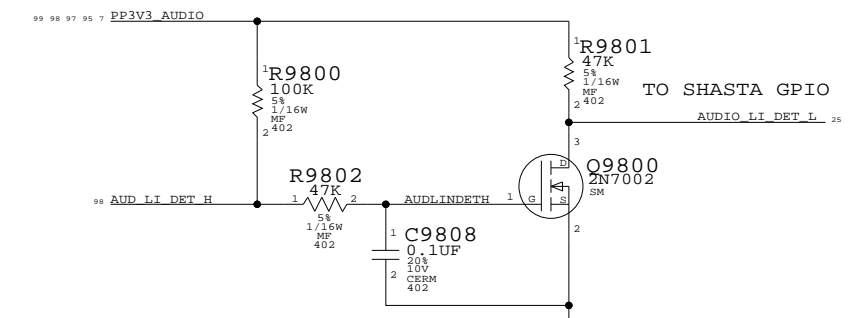
LINE IN JACK
APPLE P/N 514-0098

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0169	5	FLTR,EMI,FERR BD,180 OHM,1.5A	R9822,R9823,R9824,R9825	R9837
155S0093	31	FLTR,EMI,FERR BD,100 OHM,0.603	R9814,R9815,R9816,R9817,R9818,R9819,R9820,R9821,R9826,R9827,R9828,R9829,R9830,R9831,R9843,R9844,R9832,R9833,R9834,R9835,R9836,R9845,R9846,R9838,R9839,R9840,R9841,R9842,R9810,R9848,R9849	

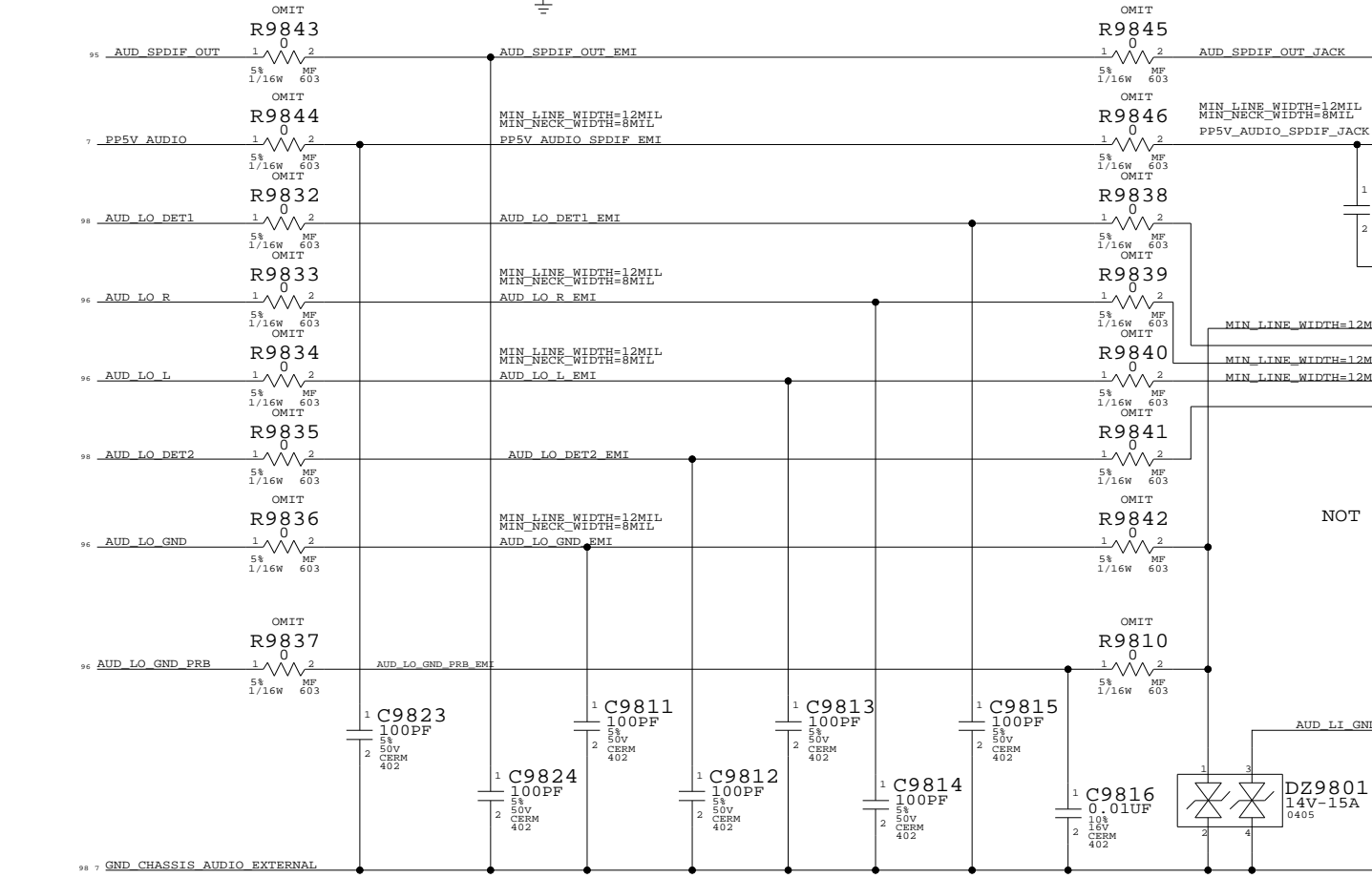
SPEAKER CABLE CONNECTOR
APPLE P/N 518-0138



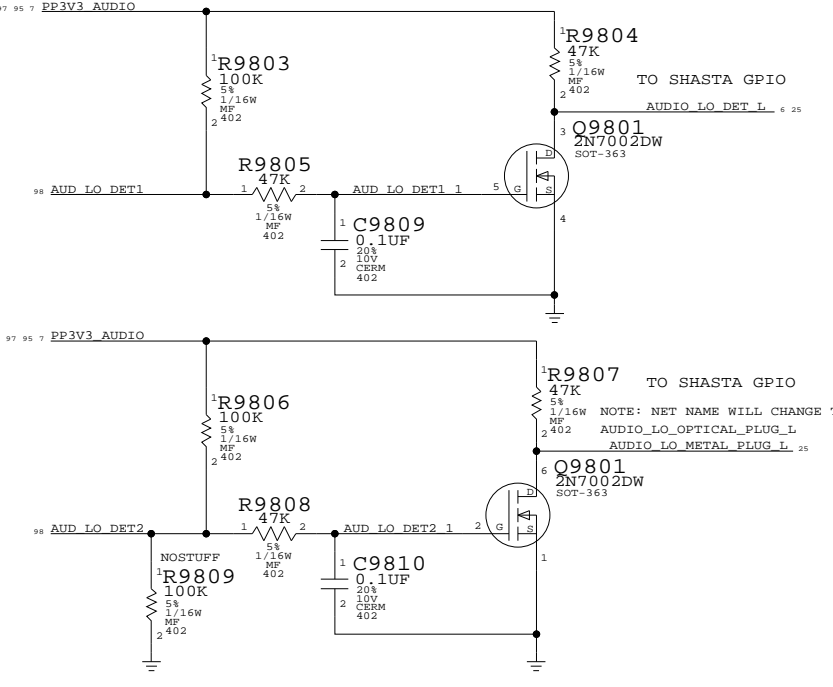
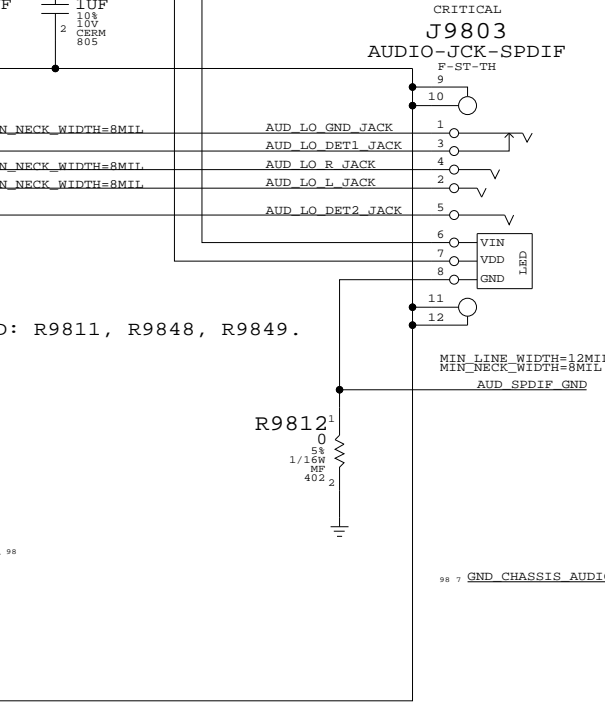
LINE IN PLUG DETECT
AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED



LINE OUT PLUG DETECTS
AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED
AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED



LINE OUT JACK
APPLE P/N 514-0116



AUDIO: Q45 CONNECTORS

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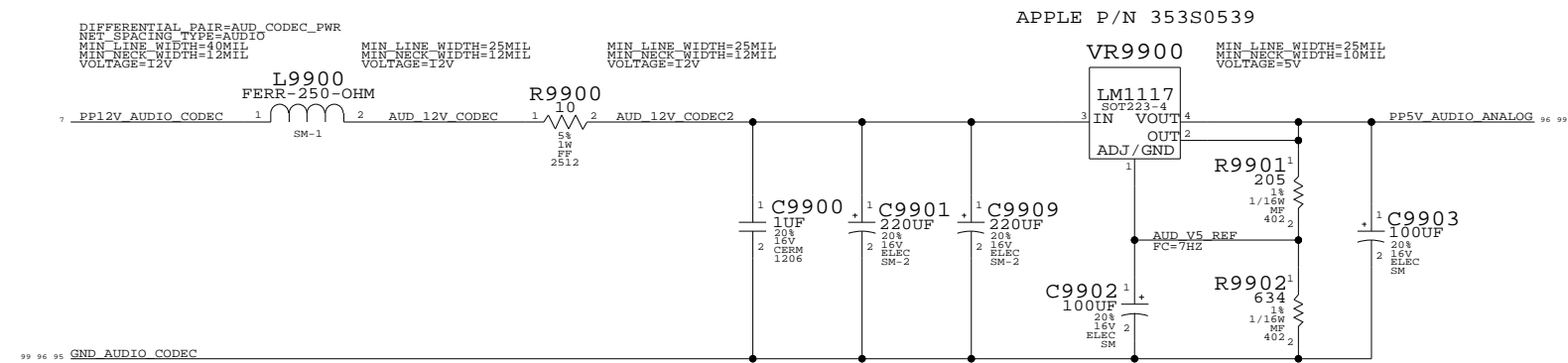
APPLE COMPUTER INC.	SCALE	DATE	REV.
	NONE	98 09 99	13

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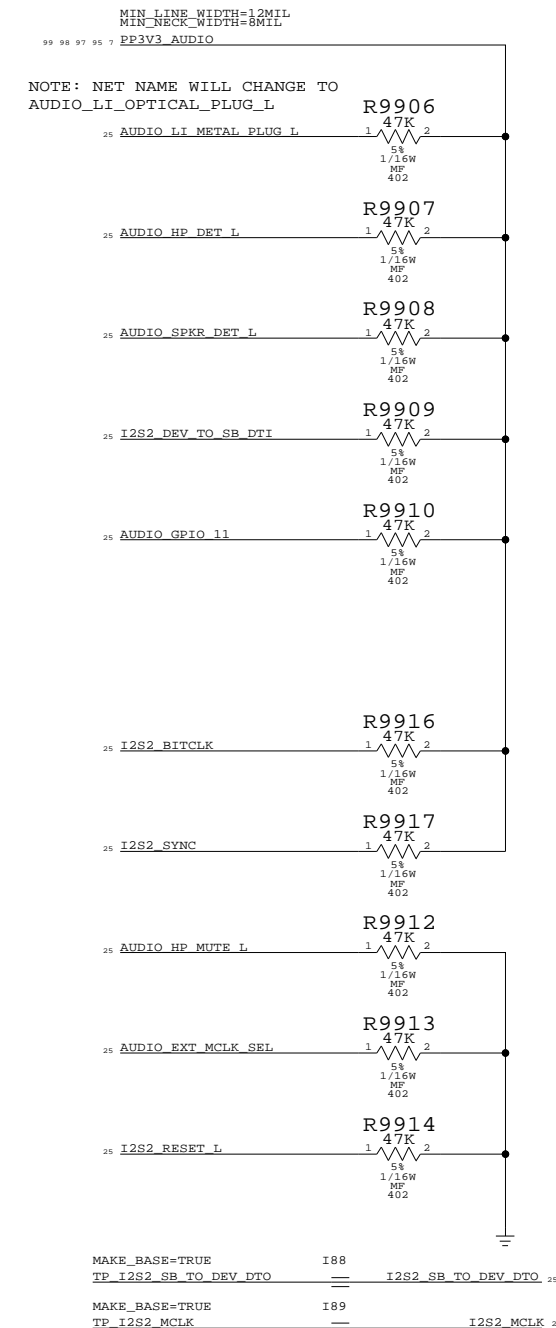
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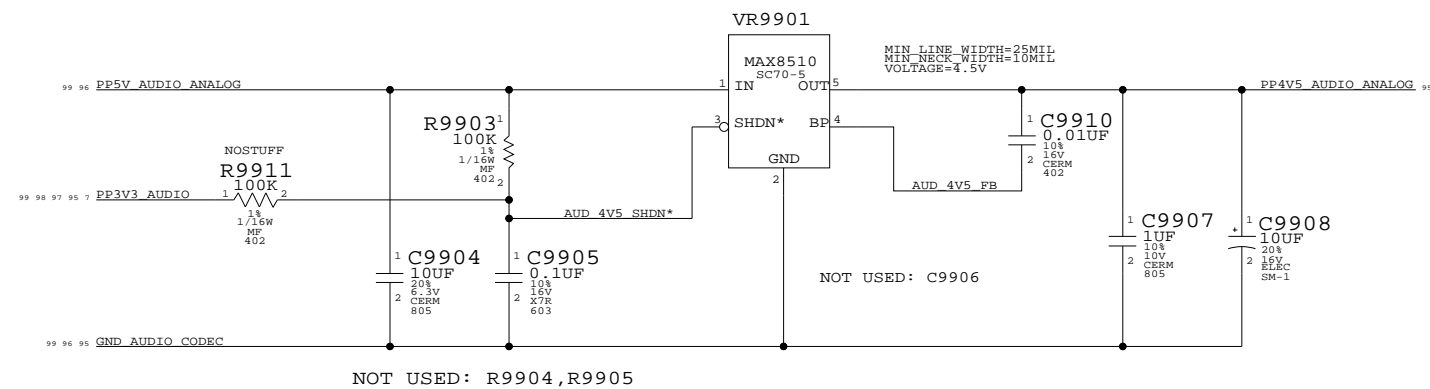
5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP



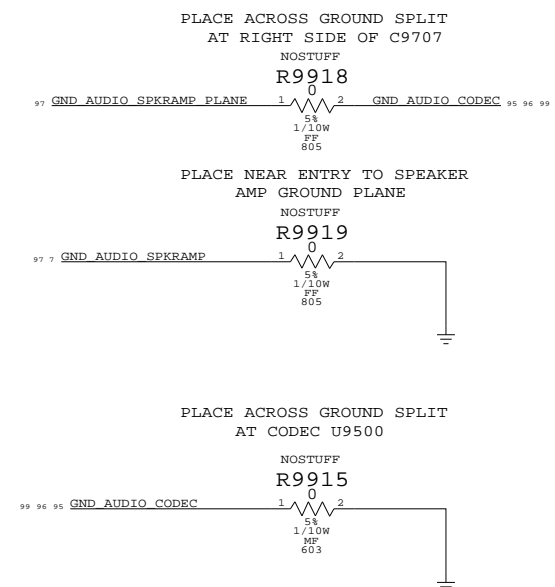
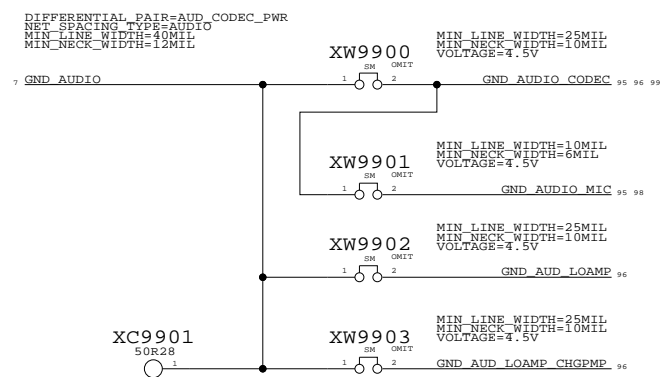
UNUSED GPIO TERMINATIONS



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP



AUDIO GROUND RETURNS



AUDIO: Q45 POWER SUPPLIES

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