

OKI

OKI SEMICONDUCTOR

お客様各位

資料中の「沖電気」、「OKI」等名称の OKI セミコンダクタ株式会社への変更について

2008年10月1日を以って沖電気工業株式会社の半導体事業は OKI セミコンダクタ株式会社に承継されました。従いまして、本資料中には「沖電気工業株式会社」、「沖電気」、「OKI」といった表記が残っておりますが、これらの表記は全て「OKI セミコンダクタ株式会社」に変更されておりますのでご理解の程お願い致します。なお、会社名、会社商標・ロゴ等以外の内容については変更しておりませんので資料としての内容変更ではありません。

Datasheet.Directory

2008年10月1日
OKI セミコンダクタ株式会社

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OKI Semiconductor

FEDR27T3202F-02-04

Issue Date: Jul. 9, 2004

MR27T3202F

2M-Word × 16-Bit or 4M-Word × 8-Bit **P2ROM**

FEATURES

- 2,097,152-word × 16-bit / 4,194,304-word × 8-bit electrically switchable configuration
- 2.7 V to 3.6 V power supply
- Access time 90 ns MAX
- Operating current 20 mA MAX (5MHz)
- Standby current 10 μA MAX
- Input/Output TTL compatible
- Three-state output

PACKAGES

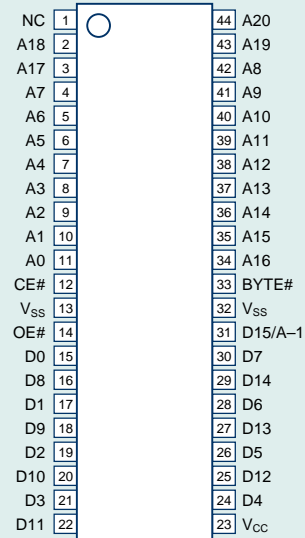
- MR27T3202F-xxxMA
44-pin plastic SOP (SOP44-P-600-1.27-K)
- MR27T3202F-xxxTP
44-pin plastic TSOP (TSOP II 44-P-400-0.80-K)
- MR27T3202F-xxxTN
48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)

P2ROM ADVANCED TECHNOLOGY

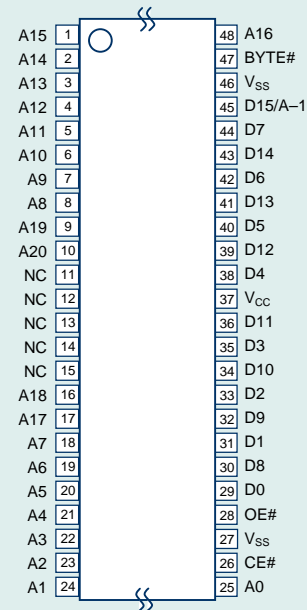
P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- **No additional programming charge**, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- **Custom Marking is** available at no additional charge.
- **Pin Compatible with Mask ROM** and some FLASH products.

PIN CONFIGURATION (TOP VIEW)



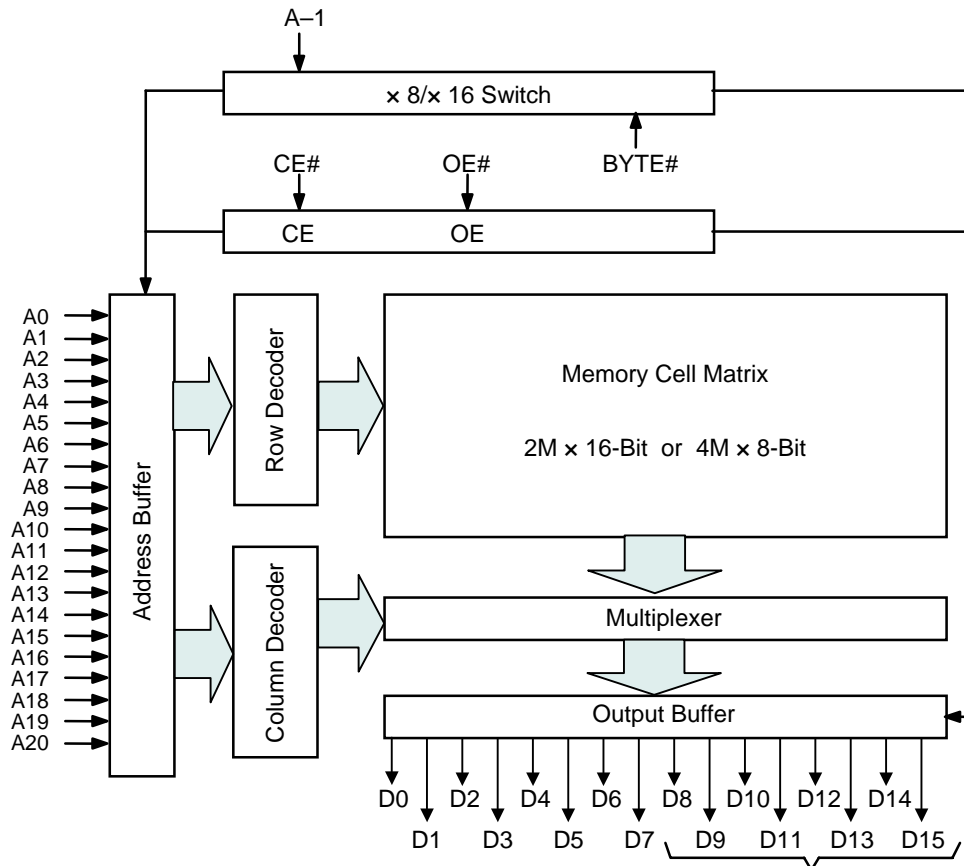
44SOP,
44TSOP(Type-II)



48TSOP(Type-I)



BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions
D15 / A-1	Data output / Address input
A0 to A20	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V _{CC}	Power supply voltage
V _{SS}	Ground
NC	No connect

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V _{CC}	D0 to D7	D8 to D14	D15/A-1
Read (16-Bit)	L	L	H	3.0 V	D _{OUT}		
Read (8-Bit)	L	L	L		D _{OUT}	Hi-Z	L/H
Output disable	L	H	H		Hi-Z		*
			L				
Standby	H	*	H		Hi-Z		*
			L				

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T _a	—	0 to 70	°C
Storage temperature	T _{stg}		-55 to 125	°C
Input voltage	V _I	relative to V _{SS}	-0.5 to V _{CC} +0.5	V
Output voltage	V _O		-0.5 to V _{CC} +0.5	V
Power supply voltage	V _{CC}		-0.5 to 5	V
Power dissipation per package	P _D	T _a = 25°C	1.0	W
Output short circuit current	I _{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

(T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V _{CC} power supply voltage	V _{CC}	V _{CC} = 2.7 to 3.6 V	2.7	—	3.6	V
Input "H" level	V _{IH}		V _{CC} +0.5*	V		
Input "L" level	V _{IL}		-0.5**	—	0.6	V

Voltage is relative to V_{SS}.

* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.0 V, T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C _{IN1}	V _I = 0 V	—	—	8	pF
BYTE#	C _{IN2}		—	—	120	
Output	C _{OUT}	V _O = 0 V	—	—	10	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I = 0 to V _{CC}	—	—	10	μA
Output leakage current	I _{LO}	V _O = 0 to V _{CC}	—	—	10	μA
V _{CC} power supply current (Standby)	I _{CCSC}	CE# = V _{CC}	—	—	10	μA
	I _{CCST}	CE# = V _{IH}	—	—	1	mA
V _{CC} power supply current (Read)	I _{CCA}	CE# = V _{IL} , OE# = V _{IH} f=5MHz	—	—	20	mA
Input "H" level	V _{IH}	—	2.2	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}	—	-0.5**	—	0.6	V
Output "H" level	V _{OH}	I _{OH} = -1 mA	2.4	—	—	V
Output "L" level	V _{OL}	I _{OL} = 2 mA	—	—	0.4	V

Voltage is relative to V_{SS}.* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C	—	90	—	ns
Address access time	t _{ACC}	CE# = OE# = V _{IL}	—	90	ns
CE# access time	t _{CE}	OE# = V _{IL}	—	90	ns
OE# access time	t _{OE}	CE# = V _{IL}	—	30	ns
Output disable time	t _{CHZ}	OE# = V _{IL}	0	30	ns
	t _{OHZ}	CE# = V _{IL}	0	25	ns
Output hold time	t _{OH}	CE# = OE# = V _{IL}	0	—	ns

Measurement conditions

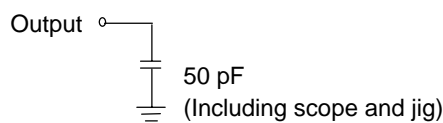
Input signal level ----- 0 V / 3 V

Input timing reference level ----- 1/2 V_{CC}

Output load ----- 50 pF

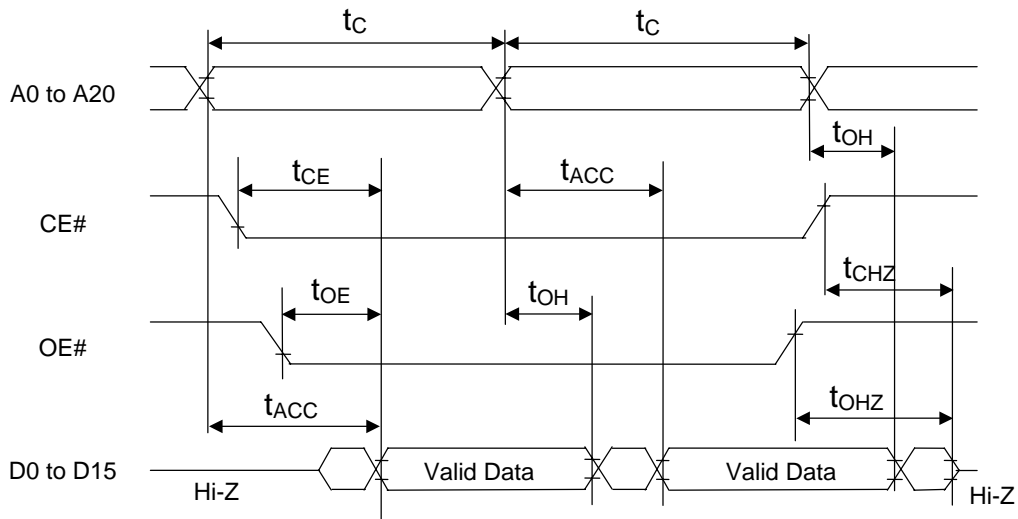
Output timing reference level ----- 1/2 V_{CC}

Output load

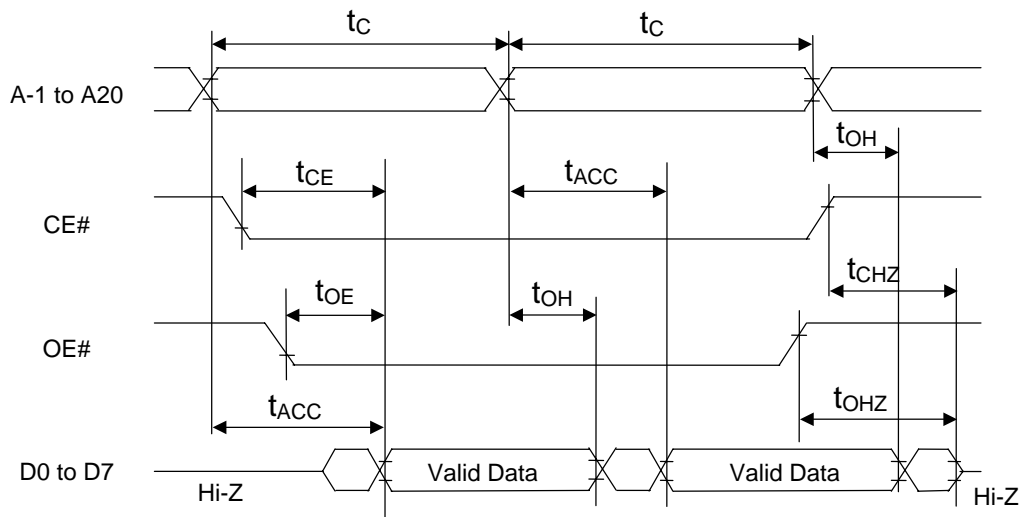


TIMING CHART (READ CYCLE)

16-Bit Read Mode (BYTE# = V_{III})

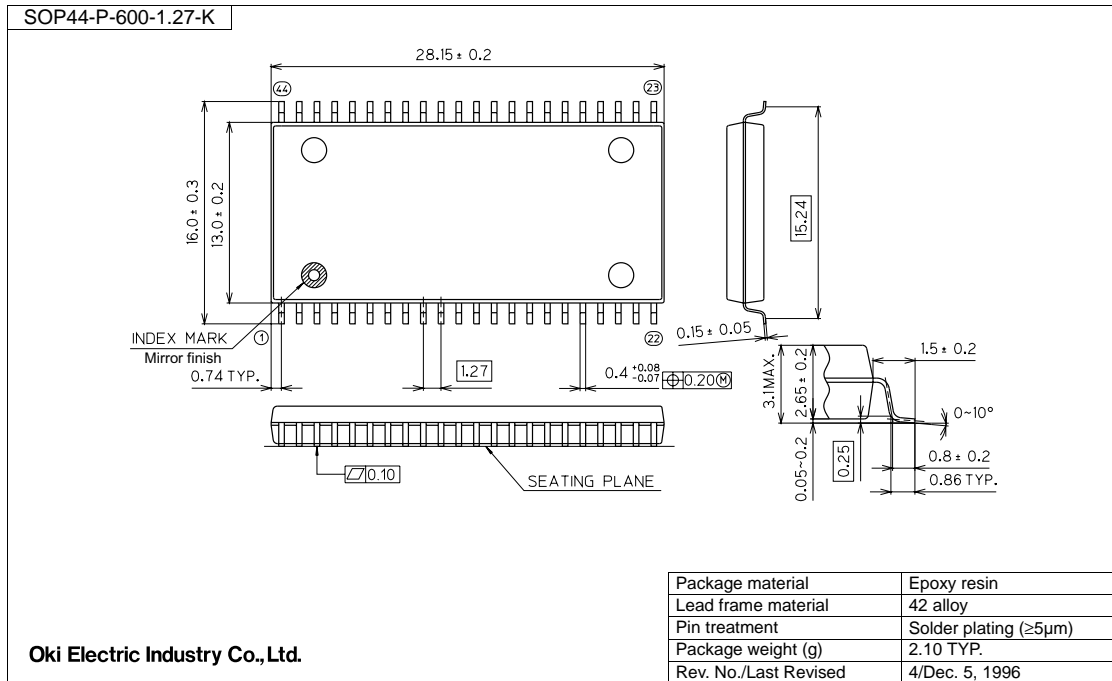


8-Bit Read Mode (BYTE# = V_{II})



PACKAGE DIMENSIONS

(Unit: mm)

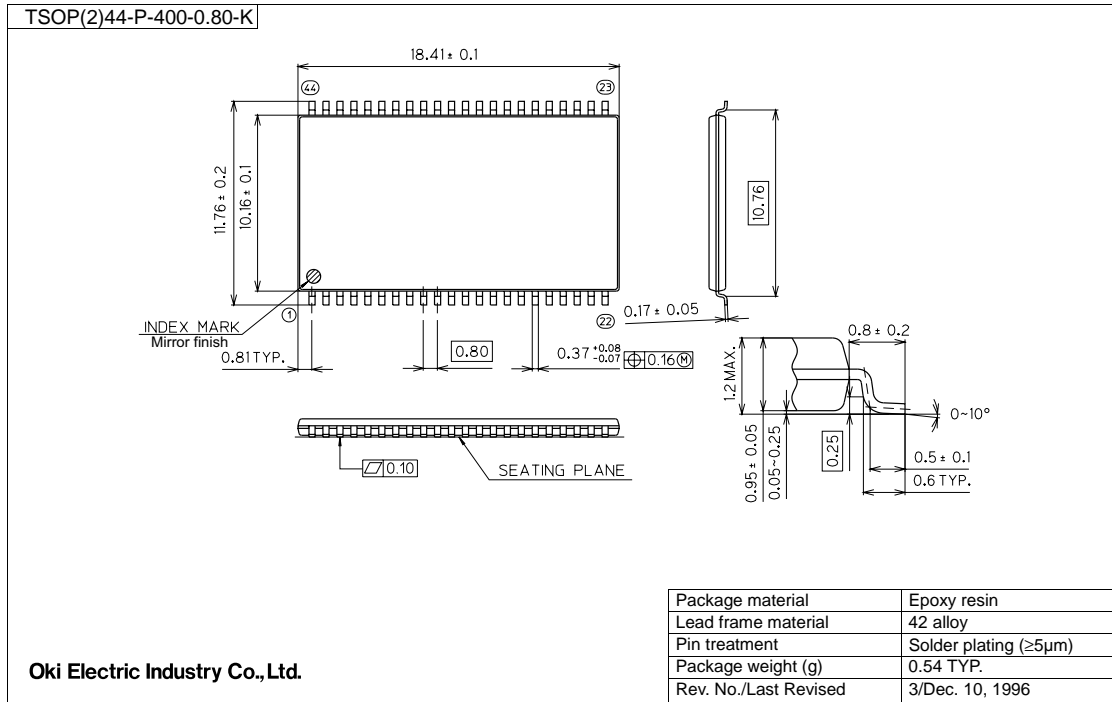


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

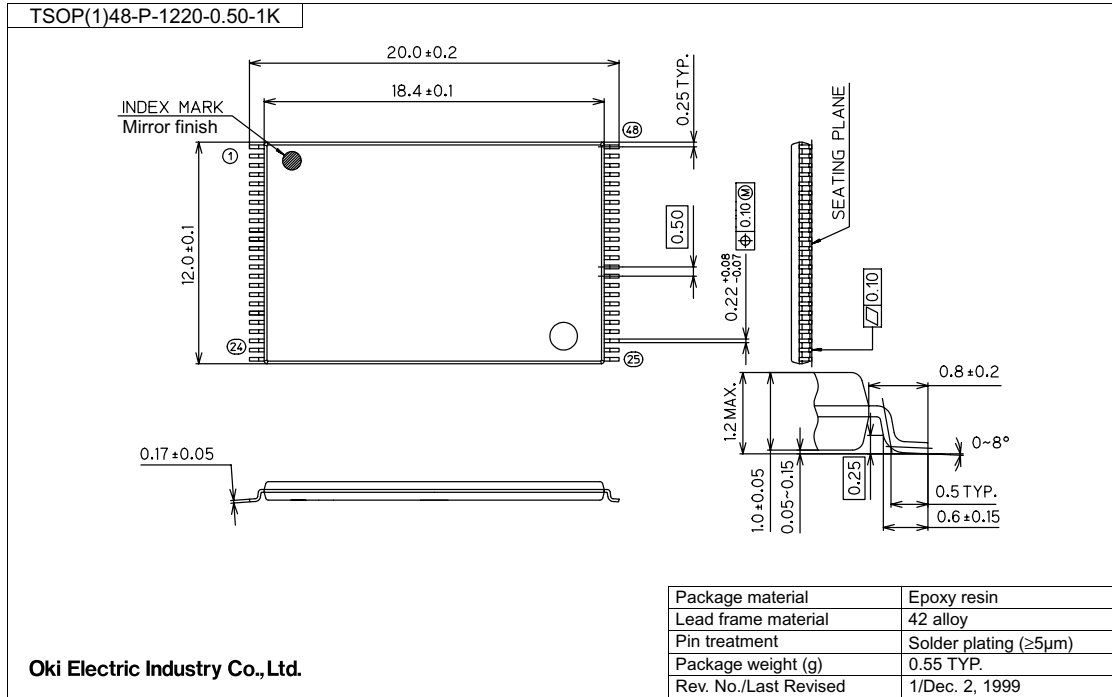


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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27T3202F-02-01	Oct., 2000	–	–	Final edition 1
FEDR27T3202F-02-02	Mar., 2002	5	4	Changed t_C , t_{ACC} , t_{CE} to 90ns
				Added I_{CCA2} at $t_C = 200ns$ Change the symbol, I_{CCA} to I_{CCA1}
				Changed I_{CCA1} to 30mA
				Changed t_{OE} to 30ns
				Changed I_{CCSC} to 10uA
				Changed I_{OH} , the condition of V_{OH} , to –1 mA
		Changed I_{OL} , the condition of V_{OL} , to 2 mA		
		1-4, 7	1-3	Changed the form
FEDR27T3202F-02-03	Jun. 4, 2003	1	1	Change 48TSOP(1) package code to –1K
		1, 4	1, 4	Unify I_{CCA} condition into $f=5MHz$
FEDR27T3202F-02-04	Jul. 9, 2004	3	3	Add P_D condition and $I_{OS} = 10mA$

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