

NC7WZ17 TinyLogic™ UHS Dual Buffer with Schmitt Trigger Inputs

General Description

The NC7WZ17 is a dual buffer with Schmitt trigger inputs from Fairchild's Ultra High Speed Series of TinyLogic™ in the SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.8V to 5.5V V_{CC} range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage. Schmitt trigger inputs typically achieve 1V hysteresis between the positive going and negative going input threshold voltage at 5V V_{CC} .

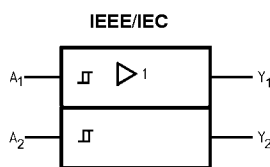
Features

- Space saving SC70 6-lead package
- Ultra High Speed: t_{PD} 3.6 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive: ± 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.8V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

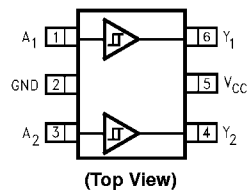
Ordering Code:

Order Number	Package Number	Package Top Mark	Package Description	Supplied As
NC7WZ17P6	MAA06A	Z17	6-Lead SC70, EIAJ SC88, 1.25mm Wide	250 Units on Tape and Reel
NC7WZ17P6X	MAA06A	Z17	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel

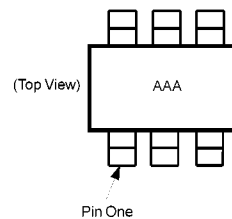
Logic Symbol



Connection Diagrams



Pin One Orientation Diagram



AAA represents Package Top Mark - see ordering code
Note: Orientation of Top Mark determines Pin One location. Read the Top Package Mark left to right, Pin One is the lower left pin (see diagram).

Pin Descriptions

Pin Names	Description
A_1, A_2	Data Inputs
Y_1, Y_2	Output

Function Table

$Y = A$

Input	Output
A	Y
L	L
H	H

H = HIGH Logic Level
L = LOW Logic Level

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Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions	
Supply Voltage (V_{CC})	-0.5V to +7V	Supply Voltage Operating (V_{CC})	1.8V to 5.5V
DC Input Voltage (V_{IN})	-0.5V to +7V	Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
DC Output Voltage (V_{OUT})	-0.5V to +7V	Input Voltage (V_{IN})	0V to 5.5V
DC Input Diode Current (I_{IK})		Output Voltage (V_{OUT})	0V to V_{CC}
@ $V_{IN} < -0.5V$	-50 mA	Operating Temperature (T_A)	-40°C to +85°C
DC Output Diode Current (I_{OK})		Thermal Resistance (θ_{JA})	350°C/W
@ $V_{OUT} < -0.5V$	-50 mA		
DC Output Current (I_{OUT})	±50 mA		
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±100 mA		
Storage Temperature (T_{STG})	-65°C to +150°C		
Junction Temperature under Bias (T_J)	150°C		
Junction Lead Temperature (T_L)			
(Soldering, 10 seconds)	260°C		
Power Dissipation (P_D) @ +85°C	180 mW		

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

DC Electrical Characteristics

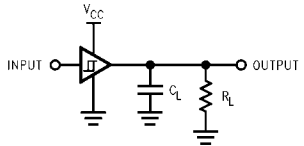
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions					
			Min	Typ	Max	Min	Max							
V_P	Positive Threshold Voltage	1.8	0.7	1.07	1.5	0.7	1.5	V						
		2.3	1.0	1.38	1.8	1.0	1.8							
		3.0	1.3	1.74	2.2	1.3	2.2							
		4.5	1.9	2.43	3.1	1.9	3.1							
		5.5	2.2	2.88	3.6	2.2	3.6							
V_N	Negative Threshold Voltage	1.8	0.25	0.56	0.9	0.25	0.9	V						
		2.3	0.40	0.75	1.15	0.40	1.15							
		3.0	0.6	0.98	1.5	0.6	1.5							
		4.5	1.0	1.42	2.0	1.0	2.0							
		5.5	1.2	1.68	2.3	1.2	2.3							
V_H	Hysteresis Voltage	1.8	0.15	0.51	1.0	0.15	1.0	V						
		2.3	0.25	0.62	1.1	0.25	1.1							
		3.0	0.4	0.76	1.2	0.4	1.2							
		4.5	0.6	1.01	1.5	0.6	1.5							
		5.5	0.7	1.20	1.7	0.7	1.7							
V_{OH}	HIGH Level Output Voltage	1.8	1.7	1.8		1.7		V	$V_{IN} = V_{IH}$	$I_{OH} = -100 \mu\text{A}$				
		2.3	2.2	2.3		2.2				$I_{OH} = -8 \text{ mA}$				
		3.0	2.9	3.0		2.9				$I_{OH} = -16 \text{ mA}$				
		4.5	4.4	4.5		4.4				$I_{OH} = -24 \text{ mA}$				
		2.3	1.9	2.14		1.9				$I_{OH} = -32 \text{ mA}$				
		3.0	2.4	2.75		2.4								
		3.0	2.3	2.62		2.3								
		4.5	3.8	4.13		3.8								
		V_{OL}	LOW Level Output Voltage	1.8		0.0	0.1				0.1	V	$V_{IN} = V_{IL}$	$I_{OL} = 100 \mu\text{A}$
				2.3		0.0	0.1				0.1			
3.0				0.0	0.1		0.1							
4.5				0.0	0.1		0.1							
2.3				0.10	0.3		0.3	$I_{OL} = 8 \text{ mA}$						
3.0				0.16	0.4		0.4	$I_{OL} = 16 \text{ mA}$						
3.0				0.24	0.55		0.55	$I_{OL} = 24 \text{ mA}$						
4.5				0.25	0.55		0.55	$I_{OL} = 32 \text{ mA}$						
I_{IN}	Input Leakage Current	0 to 5.5			±1		±10	μA	$V_{IN} = 5.5V, GND$					
I_{OFF}	Power Off Leakage Current	0.0			1		10	μA	V_{IN} or $V_{OUT} = 5.5V$					
I_{CC}	Quiescent Supply Current	1.8 to 5.5			1.0		10	μA	$V_{IN} = 5.5V, GND$					

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Fig. No.
			Min	Typ	Max	Min	Max			
t _{PLH}	Propagation Delay	1.8	2.0	6.9	11.9	2.0	13.1	ns	C _L = 15 pF, R _L = 1 MΩ	Figure 1 Figure 3
t _{PHL}		2.5 ± 0.2	1.5	4.8	8.2	1.5	9.0			
		3.3 ± 0.3	1.0	3.7	5.6	1.0	6.2			
		5.0 ± 0.5	0.8	3.0	4.7	0.8	5.2			
t _{PLH}	Propagation Delay	3.3 ± 0.3	1.5	4.3	6.6	1.5	7.3	ns	C _L = 50 pF, R _L = 500Ω	Figure 1 Figure 3
t _{PHL}		5.0 ± 0.5	1.0	3.6	5.6	1.0	6.2			
C _{IN}	Input Capacitance	0	2.5					pF		
C _{PD}	Power Dissipation	3.3	10						(Note 2)	Figure 2
	Capacitance	5.0	12					pF		

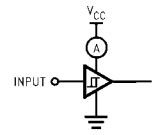
Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; t_W = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns;
 PRR = variable; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

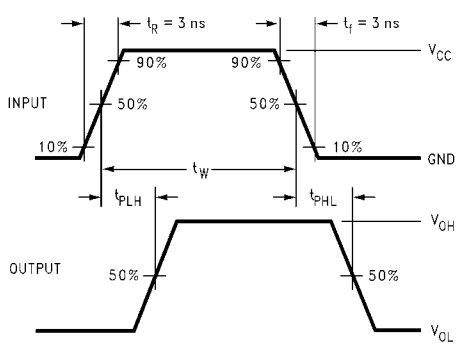
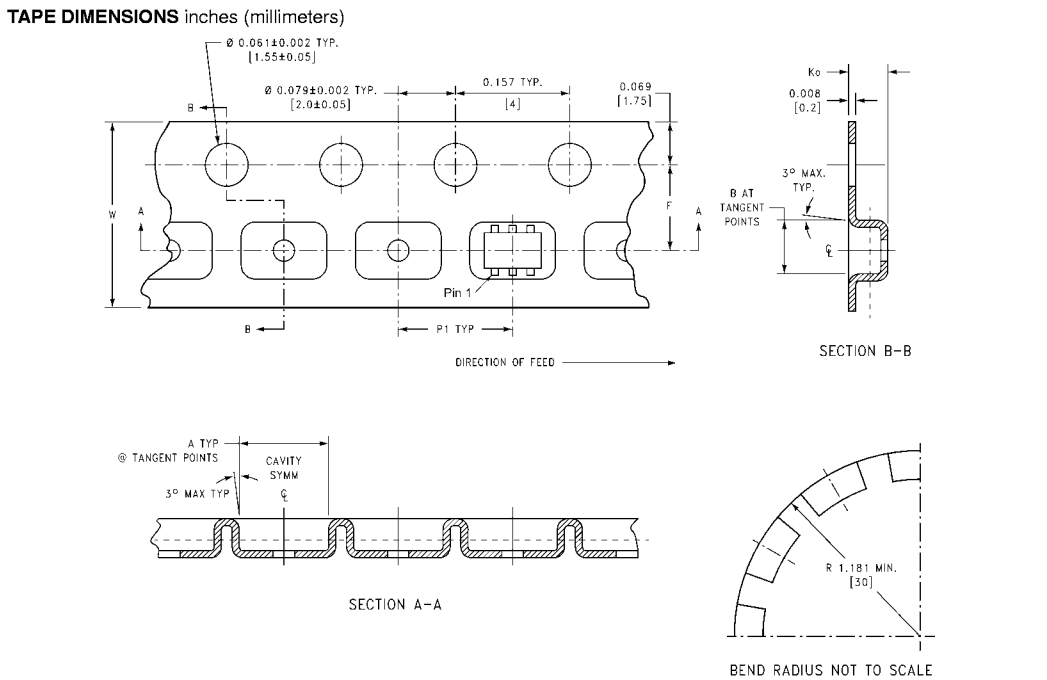


FIGURE 3. AC Waveforms

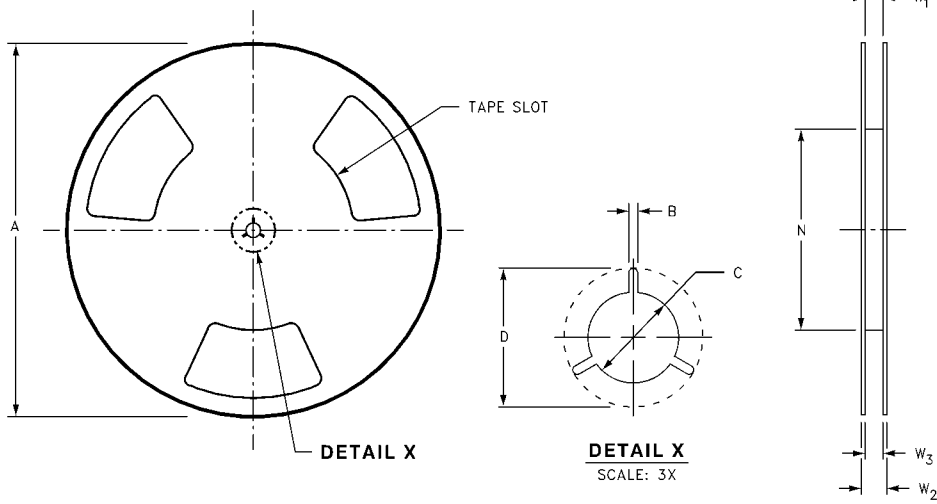
Tape and Reel Specification

TAPE FORMAT				
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed



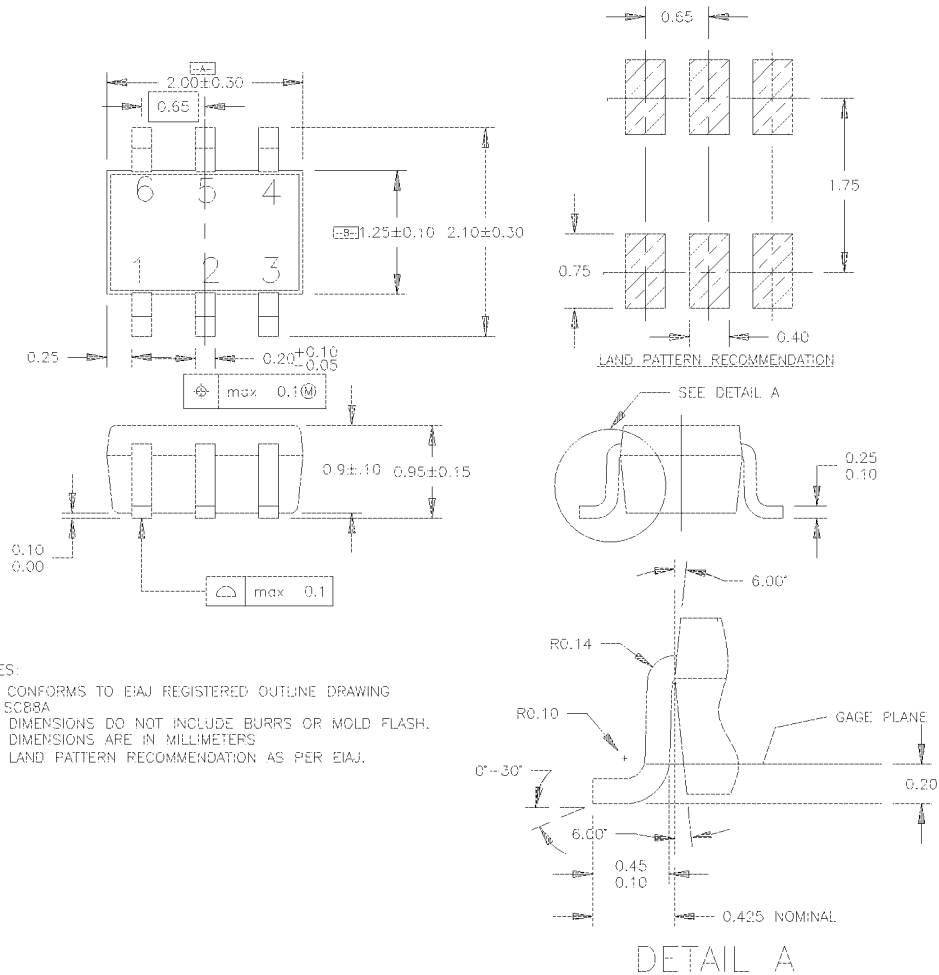
Package	Tape Size	DIM A	DIM B	DIM F	DIM K ₀	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



- NOTES:
- CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A
 - DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
 - DIMENSIONS ARE IN MILLIMETERS
 - LAND PATTERN RECOMMENDATION AS PER EIAJ.

**6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A**

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