MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N5428 thru 2N5430

MEDIUM-POWER NPN SILICON TRANSISTORS

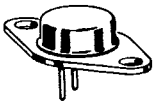
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 7 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-213AA Case

7 AMPERE

POWER TRANSISTORS NPN SILICON

80–100 VOLTS
40 WATTS



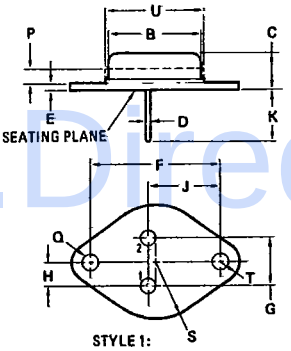
***MAXIMUM RATINGS**

Rating	Symbol	2N5428	2N5429 2N5430	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 228		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.37	°C/W

* Indicates JEDEC Registered Data



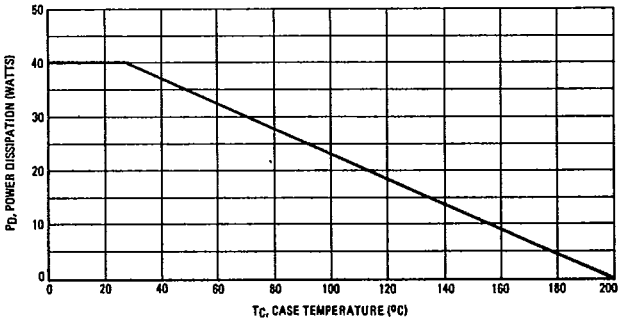
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-213AA
(TO-66)

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



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Datasheet.Directory

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N5428	–	$V_{CEO(sus)}$*	80	–	Vdc
	2N5429, 2N5430			100	–	
Collector Cutoff Current (V_{CE} = 75 Vdc, I_B = 0)	2N5428	–	I_{CEO}	–	100	µAdc
(V_{CE} = 90 Vdc, I_B = 0)	2N5429, 2N5430			–	100	
Collector Cutoff Current (V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5428	12	I_{CEX}	–	10	µAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5429, 2N5430			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5428			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5429, 2N5430			–	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		–	I_{CBO}	–	10	µAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		–	I_{EBO}	–	100	µAdc
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5429	8	h_{FE}*	30	–	–
	2N5428, 2N5430			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5429			30	120	
	2N5428, 2N5430			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5429			20	–	
	2N5428, 2N5430			40	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)		9, 11, 13	$V_{CE(sat)}$*	–	0.7	Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	1.2	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)		11, 13	$V_{BE(sat)}$*	–	1.2	Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		–	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	–	250	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	–	1,000	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	(I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	µs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data. (1)Pulse Test: Pulse Width ≈ 300 µs, Duty Cycle ≈ 2.0%.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT

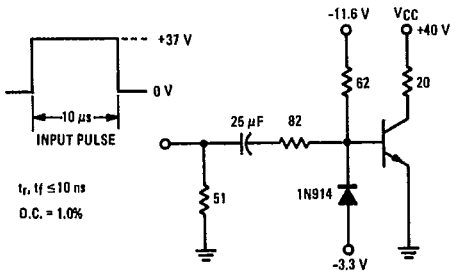


FIGURE 3 — TURN-ON TIME

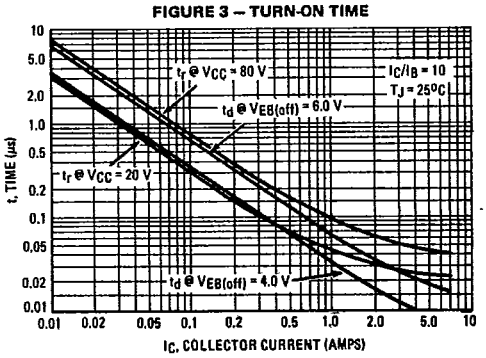


FIGURE 4 – THERMAL RESPONSE

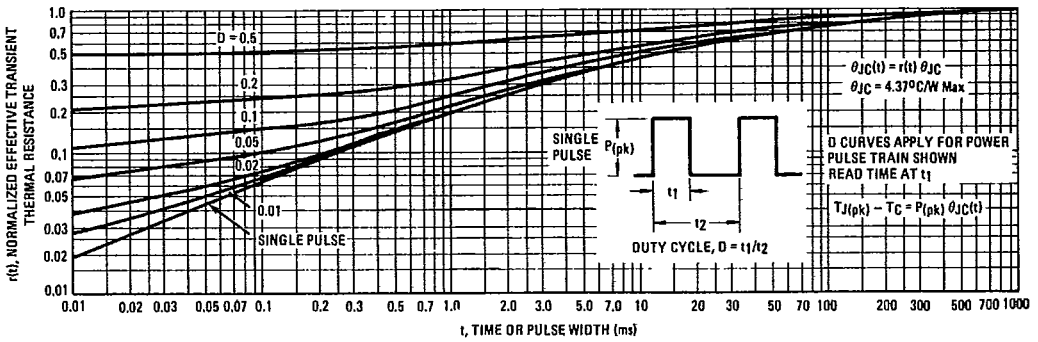
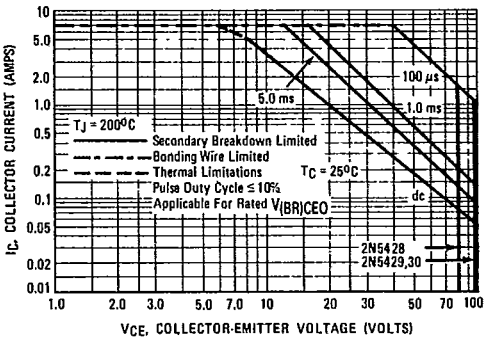


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

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FIGURE 6 – TURN-OFF TIME

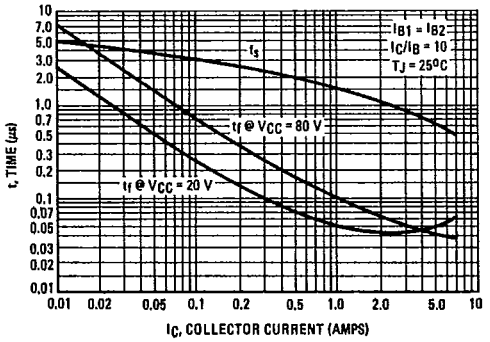

FIGURE 7 – CAPACITANCE versus VOLTAGE

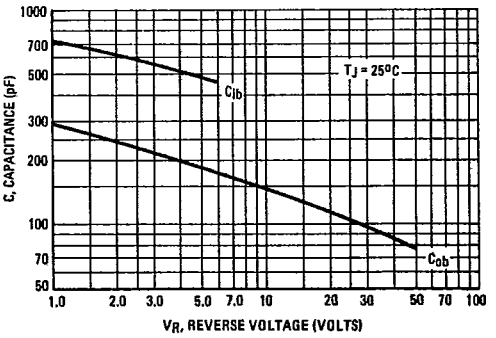

FIGURE 8 – DC CURRENT GAIN

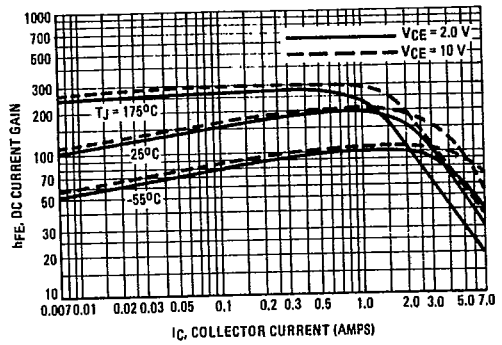

FIGURE 9 – COLLECTOR SATURATION REGION

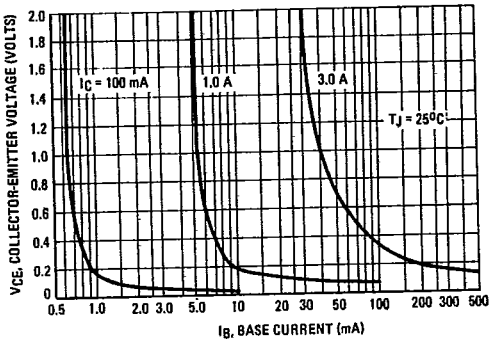

FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

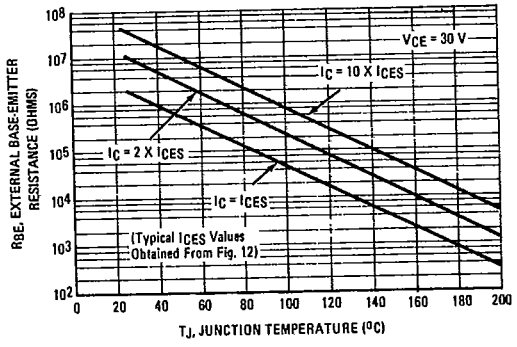

FIGURE 11 – "ON" VOLTAGES

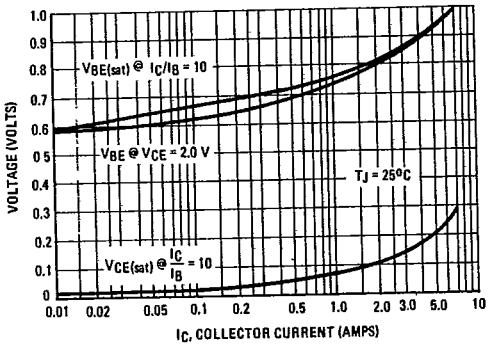

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FIGURE 12 – COLLECTOR CUT-OFF REGION

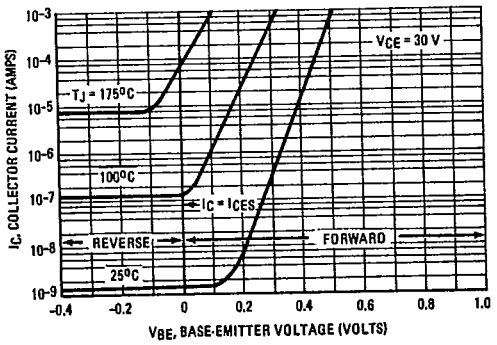
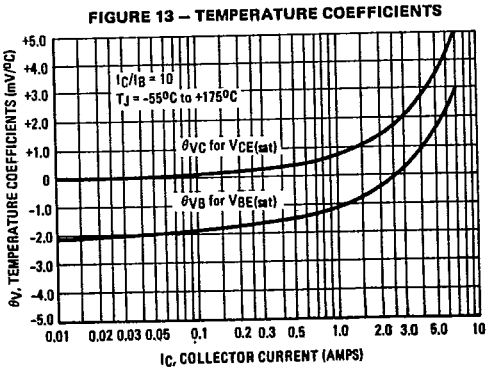
FIGURE 13 – TEMPERATURE COEFFICIENTS