Precision Rail-to-Rail Input and Output Operational Amplifiers

OP184/OP284/OP484

FEATURES

Single-supply operation
Wide bandwidth: 4 MHz
Low offset voltage: 65 µV
Unity-gain stable
High slew rate: 4.0 V/µs
Low noise: 3.9 nV/√Hz

APPLICATIONS

Battery-powered instrumentation
Power supply control and protection
Telecom
DAC output amplifier
ADC input buffer

GENERAL DESCRIPTION

The OP184/OP284/OP484 are single, dual, and quad single-supply, 4 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from 3 V to 36 V (or ±1.5 V to ±18 V) and function with a single supply as low as 1.5 V.

These amplifiers are superb for single-supply applications requiring both ac and precision dc performance. The combination of bandwidth, low noise, and precision makes the OP184/OP284/OP484 useful in a wide variety of applications, including filters and instrumentation.

Other applications for these amplifiers include portable telecom equipment, power supply control and protection, and as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The OP184/OP284/OP484 are specified over the hot extended industrial (–40°C to +125°C) temperature range. The single is available in 8-lead SOIC surface mount packages. The dual is available in 8-lead PDIP and SOIC surface mount packages. The quad OP484 is available in 14-lead PDIP and 14-lead, narrow-body SOIC packages.

PIN CONFIGURATIONS

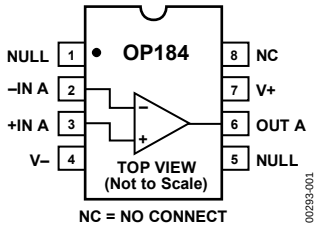

Figure 1. 8-Lead SOIC (S-Suffix)

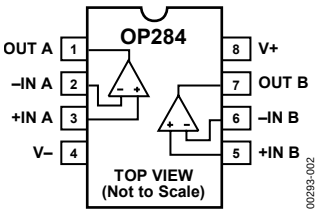

Figure 2. 8-Lead PDIP (P-Suffix)
8-Lead SOIC (S-Suffix)

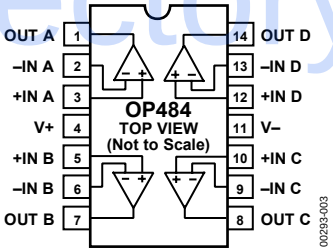

Figure 3. 14-Lead PDIP (P-Suffix)
14-Lead Narrow-Body SOIC (S-Suffix)

Rev. C

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6/02—Rev. 0 to Rev. A

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage, OP184/OP284E Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			65	µV
		−40°C ≤ T_A ≤ +125°C			165	µV
Offset Voltage, OP184/OP284F Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			125	µV
		−40°C ≤ T_A ≤ +125°C			350	µV
Offset Voltage, OP484E Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			75	µV
		−40°C ≤ T_A ≤ +125°C			175	µV
Offset Voltage, OP484F Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			150	µV
		−40°C ≤ T_A ≤ +125°C			450	µA
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C		60	450	nA
		−40°C ≤ T_A ≤ +125°C			600	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C		2	50	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	60			dB
		V_{CM} = 1.0 V to 4.0 V, −40°C ≤ T_A ≤ +125°C	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 1 V ≤ V_O ≤ 4 V	50	240		V/mV
		R_L = 2 kΩ, −40°C ≤ T_A ≤ +125°C	25			V/mV
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	4.85			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			125	mV
Output Current	I_{OUT}		±6.5			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.0 V to 10 V, −40°C ≤ T_A ≤ +125°C	76			dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V, −40°C ≤ T_A ≤ +125°C			1.45	mA
Supply Voltage Range	V_S		3		36	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	1.65	2.4		V/µs
Settling Time	t_S	To 0.01%, 1.0 V step		2.5		µs
Gain Bandwidth Product	GBP			3.25		MHz
Phase Margin	Øo			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

@ V_S = 3.0 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage, OP184/OP284E Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			65	µV
		−40°C ≤ T_A ≤ +125°C			165	µV
Offset Voltage, OP184/OP284F Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			125	µV
		−40°C ≤ T_A ≤ +125°C			350	µV
Offset Voltage, OP484E Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
Offset Voltage, OP484F Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			150	µV
		−40°C ≤ T_A ≤ +125°C			450	µA
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C		60	450	nA
		−40°C ≤ T_A ≤ +125°C			600	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	60			dB
		V_{CM} = 0 V to 3 V, −40°C ≤ T_A ≤ +125°C	56			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	2.85			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			125	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.25 V to ±1.75 V	76			dB
Supply Current/Amplifier	I_{SY}	V_O = 1.5 V, −40°C ≤ T_A ≤ +125°C			1.35	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			3		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

@ V_S = ±15.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage, OP184/OP284E Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
Offset Voltage, OP184/OP284F Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			175	µV
		−40°C ≤ T_A ≤ +125°C			375	µV
Offset Voltage, OP484E Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			150	µV
		−40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage, OP484F Grade[1]	V_{OS}	−40°C ≤ T_A ≤ +125°C			250	µV
		−40°C ≤ T_A ≤ +125°C			500	µA
Input Bias Current	I_B	−40°C ≤ T_A ≤ +125°C		80	450	nA
		−40°C ≤ T_A ≤ +125°C			575	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −14.0 V to +14.0 V, −40°C ≤ T_A ≤ +125°C	86	90		dB
		V_{CM} = −15.0 V to +15.0 V	80			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −10 V ≤ V_O ≤ 10 V	150	1000		V/mV
		R_L = 2 kΩ, −40 V ≤ T_A ≤ +125°C	75			V/mV
Offset Voltage Drift E Grade	$\Delta V_{OS}/\Delta T$			0.2	2.00	µV/°C
Bias Current Drift	$\Delta V_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	14.8			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			−14.875	V
Output Current	I_{OUT}		±10			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.0 V to ±18 V, −40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, −40°C ≤ T_A ≤ +125°C			2.0	mA
Supply Current/Amplifier	I_{SY}	V_S = ±18 V, −40°C ≤ T_A ≤ +125°C			2.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.0		V/µs
Full-Power Bandwidth	BW_p	1% distortion, R_L = 2 kΩ, V_O = 29 V p-p		35		kHz
Settling Time	t_S	To 0.01%, 10 V step		4		µs
Gain Bandwidth Product	GBP			4.25		MHz
Phase Margin	Øo			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[1]	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
P-Suffix, S-Suffix Packages	−65°C to +150°C
Operating Temperature Range	
OP184/OP284/OP484E/OP484F	−40°C to +125°C
Junction Temperature Range	
P-Suffix, S-Suffix Packages	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1]For input voltages greater than 0.6 V, the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for device in socket for CERDIP and PDIP. θ_{JA} is specified for device soldered in circuit board for SOIC packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead PDIP (P-Suffix)	103	43	°C/W
8-Lead SOIC (S-Suffix)	158	43	°C/W
14-Lead PDIP (P-Suffix)	83	39	°C/W
14-Lead SOIC (S-Suffix)	92	27	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

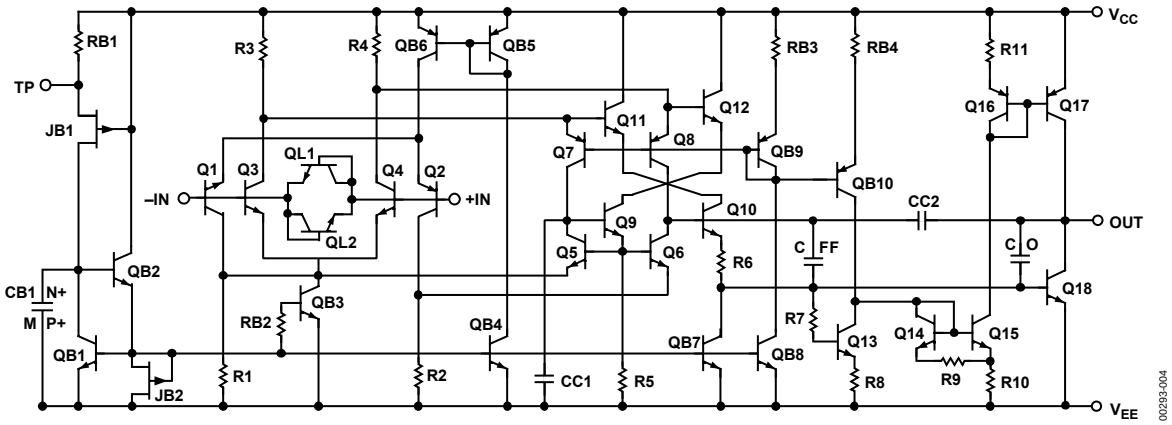


Figure 4. Simplified Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

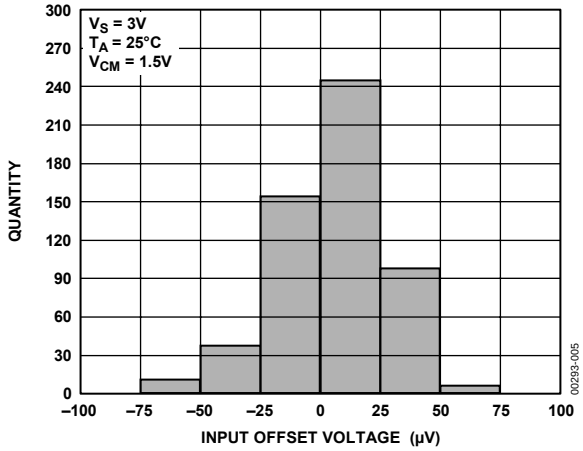


Figure 5. Input Offset Voltage Distribution

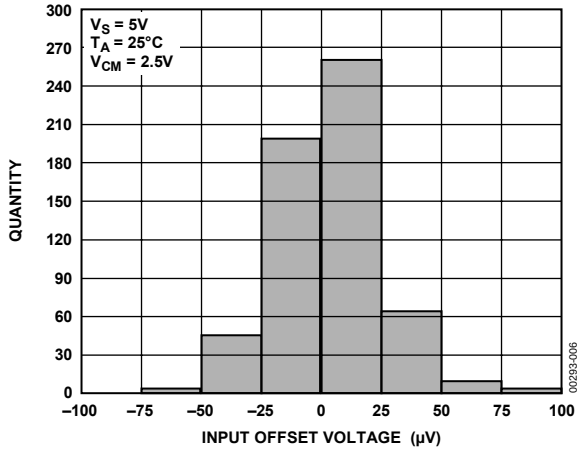


Figure 6. TPC 2. Input Offset Voltage Distribution

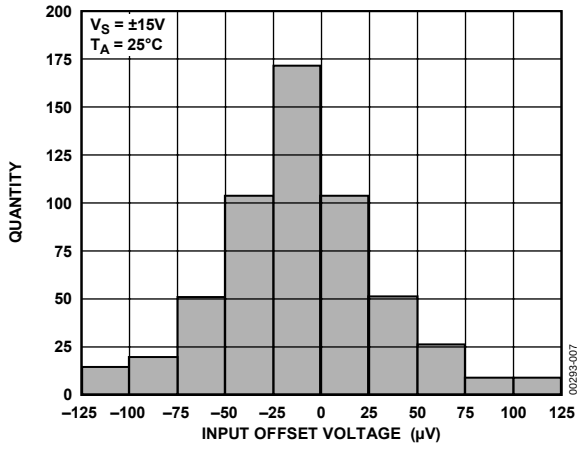


Figure 7. Input Offset Voltage Distribution

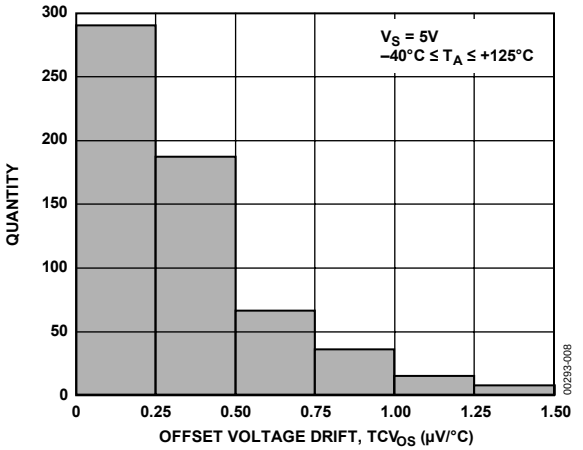


Figure 8. Input Offset Voltage Drift Distribution

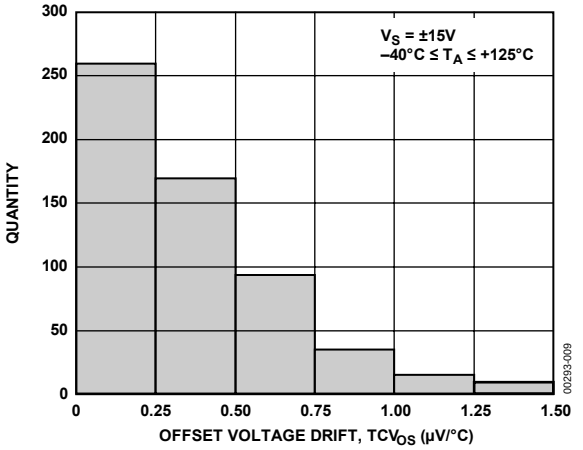


Figure 9. Input Offset Voltage Drift Distribution

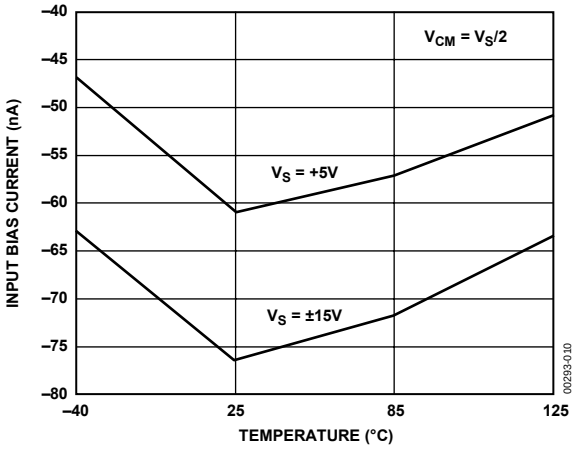


Figure 10. Bias Current vs. Temperature

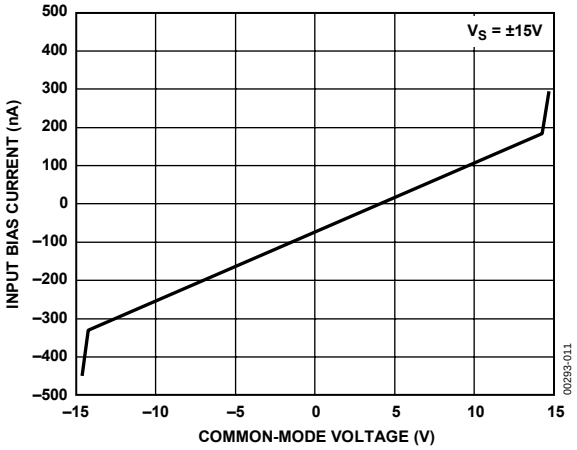


Figure 11. Input Bias Current vs. Common-Mode Voltage

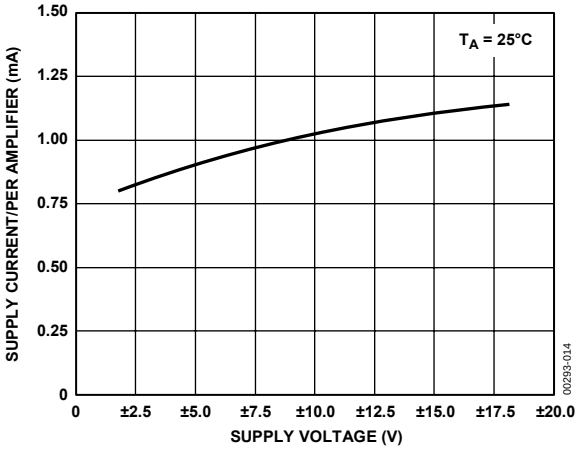


Figure 14. Supply Current vs. Supply Voltage

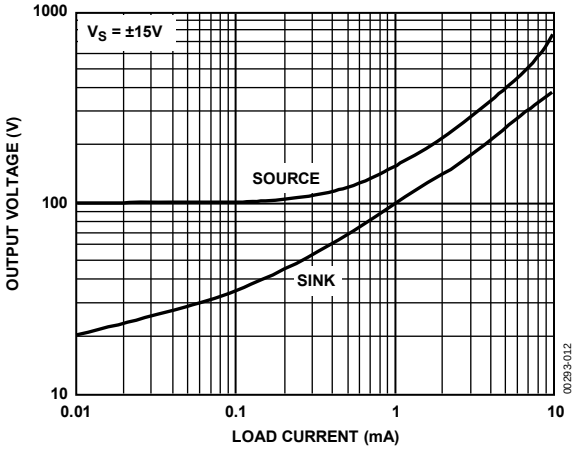


Figure 12. Output Voltage to Supply Rail vs. Load Current

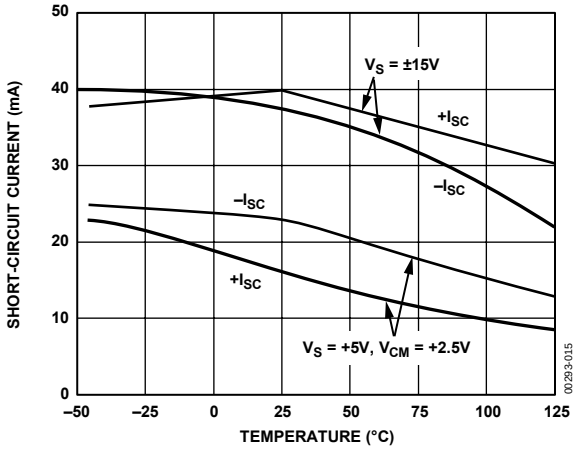


Figure 15. Short-Circuit Current vs. Temperature

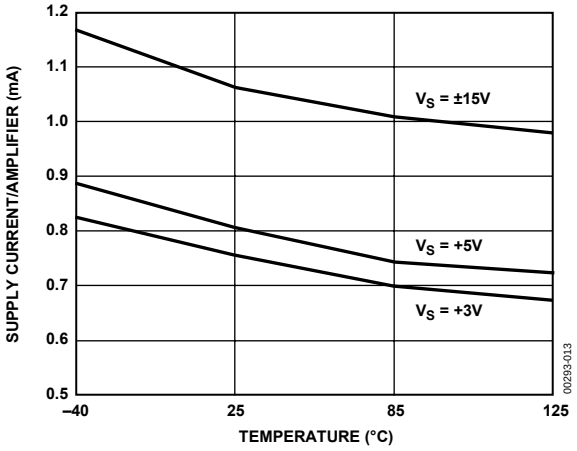


Figure 13. Supply Current vs. Temperature

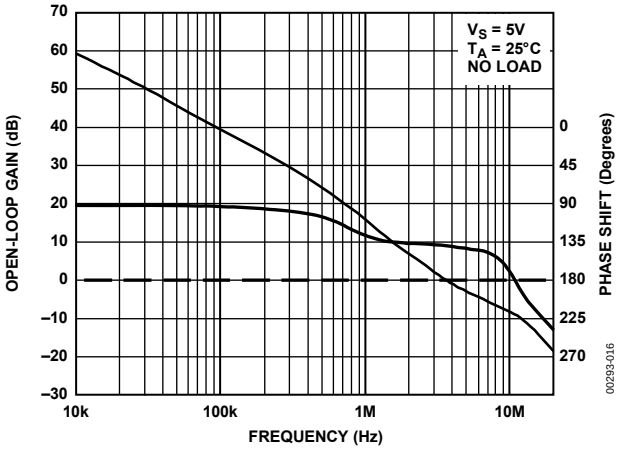


Figure 16. Open-Loop Gain and Phase vs. Frequency (No Load)

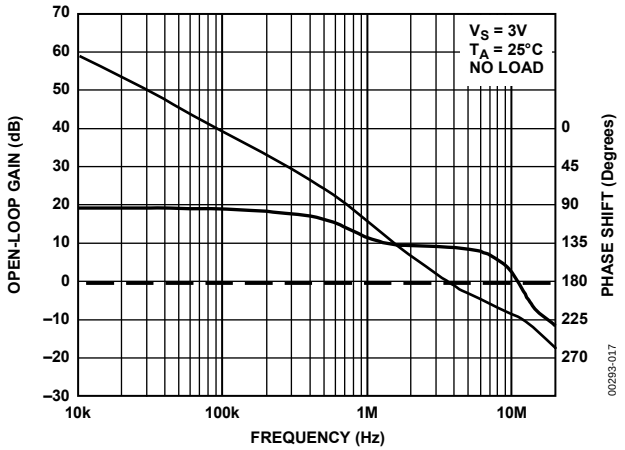


Figure 17. Open-Loop Gain and Phase vs. Frequency (No Load)

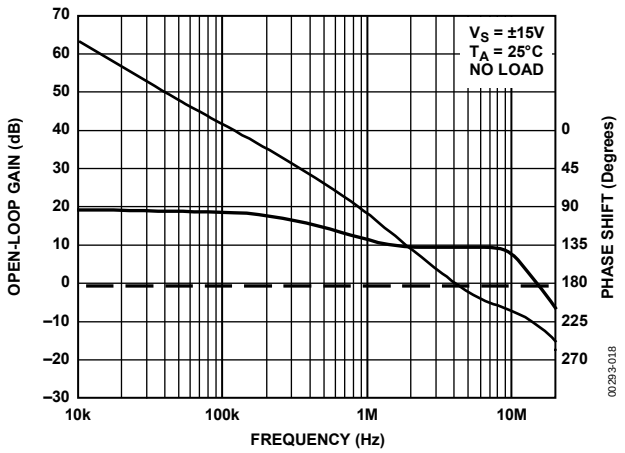


Figure 18. Open-Loop Gain and Phase vs. Frequency (No Load)

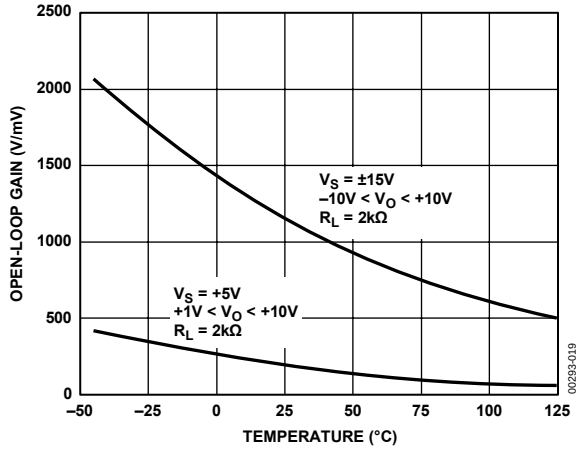


Figure 19. Open-Loop Gain vs. Temperature

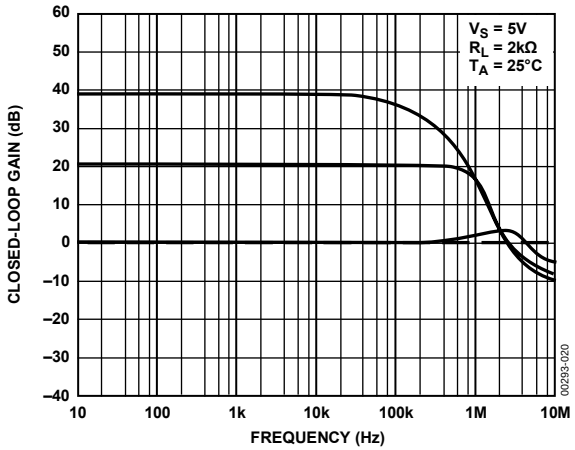


Figure 20. Closed-Loop Gain vs. Frequency (2 kΩ Load)

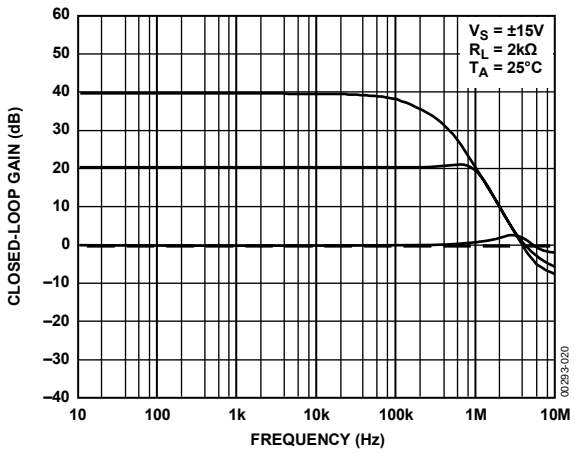


Figure 21. Closed-Loop Gain vs. Frequency (2 kΩ Load)

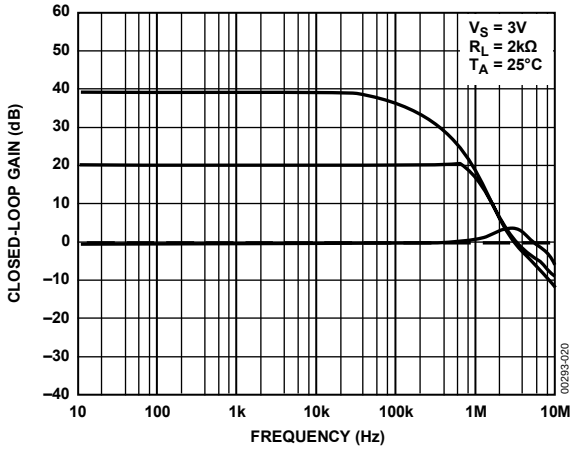


Figure 22. Closed-Loop Gain vs. Frequency (2 kΩ Load)

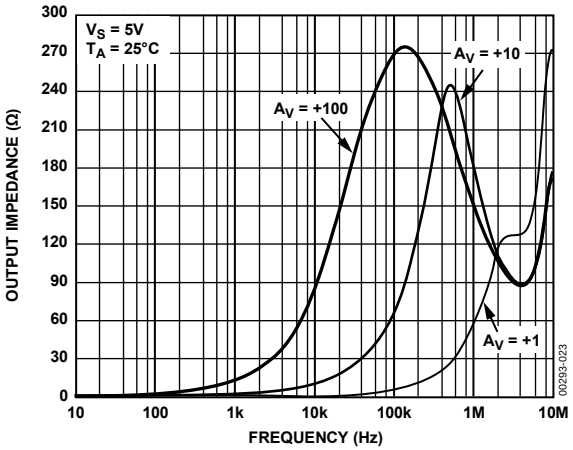


Figure 23. Output Impedance vs. Frequency

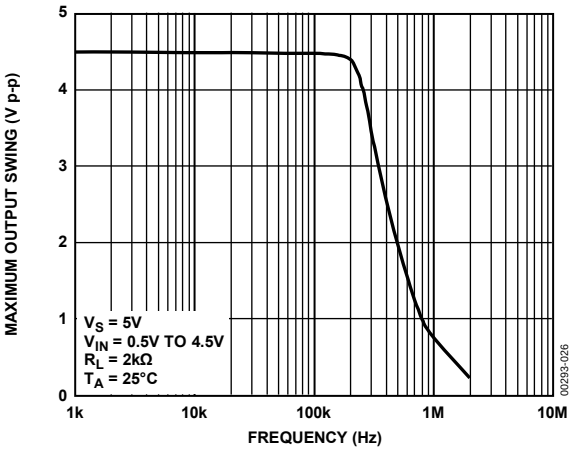


Figure 26. Maximum Output Swing vs. Frequency

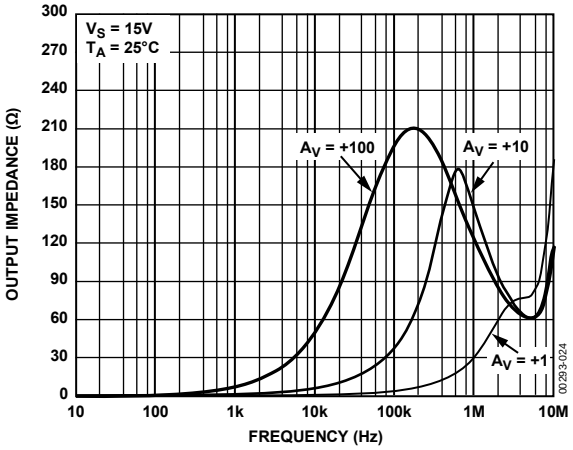


Figure 24. Output Impedance vs. Frequency

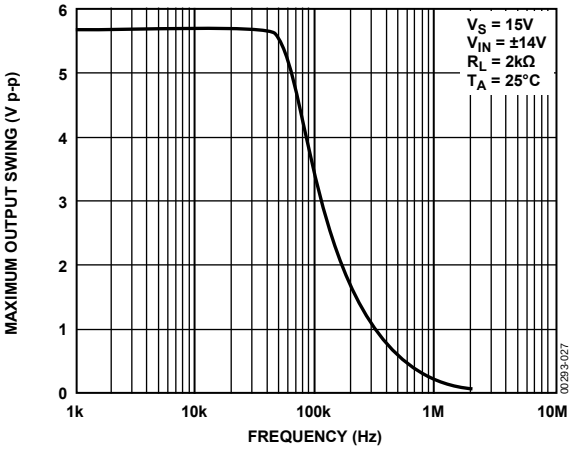


Figure 27. Maximum Output Swing vs. Frequency

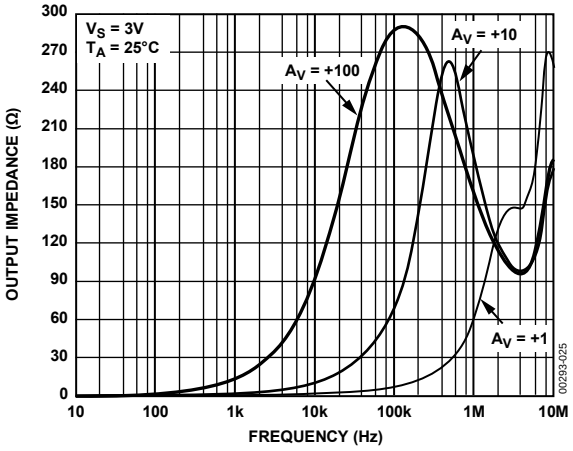


Figure 25. Output Impedance vs. Frequency

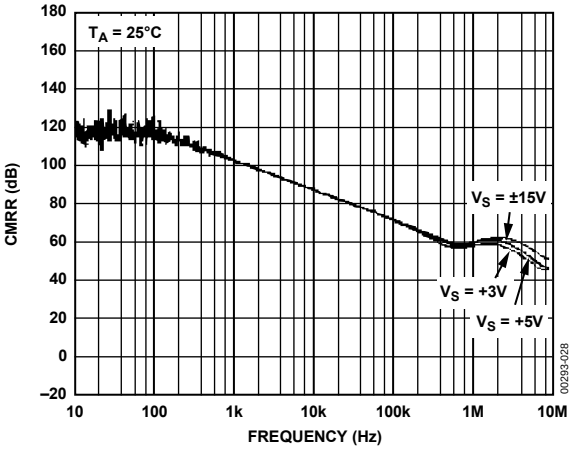


Figure 28. CMRR vs. Frequency

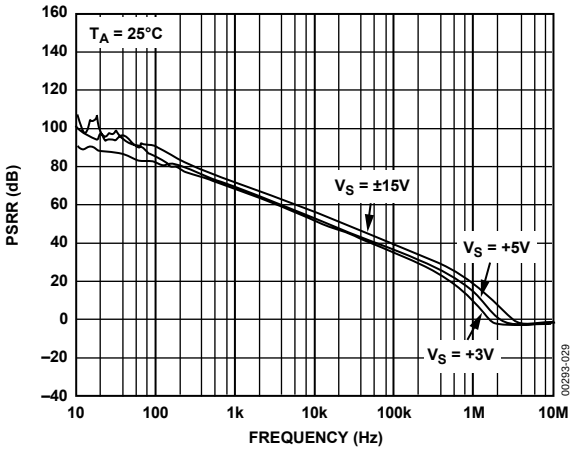


Figure 29. PSRR vs. Frequency

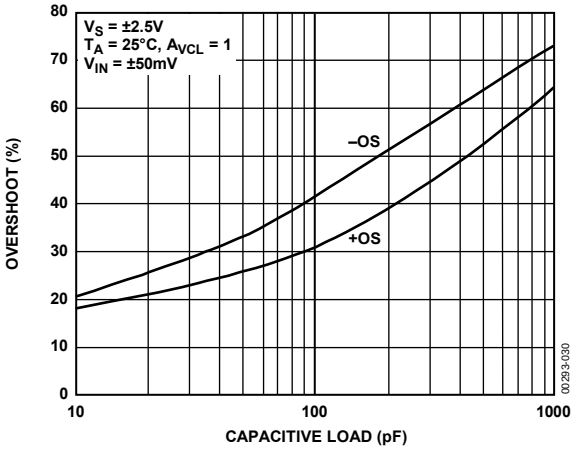


Figure 30. Small Signal Overshoot vs. Capacitive Load

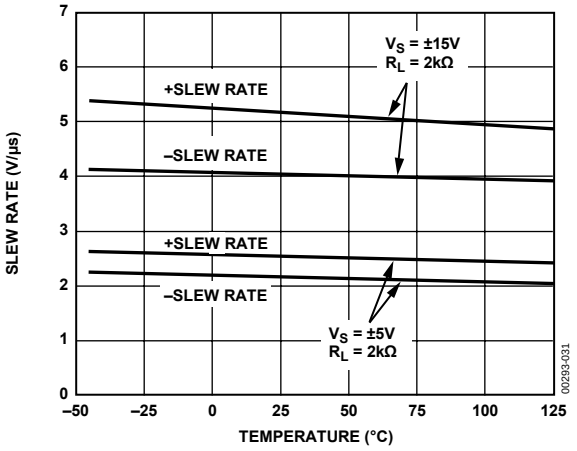


Figure 31. Slew Rate vs. Temperature

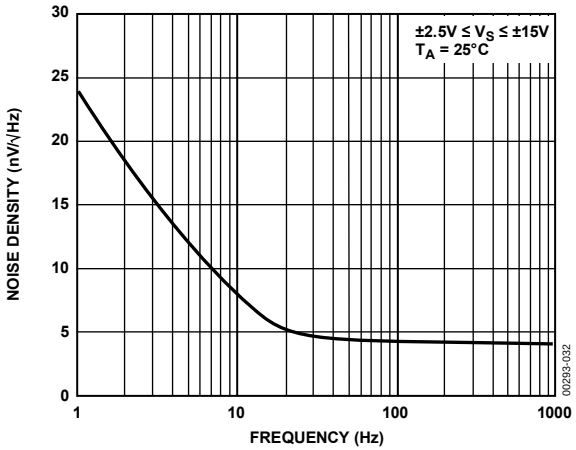


Figure 32. Voltage Noise Density vs. Frequency

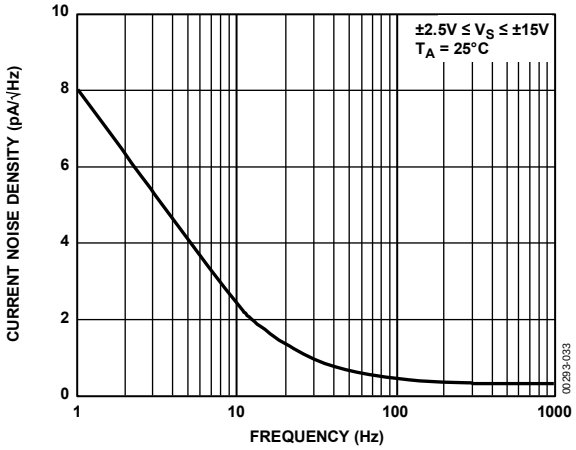


Figure 33. Current Noise Density vs. Frequency

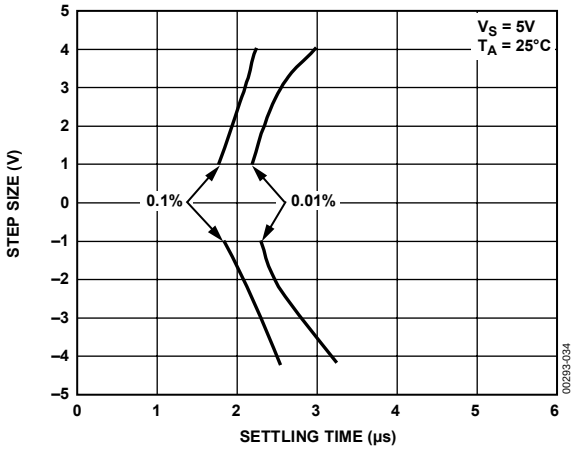


Figure 34. Step Size vs. Settling Time

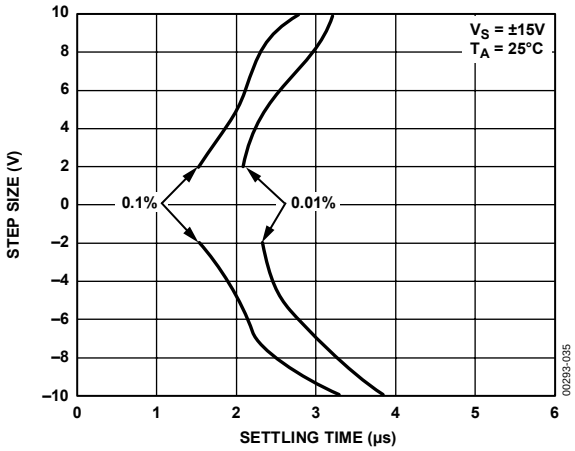


Figure 35. Step Size vs. Settling Time

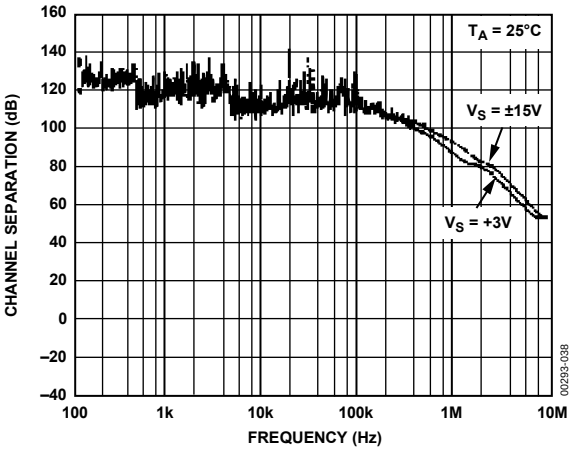


Figure 38. Channel Separation vs. Frequency

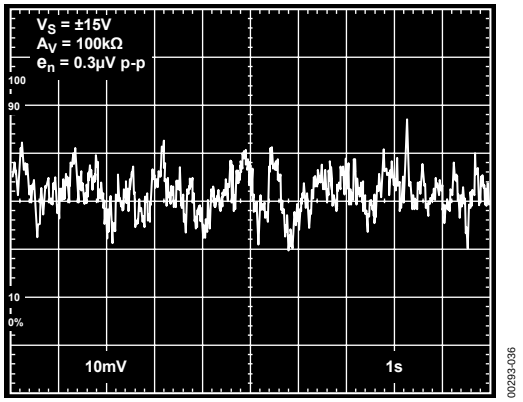


Figure 36. 0.1 Hz to 10 Hz Noise

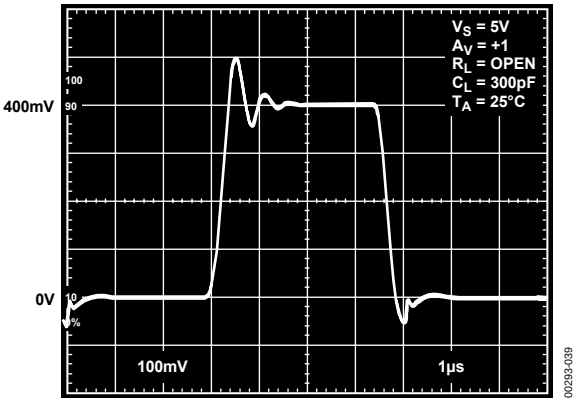


Figure 39. Small Signal Transient Response

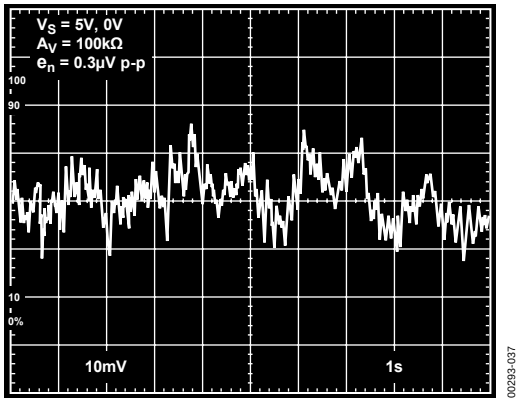


Figure 37. 0.1 Hz to 10 Hz Noise

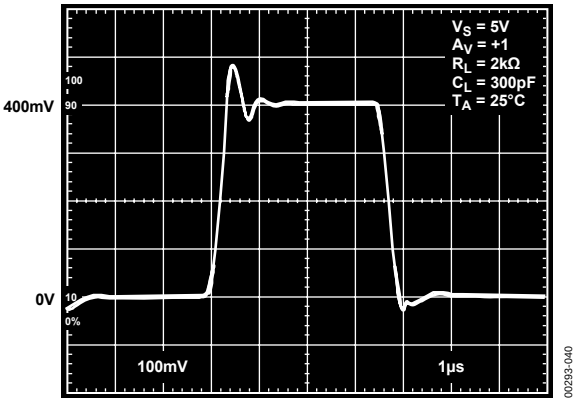


Figure 40. Small Signal Transient Response

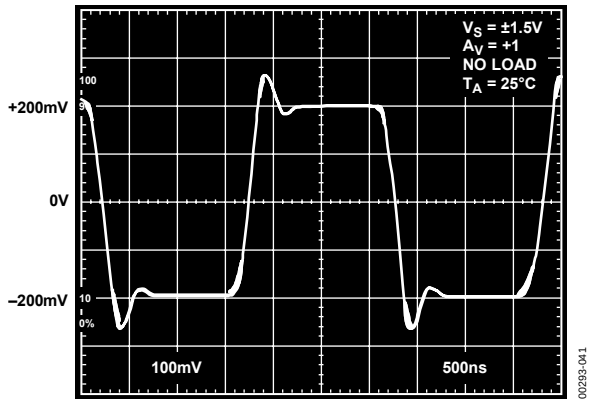


Figure 41. Small Signal Transient Response

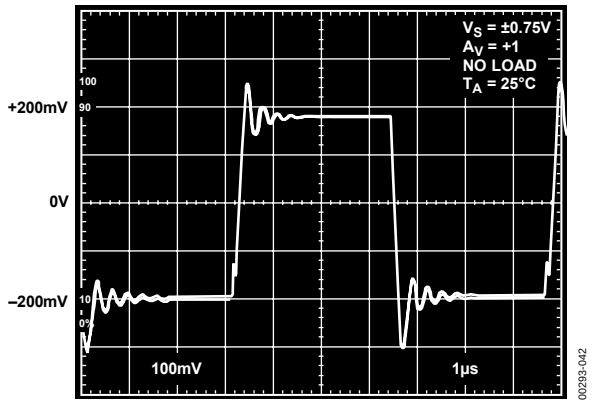


Figure 42. Small Signal Transient Response

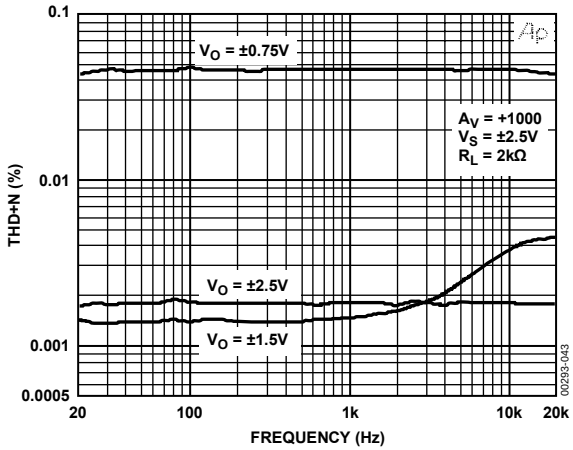


Figure 43. Total Harmonic Distortion vs. Frequency

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The OP184/OP284/OP484 are precision single-supply, rail-to-rail operational amplifiers. Intended for the portable instrumentation marketplace, the OPx84 family of devices combine the attributes of precision, wide bandwidth, and low noise to make them a superb choice in single-supply applications that require both ac and precision dc performance. Other low supply voltage applications for which the OP284 is well suited are active filters, audio microphone preamplifiers, power supply control, and telecommunications. To combine all of these attributes with rail-to-rail input/output operation, novel circuit design techniques are used.

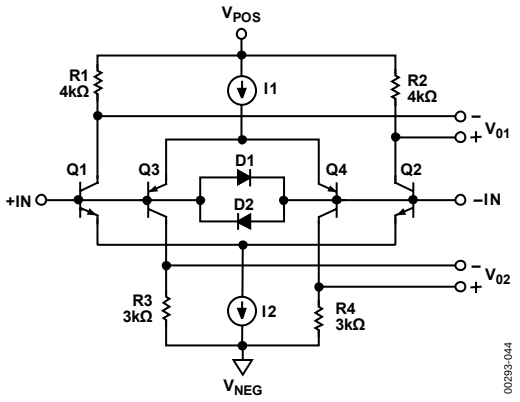


Figure 44. OP284 Equivalent Input Circuit

For example, Figure 44 illustrates a simplified equivalent circuit for the input stage of the OP184/OP284/OP484. It comprises an NPN differential pair, Q1→Q2, and a PNP differential pair, Q3→Q4, operating concurrently. Diode Network D1→Diode Network D2 serves to clamp the applied differential input voltage to the OP284, thereby protecting the input transistors against avalanche damage. Input stage voltage gains are kept low for input rail-to-rail operation. The two pairs of differential output voltages are connected to the OP284's second stage, which is a compound folded cascade gain stage. It is also in the second gain stage, where the two pairs of differential output voltages are combined into a single-ended, output signal voltage used to drive the output stage. A key issue in the input stage is the behavior of the input bias currents over the input common-mode voltage range. Input bias currents in the OP284 are the arithmetic sum of the base currents in Q1→Q3 and in Q2→Q4. As a result of this design approach, the input bias currents in the OP284 not only exhibit different amplitudes; they also exhibit different polarities. This effect is best illustrated by Figure 10. It is, therefore, of paramount importance that the effective source impedances connected to the OP284 inputs be balanced for optimum dc and ac performance.

To achieve rail-to-rail output, the OP284 output stage design employs a unique topology for both sourcing and sinking current. This circuit topology is illustrated in Figure 45. The output stage is voltage-driven from the second gain stage. The signal path through the output stage is inverting; that is, for positive input signals, Q1 provides the base current drive to Q6 so that it conducts (sinks) current. For negative input signals, the signal path via Q1→Q2→D1→Q4→Q3 provides the base current drive for Q5 to conduct (source) current. Both amplifiers provide output current until they are forced into saturation, which occurs at approximately 20 mV from the negative supply rail and 100 mV from the positive supply rail.

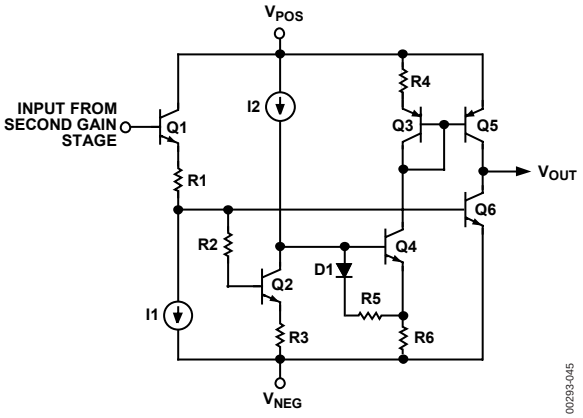


Figure 45. OP284 Equivalent Output Circuit

Thus, the saturation voltage of the output transistors sets the limit on the OP284 maximum output voltage swing. Output short-circuit current limiting is determined by the maximum signal current into the base of Q1 from the second gain stage. Under output short-circuit conditions, this input current level is approximately 100 μA. With transistor current gains around 200, the short-circuit current limits are typically 20 mA. The output stage also exhibits voltage gain. This is accomplished by the use of common-emitter amplifiers, and, as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a dependence to the total load resistance at the output of the OP284.

INPUT OVERVOLTAGE PROTECTION

As with any semiconductor device, if conditions exist where the applied input voltages to the device exceed either supply voltage, the input overvoltage I-V characteristic of the device must be considered. When an overvoltage occurs, the amplifier could be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current. Figure 46 illustrates the overvoltage I-V characteristic of the OP284. This graph was generated with the supply pins connected to GND and a curve tracer's collector output drive connected to the input.

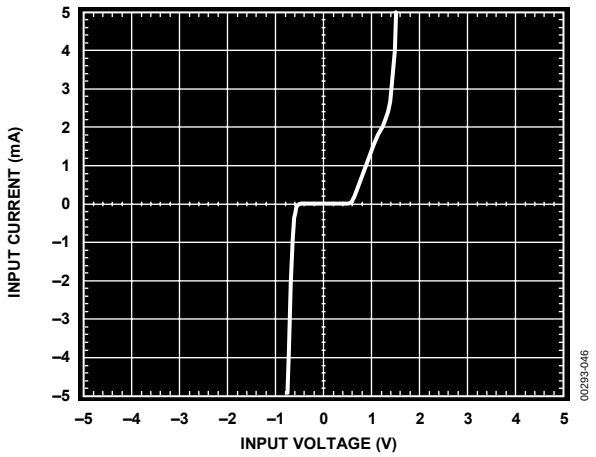


Figure 46. Input Overvoltage I-V Characteristics of the OP284

As shown in Figure 46, internal p-n junctions to the OP284 energize and permit current flow from the inputs to the supplies when the input is 1.8 V more positive and 0.6 V more negative than the respective supply rails. As illustrated in the simplified equivalent circuit shown in Figure 44, the OP284 does not have any internal current limiting resistors; thus, fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, provided that it is limited to 5 mA or less. For the OP284, once the input exceeds the negative supply by 0.6 V, the input current quickly exceeds 5 mA. If this condition continues to exist, an external series resistor should be added at the expense of additional thermal noise. Figure 47 illustrates a typical noninverting configuration for an overvoltage-protected amplifier where the series resistance, R_S, is chosen such that

$$R_S = \frac{V_{IN(MAX)} - V_{SUPPLY}}{5\text{ mA}}$$

For example, a 1 kΩ resistor protects the OP284 against input signals up to 5 V above and below the supplies. For other configurations where both inputs are used, then each input should be protected against abuse with a series resistor. Again, in order to ensure optimum dc and ac performance, it is recommended to balance source impedance levels. For more information on the general overvoltage characteristics of amplifiers, please refer to the *1993 System Applications Guide*, Section 1, Pages 56-69. This reference textbook is available from the Analog Devices Literature Center.

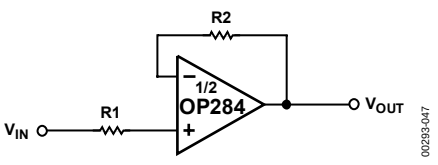


Figure 47. Resistance in Series with Input Limits Overvoltage Currents to Safe Values

OUTPUT PHASE REVERSAL

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically, for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, prevent input signal excursions from exceeding the device's negative supply (that is, GND), preventing a condition that causes the output voltage to change phase. JFET-input amplifiers can also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The OP284 is free from reasonable input voltage range restrictions, provided that input voltages no greater than the supply voltages are applied. Although device output does not change phase, large currents can flow through the input protection diodes as shown in Figure 46. Therefore, the technique recommended in the Input Overvoltage Protection section should be applied to those applications where the likelihood of input voltages exceeding the supply voltages is high.

DESIGNING LOW NOISE CIRCUITS IN SINGLE-SUPPLY APPLICATIONS

In single-supply applications, devices like the OP284 extend the dynamic range of the application through the use of rail-to-rail operation. In fact, the OPx84 family is the first of its kind to combine single-supply, rail-to-rail operation and low noise in one device. It is the first device in the industry to exhibit an input noise voltage spectral density of less than 4 nV/√Hz at 1 kHz. It was also designed specifically for low-noise, single-supply applications, and as such, some discussion on circuit noise concepts in single-supply applications is appropriate.

Referring to the op amp noise model circuit configuration illustrated in Figure 48, the expression for an amplifier's total equivalent input noise voltage for a source resistance level, R_S, is given by

$$e_{nT} = \sqrt{2\left[\left(e_{nR}\right)2 + \left(i_{nOA} \times R\right)^2\right] + \left(e_{nOA}\right)^2}\text{, units in } \frac{V}{\sqrt{Hz}}$$

where:

$R_S = 2R$ is the effective, or equivalent, circuit source resistance.

$(e_{nOA})^2$ is the op amp equivalent input noise voltage spectral power (1 Hz BW).

$(i_{nOA})^2$ is the op amp equivalent input noise current spectral power (1 Hz BW).

$(e_{nR})^2$ is the source resistance thermal noise voltage power (4 kTR).

k = Boltzmann's constant = 1.38×10^{-23} J/K.

T is the ambient temperature in Kelvins of the circuit = 273.15 + T_A (°C).

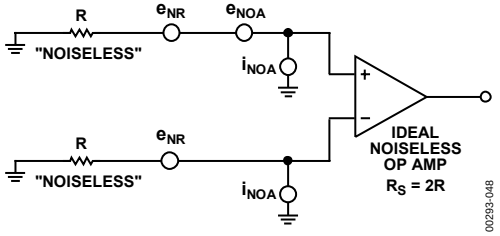


Figure 48. Op Amp Noise Circuit Model Used to Determine Total Circuit Equivalent Input Noise Voltage and Noise Figure

As a design aid, Figure 49 shows the total equivalent input noise of the OP284 and the total thermal noise of a resistor for comparison. Note that for source resistance less than 1 kΩ, the equivalent input noise voltage of the OP284 is dominant.

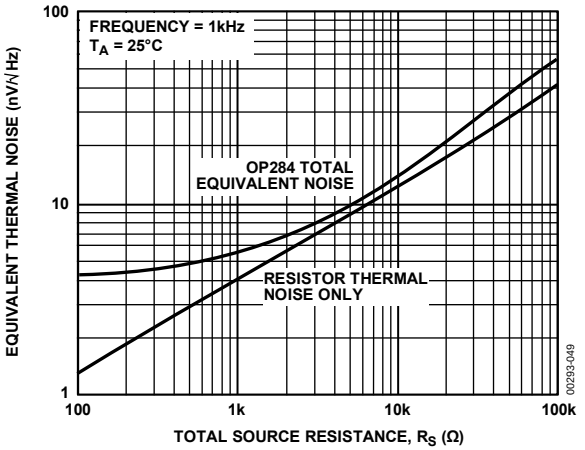


Figure 49. OP284 Total Noise vs. Source Resistance

Because circuit SNR is the critical parameter in the final analysis, the noise behavior of a circuit is often expressed in terms of its noise figure, NF. Noise figure is defined as the ratio of a circuit's output signal-to-noise to its input signal-to-noise. An expression of a circuit NF in dB, and in terms of the operational amplifier voltage and current noise parameters defined previously, is given by

$$NF(dB) = 10\log\left[1+\left(\frac{(e_{nOA})^2+(i_{nOA}\ R_S)^2}{(e_{nRS})^2}\right)\right]$$

where:

NF (dB) is the noise figure of the circuit, expressed in dB.

R_S is the effective, or equivalent, source resistance presented to the amplifier.

$(e_{nOA})^2$ is the OP284 noise voltage spectral power (1 Hz BW).

$(i_{nOA})^2$ is the OP284 noise current spectral power (1 Hz BW).

$(e_{nRS})^2$ is the source resistance thermal noise voltage power = $(4kTR_S)$.

Circuit noise figure is straightforward to calculate because the signal level in the application is not required to determine it. However, many designers using NF calculations as the basis for achieving optimum SNR believe that low noise figure is equal to low total noise. In fact, the opposite is true, as shown in Figure 50. Here, the noise figure of the OP284 is expressed as a function of the source resistance level. Note that the lowest noise figure for the OP284 occurs at a source resistance level of 10 kΩ. However, Figure 49 shows that this source resistance level and the OP284 generate approximately 14 nV/√Hz of total equivalent circuit noise. Signal levels in the application invariably increase to maximize circuit SNR, which is not an option in low voltage, single-supply applications.

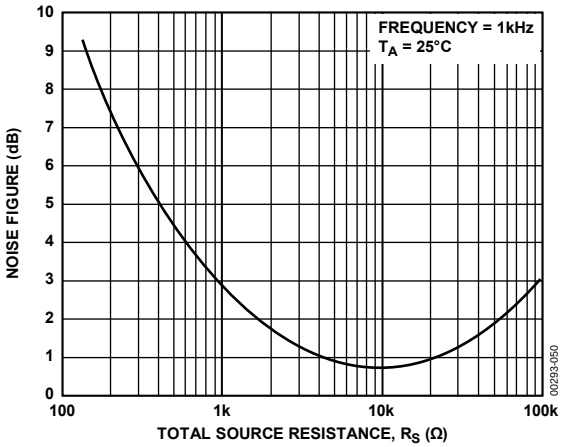


Figure 50. OP284 Noise Figure vs. Source Resistance

In single-supply applications, therefore, it is recommended for optimum circuit SNR to choose an operational amplifier with the lowest equivalent input noise voltage and to choose source resistance levels consistent in maintaining low total circuit noise.

OVERDRIVE RECOVERY

The overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to its linear region from a saturated condition. The recovery time is important in applications where the amplifier must recover quickly after a large transient event. The circuit shown in Figure 51 was used to evaluate the OP284 overload recovery time. The OP284 takes approximately 2 µs to recover from positive saturation and approximately 1 µs to recover from negative saturation.

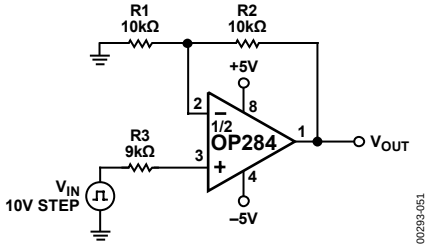


Figure 51. Output Overload Recovery Test Circuit

SINGLE-SUPPLY, 3 V INSTRUMENTATION AMPLIFIER

The low noise, wide bandwidth, and rail-to-rail input/output operation of the OP284 make it ideal for low supply voltage applications such as in the two op amp instrumentation amplifier shown in Figure 52. The circuit uses the classic two op amp instrumentation amplifier topology with four resistors to set the gain. The transfer equation of the circuit is identical to that of a noninverting amplifier. Resistor R2 and Resistor R3 should be closely matched to each other, as well as to Resistors (R1 + P1) and Resistor R4 to ensure good common-mode rejection performance. Resistor networks should be used in this circuit for R2 and R3 because they exhibit the necessary relative tolerance matching for good performance. Matched networks also exhibit tight relative resistor temperature coefficients for good circuit temperature stability. Trimming Potentiometer P1 is used for optimum dc CMR adjustment, and C1 is used to optimize ac CMR. With the circuit values as shown, Circuit CMR is better than 80 dB over the frequency range of 20 Hz to 20 kHz. Circuit RTI (Referred-to-Input) noise in the 0.1 Hz to 10 Hz band is an impressively low 0.45 µV p-p. Resistor RP1 and Resistor RP2 serve to protect the OP284 inputs against input overvoltage abuse. Capacitor C2 can be included to the limit circuit bandwidth and, therefore, wide bandwidth noise in sensitive applications. The value of this capacitor should be adjusted depending on the required closed-loop bandwidth of the circuit. The R4 to C2 time constant creates a pole at a frequency equal to

$$f(3\,dB) = \frac{1}{2\pi R4\,C2}$$

2.5 V REFERENCE FROM A 3 V SUPPLY

In many single-supply applications, the need for a 2.5 V reference often arises. Many commercially available monolithic 2.5 V references require at least a minimum operating supply of 4 V. The problem is exacerbated when the minimum operating supply voltage is 3 V. The circuit illustrated in Figure 53 is an example of a 2.5 V reference that operates from a single 3 V supply. The circuit takes advantage of the OP284 rail-to-rail input/output voltage ranges to amplify an AD589 1.235 V output to 2.5 V.

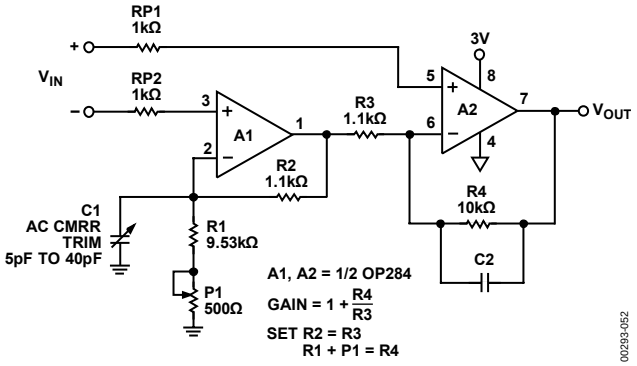


Figure 52. Single Supply, 3 V Low Noise Instrumentation Amplifier

The low TCV_{OS} of the OP284 at 1.5 µV/°C helps maintain an output voltage temperature coefficient that is dominated by the temperature coefficients of R2 and R3. In this circuit with 100 ppm/°C TCR resistors, the output voltage exhibits a temperature coefficient of 200 ppm/°C. Lower tempco resistors are recommended for more accurate performance over temperature.

One measure of the performance of a voltage reference is its capacity to recover from sudden changes in load current. While sourcing a steady-state load current of 1 mA, this circuit recovers to 0.01% of the programmed output voltage in 1.5 µs for a total change in load current of ±1 mA.

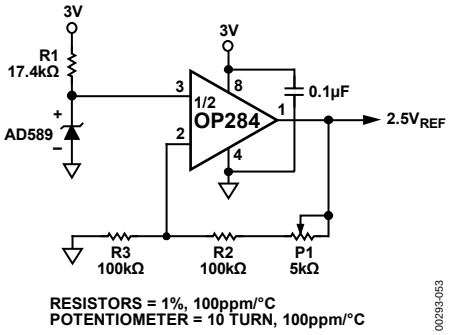


Figure 53. 2.5 V Reference That Operates on a Single 3 V Supply

5 V ONLY, 12-BIT DAC SWINGS RAIL-TO-RAIL

The OP284 is ideal for use with a CMOS DAC to generate a digitally controlled voltage with a wide output range. Figure 54 shows a DAC8043 used in conjunction with the AD589 to generate a voltage output from 0 V to 1.23 V. The DAC is actually operating in voltage switching mode, where the reference is connected to the current output, I_{OUT}, and the output voltage is taken from the V_{REF} pin. This topology is inherently noninverting, as opposed to the classic current output mode, which is inverting and not usable in single-supply applications.

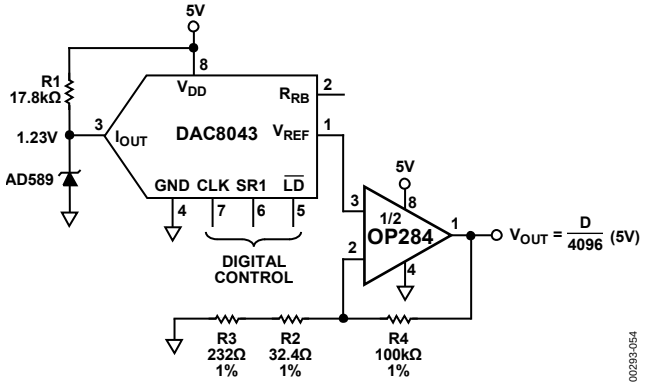


Figure 54. 5 V Only, 12-Bit DAC Swings Rail-to-Rail

In this application the OP284 serves two functions. First, it buffers the high output impedance of the DAC's V_{REF} pin, which is on the order of 10 kΩ. The op amp provides a low impedance output to drive any following circuitry.

Second, the op amp amplifies the output signal to provide a rail-to-rail output swing. In this particular case, the gain is set to 4.1 so that the circuit generates a 5 V output when the DAC output is at full scale. If other output voltage ranges are needed, such as $0\ V \le V_{OUT} \le 4.095\ V$, the gain can be easily changed by adjusting the values of R2 and R3.

HIGH-SIDE CURRENT MONITOR

In the design of power supply control circuits, a great deal of design effort is focused on ensuring the long-term reliability a of a pass transistor over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. The circuit illustrated in Figure 55 is an example of a 3 V, single-supply, high-side current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. This design uses an OP284's rail-to-rail input voltage range to sense the voltage drop across a 0.1 Ω current shunt. A p-channel MOSFET used as the feedback element in the circuit converts the op amp's differential input voltage into a current. This current is applied to R2 to generate a voltage that is a linear representation of the load current. The transfer equation for the current monitor is given by

$$Monitor\ Output = R2 \times \left(\frac{R_{SENSE}}{R1} \right) \times I_L$$

For the element values shown, the transfer characteristic of the monitor output is 2.5 V/A.

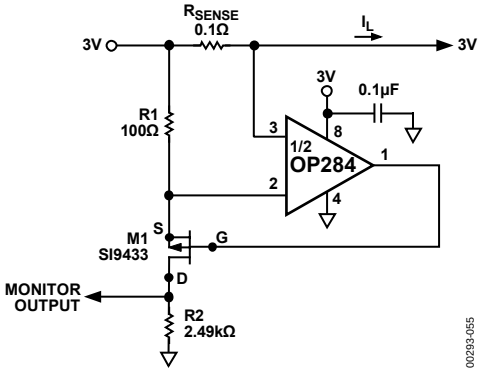


Figure 55. High-Side Load Current Monitor

CAPACITIVE LOAD DRIVE CAPABILITY

The OP284 exhibits excellent capacitive load driving capabilities. It can drive up to 1 nF, as shown in Figure 28. Even though the device is stable, a capacitive load does not come without penalty in bandwidth. The bandwidth is reduced to less than 1 MHz for loads greater than 2 nF. A snubber network on the output does not increase the bandwidth, but it does significantly reduce the amount of overshoot for a given capacitive load.

A snubber consists of a series R-C network (R_S, C_S), as shown in Figure 56, connected from the output of the device to ground. This network operates in parallel with the load capacitor, C_L, to provide the necessary phase lag compensation. The value of the resistor and capacitor is best determined empirically.

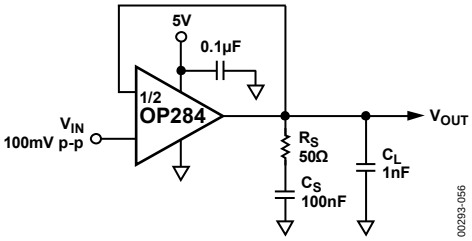


Figure 56. Snubber Network Compensates for Capacitive Load

The first step is to determine the value of Resistor R_S. A good starting value is 100 Ω (typically, the optimum value is less than 100 Ω). This value is reduced until the small-signal transient response is optimized. Next, C_S is determined; 10 µF is a good starting point. This value is reduced to the smallest value for acceptable performance (typically, 1 µF). For the case of a 10 nF load capacitor on the OP284, the optimal snubber network is a 20 Ω in series with 1 µF. The benefit is immediately apparent, as shown in the scope photo in Figure 57. The top trace was taken with a 1 nF load, and the bottom trace was taken with the 50 Ω, 100 nF snubber network in place. The amount of overshoot and ringing is dramatically reduced. Table 6 shows a few sample snubber networks for large load capacitors.

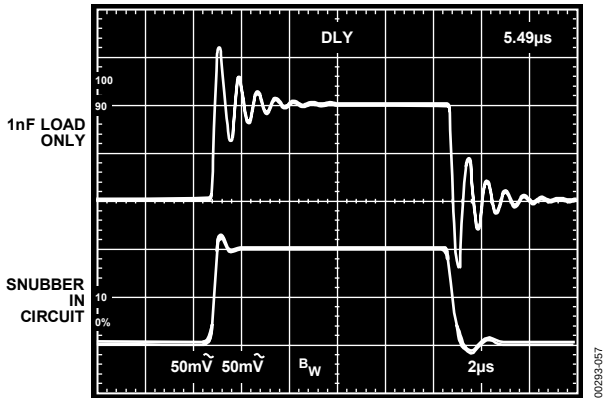


Figure 57. Overshoot and Ringing Is Reduced by Adding a Snubber Network in Parallel with the 1 nF Load

Table 6. Snubber Networks for Large Capacitive Loads

Load Capacitance (C_L)	Snubber Network (R_S, C_S)
1 nF	50 Ω, 100 nF
10 nF	20 Ω, 1 µF
100 nF	5 Ω, 10 µF

LOW DROPOUT REGULATOR WITH CURRENT LIMITING

Many circuits require stable, regulated voltages relatively close in potential to an unregulated input source. This low dropout type of regulator is readily implemented with a rail-to-rail output op amp, such as the OP284, because the wide output swing allows easy drive to a low saturation voltage pass device. Furthermore, it is particularly useful when the op amp also employs a rail-to-rail input feature because this factor allows it to perform high-side current sensing for positive rail current limiting. Typical examples are voltages developed from 3 V to 9 V range system sources or anywhere that low dropout performance is required for power efficiency. This 4.5 V example here works from 5 V nominal sources with worst-case levels down to 4.6 V or less. Figure 58 shows such a regulator set up, using an OP284 plus a low $R_{DS(ON)}$, P-channel MOSFET pass device. Part of the low dropout performance of this circuit is provided by Q1, which has a rating of 0.11 Ω with a gate drive voltage of only 2.7 V. This relatively low gate drive threshold allows operation of the regulator on supplies as low as 3 V without compromising overall performance.

The circuit's main voltage control loop operation is provided by U1B, half of the OP284. This voltage control amplifier amplifies the 2.5 V reference voltage produced by Three Terminal U2, a REF192. The regulated output voltage V_{OUT} is then

$$V_{OUT} = V_{OUT2}\left(1+\frac{R2}{R3}\right)$$

For this example, because V_{OUT} of 4.5 V with V_{OUT2} = 2.5 V requires a U1B gain of 1.8 times, R3 and R2 are chosen for a ratio of 1.2:1 or 10.0 kΩ:8.06 kΩ (using closest 1% values). Note that for the lowest V_{OUT} dc error, R2||R3 should be maintained equal to R1 (as in this example), and the R2 to R3 resistors should be stable, close tolerance metal film types. The table in Figure 58 summarizes R1 to R3 values for some popular voltages. However, note that, in general, the output can be anywhere between V_{OUT2} and the 12 V maximum rating of Q1.

While the low voltage saturation characteristic of Q1 is a key part of the low dropout, another component is a low current sense comparison threshold with good dc accuracy. Here, this is provided by Current Sense Amplifier U1A, which is provided by a 20 mV reference from the 1.235 V, AD589 Reference Diode D2 and the R7 to R8 divider. When the product of the output current and the R_S value match this voltage threshold, the current control loop is activated, and U1A drives the Q1 gate through D1. This causes the overall circuit operation to enter current mode control with a current limit, I_{LIMIT}, defined as

$$I_{LIMIT} = \left(\frac{V_{R(D2)}}{R_S}\right)\left(\frac{R7}{R7+R8}\right)$$

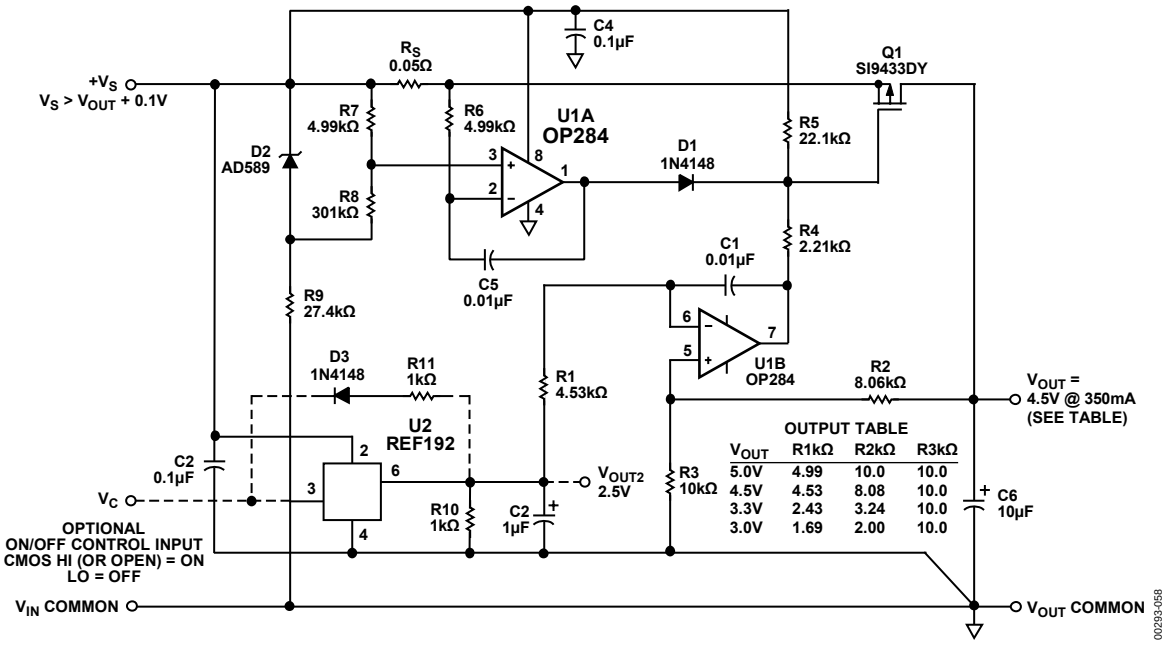


Figure 58. Low Dropout Regulator with Current Limiting

Obviously, it is desirable to keep this comparison voltage small because it becomes a significant portion of the overall dropout voltage. Here, the 20 mV reference is higher than the typical offset of the OP284 but is still reasonably low as a percentage of V_{OUT} (<0.5%). In adapting the limiter for other I_{LIMIT} levels, Sense Resistor R_S should be adjusted along with R7 to R8, to maintain this threshold voltage between 20 mV and 50 mV.

Performance of the circuit is excellent. For the 4.5 V output version, the measured dc output change for a 225 mA load change was on the order of a few micro volts, while the dropout voltage at this same current level was about 30 mV. The current limit, as shown, is 400 mA, allowing the circuit to be used at levels up to 300 mA or more. While the Q1 device can actually support currents of several amperes, a practical current rating takes into account the 2.5 W, 25°C dissipation of the the SOIC-8 device. Because a short-circuit current of 400 mA at an input level of 5 V causes a 2 W dissipation in Q1, other input conditions should be considered carefully in terms of potential overheating of Q1. Of course, if higher powered devices are used for Q1, this circuit can support outputs of tens of amperes as well as the higher V_{OUT} levels already noted.

The circuit shown can be used as either a standard low dropout regulator, or it can be used with on/off control. By driving Pin 3 of U1 with the optional logic control signal, V_C, the output is switched between on and off. Note that when the output is off in this circuit, it is still active (that is, not an open circuit). This is because the off state simply reduces the voltage input to R1, leaving the U1A/U1B amplifiers and Q1 still active.

When the on/off control is used, Resistor R10 should be used with U1 to speed on/off switching and to allow the output of the circuit to settle to a nominal zero voltage. Component D3 and Component R11 also aid in speeding up the on/off transition by providing a dynamic discharge path for C2. Off/on transition time is less than 1 ms, while the on/off transition is longer, but less than 10 ms.

3 V, 50 HZ/60 HZ ACTIVE NOTCH FILTER WITH FALSE GROUND

To process signals in a single-supply system, it is often best to use a false ground biasing scheme. A circuit that uses this approach is shown in Figure 59. In this circuit, a false ground circuit biases an active notch filter used to reject 50 Hz/60 Hz power line interference in portable patient monitoring equipment.

Notch filters are commonly used to reject power line frequency interference that often obscures low frequency physiological signals, such as heart rates, blood pressure readings, EEGs, and EKGs. This notch filter effectively squelches 60 Hz pickup at a Filter Q of 0.75. Substituting 3.16 kΩ resistors for the 2.67 kΩ resistor in the Twin-T section (R1 through R5) configures the active filter to reject 50 Hz interference.

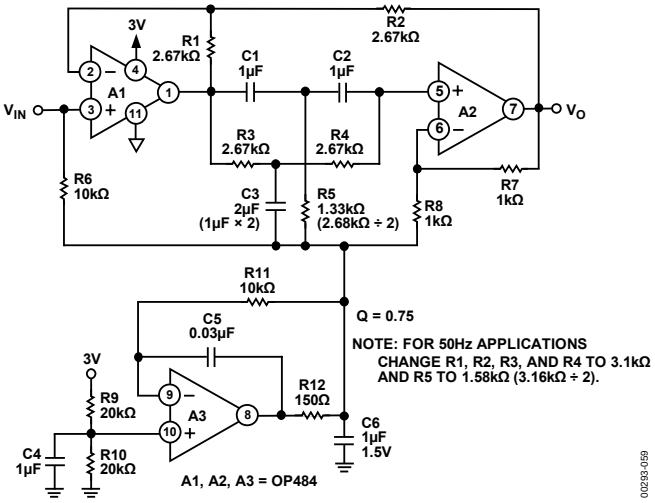
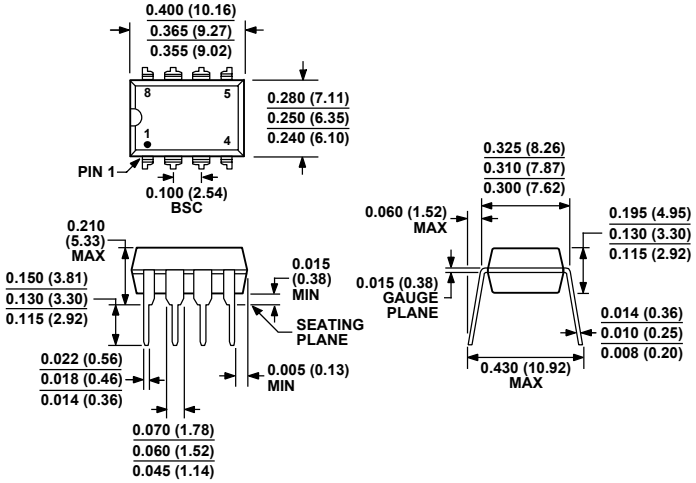


Figure 59. A 3 V Single-Supply, 50Hz to 60 Hz Active Notch Filter with False Ground

Amplifier A3 is the heart of the false ground bias circuit. It buffers the voltage developed at R9 and R10 and is the reference for the active notch filter. Because the OP484 exhibits a rail-to-rail input common-mode range, R9 and R10 are chosen to split the 3 V supply symmetrically. An in-the-loop compensation scheme is used around the OP484 that allows the op amp to drive C6, a 1 µF capacitor, without oscillation. C6 maintains a low impedance ac ground over the operating frequency range of the filter.

The filter section uses an OP484 in a Twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the Twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the pass band symmetry of the filter. Using 1% resistors and 5% capacitors produces satisfactory results.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 60. 8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)
P-Suffix
Dimensions shown in inches and (millimeters)

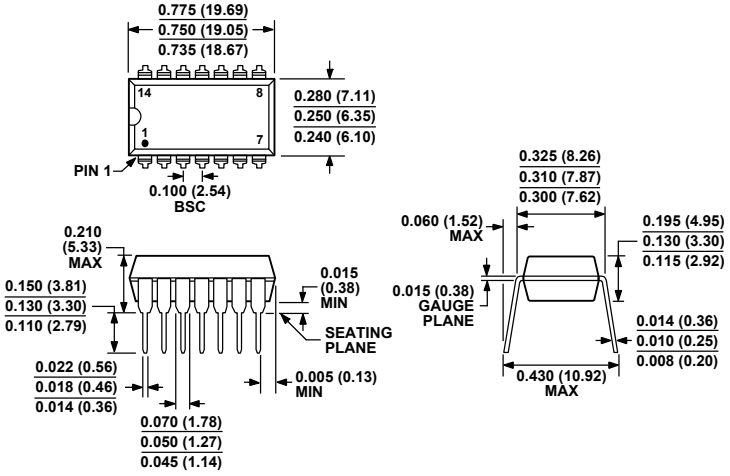


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Figure 61. 14-Lead Plastic Dual-in-Line Package [PDIP]
(N-14)
P-Suffix
Dimensions shown in inches and (millimeters)

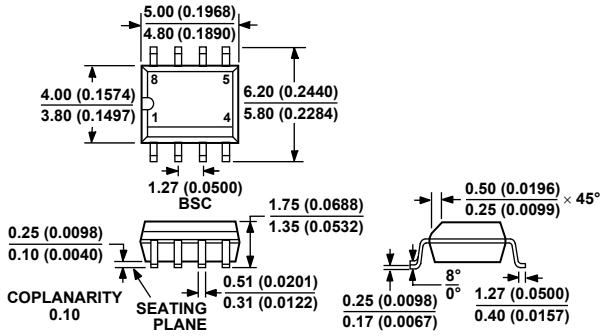

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Figure 62. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)
S-Suffix
Dimensions shown in millimeters and (inches)

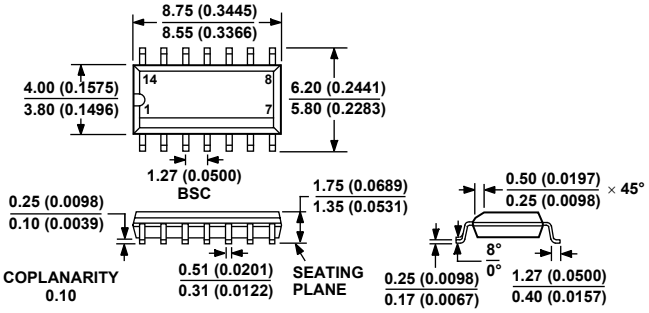

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Figure 63. 14-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-14)
S-Suffix
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP184ES	–40°C to +125°C	8-Lead SOIC	R-8
OP184ES-REEL	–40°C to +125°C	8-Lead SOIC	R-8
OP184ES-REEL7	–40°C to +125°C	8-Lead SOIC	R-8
OP184ESZ[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP184ESZ-REEL[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP184ESZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP184FS	–40°C to +125°C	8-Lead SOIC	R-8
OP184FS-REEL	–40°C to +125°C	8-Lead SOIC	R-8
OP184FS–REEL7	–40°C to +125°C	8-Lead SOIC	R-8
OP184FSZ[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP184FSZ-REEL[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP184FSZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP284EP	–40°C to +125°C	8-Lead PDIP	N-8
OP284EPZ[1]	–40°C to +125°C	8-Lead PDIP	N-8
OP284ES	–40°C to +125°C	8-Lead SOIC	R-8
OP284ES-REEL	–40°C to +125°C	8-Lead SOIC	R-8
OP284ES-REEL7	–40°C to +125°C	8-Lead SOIC	R-8
OP284ESZ[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP284ESZ-REEL[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP284ESZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP284FS	–40°C to +125°C	8-Lead SOIC	R-8
OP284FS-REEL	–40°C to +125°C	8-Lead SOIC	R-8
OP284FS-REEL7	–40°C to +125°C	8-Lead SOIC	R-8
OP284FSZ[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP284FSZ-REEL[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP284FSZ-REEL7[1]	–40°C to +125°C	8-Lead SOIC	R-8
OP284GBC		Die	
OP484ES	–40°C to +125°C	14-Lead SOIC	R-14
OP484ES-REEL	–40°C to +125°C	14-Lead SOIC	R-14
OP484ESZ[1]	–40°C to +125°C	14-Lead SOIC	R-14
OP484ESZ-REEL[1]	–40°C to +125°C	14-Lead SOIC	R-14
OP484FP	–40°C to +125°C	14-Lead PDIP	N-14
OP484FPZ[1]	–40°C to +125°C	14-Lead PDIP	N-14
OP484FS	–40°C to +125°C	14-Lead SOIC	R-14
OP484FS-REEL	–40°C to +125°C	14-Lead SOIC	R-14
OP484FS-REEL7	–40°C to +125°C	14-Lead SOIC	R-14
OP484FSZ[1]	–40°C to +125°C	14-Lead SOIC	R-14
OP484FSZ-REEL[1]	–40°C to +125°C	14-Lead SOIC	R-14
OP484FSZ-REEL7[1]	–40°C to +125°C	14-Lead SOIC	R-14

[1] Z = Pb-free part.

NOTES

NOTES

C00293-0-3/06(C)