PHASE CONTROL SCR's

25 TO 35 AMPERES

GE TYPE		–	C230-2	C231-3	–	C228-9	C35	C38	–	C137
JEDEC		2N681-92*	–	–	2N3870-3 2N3896-9	–	–	–	2N5204-7	–
ELECTRICAL SPECIFICATIONS										
VOLTAGE RANGE		25-800	25-600	25-800	100-600	50-600	25-700	25-800	600-1200	600-1200
FORWARD CONDUCTION										
$I_{T(RMS)}$	Max. RMS on-state current (A)	25	25	25	35	35	35	35	35	35
$I_{T(AV)}$	Max. average on-state current @ 180° conduction (A) @ T_C (°C)	16 @ 65°C	16 @ 70°C	16 @ 70°C	22.5 @ 65°C	20 @ 73°C	22.3 @ 35°C	22.5 @ 70°C	22.3 @ 40°C	22.3 @ 40°C
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)	150	300	300	350	300	150	150	300	350
I^2t	Max. I^2t for fusing for ⩾ 1.5 msec. (A^2 sec)	75	260	260	260	260	75	75	260	350
V_{TM}	Peak on-state voltage @ 25°C, 180° conduction, rated $I_{T(AV)}$ (V)	2.0	1.5	1.5	1.85	1.5	1.6	1.6	1.8	1.8
$R_{\theta JC}$	Max. internal thermal resistance, dc, junction-to-case (°C/W)	1.7	1.0	1.0	.9	1.7	1.7	1.5	1.5	1.0
I_H	Max. holding current @ 25°C (mA)	100	50	50	70	75	100	80	100	100
t_q	Typical turn-off time (μsec) at rated T_J (max.)	–	–	–	40	–	–	25	–	–
$t_d + t_r$	Typical turn-on time (μsec)	1.6	3	3	2	–	1.6	1.6	1.6	1.6
di/dt	Max. rate-of-rise turned-on current (A/μsec)	80	20	20	100	–	80	80	150	150
T_J	Junction operating temperature range (°C)	–65 to 125	–40 to 100	–40 to 100	–40 to 100	–40 to 125	–65 to 125	–65 to 150	–40 to 125	–65 to 125
BLOCKING										
dv/dt	Typical critical rate-of-rise of off-state voltage, Exponential @ max. rated T_J (V/μsec)	50	100	100	50	50	50	20	200	200
FIRING										
I_{GT}	Max. required gate current to trigger (mA) @ –65°C	80	–	–	–	–	80	80	–	80
	@ –40°C	–	40	20	80	80	–	–	80	–
	@ 25°C	40	25	9	40	40	40	40	40	40
V_{GT}	Max. required gate voltage to trigger (V) @ –65°C	3.0	–	–	–	–	3.0	3.0	–	3.0
	@ –40°C	–	2.0	2.0	3.0	3.0	–	–	3.0	–
	@ 25°C	3.0	1.5	1.5	2.0	2.5	3.0	3.0	3.0	3.0
V_{GT}	Min. required gate voltage to trigger @ 100°C	–	0.2	0.2	0.2	–	–	–	–	–
	@ 125°C	0.25	–	–	–	0.2	0.25	–	0.25	0.25
	@ 150°C	–	–	–	–	–	–	0.15	–	–
VOLTAGE TYPES										
Repetitive Peak Forward and Reverse Voltages										
25		2N681	C230/2U	C231/3U	–	C228/9U	C35U	C38U	–	–
50		2N682*	C230/2F	C231/3F	–	C228/9F	C35F	C38F	–	–
100		2N683*	C230/2A	C231/3A	2N3870 2N3896	C228/9A	C35A	C38A	–	–
150		2N684	–	–	–	–	C35G	C38G	–	–
200		2N685*	C230/2B	C231/3B	2N3871 2N3897	C228/9B	C35B	C38B	–	–
250		2N686*	–	–	–	–	C35H	C38H	–	–
300		2N687*	C230/2C	C231/3C	–	C228/9C	C35C	C38C	–	–
400		2N688*	C230/2D	C231/3D	2N3872 2N3898	C228/9D	C35D	C38D	–	–
500		2N689*	C230/2E	C231/3E	–	C228/9E	C35E	C38E	–	C137E
600		2N690	C230/2M	C231/3M	2N3873 2N3899	C228/9M	C35M	–	2N5204	C137M
700		2N691	–	–	–	–	C35S	–	–	C137S
800		2N692	–	–	–	–	–	–	2N5205	C137N
900		–	–	–	–	–	–	–	–	C137T
1000		–	–	–	–	–	–	–	2N5206	C137P
1100		–	–	–	–	–	–	–	–	C137PA
1200		–	–	–	–	–	–	–	2N5207	C137PB
PACKAGE OUTLINE NO.		107	241 (C232) 2, 3, 4, 5 & 6 (C230)	241 (C233) 2, 3, 4, 5 & 6 (C231)	241 242	251 (C229) 2, 3, 4, 5 & 6 (C228)	107	107	107	107

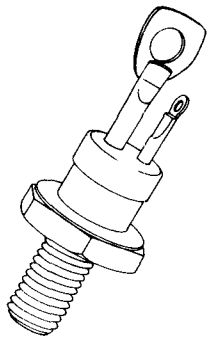
*JAN & JANTX types available.

SCR

2N5204-07

The 2N5204-07 series of silicon controlled rectifiers are reverse blocking triode thyristor semiconductor devices for use in medium power switching and phase control applications requiring blocking voltage up to 1200 volts, and average load current (single-phase, 180° conduction angle) up to 22 amperes.

General Electric's C137 SCR is recommended where a higher level of performance is required for a device of this size.



MAXIMUM ALLOWABLE RATINGS

Type	Repetitive Peak Off-State Voltage, V_{DRM} (1) (2) T_C = −40°C to +125°C	Repetitive Peak Reverse Voltage V_{RRM} (1) (2) T_C = −40°C to +125°C	Non-repetitive Peak Reverse Voltage V_{RSM} (1) (3) T_C = −40°C to +125°C
2N5204	600 Volts†	600 Volts†	720 Volts†
2N5205	800 Volts†	800 Volts†	960 Volts†
2N5206	1000 Volts†	1000 Volts†	1200 Volts†
2N5207	1200 Volts†	1200 Volts†	1440 Volts†

(1) Values apply for gate terminal open-circuited. (Negative gate bias is permissible.)
(2) Maximum case-to-ambient thermal resistance for which maximum V_{DRM} and V_{RRM} ratings apply equals 5.0°C per watt for full sine wave or full-wave rectified sinusoidal volatge waveform. (3.0°C per watt is maximum case-to-ambient thermal resistance for pure dc voltage waveform.)
(3) Half sine wave voltage pulse, 10 millisecond maximum duration.
(4) di/dt rating is established in accordance with EIA Standard RS-397, Section 5.2.2.6. Off-state (blocking) voltage capability may be temporarily lost immediately after each current pulse for duration less than the period of the applied pulse repetition rate. The pulse repetition rate for this test is 400 Hz. The duration of the JEDEC di/dt test condition is 5.0 seconds (minimum).

RMS On-State Current, $I_{T(RMS)}$ ..... 35 Amperes (all conduction angles)
Average On-State Current, $I_{T(AV)}$ ..... Depends on conduction angle (See Charts 3 and 5)
Critical Rate-of-Rise of On-State Current, di/dt: (4)
Gate triggered operation ..... (See Chart 6)
Switching from 1200 volts ..... 75 Amperes per microsecond†
1000 volts ..... 80 Amperes per microsecond†
800 volts ..... 90 Amperes per microsecond†
600 volts ..... 100 Amperes per microsecond†
Breakover voltage triggered operation ..... 10 Amperes per microsecond
Peak One Cycle Surge (non-rep) On-State Current, I_{TSM} ..... 300 Amperes†
I^2t (for fusing), for time = 1.0 milliseconds (See Chart 9) ..... 200 Ampere² seconds
for time = 8.3 milliseconds (See Chart 9) ..... 375 Ampere² seconds
Peak Gate Power Dissipation, P_{GM} ..... 60 Watts for 500 microseconds†
Average Gate Power Dissipation, $P_{G(AV)}$ ..... 10 Watts†
Peak Negative Gate Voltage, V_{GM} ..... 5 Volts†
Storage Temperature, T_{STG} ..... −40°C to +150°C†
Operating Temperature, T_J ..... −40°C to +125°C†
Maximum Stud Torque ..... 30 Lb-in (35 Kg-cm)

†Indicates data included on JEDEC Type Number Registration.

CHARACTERISTICS

Test	Symbol	Min.	Max.	Units	Test Conditions
Peak Off-State or Reverse Current (1)(2)	I_{DRM} or I_{RRM}			mA	$T_C = -40°$ to $+125°C$
2N5204		—	3.3†		$V_{DRM} = V_{RRM} =$ 600 Volts Peak
2N5205		—	2.5†		800
2N5206		—	2.0†		1000
2N5207		—	1.7†		1200
D.C. Gate Trigger Current	I_{GT}	—	40	mAdc	$T_C = +25°C$, $V_D = 12$ Vdc, $R_L = 12$ ohms
		—	80†		$T_C = -40°C$, $V_D = 12$ Vdc, $R_L = 12$ ohms
D.C. Gate Trigger Voltage	V_{GT}	—	3.0	Vdc	$T_C = +25°C$, $V_D = 12$ Vdc, $R_L = 12$ ohms
		—	3.0†		$T_C = -40°C$, $V_D = 12$ Vdc, $R_L = 12$ ohms
		0.25†	—		$T_C = +125°C$, Rated V_{DRM}, $R_L = 1000$ ohms
Peak On-State Voltage	V_{TM}	—	2.3†	Volts	$T_C = +25°C$, $I_{TM} = 70$ A peak, 1 msec wide pulse. Duty cycle $\leqq 2\%$.
Holding Current	I_H			mAdc	Anode supply = 24 Vdc, Gate supply = 10 V, 20 ohms. Initial Forward Current Pulse = 0.5 A, 0.1 to 10.0 msec. wide.
		—	100		$T_C = +25°C$
		—	200†		$T_C = -40°C$
Critical Rate of Rise of Forward Blocking Voltage. (Higher values may cause device switching.)	dv/dt	100†	—	Volts/μsec	$T_C = +125°C$, Rated V_{DRM}, Gate open circuited.
Thermal Resistance	θ_{J-C}	—	1.5†	°C/watt	Junction-to-case, dc

(1) Values apply for gate terminal open-circuited. (Negative gate bias is permissible.)

(2) Maximum case-to-ambient thermal resistance for which maximum V_{DRM} and V_{RRM} ratings apply equals 5.0°C per watt for full sine wave or full-wave rectified sinusoidal voltage waveform. (3.0°C per watt is maximum case-to-ambient thermal resistance for pure dc voltage waveform.)

†Indicates data included on JEDEC Type Number Registration.

OUTLINE DRAWING

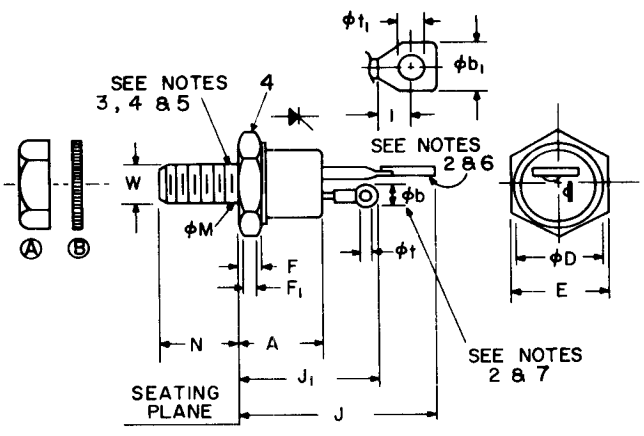
(COMPLIES WITH JEDEC TO-48)

NOTES:

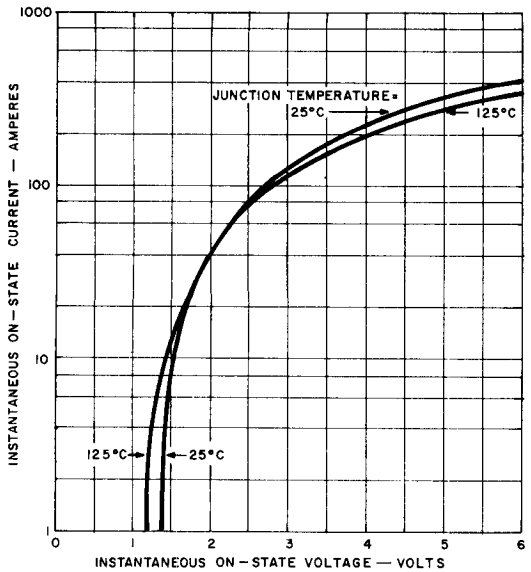
1. Complete threads to extend within 2½ threads of seating plane. Diameter of unthreaded portion. 249" (6.32MM) Maximum, .220" (5.59MM) Minimum.
2. Angular orientation of these terminals is undefined.
3. ¼-28 UNF-2A. Maximum pitch diameter of plated threads shall be basic pitch diameter .2268" (5.76MM), minimum pitch diameter .2225" (5.66MM), reference: screw thread standards for Federal Service 1957, Handbook H28, 1957, P1.
4. A chamfer (or undercut) on one or both ends of hexagonal portions is optional.
5. Case is anode connection.
6. Large terminal is cathode connection.
7. Small terminal is gate connection.
8. Insulating kit available upon request.

A. ¼-28 steel nut, Ni. plated, .178 min. thk.

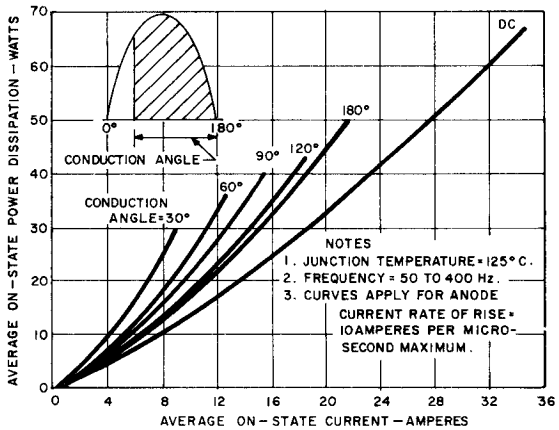
B. Ext. tooth lockwasher, steel, Ni. plated, .023 min. thk.



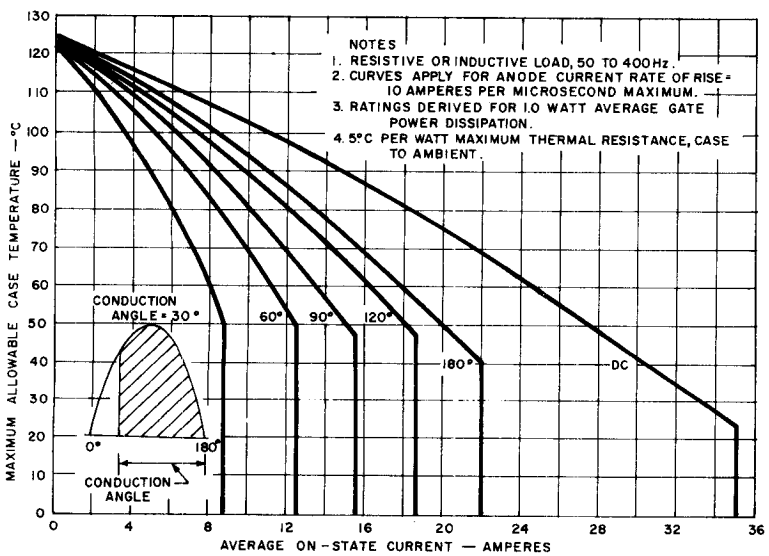
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.330	.505	8.38	12.83	
ϕb	.115	.140	2.92	3.56	2
ϕb_1	.210	.300	5.33	7.62	2
ϕD		.544		13.82	
E	.544	.562	13.82	14.27	
F	.113	.200	2.87	5.08	4
F_1	.060		1.52		
J		1.193		30.30	
J_1		.875		22.23	
I	.120		3.05		
ϕM					1
N	.422	.453	10.72	11.51	
ϕt	.060	.075	1.52	1.91	
ϕt_1	.125	.165	3.18	4.19	
W					3



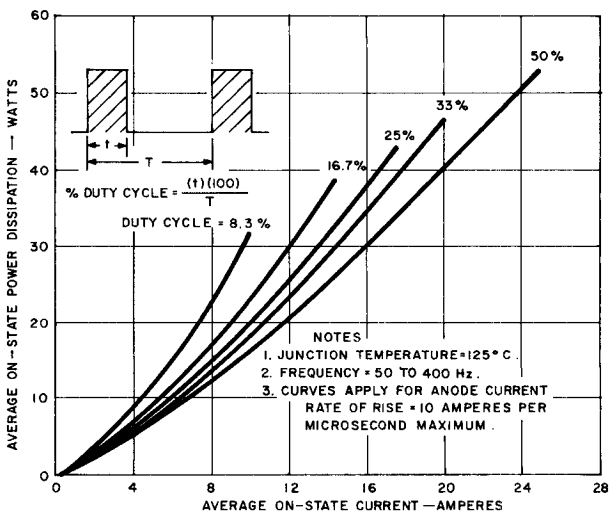
1. MAXIMUM ON-STATE CHARACTERISTICS



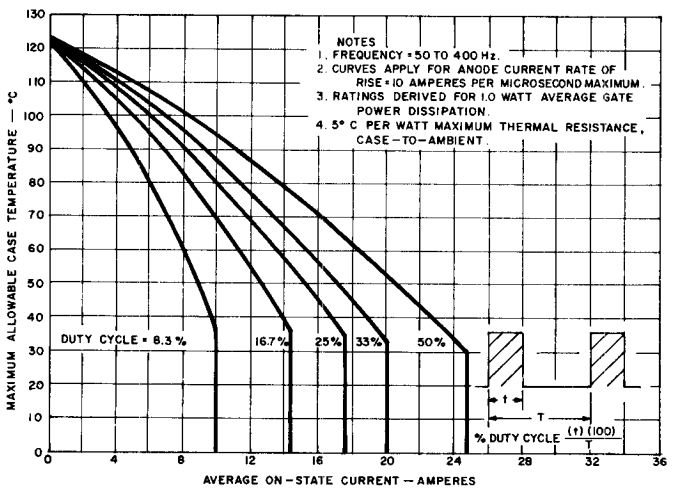
2. MAXIMUM ON-STATE POWER DISSIPATION FOR HALF-WAVE RECTIFIED SINE WAVE OF CURRENT



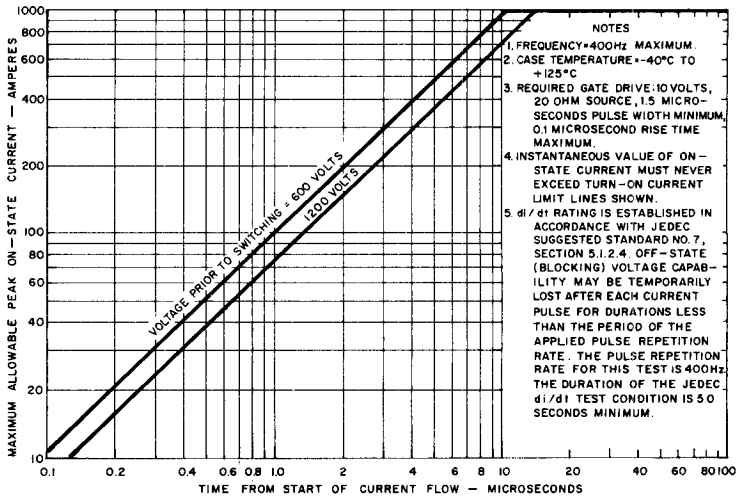
3. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR HALF-WAVE RECTIFIED SINE WAVE OF CURRENT



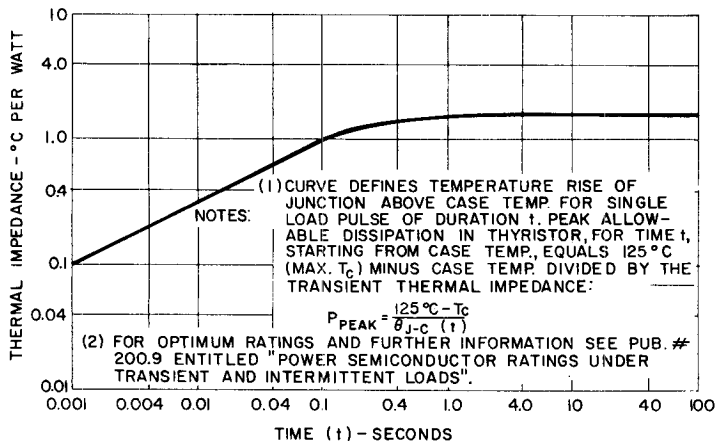
4. MAXIMUM ON-STATE POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



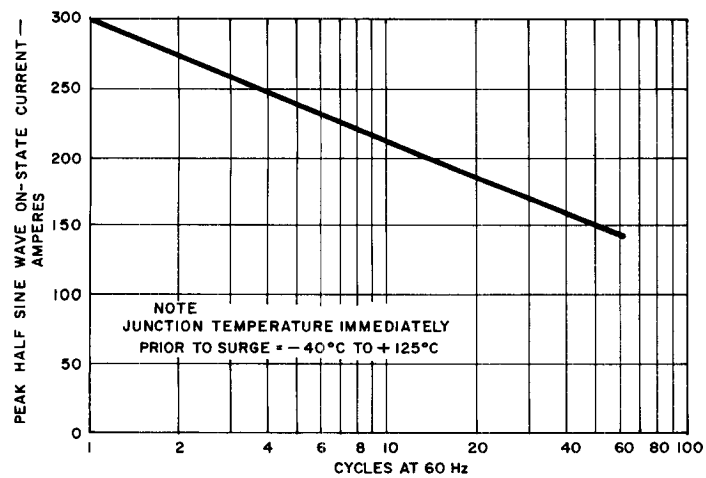
5. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM



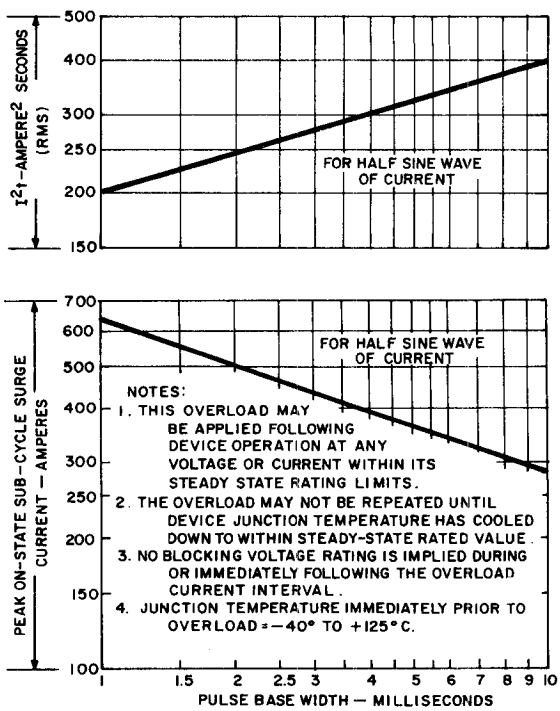
6. TURN-ON CURRENT LIMIT



7. MAXIMUM TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE



8. MAXIMUM ALLOWABLE SURGE (NON-REPETITIVE) ON-STATE CURRENT



9. MAXIMUM ALLOWABLE SUB-CYCLE SURGE (NON-REPETITIVE) ON-STATE CURRENT AND I^2T RATING