

M38A - DVT

06/22/06

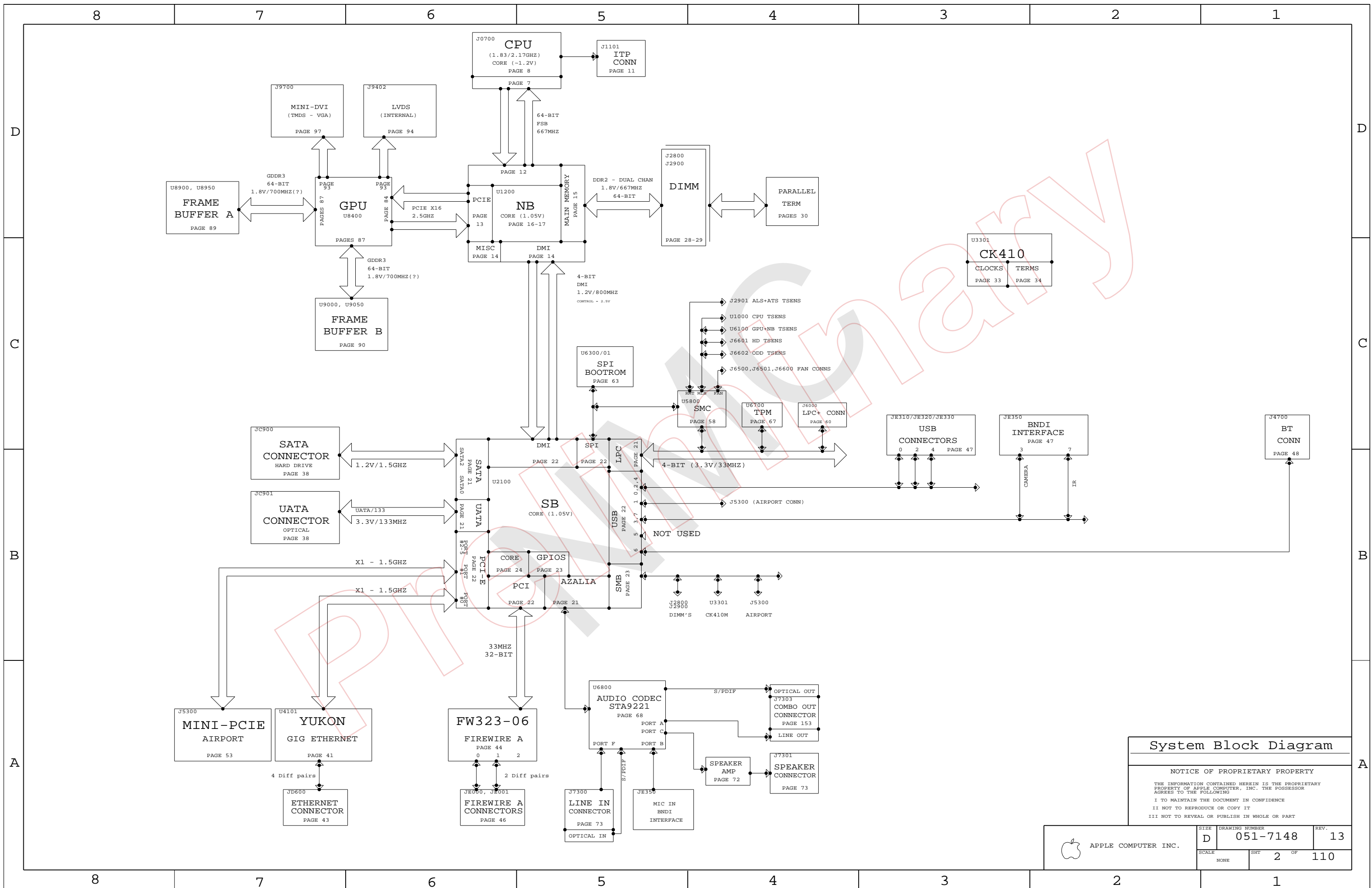
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
13		445818	ENGINEERING RELEASED	06/22/06	06/22/04

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9	MS JD 9	CPU - DECAPS
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14	PS JH 14	NB - MISC INTERFACES
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21	JD 21	SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD 22	SB - PCIE, SPI, USB, DMI, PCI
23	JD 23	SB - SMB, GPIO, PM, CLKS
24	JD 24	SB - POWERS AND GROUNDS
25	JD 25	SB - DECAPS
26	JD 26	SB - MISC
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58	MS 45	SMC - H8S2116
59	MS 46	SMC - SMB BUSSES, MISC
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61	JH 48	SMC - GPU/NB THERMAL SENSOR
RX 63	MS JD 49	SMC - SPI BOOTROM
65	MS 50	SMC - FANS
66	MS 51	SMC - FANS
67	JD 52	SMC - TPM
SO 68	PT JD 53	AUDIO - CODEC, VREG, MIC BIAS
SO 72	PT JD 54	AUDIO - INTERNAL SPEAKER AMP
SO 73	PT JD 55	AUDIO - I/O CONN'S, EMC
SO 74	PT JD 56	AUDIO - DETECT TRANSLATORS
RP 75	RT RT 57	VR - CPU CORE
RP 76	RT RT 58	VR - CPU I-V SENSE CKT
RP 77	RT RT 59	VR - "S0" 1.2V & 2.5V (GRAFIX)
RP 78	RT RT 60	VR - "S0" 1.8V
RP 79	RT RT 61	VR - "S3" 1.8V
RP 80	RT RT 62	VR - "S0" 1.5V
RP 81	RT RT 63	VR - "S0" 1.05V
RP 83	RT RT 64	VR - "S3" 3.3V AND 5V
JH 84	JH JH 65	GPU - M56 PCI-E
M1 85	JH JH 66	GPU - VCORE SUPPLY
M1 86	JH JH 67	GPU - M56 CORE PWR
M1 87	JH JH 68	GPU - M56 FRAME BUFFER
M1 88	JH JH 69	GPU - MISC
M1 89	JH JH 70	GPU - GDDR SDRAM A
M1 90	JH JH 71	GPU - GDDR SDRAM B
M1 91	JH JH 72	GPU - M56 GPIO, DVO, MISC
M1 92	JH JH 73	GPU - M56 CLOCKS
M1 93	JH JH 74	GPU - M56 VIDEO INTERFACES
JH 94	JH JH 75	GPU - INTERNAL DISPLAY CONN'S
JH 95	JH JH 76	GPU - TP'S
JH 96	JH JH 77	GPU - TMDS, INVERTER, EXT VGA
JH 97	JH JH 78	GPU - EXTERNAL DISPLAY CONN'S

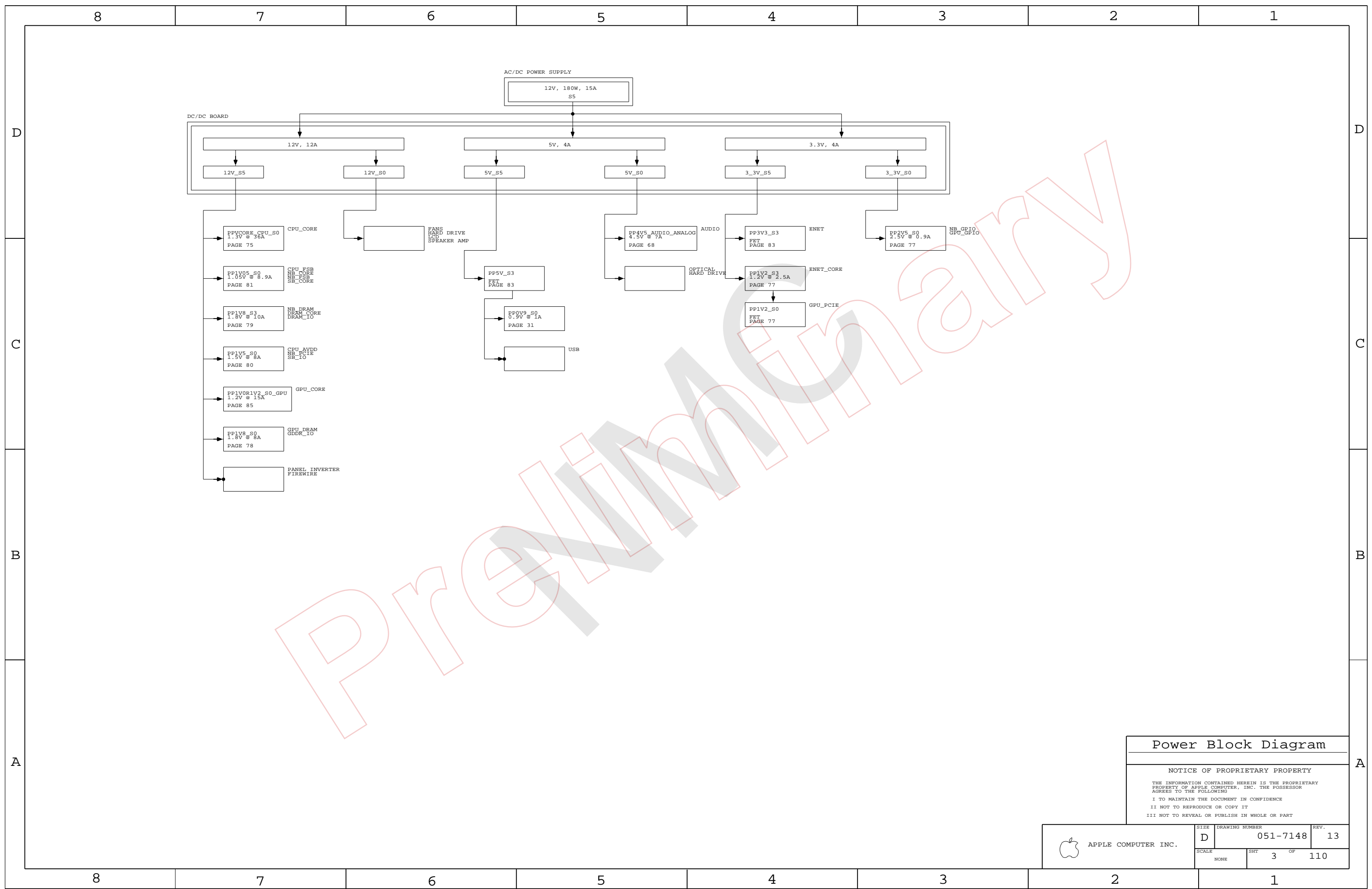
<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	<div style="text-align: center;"> <p>Apple Computer Inc.</p> </div> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small; text-align: center;">II NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small; text-align: center;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <div style="text-align: center;"> <p>TITLE</p> <p>SCH, MLB, M38A</p> </div> <div style="display: flex; justify-content: space-between;"> <p>DRAWING NUMBER</p> <p>051-7148</p> </div> <div style="display: flex; justify-content: space-between;"> <p>REV.</p> <p>13</p> </div>
RELEASE	SCALE	NONE
MATERIAL/FINISH NOTED AS APPLICABLE	SIZE	D
SHEET 1 OF 110		



System Block Diagram

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 2	OF 110



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Power Block Diagram

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	3	110	

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
338S0344	1	IC,ATI,M56P,GRAPHICCTRL,880BGA,LF	U8400	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN SMD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	

341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

128S0078	3	CAP,EL,AL,330UF,204,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	
825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16CK680EX 680UF 16V LP
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330F8 330UF 6.3V LP
128S0080	128S0078		C7517,C7518,C7910	SANYO 165VP330W 330UF 16V SMD LP
124-0338	124-0333		C7501,C8014	CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
353S1321	353S1105		U7910	LM339
378S0141	378S0140		LED01,LED602,LED603	SMD
353S1461	353S1465		U7500	CPU REGULATOR - ISL9504

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7148	1	PCB,SCHM,MLB,M38A	SCH1		17_INCH_LCD
820-2052	1	PCB,FAB,MLB,M38A	MLB1		17_INCH_LCD
341T0040	1	EFI ROM,M38A	U6301	CRITICAL	17_INCH_LCD
114S0264	1	3.01K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_IP2V
341T0039	1	IC,SMC,M38A	U5800	CRITICAL	17_INCH_LCD
338S0315	1	IC,ATI,M56LP,GRAPHIC CTRL,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
114S0287	1	5.11K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_0P953V
114S0281	1	4.53K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_IP0V
337S3299	1	2.00GHZ MEROM	CPU	CRITICAL	2P00_CPU
337S3293	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU

(341S1908 - DEVEL)
(341S1909 - FINAL)
(335S0384 - BLNK)

(341S1907 - PROG)
(338S0274 - BLNK)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

Table Items

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SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE	SHT	OF
NONE	4	110

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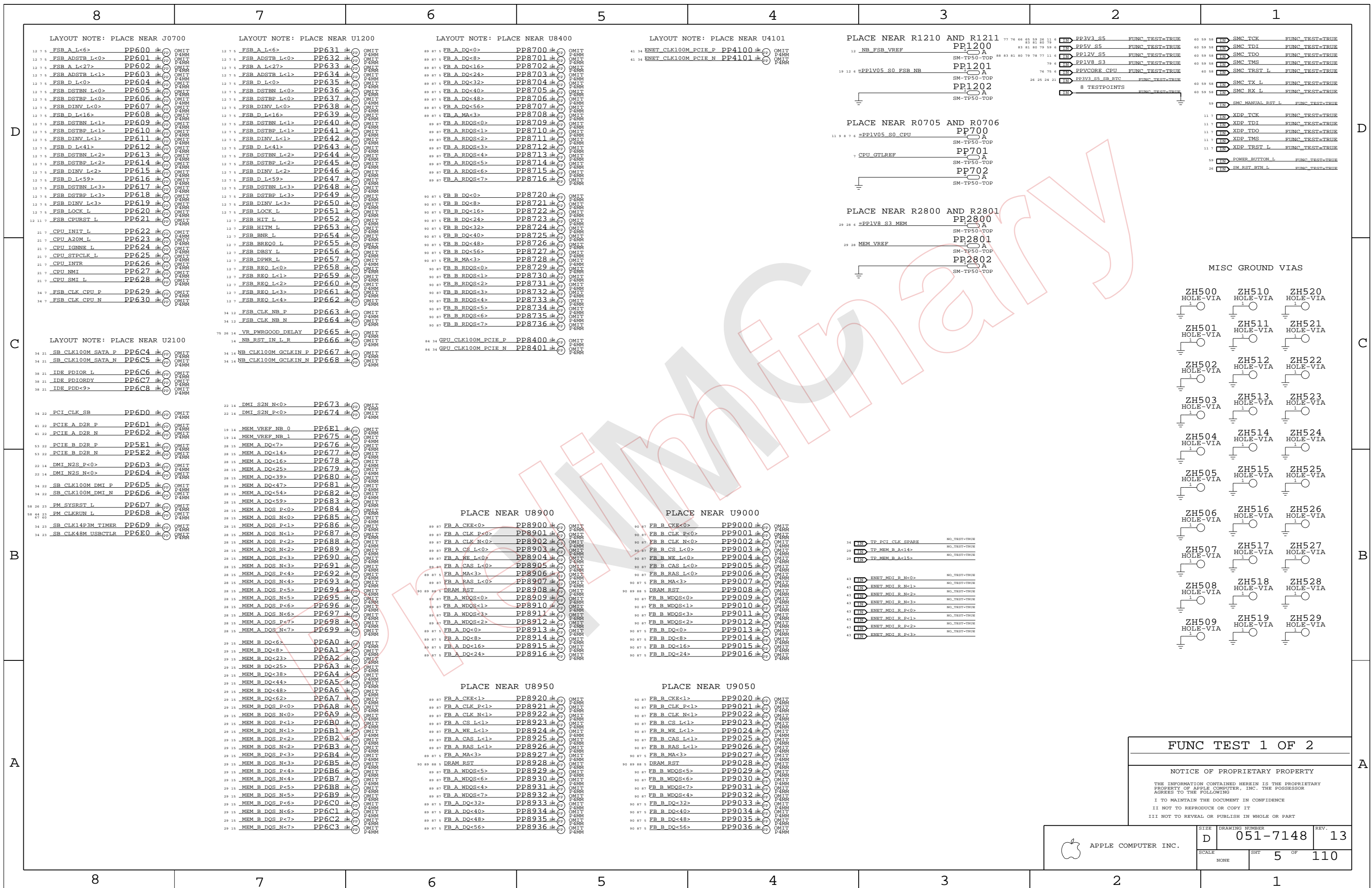
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1



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U8400

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

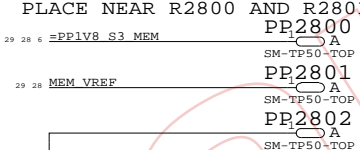
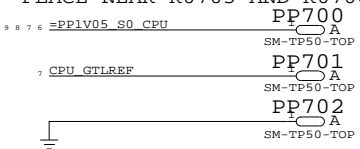
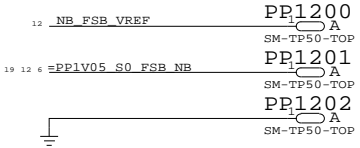
PLACE NEAR R2800 AND R2801

- 12 7 5 FSB A L<6> PP600
- 12 7 5 FSB ADSTB L<0> PP601
- 12 7 5 FSB A L<27> PP602
- 12 7 5 FSB ADSTB L<1> PP603
- 12 7 5 FSB D L<0> PP604
- 12 7 5 FSB DSTBN L<0> PP605
- 12 7 5 FSB DSTBP L<0> PP606
- 12 7 5 FSB DINV L<0> PP607
- 12 7 5 FSB D L<16> PP608
- 12 7 5 FSB DSTBN L<1> PP609
- 12 7 5 FSB DSTBP L<1> PP610
- 12 7 5 FSB DINV L<1> PP611
- 12 7 5 FSB D L<41> PP612
- 12 7 5 FSB DSTBN L<2> PP613
- 12 7 5 FSB DSTBP L<2> PP614
- 12 7 5 FSB DINV L<2> PP615
- 12 7 5 FSB D L<59> PP616
- 12 7 5 FSB DSTBN L<3> PP617
- 12 7 5 FSB DSTBP L<3> PP618
- 12 7 5 FSB DINV L<3> PP619
- 12 7 5 FSB LOCK L PP620
- 12 7 5 FSB CPURST L PP621
- 21 7 CPU INIT L PP622
- 21 7 CPU A20M L PP623
- 21 7 CPU IGNEE L PP624
- 21 7 CPU STCLK L PP625
- 21 7 CPU INTR PP626
- 21 7 CPU NMI PP627
- 21 7 CPU SMI L PP628
- 34 7 FSB CLK CPU P PP629
- 34 7 FSB CLK CPU N PP630

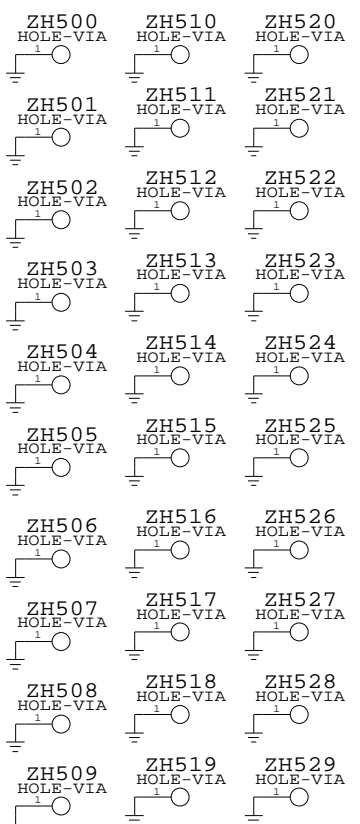
- 12 7 5 FSB A L<6> PP631
- 12 7 5 FSB ADSTB L<0> PP632
- 12 7 5 FSB A L<27> PP633
- 12 7 5 FSB ADSTB L<1> PP634
- 12 7 5 FSB D L<0> PP635
- 12 7 5 FSB DSTBN L<0> PP636
- 12 7 5 FSB DSTBP L<0> PP637
- 12 7 5 FSB DINV L<0> PP638
- 12 7 5 FSB D L<16> PP639
- 12 7 5 FSB DSTBN L<1> PP640
- 12 7 5 FSB DSTBP L<1> PP641
- 12 7 5 FSB DINV L<1> PP642
- 12 7 5 FSB D L<41> PP643
- 12 7 5 FSB DSTBN L<2> PP644
- 12 7 5 FSB DSTBP L<2> PP645
- 12 7 5 FSB DINV L<2> PP646
- 12 7 5 FSB D L<59> PP647
- 12 7 5 FSB DSTBN L<3> PP648
- 12 7 5 FSB DSTBP L<3> PP649
- 12 7 5 FSB DINV L<3> PP650
- 12 7 5 FSB LOCK L PP651
- 12 7 5 FSB HIT L PP652
- 12 7 5 FSB HITM L PP653
- 12 7 5 FSB BNR L PP654
- 12 7 5 FSB BREQ0 L PP655
- 12 7 5 FSB DBSY L PP656
- 12 7 5 FSB DPWR L PP657
- 12 7 5 FSB REQ L<0> PP658
- 12 7 5 FSB REQ L<1> PP659
- 12 7 5 FSB REQ L<2> PP660
- 12 7 5 FSB REQ L<3> PP661
- 12 7 5 FSB REQ L<4> PP662
- 34 12 FSB CLK NB P PP663
- 34 12 FSB CLK NB N PP664

- 88 87 5 FB A DQ<0> PP8700
- 88 87 5 FB A DQ<8> PP8701
- 88 87 5 FB A DQ<16> PP8702
- 88 87 5 FB A DQ<24> PP8703
- 88 87 5 FB A DQ<32> PP8704
- 88 87 5 FB A DQ<40> PP8705
- 88 87 5 FB A DQ<48> PP8706
- 88 87 5 FB A DQ<56> PP8707
- 88 87 5 FB A MA<3> PP8708
- 88 87 5 FB A RDQS<0> PP8709
- 88 87 5 FB A RDQS<1> PP8710
- 88 87 5 FB A RDQS<2> PP8711
- 88 87 5 FB A RDQS<3> PP8712
- 88 87 5 FB A RDQS<4> PP8713
- 88 87 5 FB A RDQS<5> PP8714
- 88 87 5 FB A RDQS<6> PP8715
- 88 87 5 FB A RDQS<7> PP8716
- 90 87 5 FB B DQ<0> PP8720
- 90 87 5 FB B DQ<8> PP8721
- 90 87 5 FB B DQ<16> PP8722
- 90 87 5 FB B DQ<24> PP8723
- 90 87 5 FB B DQ<32> PP8724
- 90 87 5 FB B DQ<40> PP8725
- 90 87 5 FB B DQ<48> PP8726
- 90 87 5 FB B DQ<56> PP8727
- 90 87 5 FB B MA<3> PP8728
- 90 87 5 FB B RDQS<0> PP8729
- 90 87 5 FB B RDQS<1> PP8730
- 90 87 5 FB B RDQS<2> PP8731
- 90 87 5 FB B RDQS<3> PP8732
- 90 87 5 FB B RDQS<4> PP8733
- 90 87 5 FB B RDQS<5> PP8734
- 90 87 5 FB B RDQS<6> PP8735
- 90 87 5 FB B RDQS<7> PP8736

- 41 34 ENET CLK100M PCIE P PP4100
- 41 34 ENET CLK100M PCIE N PP4101
- 84 34 GPU CLK100M PCIE P PP8400
- 84 34 GPU CLK100M PCIE N PP8401



MISC GROUND VIAS



LAYOUT NOTE: PLACE NEAR U2100

- 34 21 SB CLK100M SATA P PP6C4
- 34 21 SB CLK100M SATA N PP6C5
- 38 21 IDE PDIOR L PP6C6
- 38 21 IDE PDIORP PP6C7
- 38 21 IDE PDD<9> PP6C8
- 34 21 PCI CLK SB PP6D0
- 41 22 PCIE A D2R P PP6D1
- 41 22 PCIE A D2R N PP6D2
- 53 22 PCIE B D2R P PP5E1
- 53 22 PCIE B D2R N PP5E2
- 22 14 DMI N2S P<0> PP6D3
- 22 14 DMI N2S N<0> PP6D4
- 34 22 SB CLK100M DMI P PP6D5
- 34 22 SB CLK100M DMI N PP6D6
- 58 26 23 FM SYSRST L PP6D7
- 58 26 23 FM CLKRUN L PP6D8
- 34 23 SB CLK14PM TIMER PP6D9
- 34 23 SB CLK48M USBCTLR PP6E0

- 22 14 DMI S2N N<0> PP673
- 22 14 DMI S2N P<0> PP674
- 19 14 MEM VREF NB 0 PP6E1
- 19 14 MEM VREF NB 1 PP6E2
- 28 15 MEM A DQ<7> PP6E6
- 28 15 MEM A DQ<14> PP6E7
- 28 15 MEM A DQ<16> PP6E8
- 28 15 MEM A DQ<25> PP6E9
- 28 15 MEM A DQ<39> PP6E0
- 28 15 MEM A DQ<47> PP6E1
- 28 15 MEM A DQ<54> PP6E2
- 28 15 MEM A DQ<59> PP6E3
- 28 15 MEM A DQS P<0> PP6E5
- 28 15 MEM A DQS N<0> PP6E6
- 28 15 MEM A DQS P<1> PP6E7
- 28 15 MEM A DQS N<1> PP6E8
- 28 15 MEM A DQS P<2> PP6E9
- 28 15 MEM A DQS N<2> PP6E0
- 28 15 MEM A DQS P<3> PP6E1
- 28 15 MEM A DQS N<3> PP6E2
- 28 15 MEM A DQS P<4> PP6E3
- 28 15 MEM A DQS N<4> PP6E4
- 28 15 MEM A DQS P<5> PP6E5
- 28 15 MEM A DQS N<5> PP6E6
- 28 15 MEM A DQS P<6> PP6E7
- 28 15 MEM A DQS N<6> PP6E8
- 28 15 MEM A DQS P<7> PP6E9
- 28 15 MEM A DQS N<7> PP6E0
- 28 15 MEM B DQ<6> PP6A0
- 28 15 MEM B DQ<8> PP6A1
- 28 15 MEM B DQ<23> PP6A2
- 28 15 MEM B DQ<25> PP6A3
- 28 15 MEM B DQ<38> PP6A4
- 28 15 MEM B DQ<44> PP6A5
- 28 15 MEM B DQ<48> PP6A6
- 28 15 MEM B DQ<62> PP6A7
- 28 15 MEM B DQS P<0> PP6A8
- 28 15 MEM B DQS N<0> PP6A9
- 28 15 MEM B DQS P<1> PP6B0
- 28 15 MEM B DQS N<1> PP6B1
- 28 15 MEM B DQS P<2> PP6B2
- 28 15 MEM B DQS N<2> PP6B3
- 28 15 MEM B DQS P<3> PP6B4
- 28 15 MEM B DQS N<3> PP6B5
- 28 15 MEM B DQS P<4> PP6B6
- 28 15 MEM B DQS N<4> PP6B7
- 28 15 MEM B DQS P<5> PP6B8
- 28 15 MEM B DQS N<5> PP6B9
- 28 15 MEM B DQS P<6> PP6C0
- 28 15 MEM B DQS N<6> PP6C1
- 28 15 MEM B DQS P<7> PP6C2
- 28 15 MEM B DQS N<7> PP6C3

PLACE NEAR U8900

- 88 87 5 FB A CKE<0> PP8900
- 88 87 5 FB A CLK P<0> PP8901
- 88 87 5 FB A CLK N<0> PP8902
- 88 87 5 FB A CS L<0> PP8903
- 88 87 5 FB A WE L<0> PP8904
- 88 87 5 FB A CAS L<0> PP8905
- 88 87 5 FB A MA<3> PP8906
- 88 87 5 FB A RAS L<0> PP8907
- 90 88 5 DRAM RST PP8908
- 90 88 5 FB B WDQS<0> PP8909
- 90 88 5 FB B WDQS<1> PP8910
- 90 88 5 FB B WDQS<3> PP8911
- 90 88 5 FB A WDQS<2> PP8912
- 90 88 5 FB A DQ<0> PP8913
- 90 88 5 FB A DQ<8> PP8914
- 90 88 5 FB A DQ<16> PP8915
- 90 88 5 FB A DQ<24> PP8916

PLACE NEAR U9000

- 90 87 5 FB B CKE<0> PP9000
- 90 87 5 FB B CLK P<0> PP9001
- 90 87 5 FB B CLK N<0> PP9002
- 90 87 5 FB B CS L<0> PP9003
- 90 87 5 FB B WE L<0> PP9004
- 90 87 5 FB B CAS L<0> PP9005
- 90 87 5 FB B MA<3> PP9006
- 90 87 5 FB B RAS L<0> PP9007
- 90 88 5 DRAM RST PP9008
- 90 88 5 FB B WDQS<0> PP9009
- 90 88 5 FB B WDQS<1> PP9010
- 90 88 5 FB B WDQS<3> PP9011
- 90 88 5 FB B WDQS<2> PP9012
- 90 88 5 FB B DQ<0> PP9013
- 90 88 5 FB B DQ<8> PP9014
- 90 88 5 FB B DQ<16> PP9015
- 90 88 5 FB B DQ<24> PP9016

PLACE NEAR U8950

- 88 87 5 FB A CKE<1> PP8920
- 88 87 5 FB A CLK P<1> PP8921
- 88 87 5 FB A CLK N<1> PP8922
- 88 87 5 FB A CS L<1> PP8923
- 88 87 5 FB A WE L<1> PP8924
- 88 87 5 FB A CAS L<1> PP8925
- 88 87 5 FB A RAS L<1> PP8926
- 88 87 5 FB A MA<3> PP8927
- 90 88 5 DRAM RST PP8928
- 90 88 5 FB B WDQS<5> PP8929
- 90 88 5 FB B WDQS<6> PP8930
- 90 88 5 FB B WDQS<4> PP8931
- 90 88 5 FB A WDQS<7> PP8932
- 90 88 5 FB A DQ<32> PP8933
- 90 88 5 FB A DQ<40> PP8934
- 90 88 5 FB A DQ<48> PP8935
- 90 88 5 FB A DQ<56> PP8936

PLACE NEAR U9050

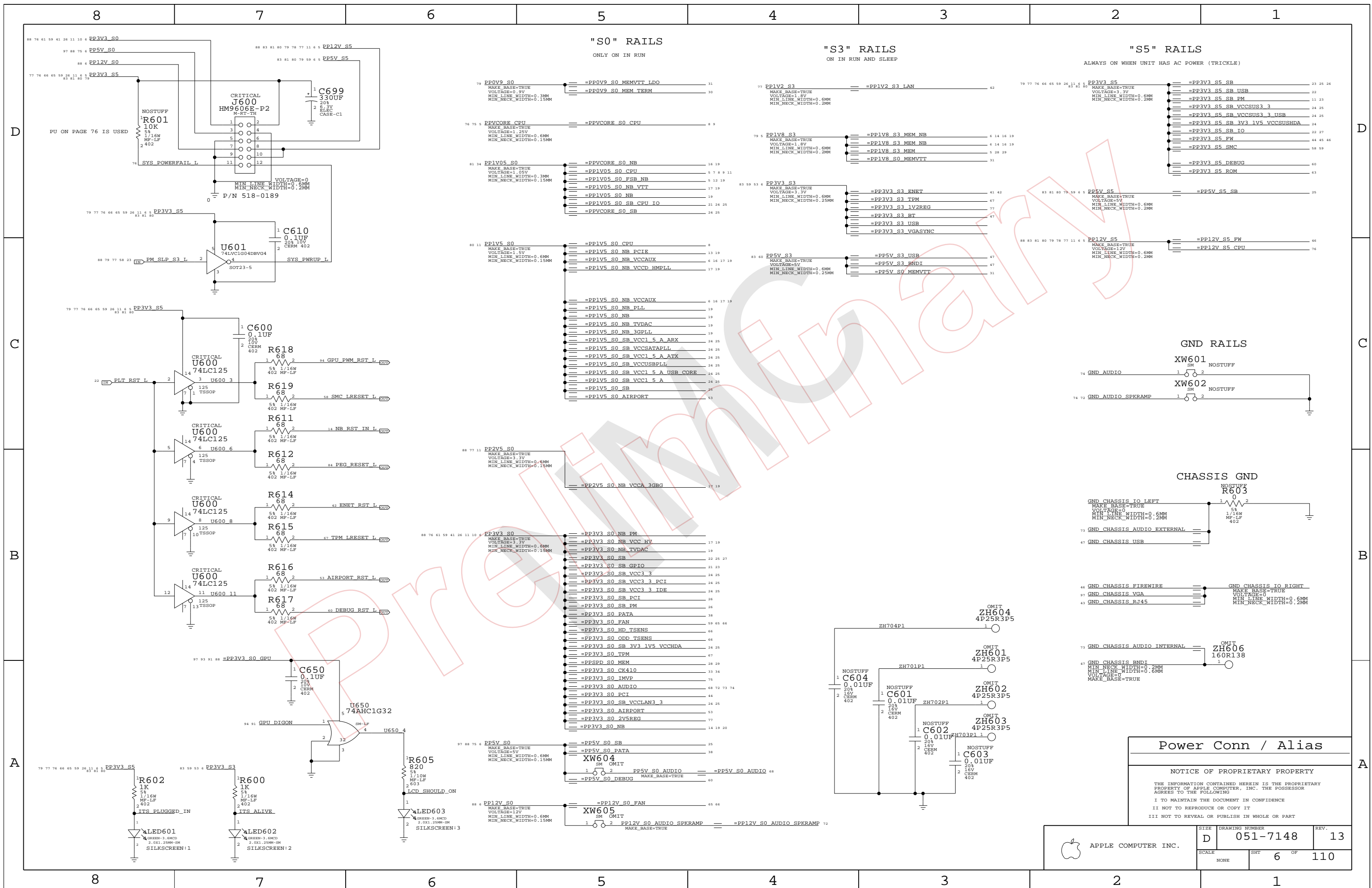
- 90 87 5 FB B CKE<1> PP9020
- 90 87 5 FB B CLK P<1> PP9021
- 90 87 5 FB B CLK N<1> PP9022
- 90 87 5 FB B CS L<1> PP9023
- 90 87 5 FB B WE L<1> PP9024
- 90 87 5 FB B CAS L<1> PP9025
- 90 87 5 FB B RAS L<1> PP9026
- 90 87 5 FB B MA<3> PP9027
- 90 88 5 DRAM RST PP9028
- 90 88 5 FB B WDQS<5> PP9029
- 90 88 5 FB B WDQS<6> PP9030
- 90 88 5 FB B WDQS<7> PP9031
- 90 88 5 FB B WDQS<4> PP9032
- 90 88 5 FB B DQ<32> PP9033
- 90 88 5 FB B DQ<40> PP9034
- 90 88 5 FB B DQ<48> PP9035
- 90 88 5 FB B DQ<56> PP9036

FUNC TEST 1 OF 2

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	D	051-7148	13
SCALE	SHEET	OF	
NONE	5	110	



"S0" RAILS
ONLY ON IN RUN

"S3" RAILS
ON IN RUN AND SLEEP

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

GND RAILS

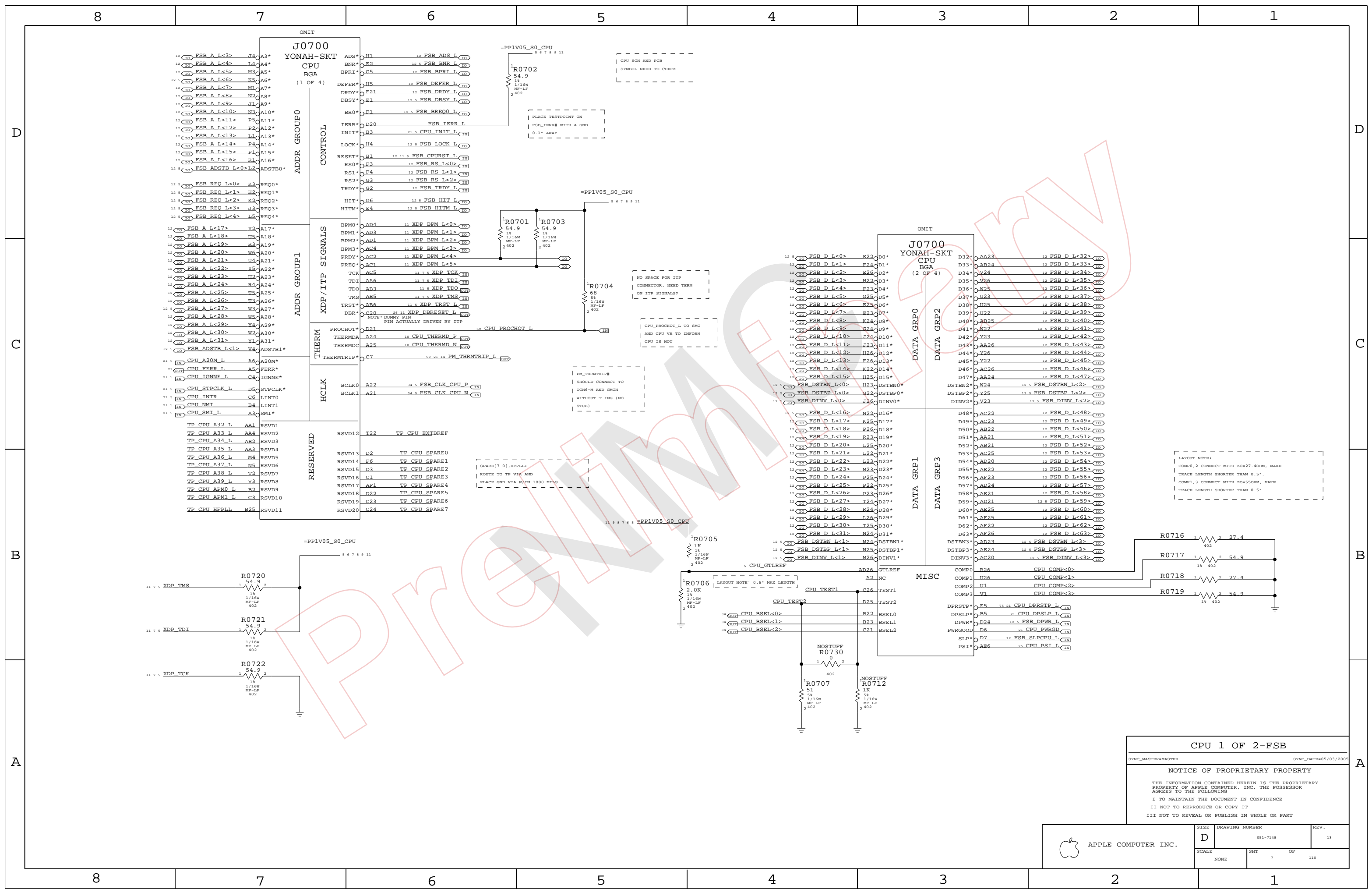
CHASSIS GND

Power Conn / Alias

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	D	051-7148	13
SCALE	SHT	OF	
NONE	6	110	



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

NOTICE OF PROPRIETARY PROPERTY

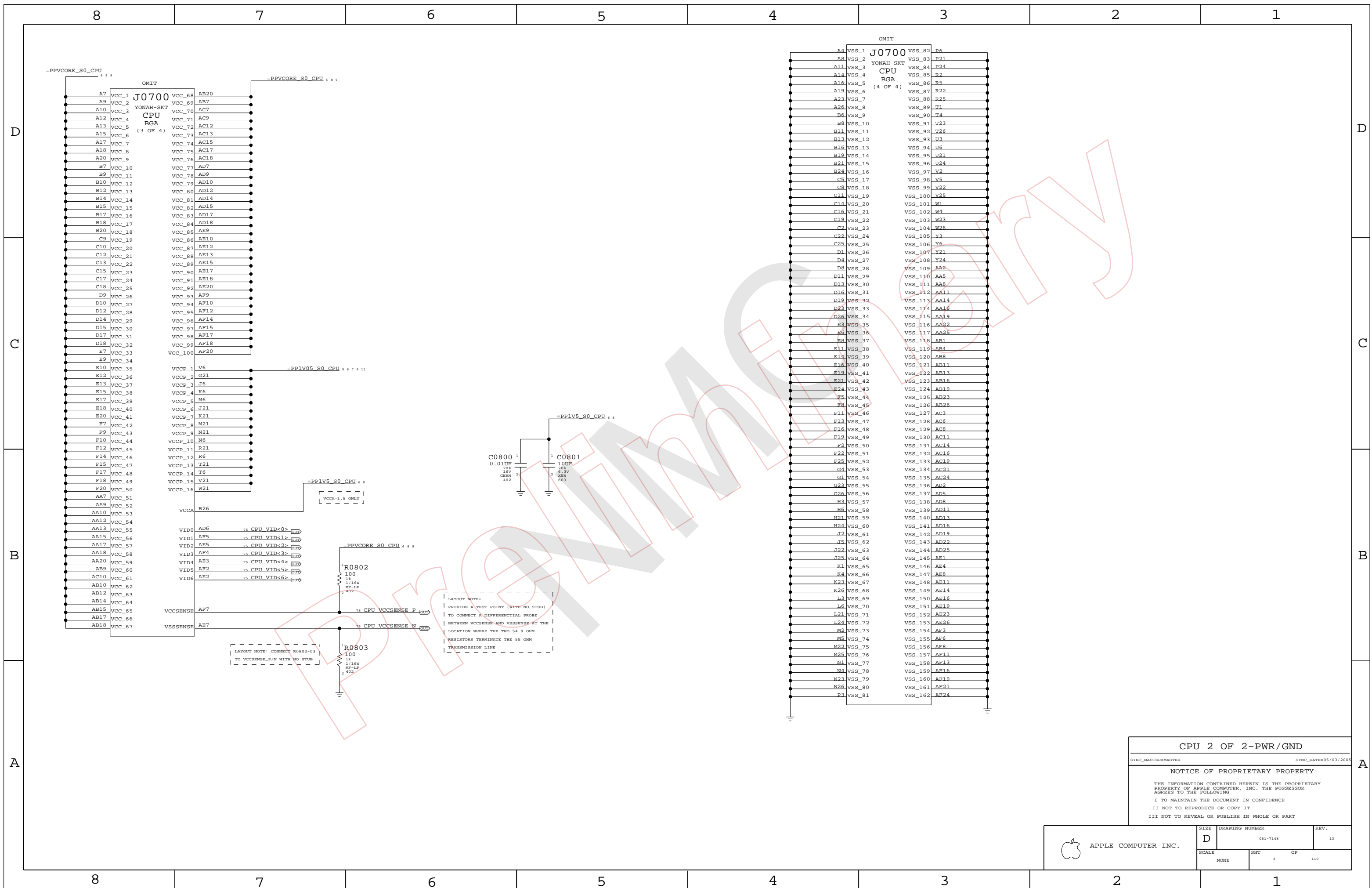
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 7	OF 110



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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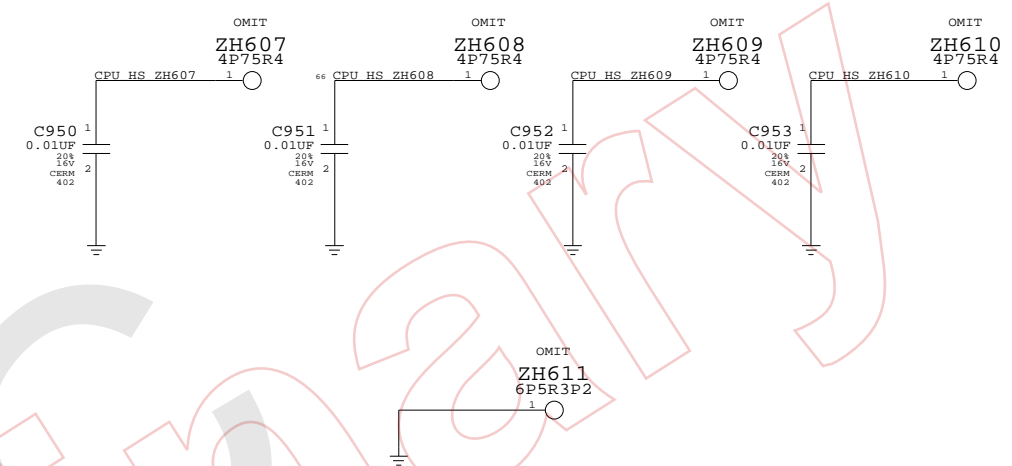
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	REV.
NONE	8	110	

D

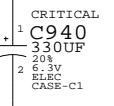
D

CPU HEATSINK MOUNTING HOLES

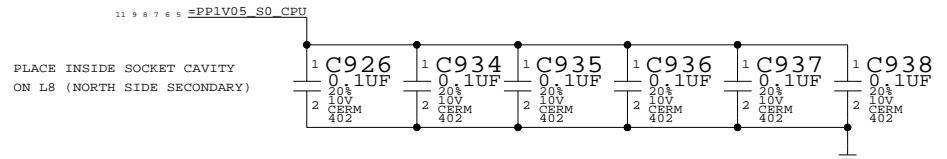


C

C



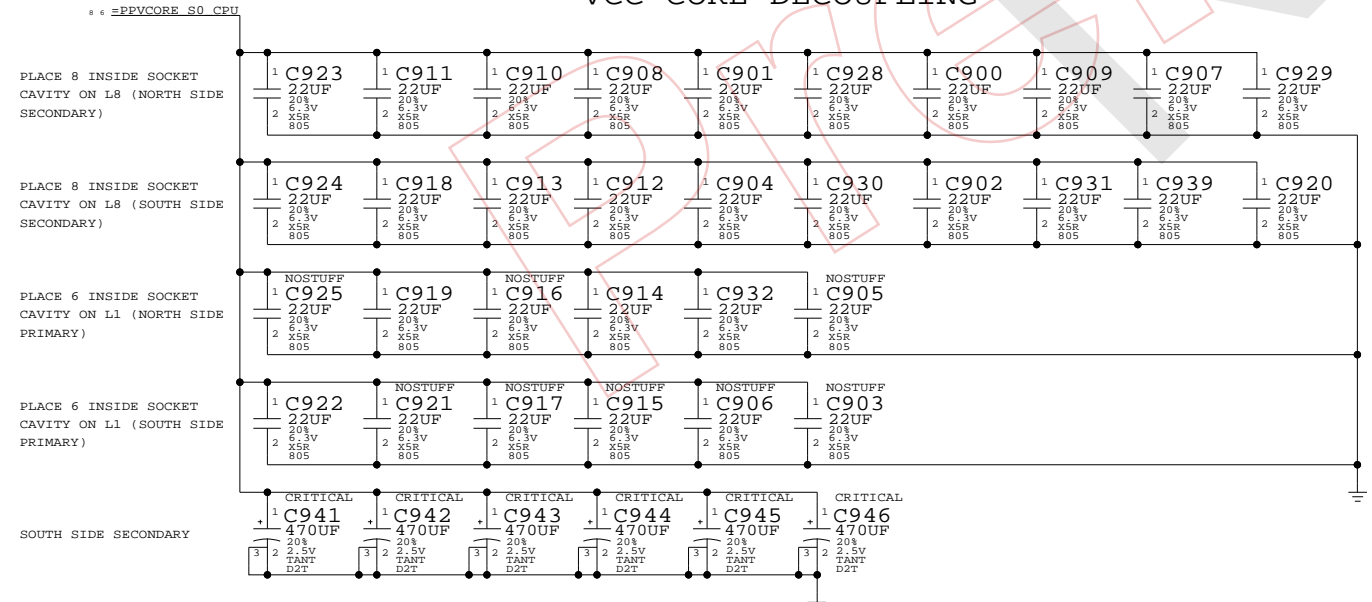
VCCP CORE DECOUPLING



B

B

VCC CORE DECOUPLING



A

A

CPU DECAPS & VID<>

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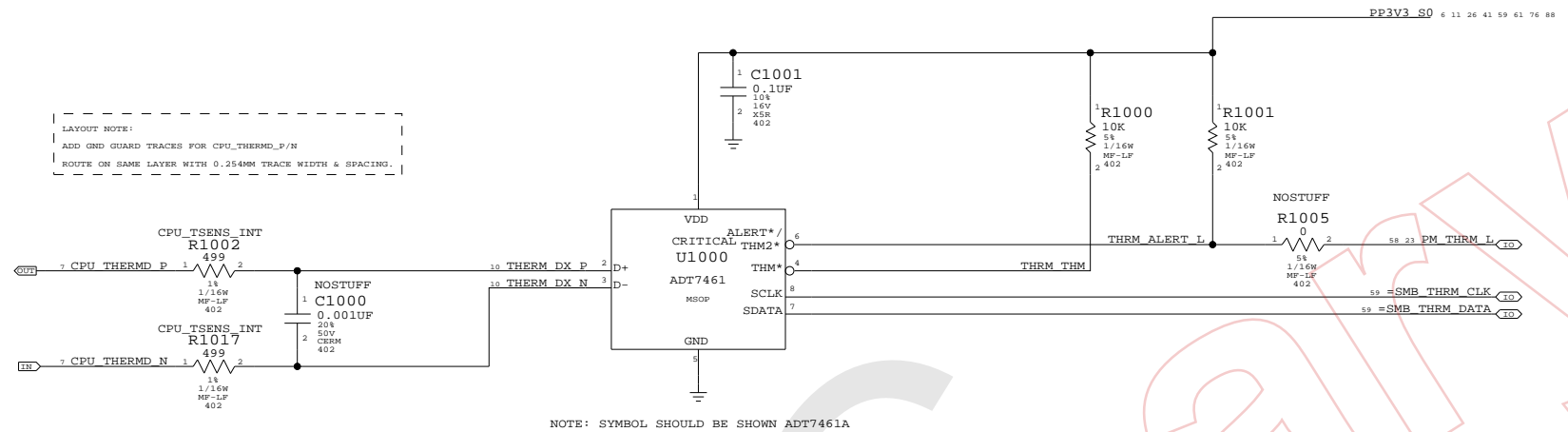
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT 9 OF 110		
NONE			

CPU THERMAL SENSOR

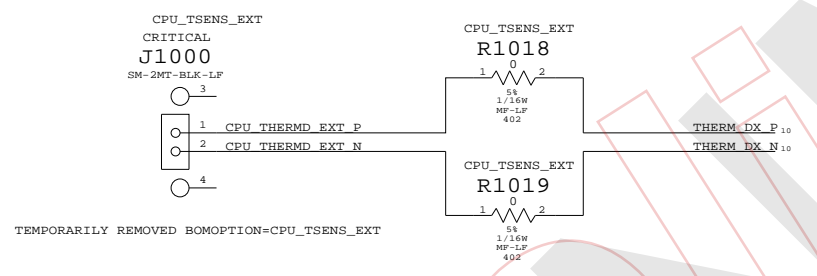
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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	D	051-7148	13
SCALE	SHT		OF
NONE	10		110

D

D

C

C

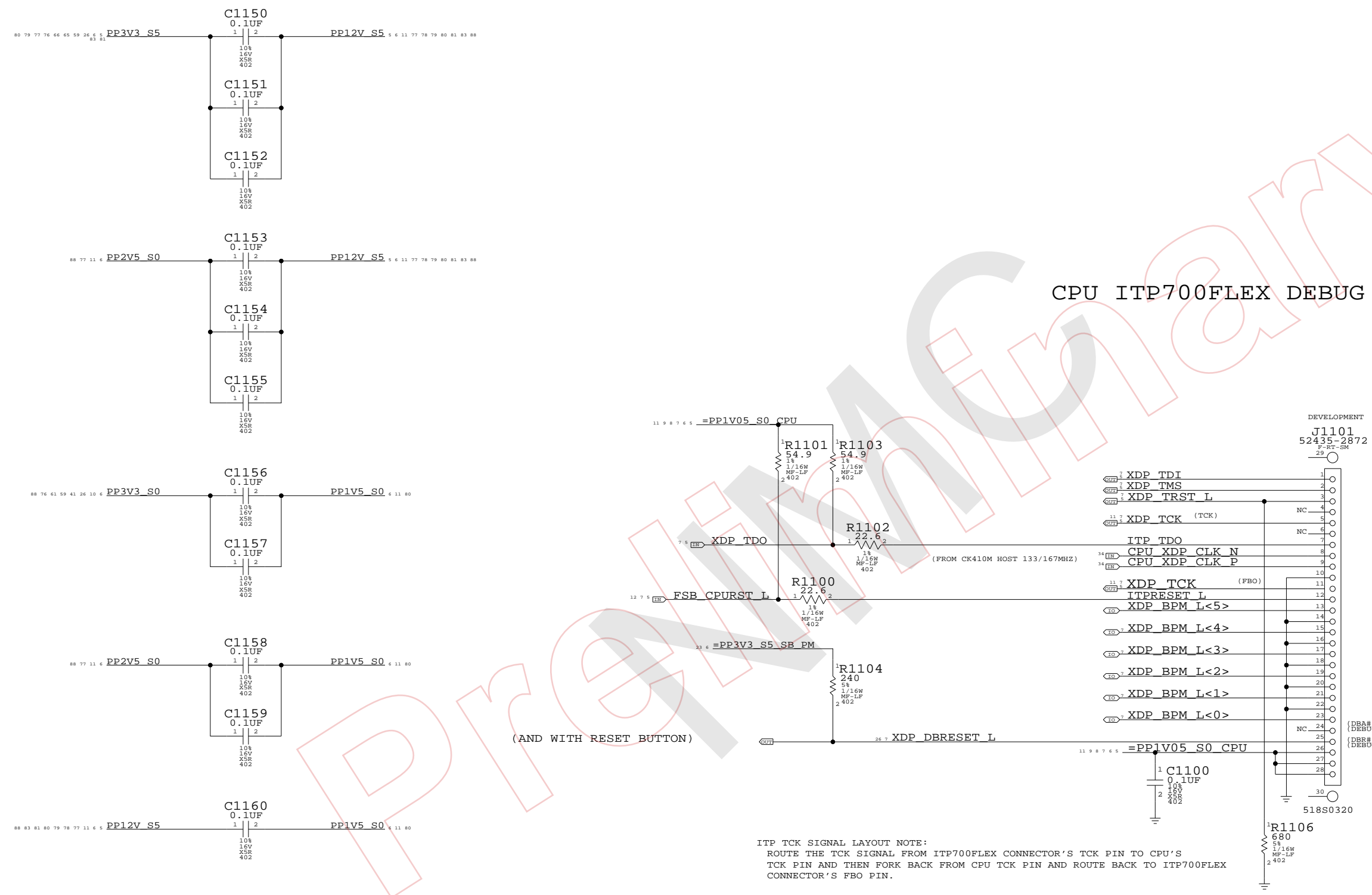
B

B

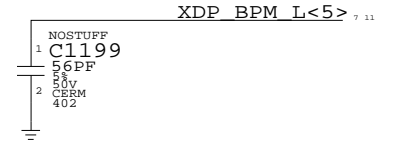
A

A

CPU ITP700FLEX DEBUG SUPPORT



NOTE: PLACE C1199 AT J1101 PINS 13 AND 14



(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM. (DEBUG PORT ACTIVE)
 (DBB#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

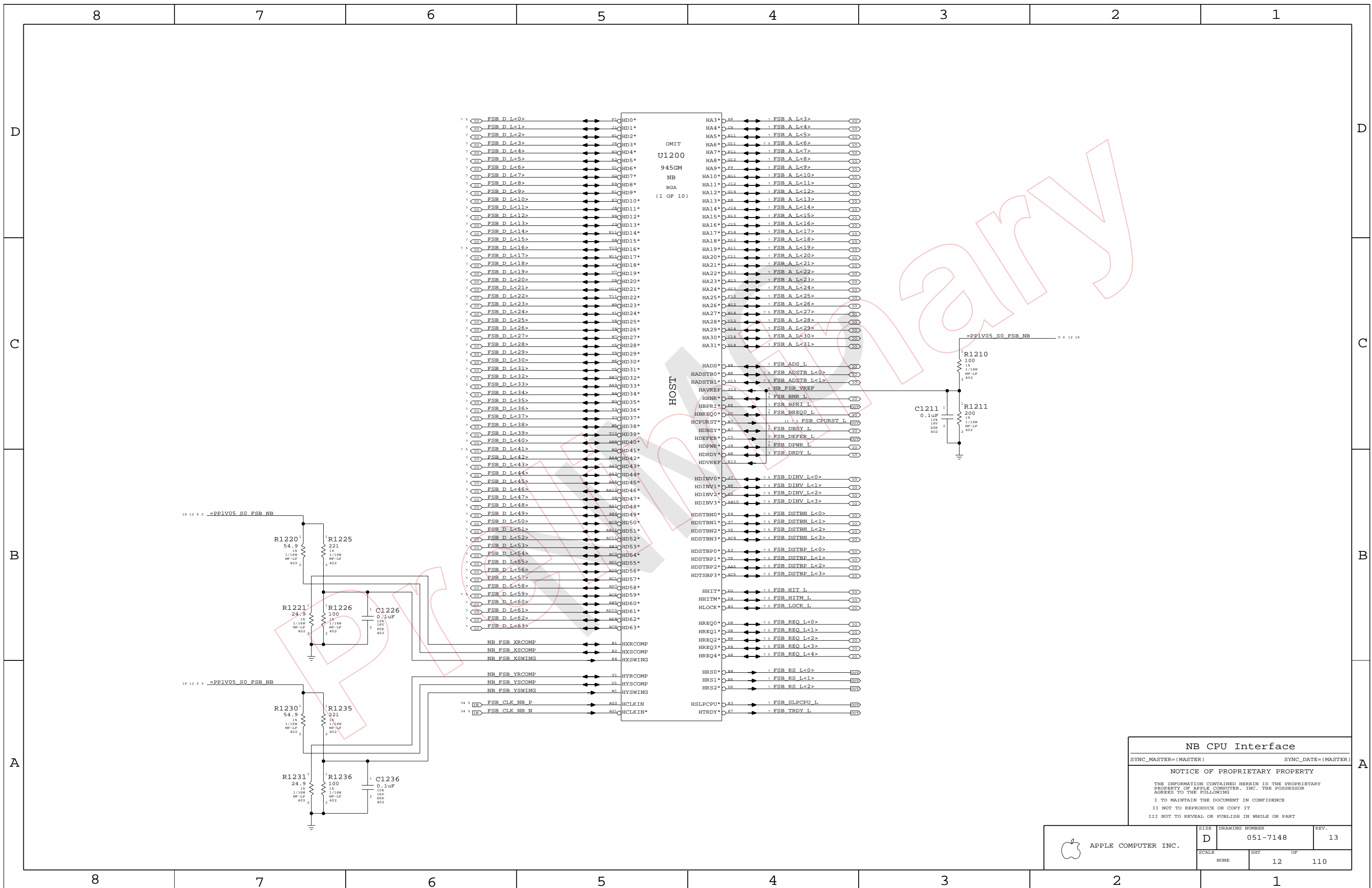
CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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	D	051-7148	13
SCALE	SHT	OF	110
NONE	11		



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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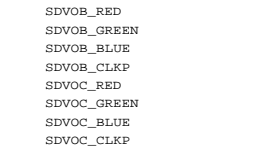
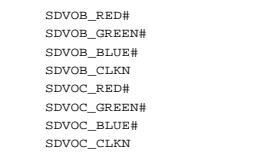
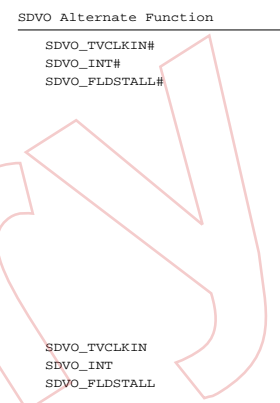
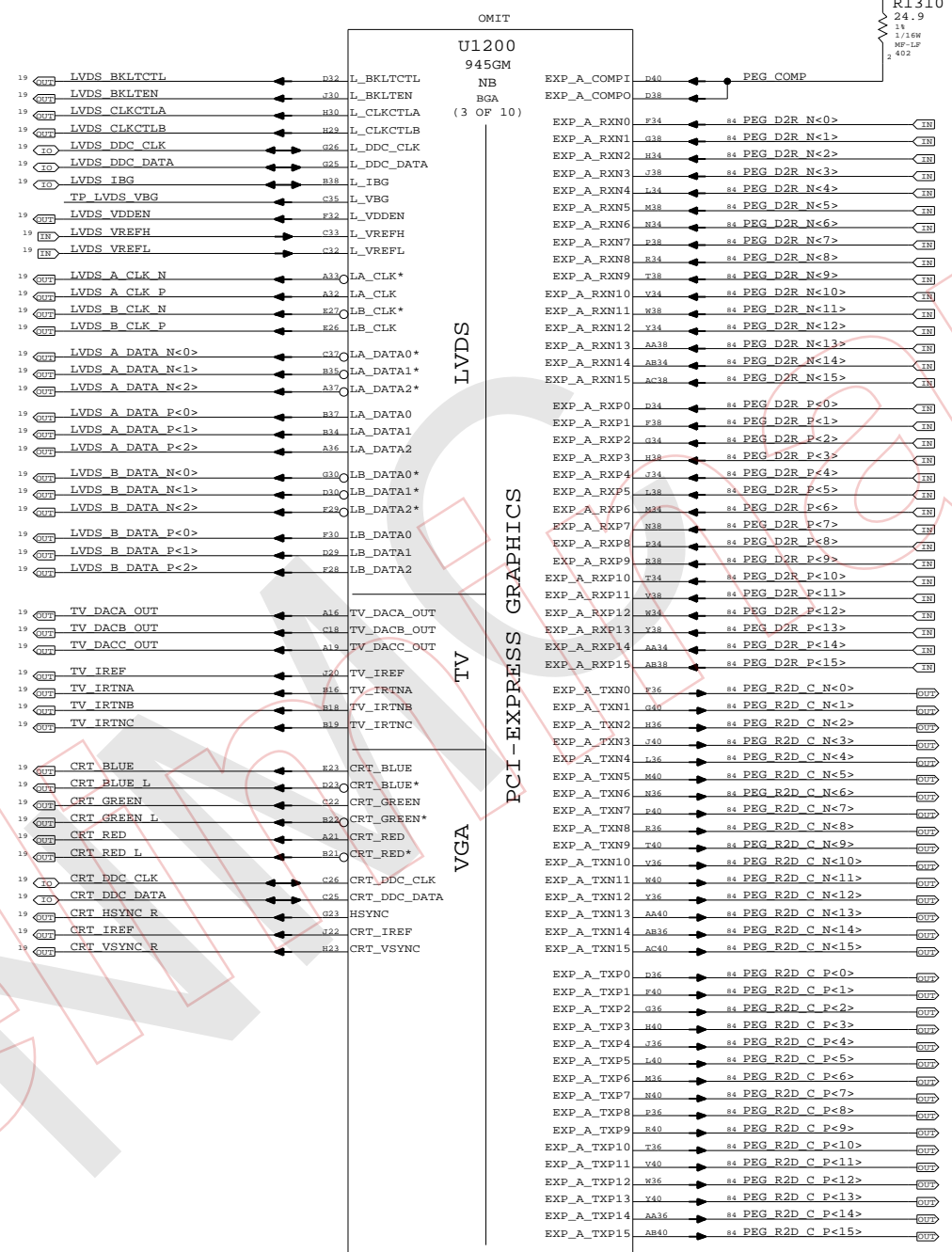
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	12	110	

LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC
 Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

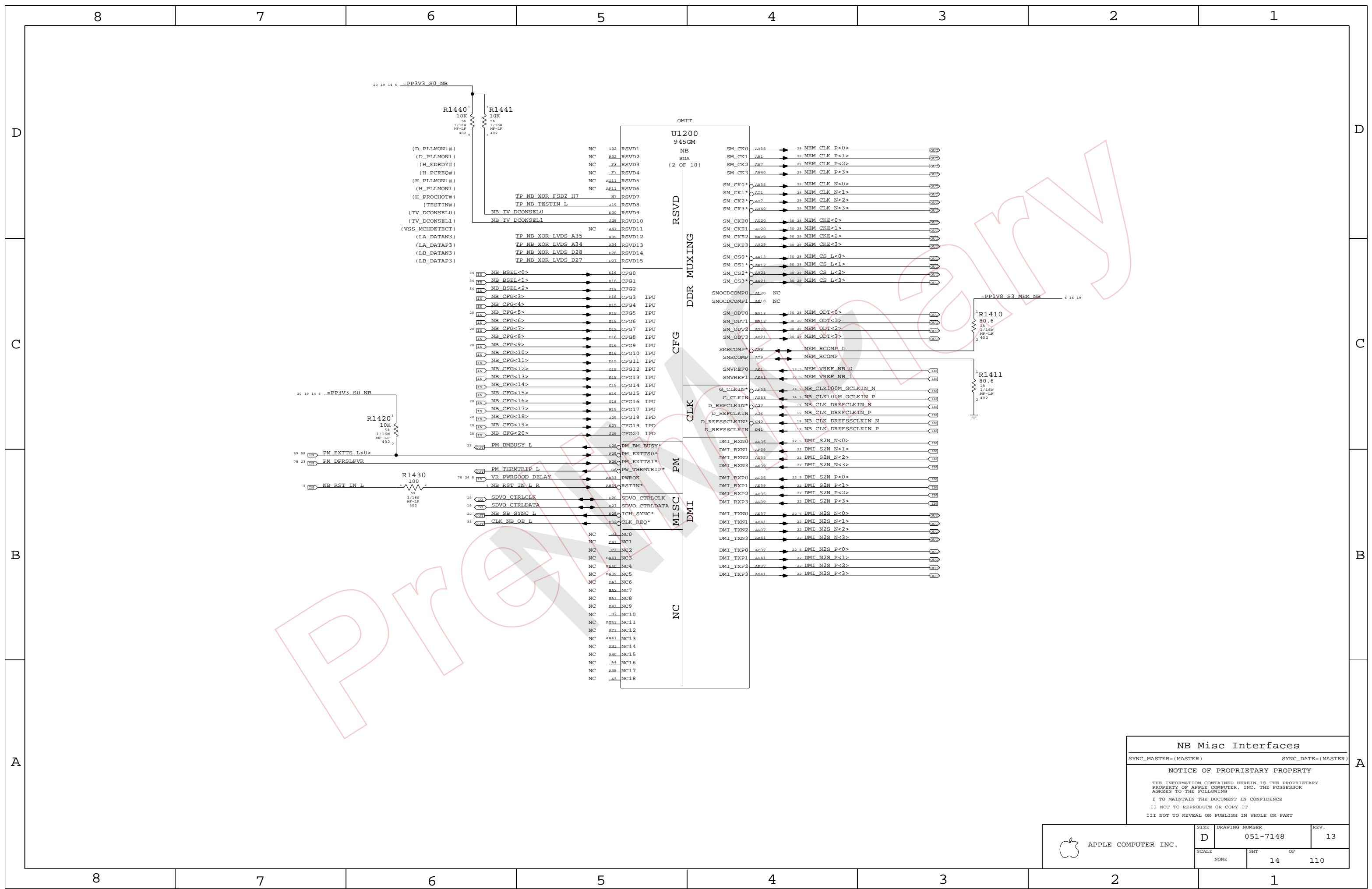
TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT OF		
NONE	13	110	



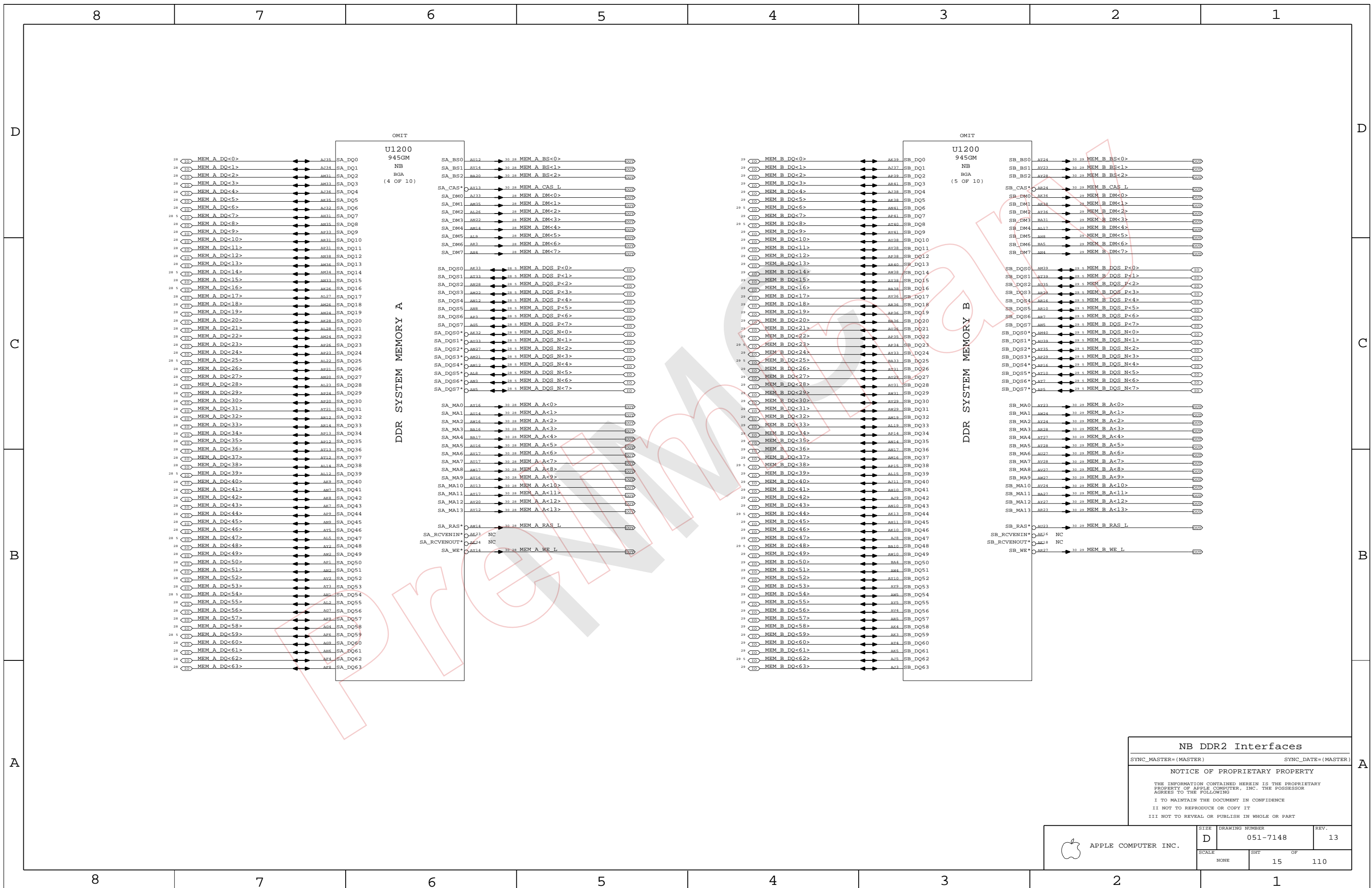
NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7148	13
SCALE	SHT OF		
NONE	14 OF		110



NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

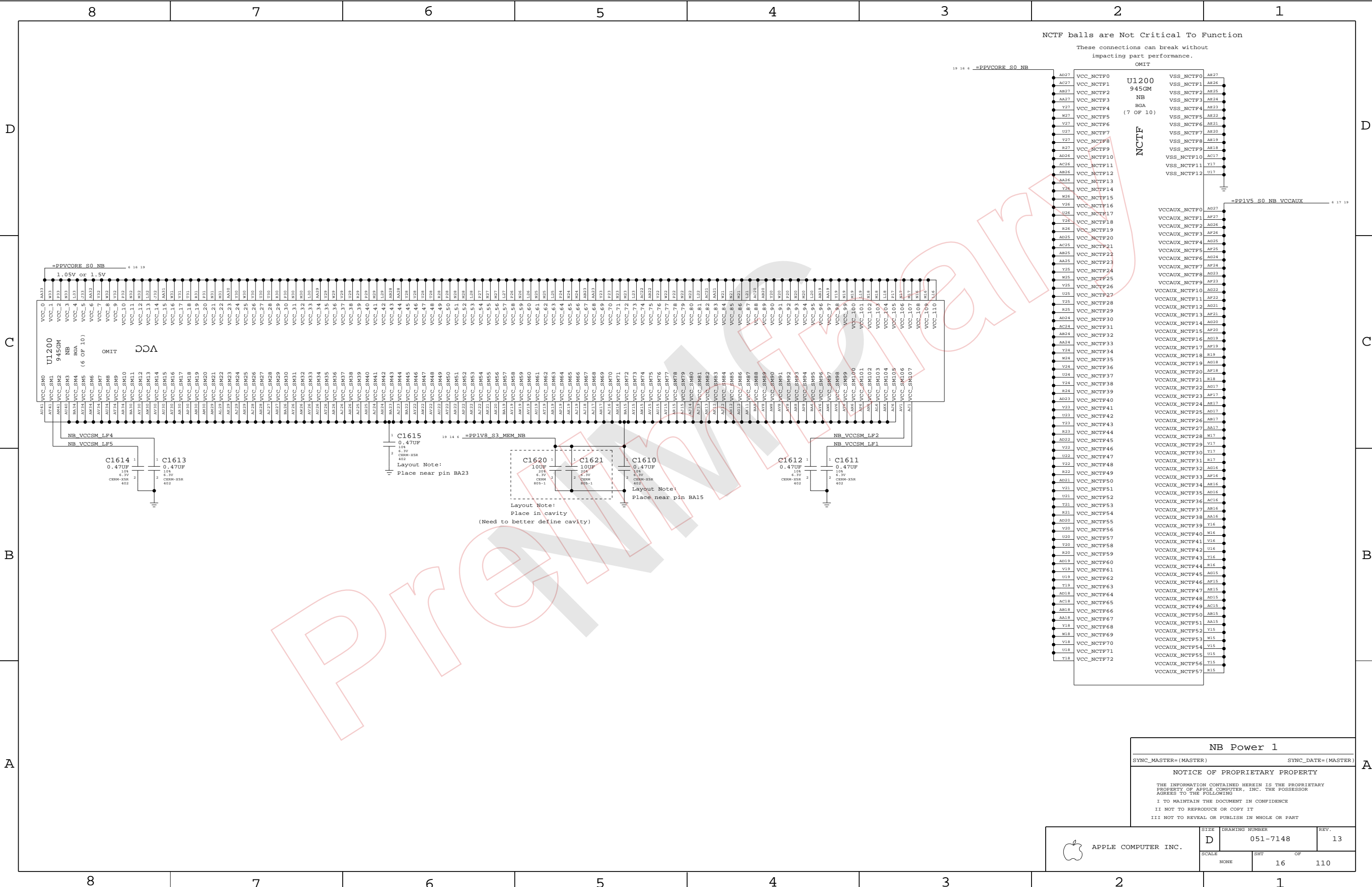
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	SCALE NONE	SHEET 15	OF 110



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)

NCTF

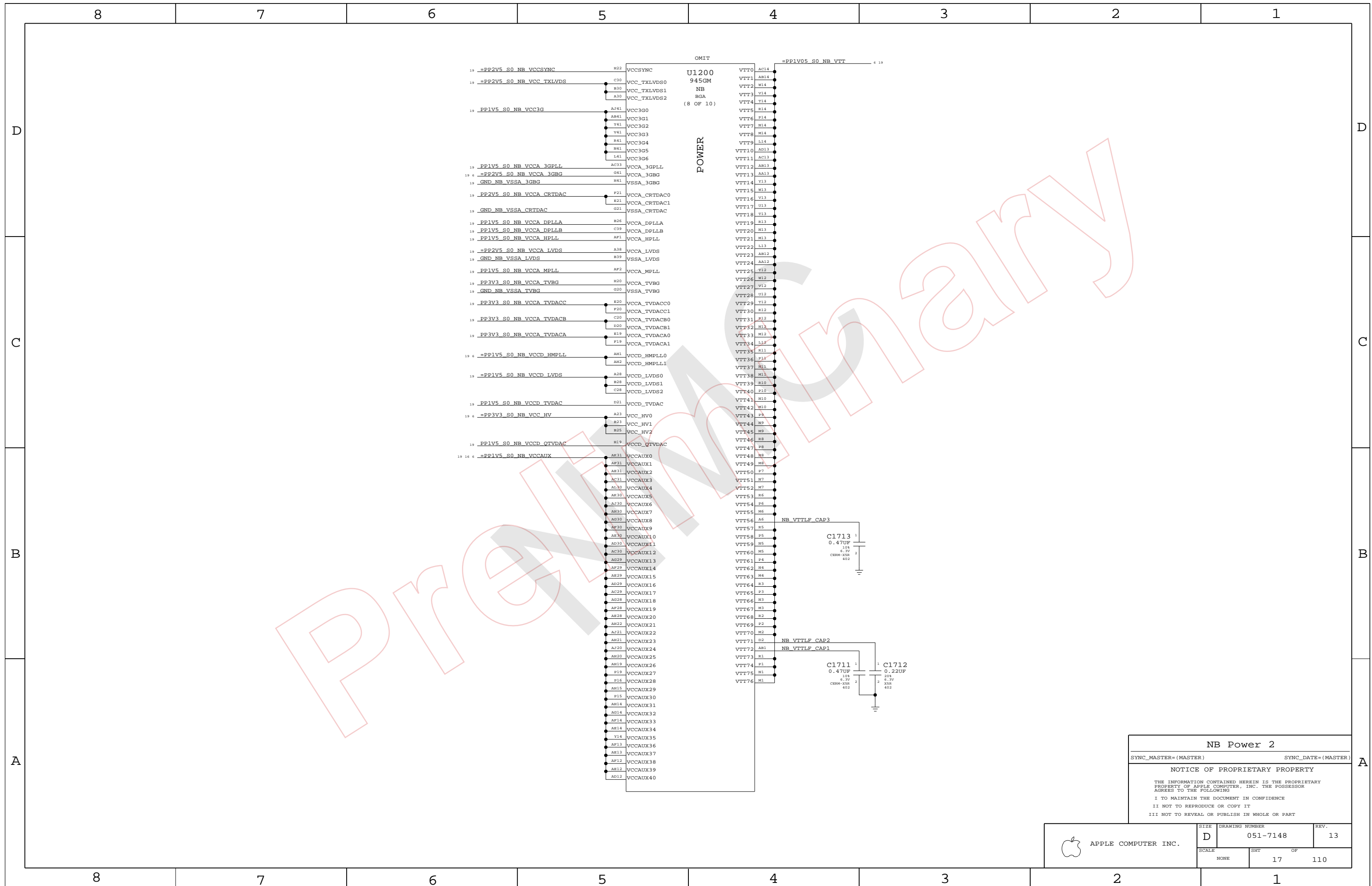
VCC

VCCAUX

NB Power 1
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7148	13
SCALE	SHT	OF	
NONE	16	110	



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

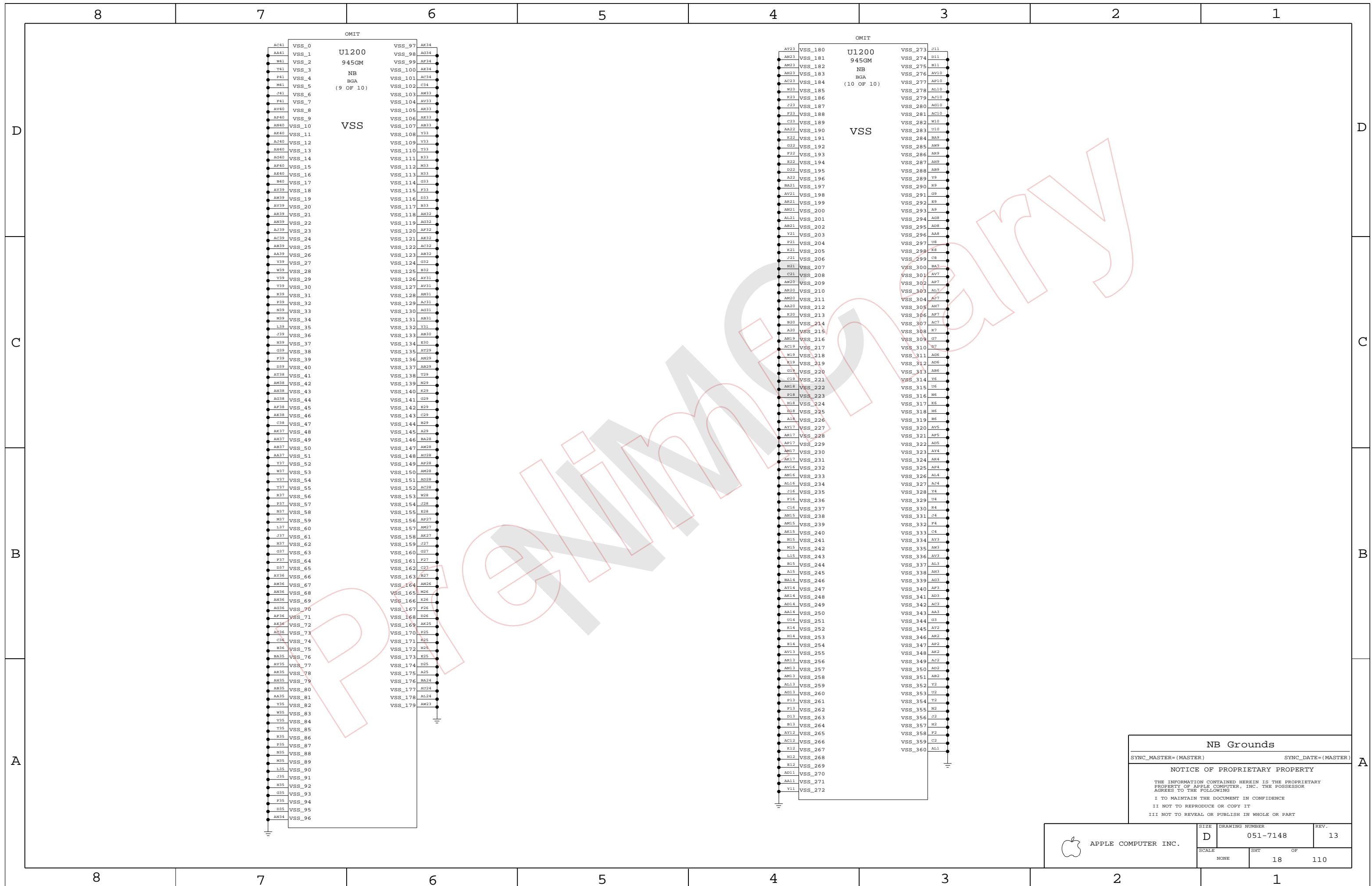
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	SCALE NONE	SHEET 17	OF 110



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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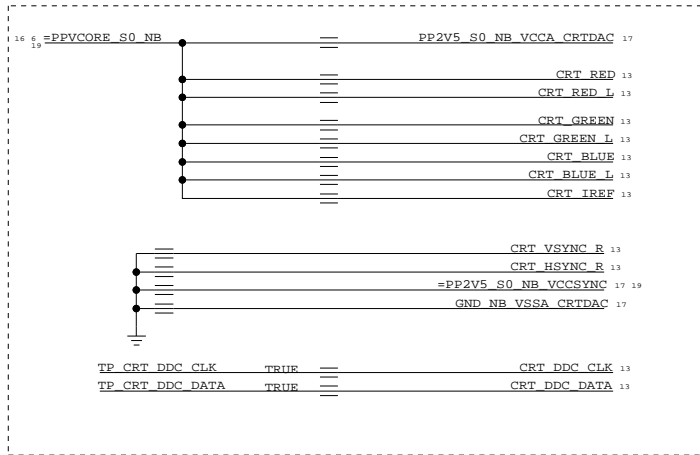
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHT 18	OF 110

Power Interface

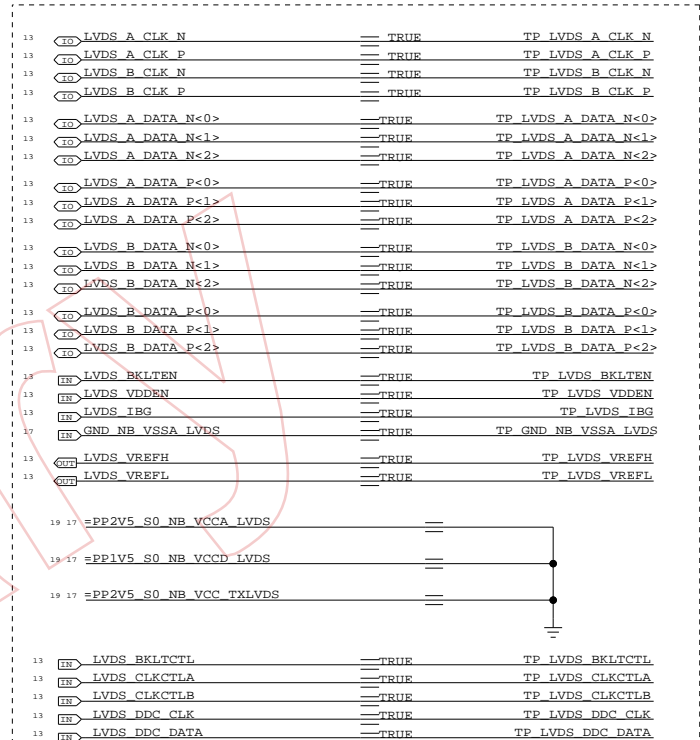
These are the power signals that leave the NB "block"

- =PP1V05_S0_FSB_NB 5 6 12
- =PPVCORE_S0_NB 6 16 19
- =PP1V05_S0_NB 6
- =PP1V05_S0_NB_VTT 6 17 19
- =PP1V5_S0_NB 6 19
- =PP1V5_S0_NB_PCIE 6 13
- =PP1V5_S0_NB_PLL 6 19
- =PP1V5_S0_NB_TVDAC 6 19
- =PP1V5_S0_NB_VCCD_HMPLL 6 19
- =PP1V5_S0_NB_VCCD_LVDS 17 19
- =PP1V5_S0_NB_VCCAUX 6 16 17 19
- =PP1V8_S3_MEM_NB 6 14 16 19
- =PP2V5_S0_NB_VCCSYNCR 17 19
- =PP2V5_S0_NB_VCC_TXLVDS 17 19
- =PP2V5_S0_NB_VCCA_3GBG 6 17 19
- =PP2V5_S0_NB_VCCA_LVDS 17 19
- =PP3V3_S0_NB 6 14 20
- =PP3V3_S0_NB_TVDAC 6
- =PP3V3_S0_NB_VCC_HV 6 17 19

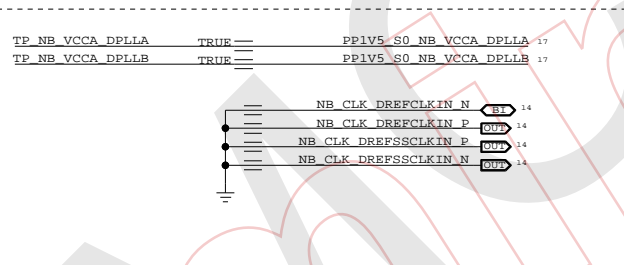
TVOUT DISABLE



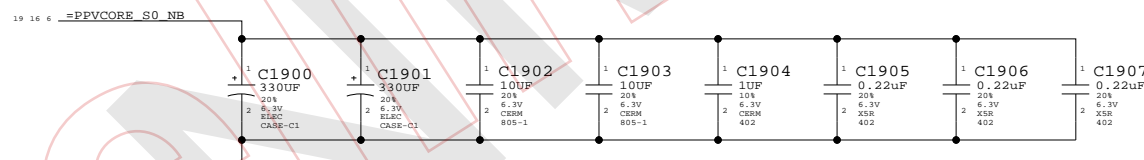
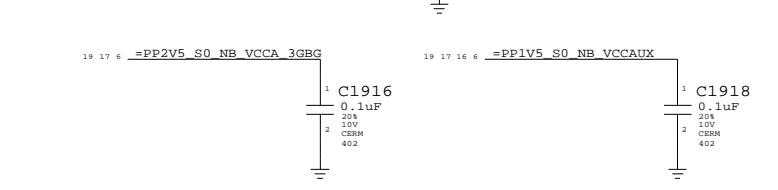
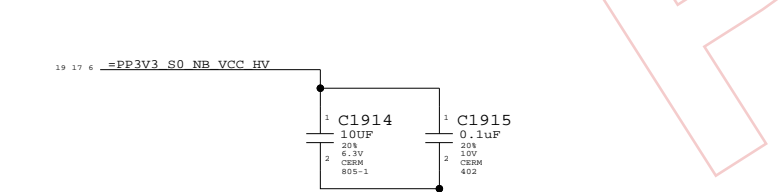
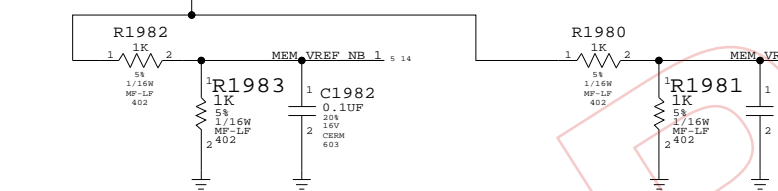
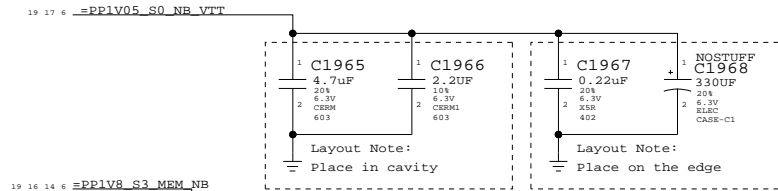
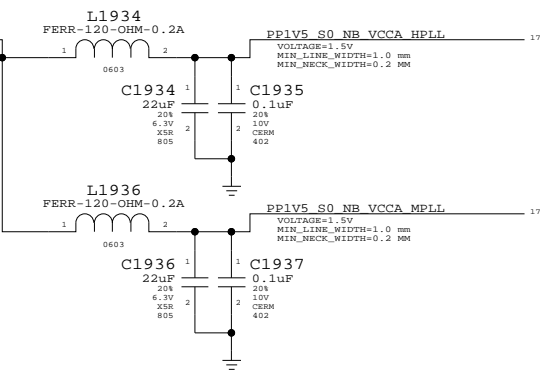
LVDS DISABLE



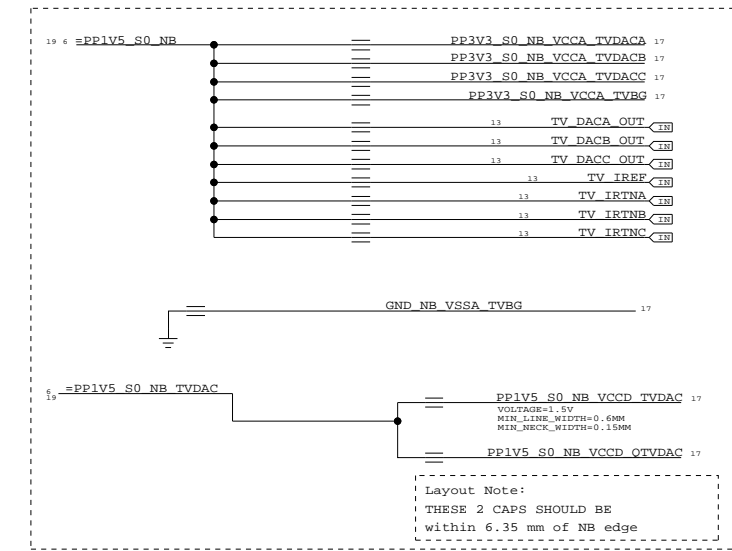
DISPLAY DISABLE



Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge



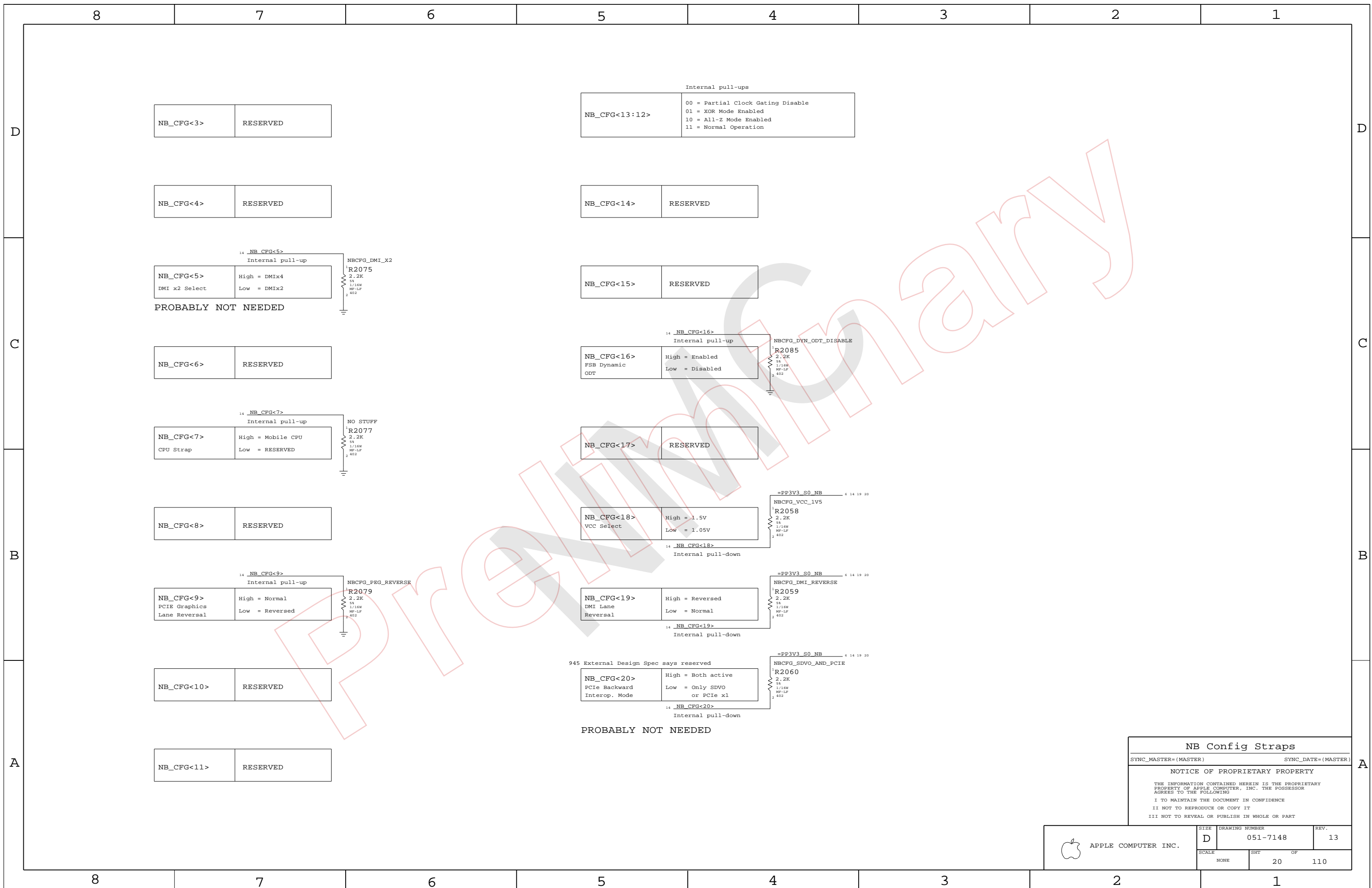
TVOUT DISABLE



Layout Note:
THESE 2 CAPS SHOULD BE WITHIN 6.35 mm OF NB EDGE

NB (GM) Decoupling
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7148	13
SCALE	SHT	OF	
NONE	19		110



NB_CFG<3>	RESERVED
-----------	----------

Internal pull-ups	
NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

14_NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMiX4 DMI x2 Select Low = DMiX2
PROBABLY NOT NEEDED	

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14_NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic Low = Disabled ODT

14_NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

=PP3V3_S0_NB NBCFG_VCC_LV5	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
14_NB_CFG<18> Internal pull-down	

14_NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Low = Reversed Lane Reversal

=PP3V3_S0_NB NBCFG_DMI_REVERSE	
NB_CFG<19>	High = Reversed DMI Lane Low = Normal Reversal
14_NB_CFG<19> Internal pull-down	

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved	
NB_CFG<20>	High = Both active PCIe Backward Low = Only SDVO Interop. Mode or PCIe x1
14_NB_CFG<20> Internal pull-down	
PROBABLY NOT NEEDED	

NB_CFG<11>	RESERVED
------------	----------

NB Config Straps

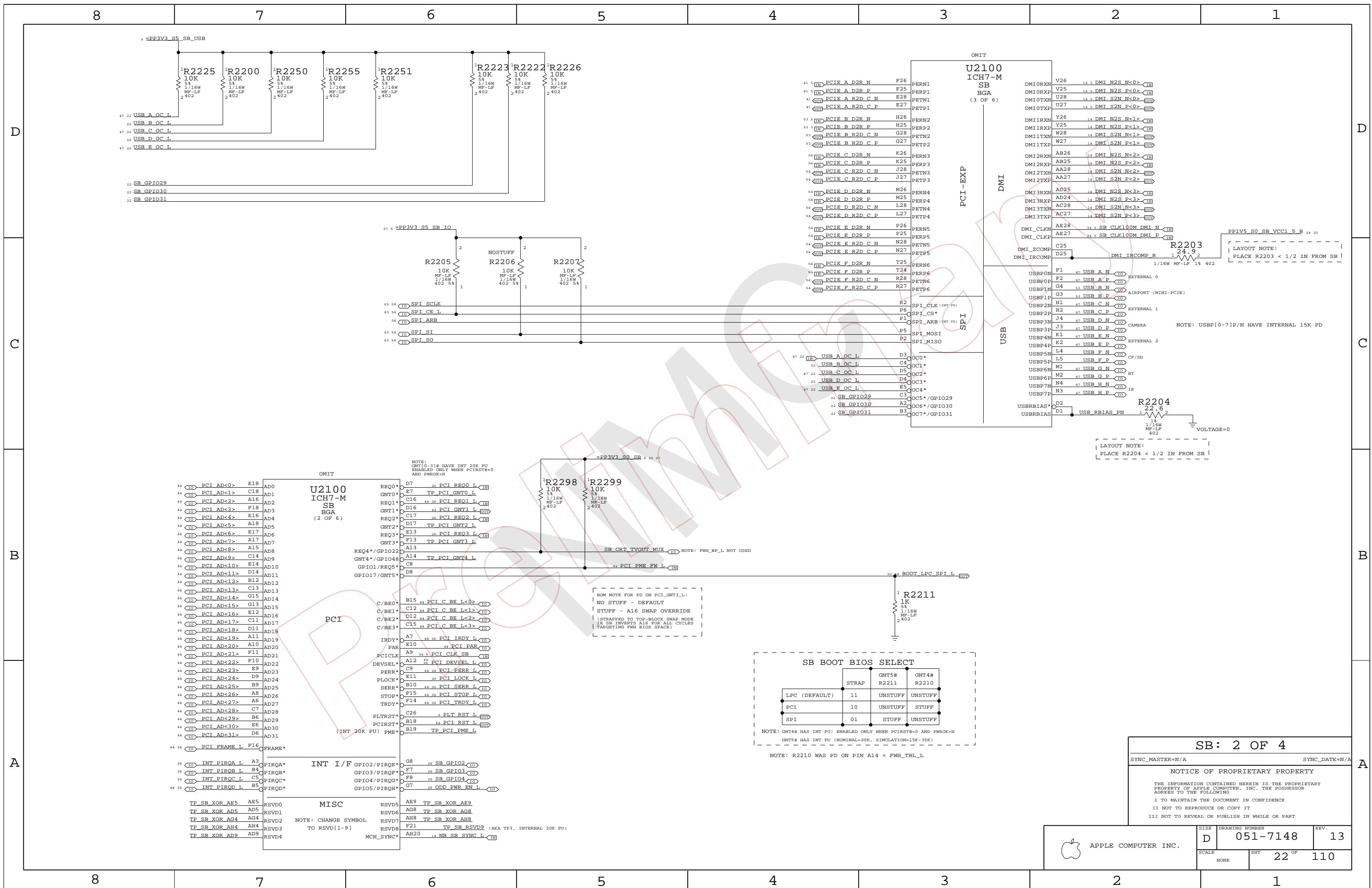
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
NONE	20	110	



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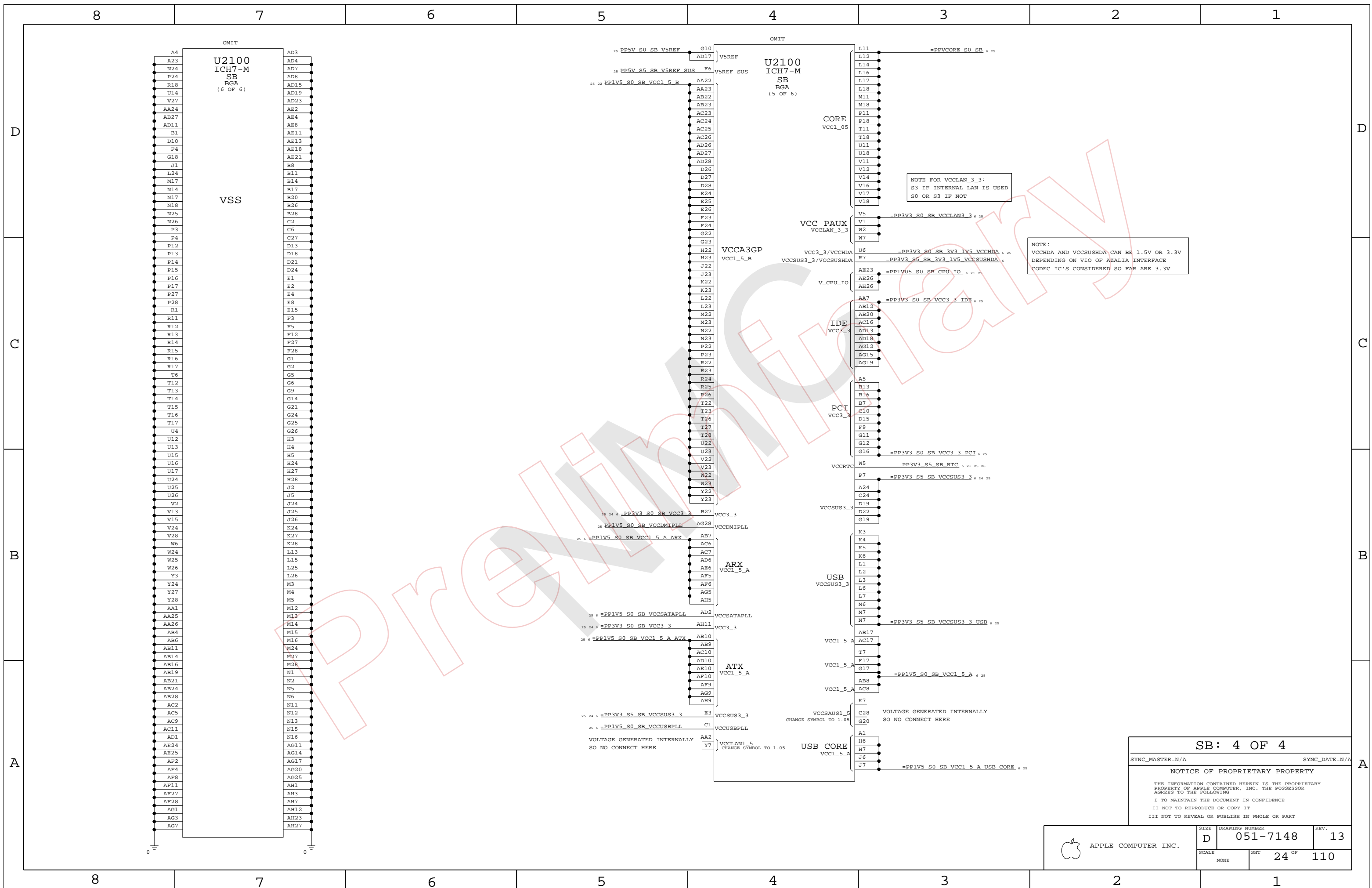
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	D	051-7148	13
SCALE	SHT	22 OF	110
NONE			



NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCCHDA AND VCCSUS3_3 CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODER IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

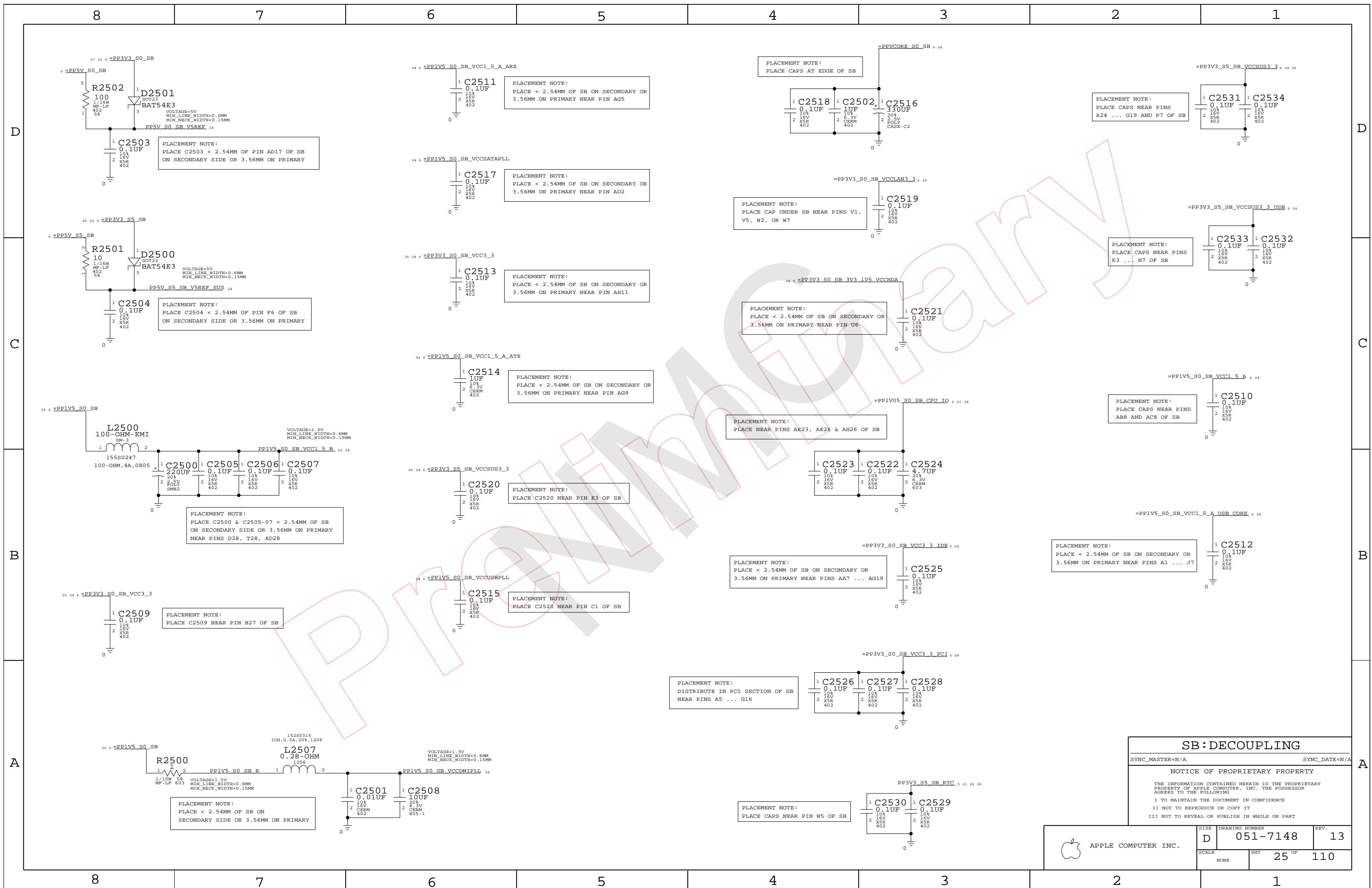
SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	24 OF 110	
NONE			



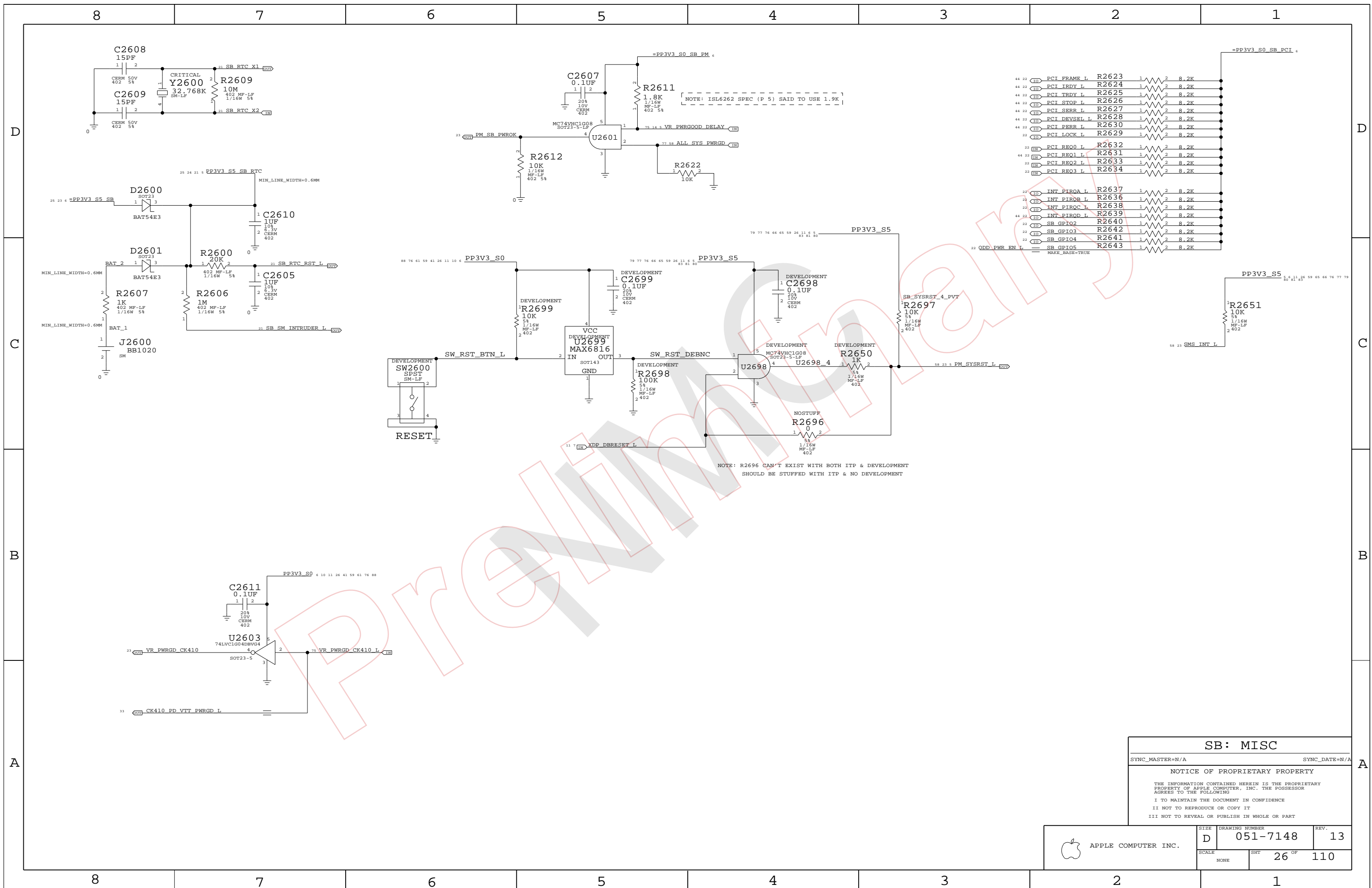
SB: DECOUPLING

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	25 OF	110
NONE			



SB: MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

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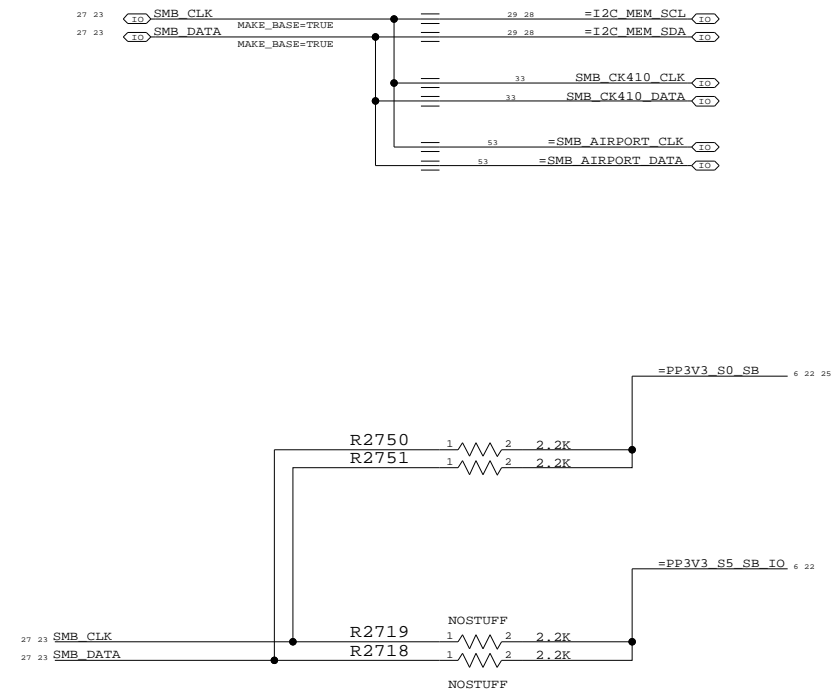
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHT 26 OF 110	

SB I2C BUSSES



Pre-Announcement


SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	27 OF 110	
NONE			

Page Notes

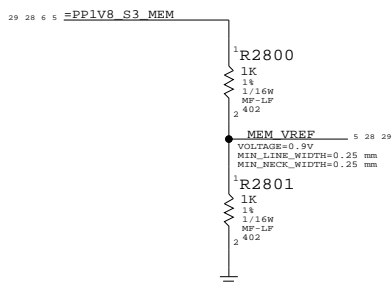
Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

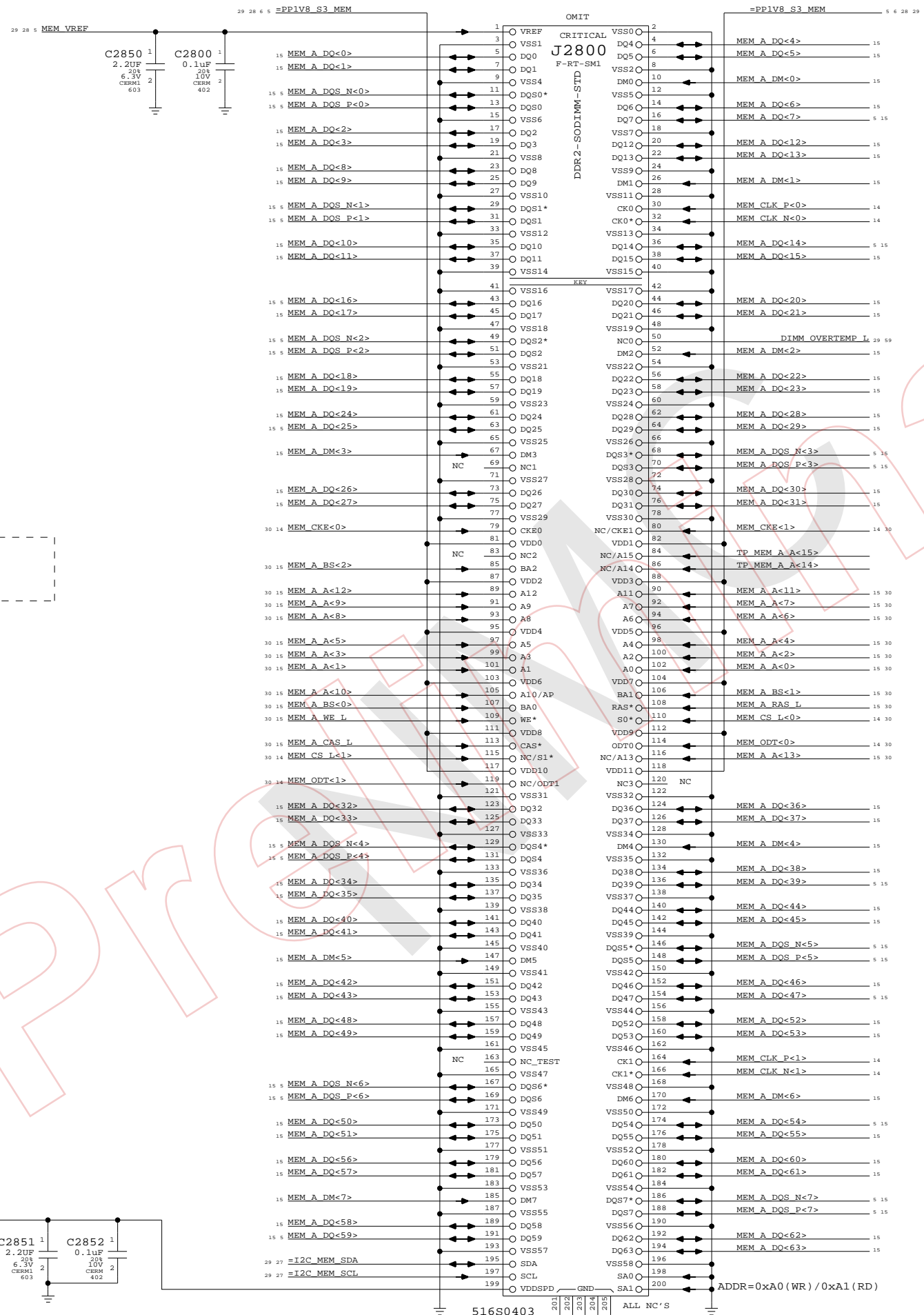
BOM options provided by this page:
 (NONE)

DDR2 VRef

One 0.1uF per connector



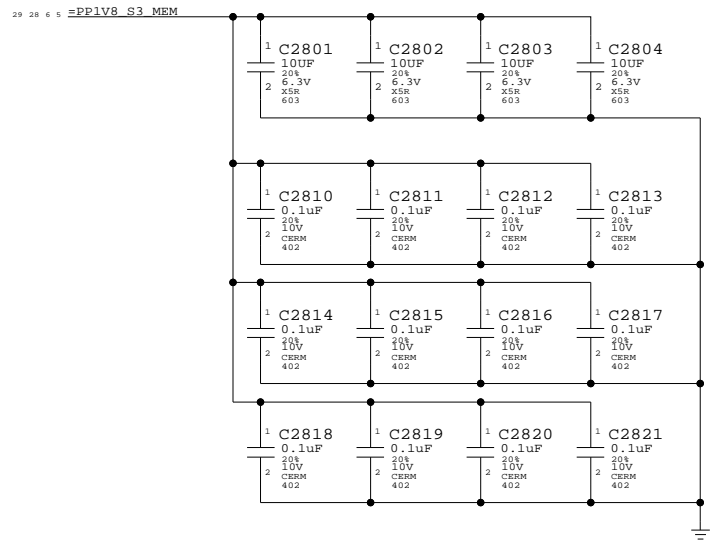
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
 (See Capell Valley pg 47)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51680503	1	DDR2 SODIMM STD CONN	J2800	CRITICAL	

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	28	110	

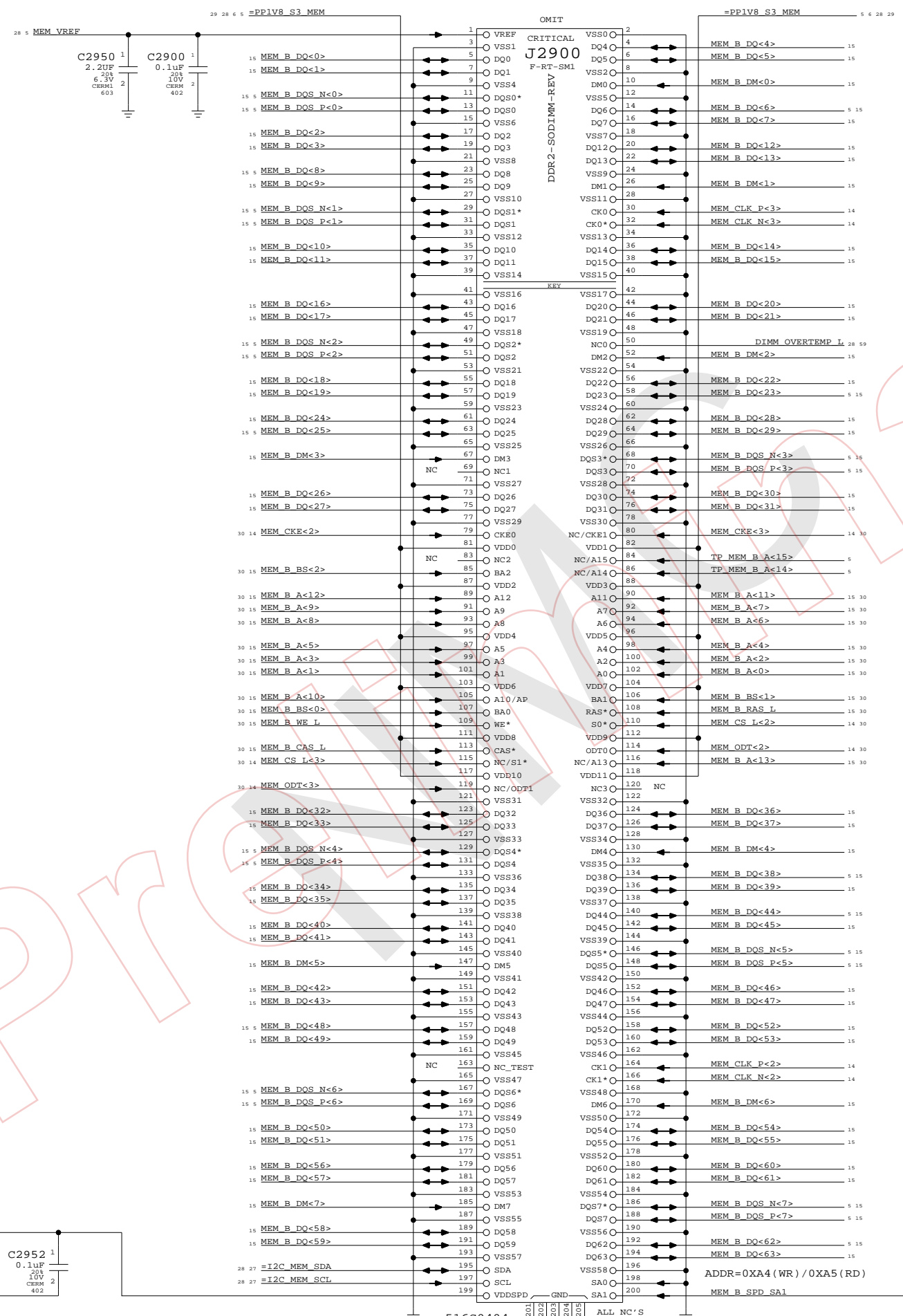
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

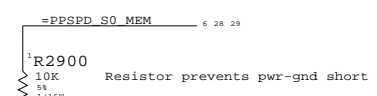
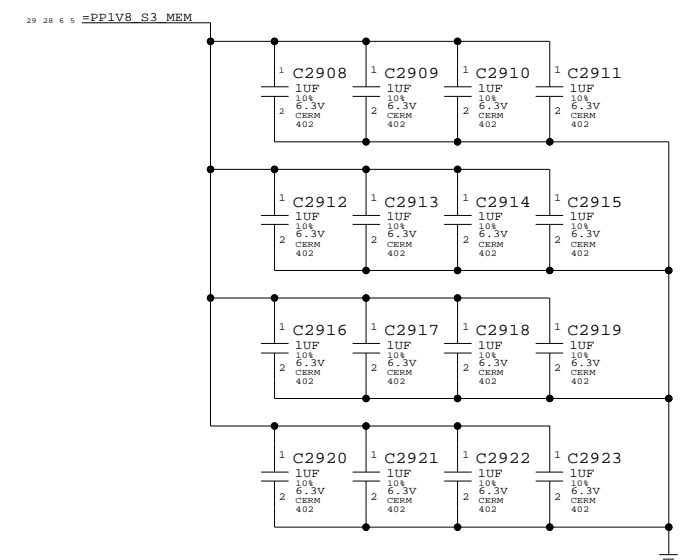
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0504	1	DDR2 SODIMM REV CONN	J2900	CRITICAL	

DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	29	110	

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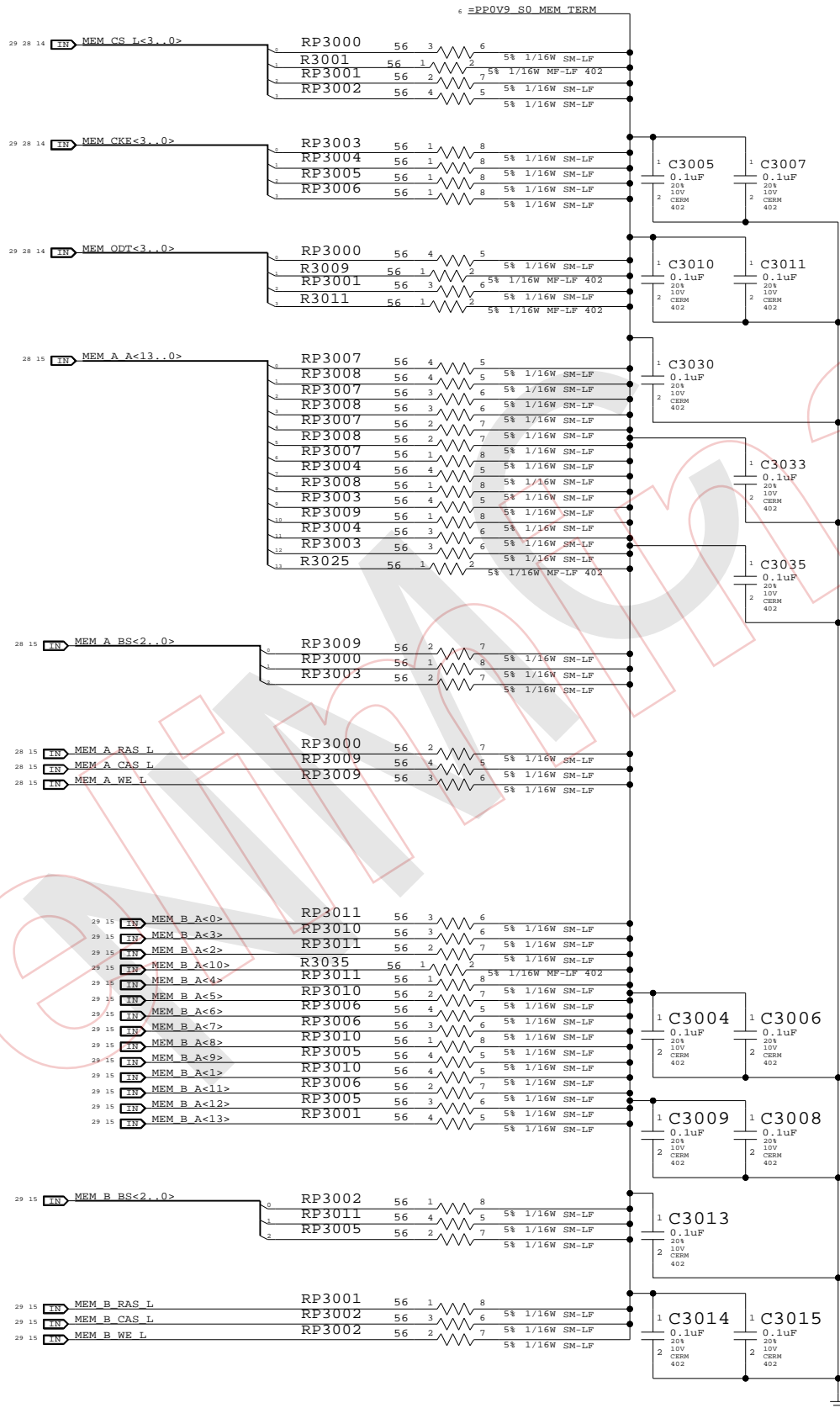
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	30	110	

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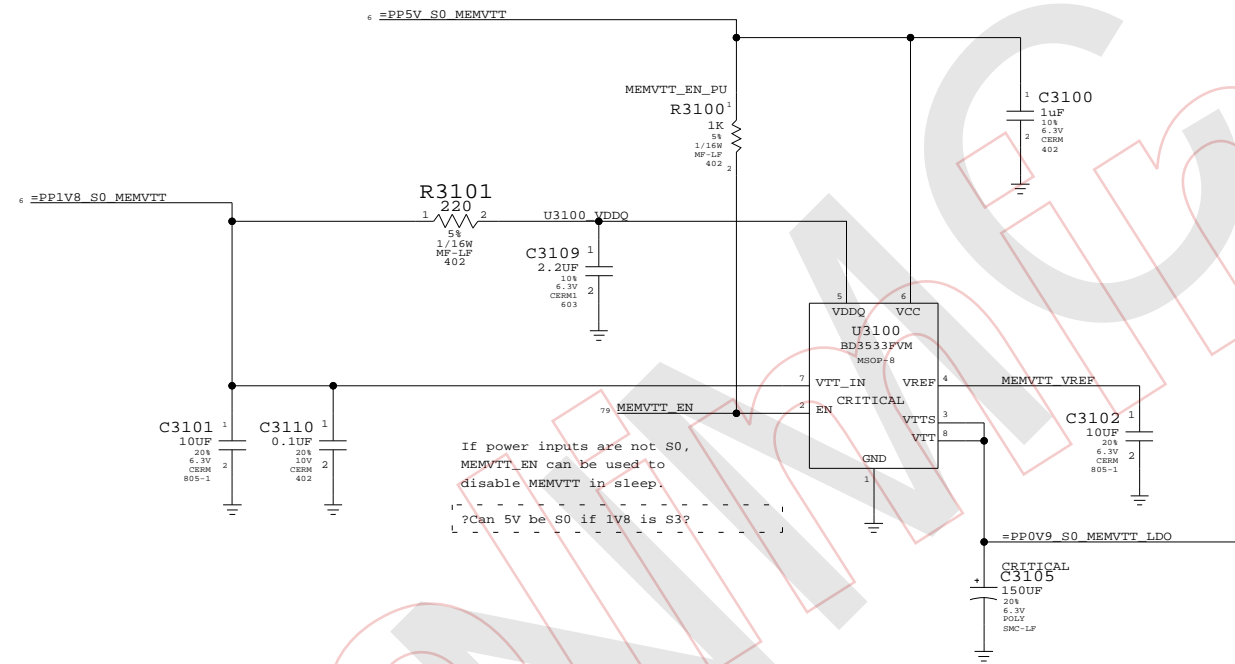
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

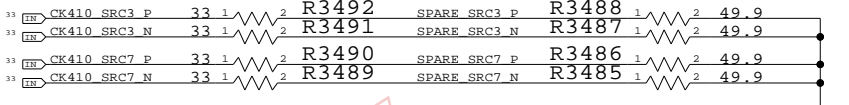
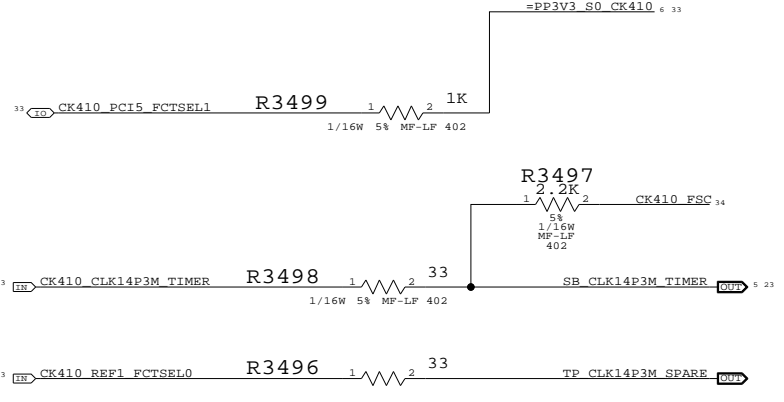
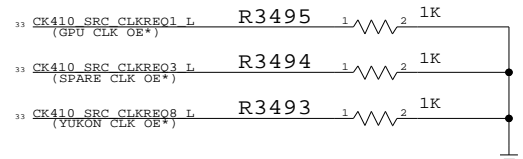
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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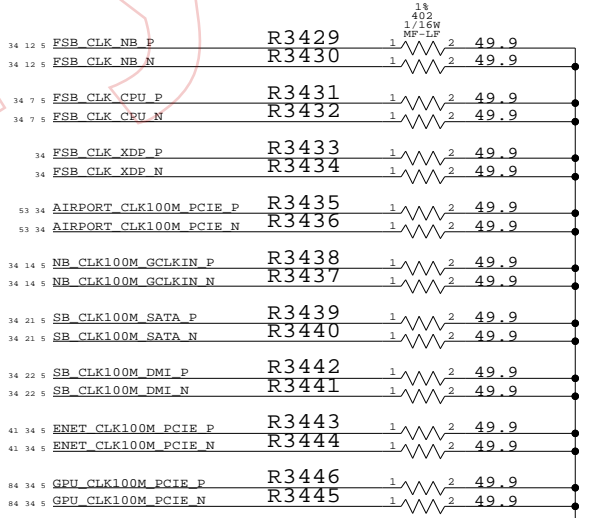
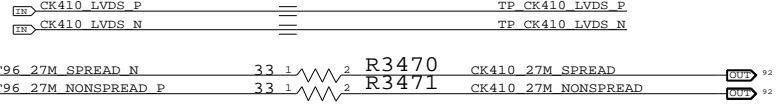
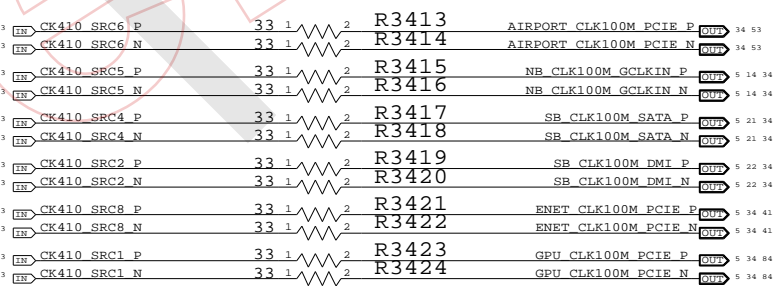
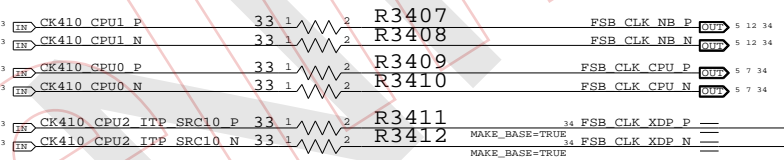
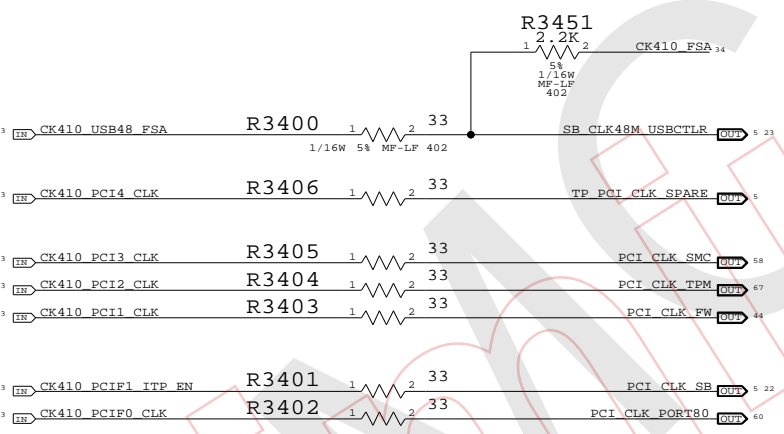
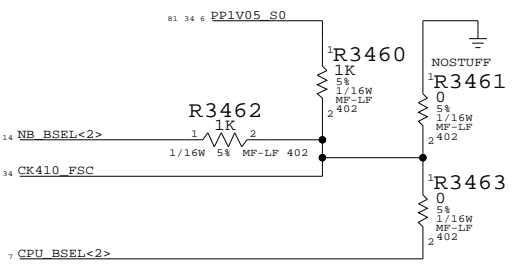
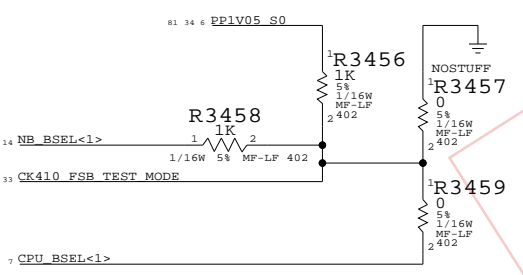
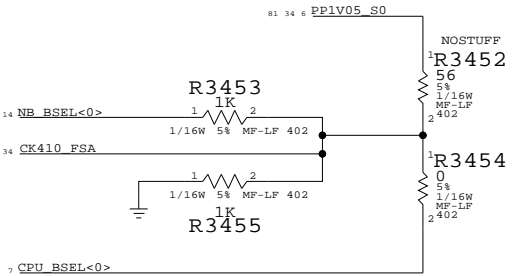
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	31	110	

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457



CLOCKS: TERMINATIONS

SYNC_MASTER=N/A SYNC_DATE=N/A

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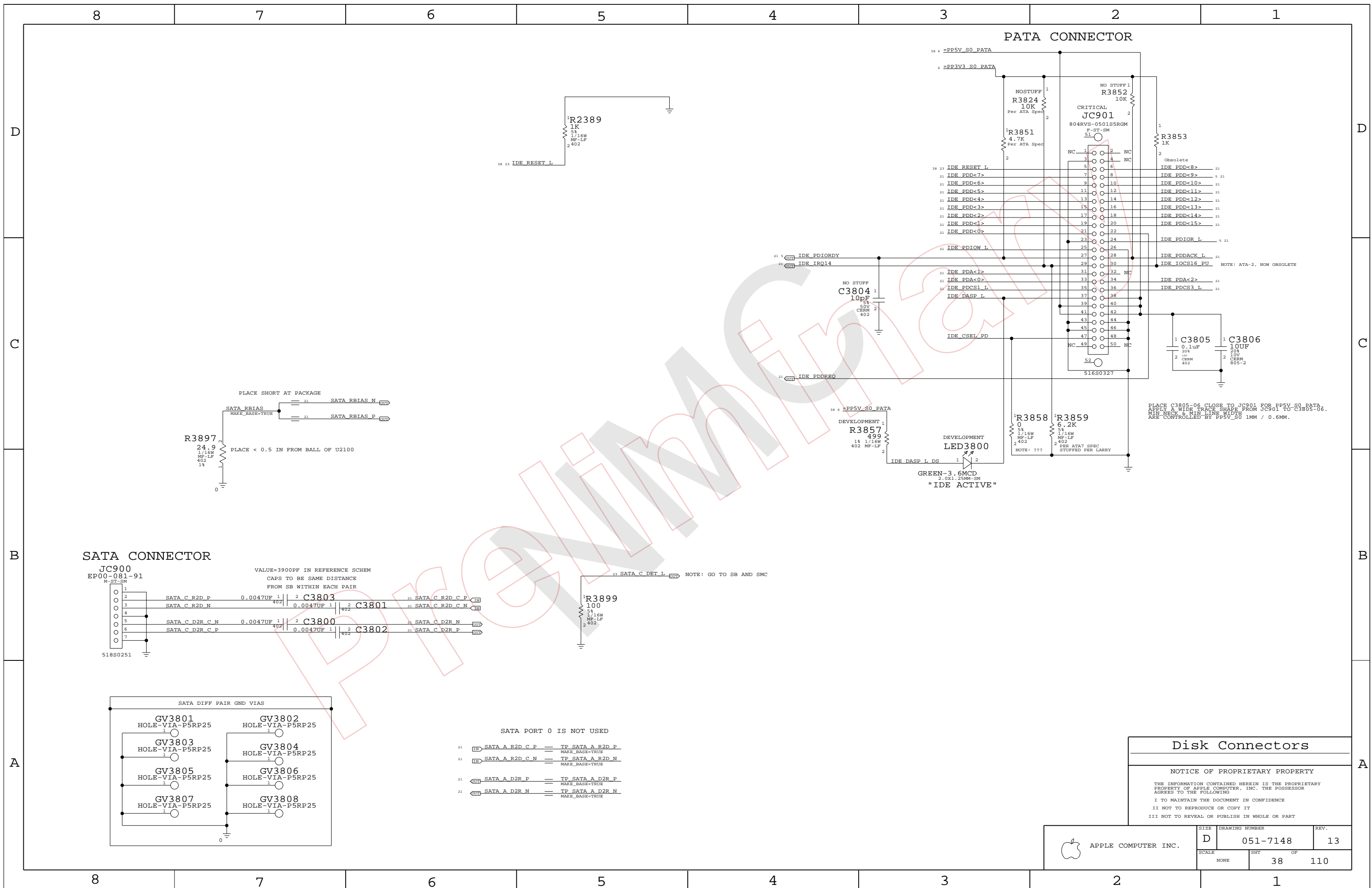
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE	SHT	OF
NONE	34	110



PATA CONNECTOR

SATA CONNECTOR

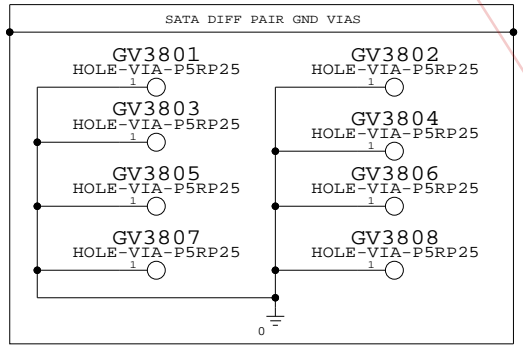
Disk Connectors

NOTICE OF PROPRIETARY PROPERTY

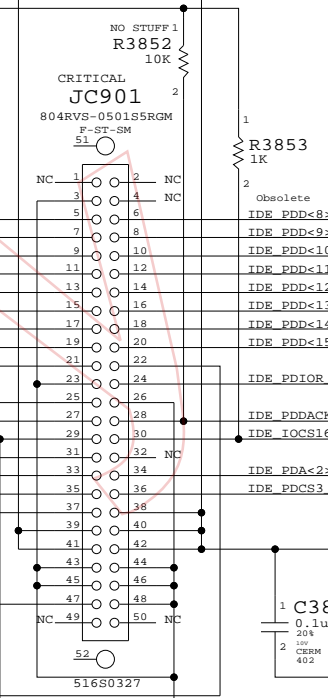
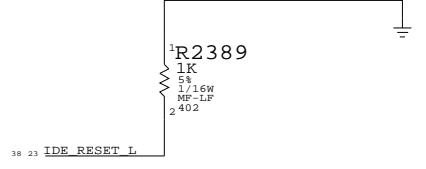
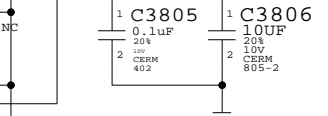
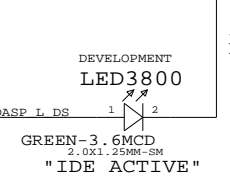
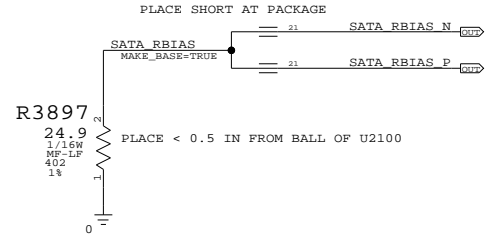
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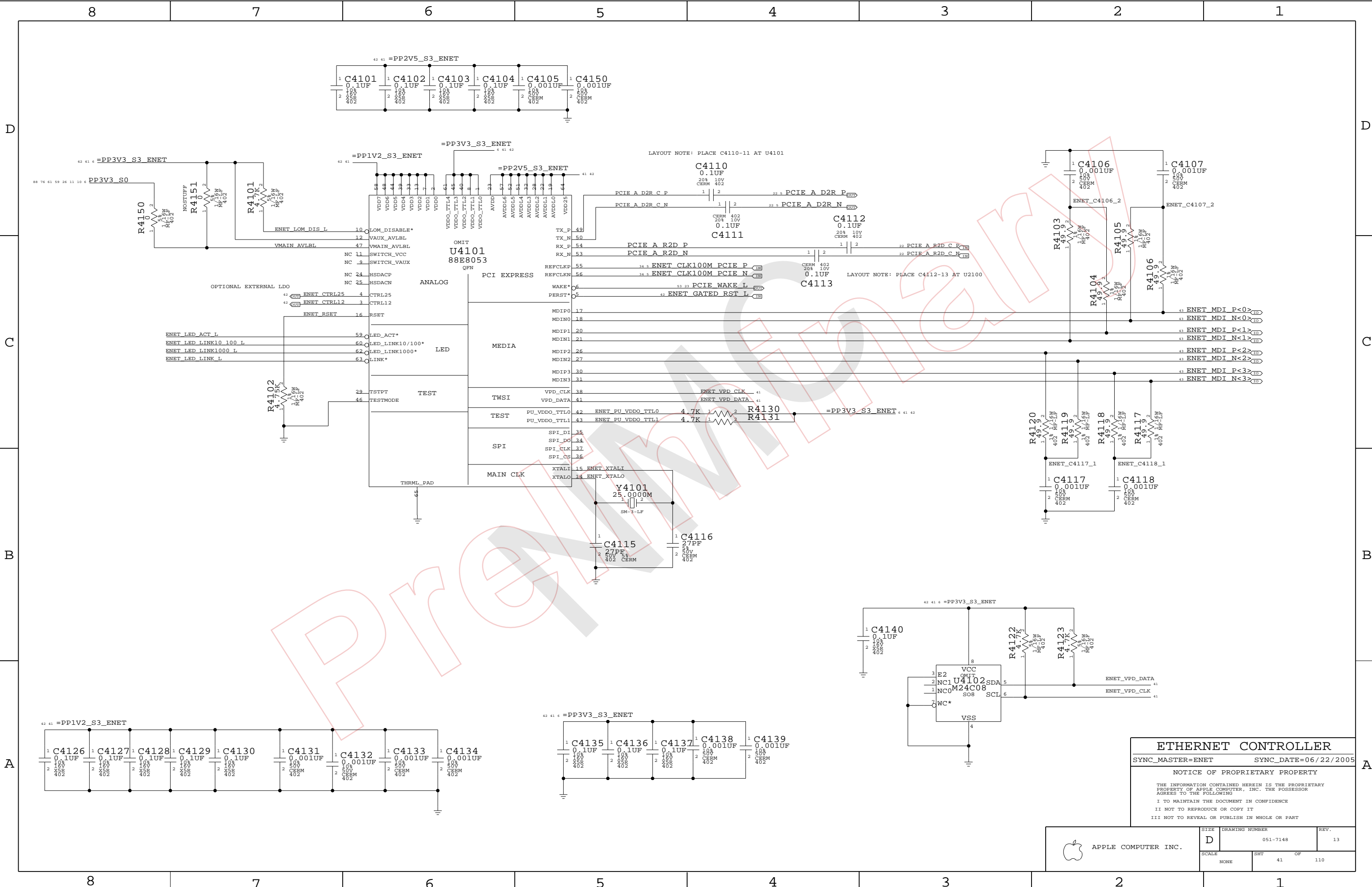
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT	OF
		38	110

- SATA PORT 0 IS NOT USED
- 21 (IN) SATA A R2D C P == TP SATA A R2D P
MAKE_BASE=TRUE
 - 21 (IN) SATA A R2D C N == TP SATA A R2D N
MAKE_BASE=TRUE
 - 21 (OUT) SATA A D2R P == TP SATA A D2R P
MAKE_BASE=TRUE
 - 21 (OUT) SATA A D2R N == TP SATA A D2R N
MAKE_BASE=TRUE



PLACE C3805-06 CLOSE TO JC901 FOR PP5V_S0_PATA. APPLY A WIDE TRACE SHAPE FROM JC901 TO C3805-06. MIN NECK & MIN LINE WIDTHS ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.





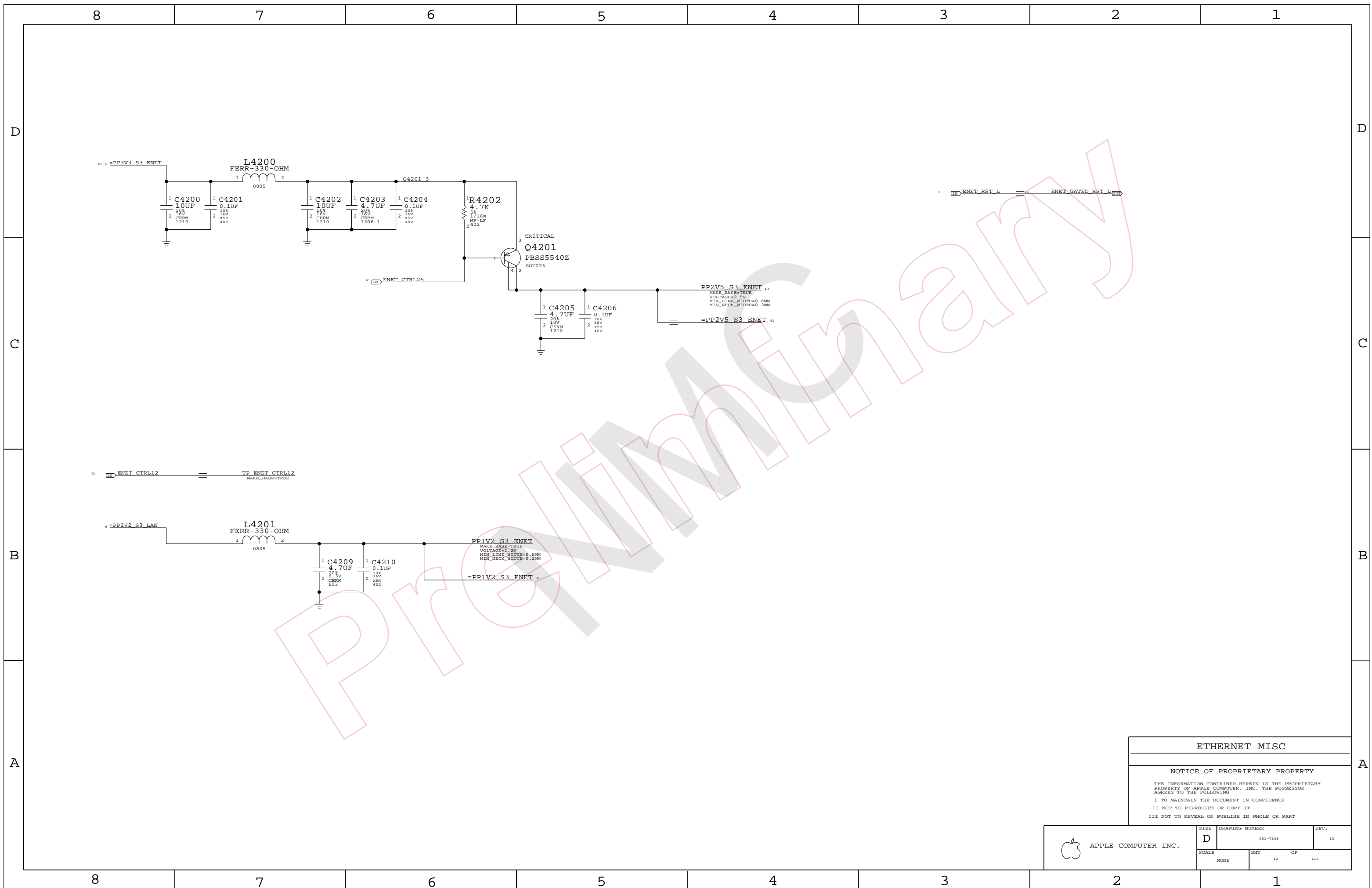
ETHERNET CONTROLLER
 SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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	D	051-7148	13
SCALE	NONE	SHT	41 OF 110



ETHERNET MISC

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 42	OF 110

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C

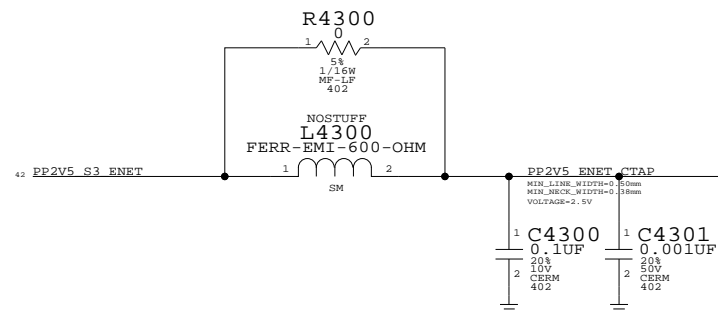
C

B

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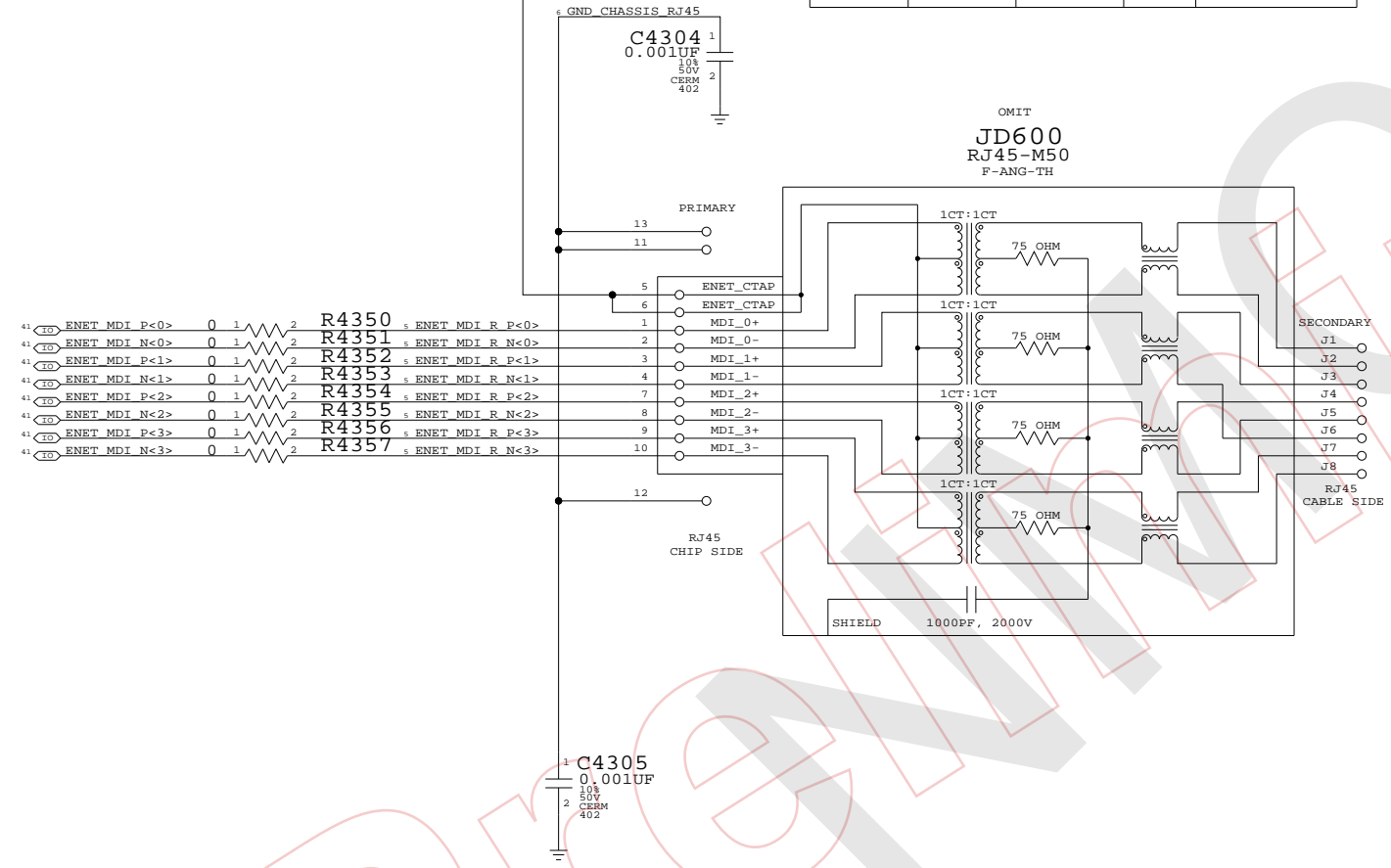
A

A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0366	1	FOXCONN AND DELTA RJ45	JD600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
-------------	---------------------------	------------	---------	-----------



ETHERNET CONNECTOR

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	D	051-7148	13
SCALE		SHT	OF
NONE		43	110

8

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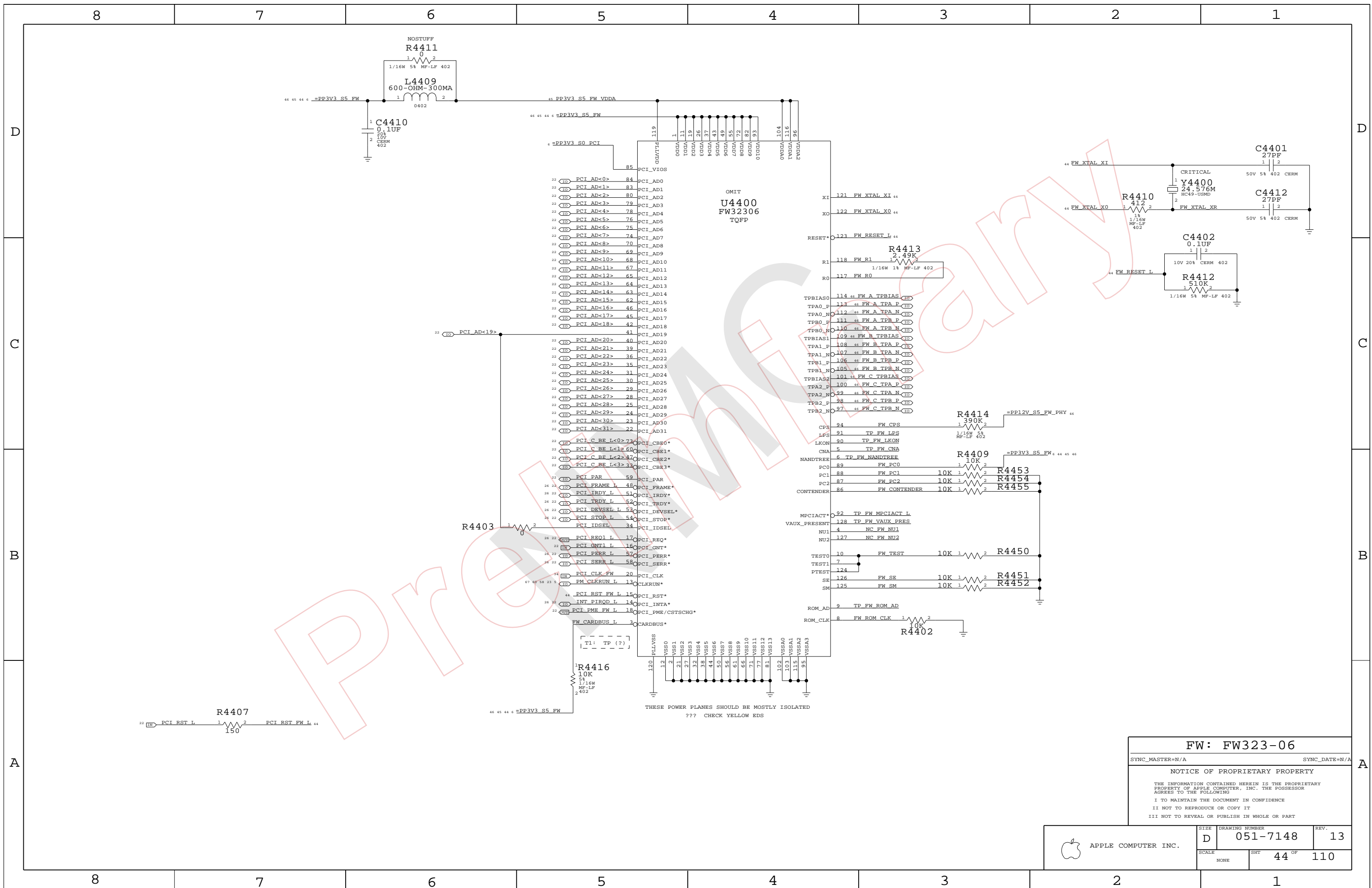
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FW: FW323-06

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

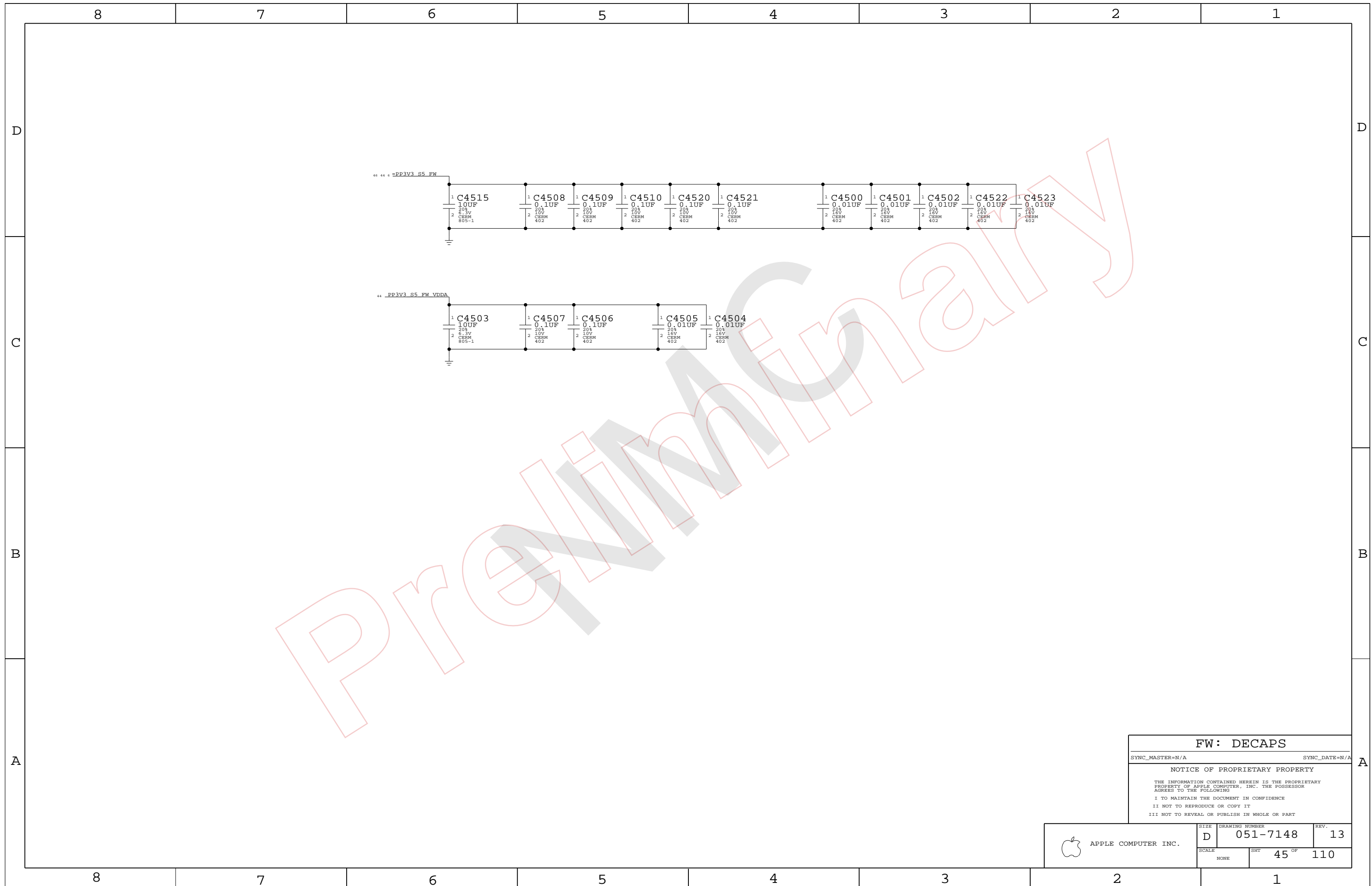
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	SCALE NONE	SHEETS 44 OF 110	



PRELIMINARY

FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

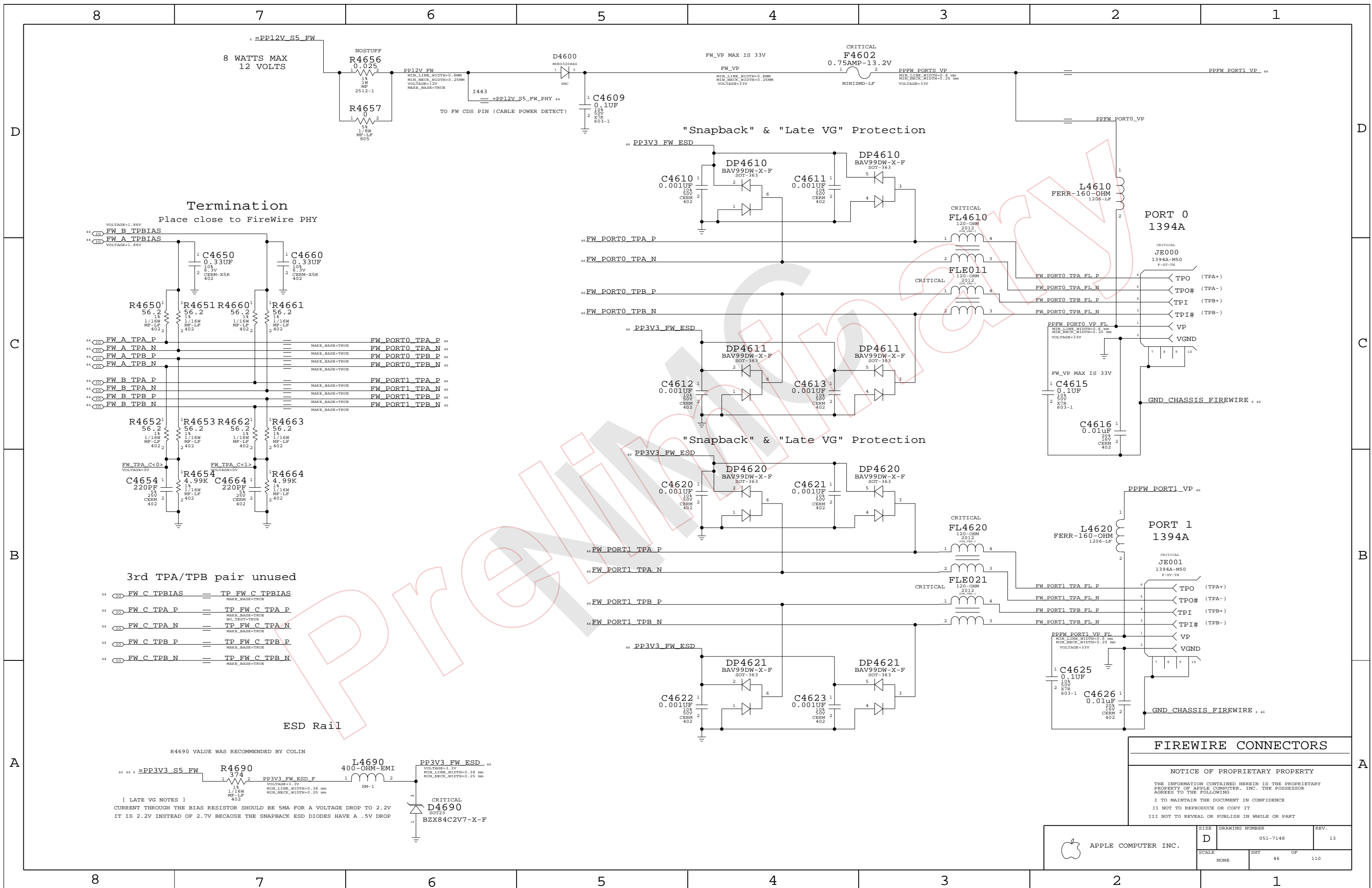
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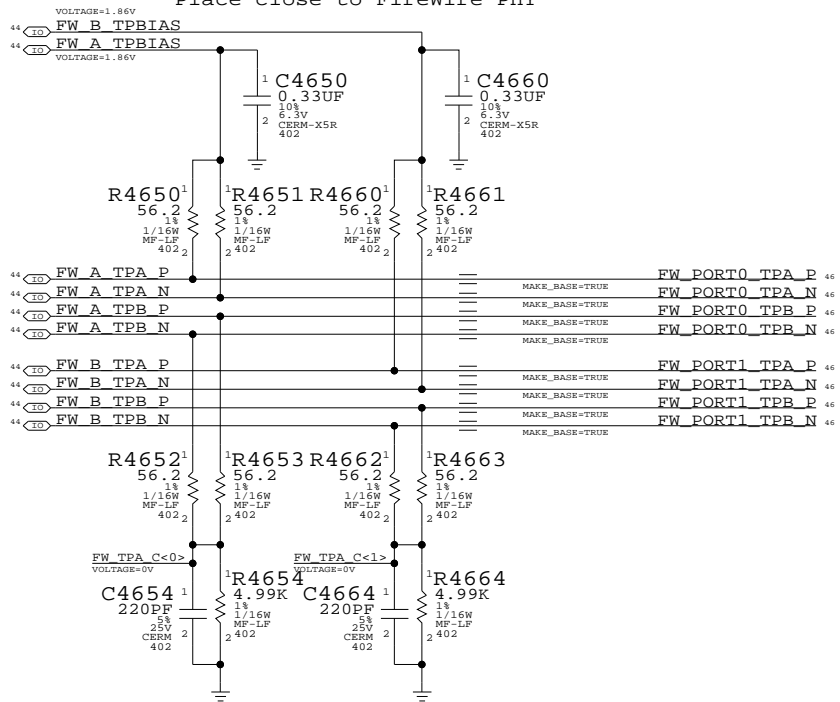
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

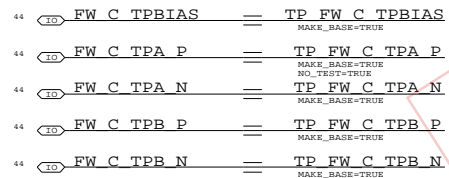
APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7148	REV.	13
	SCALE	NONE	SHT	45 OF	110	



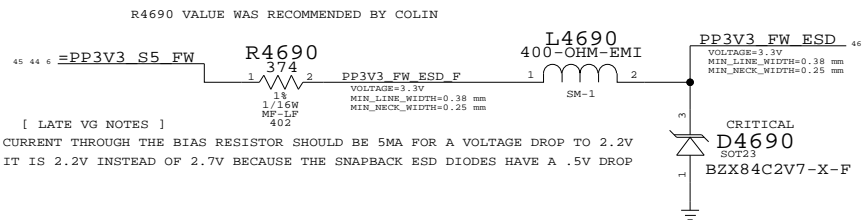
Termination
Place close to FireWire PHY



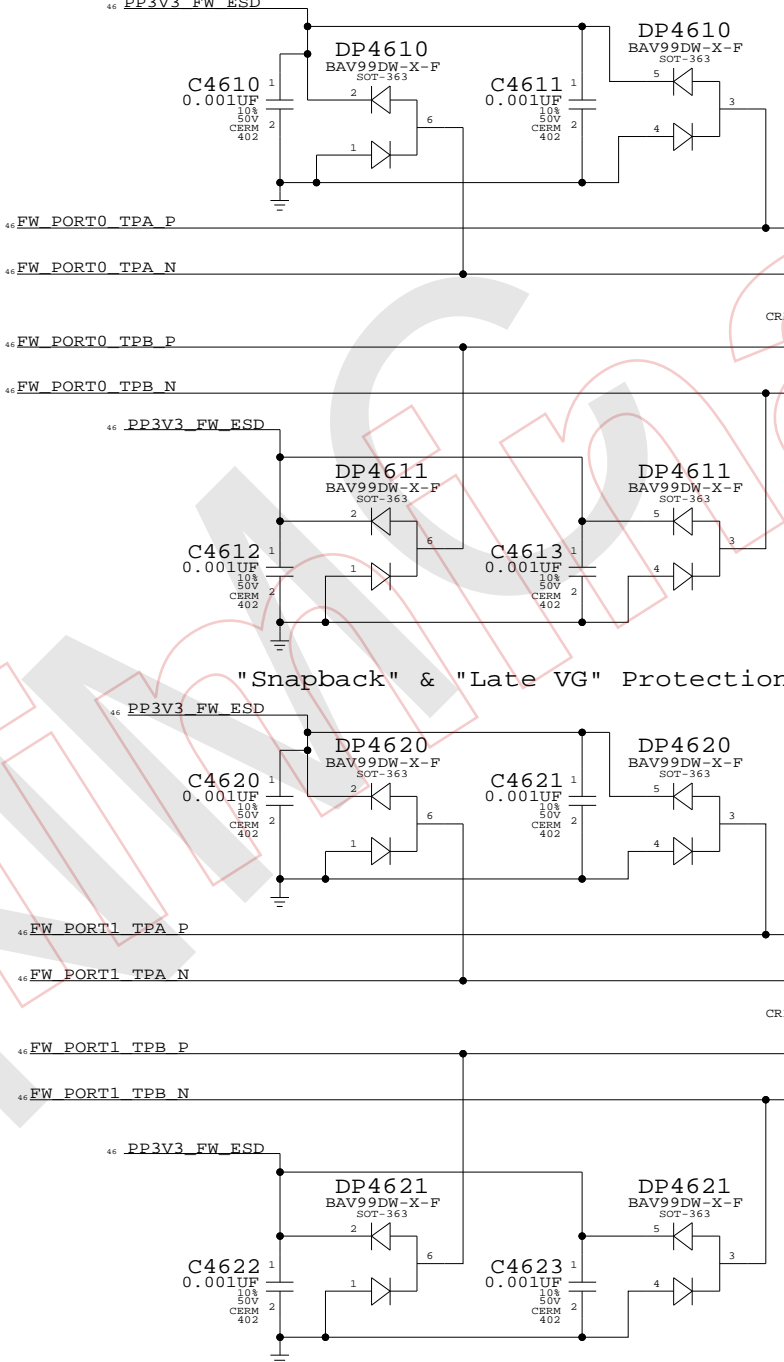
3rd TPA/TPB pair unused



ESD Rail



"Snapback" & "Late VG" Protection



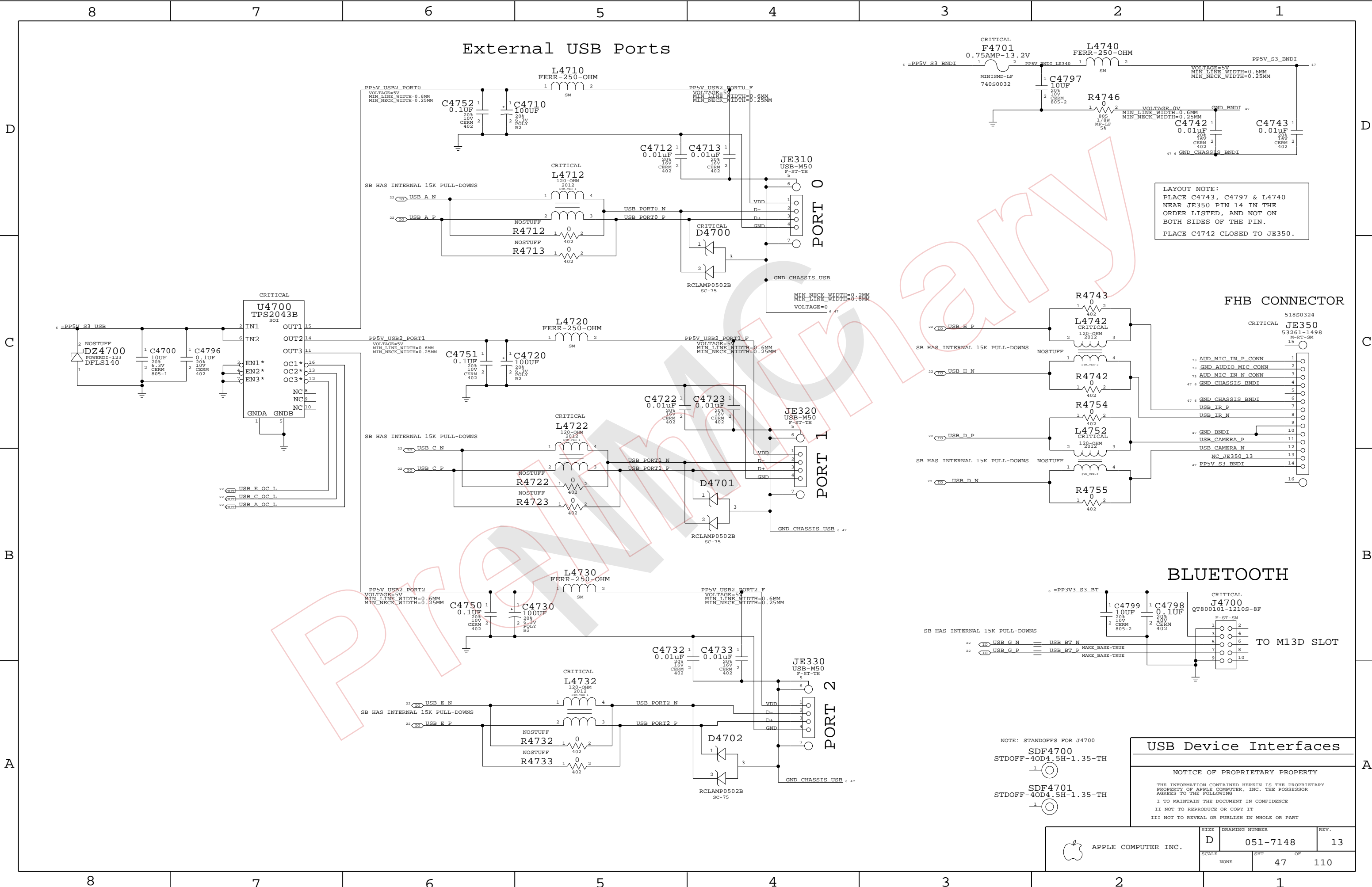
FIREWIRE CONNECTORS

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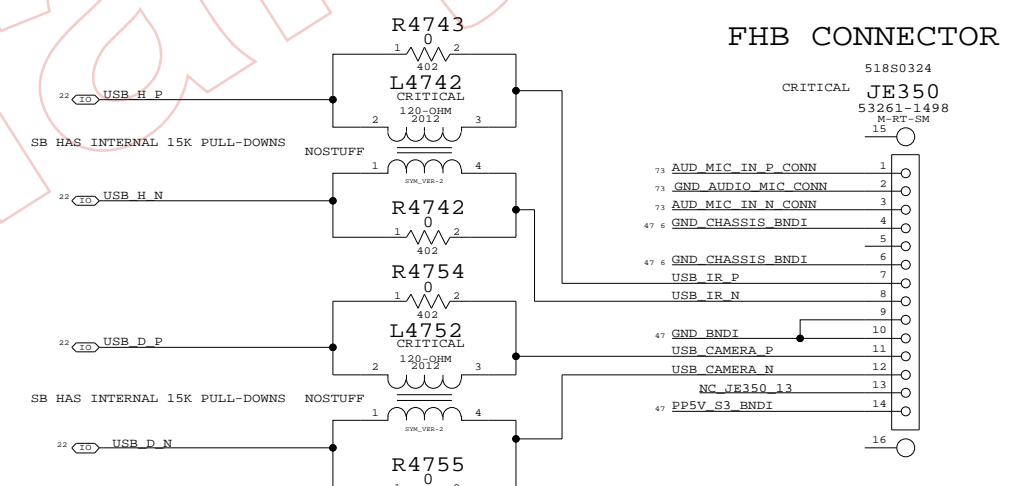
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	110
NONE	46		

External USB Ports

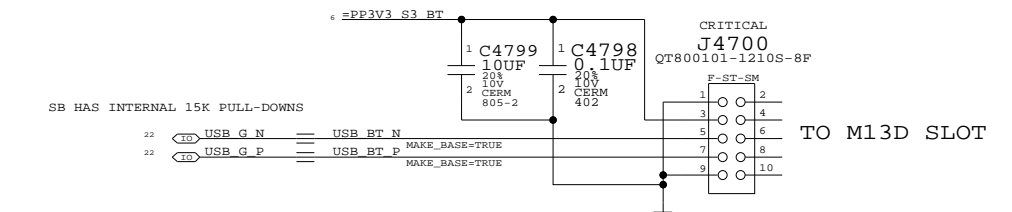


LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE350 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE350.

FHB CONNECTOR



BLUETOOTH

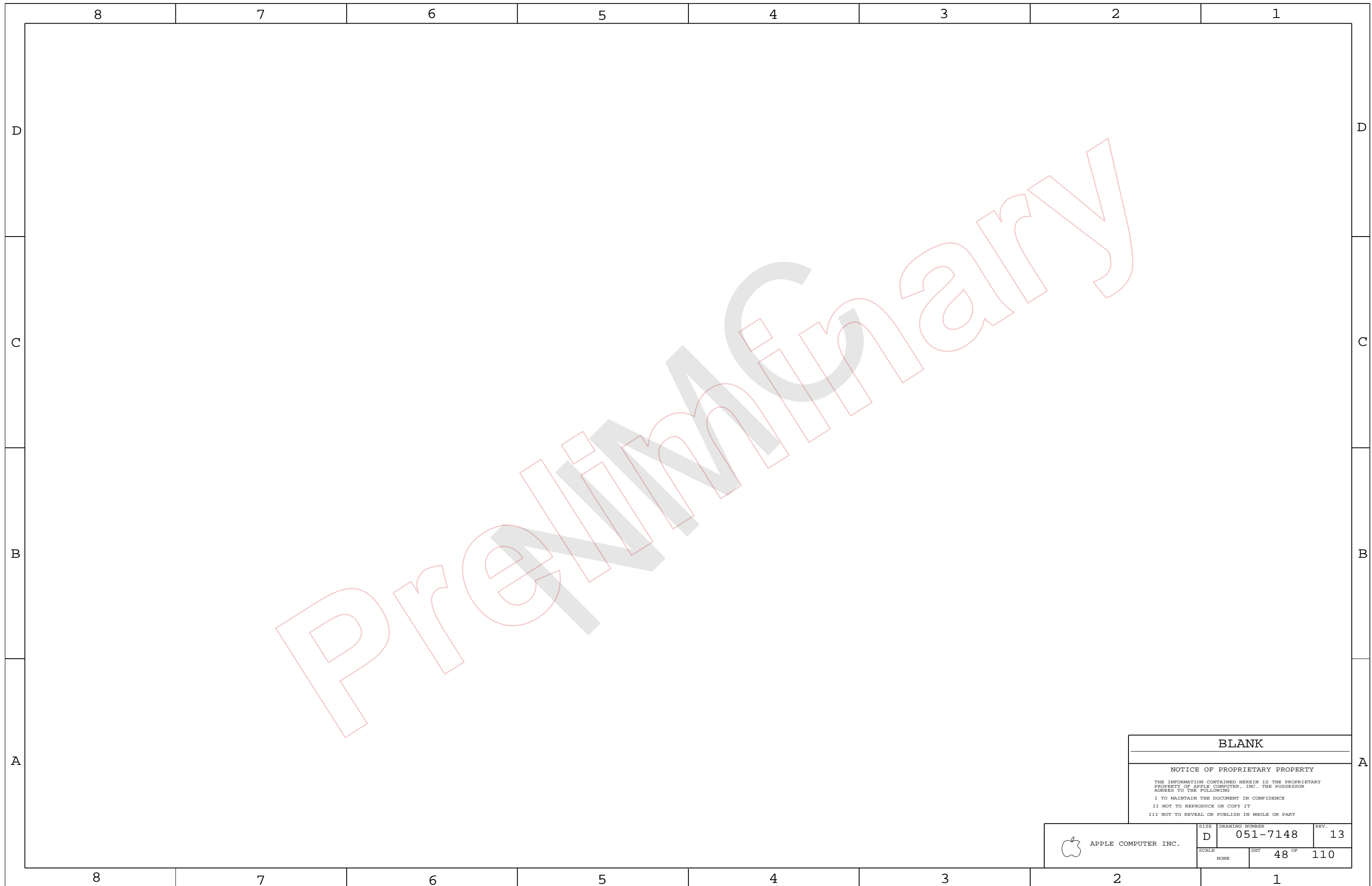


NOTE: STANDOFFS FOR J4700
 SDF4700
 STDOFF-40D4.5H-1.35-TH
 SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT	OF
		47	110



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NOTICE OF PROPRIETARY PROPERTY

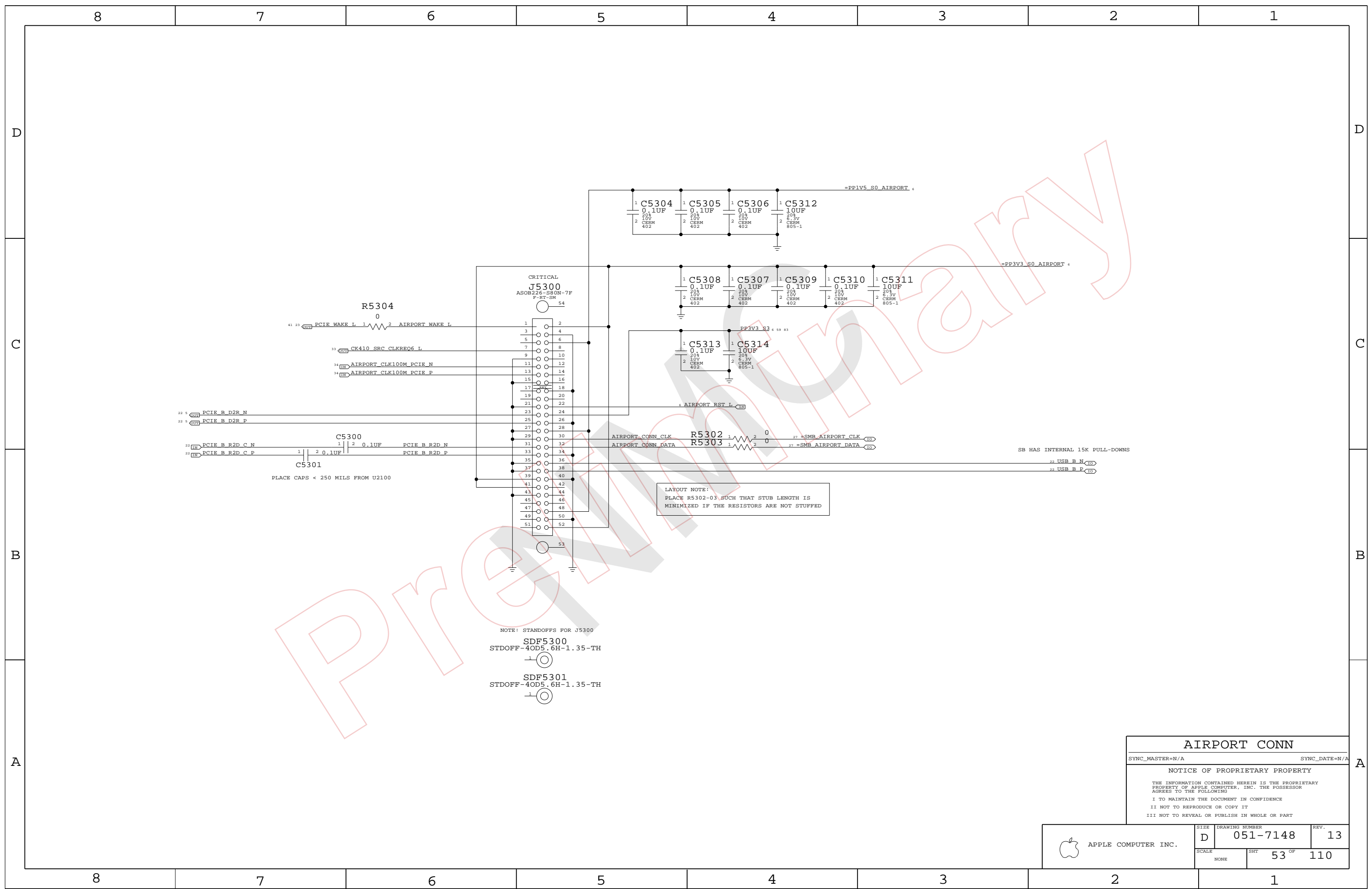
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE



II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	<small>SIZE</small> D	<small>DRAWING NUMBER</small> 051-7148	<small>REV.</small> 13
	<small>SCALE</small> NONE	<small>SHT</small> 48 OF	<small>110</small>



LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH

 SDF5301
 STDOFF-40D5.6H-1.35-TH



AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 53 OF	TOTAL SHEETS 110

8

7

6

5

4

3

2

1

D

D

C


C


B


B


A


A


22  PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE


22  PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE


22  PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE


22  PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE


22  PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE


22  PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE


22  PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE


22  PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE


22  PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE


22  PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE


22  PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22  PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE

22  PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22  PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22  PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22  PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

ProtonMinimally


PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	54	110	

8

7

6

5

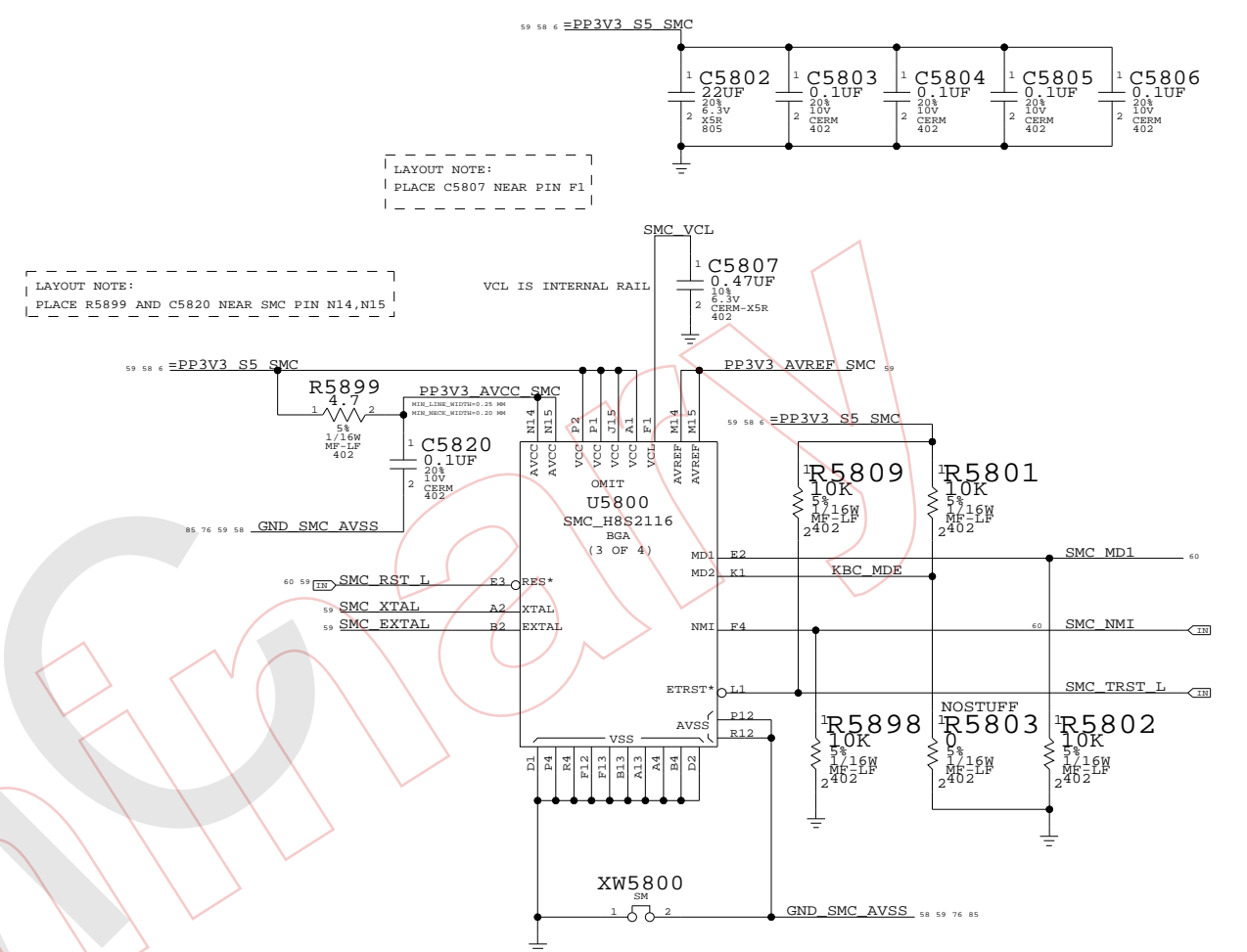
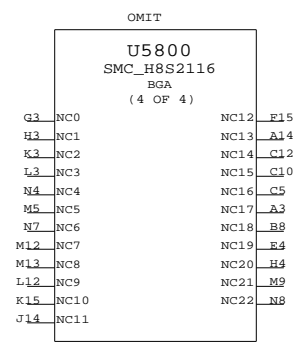
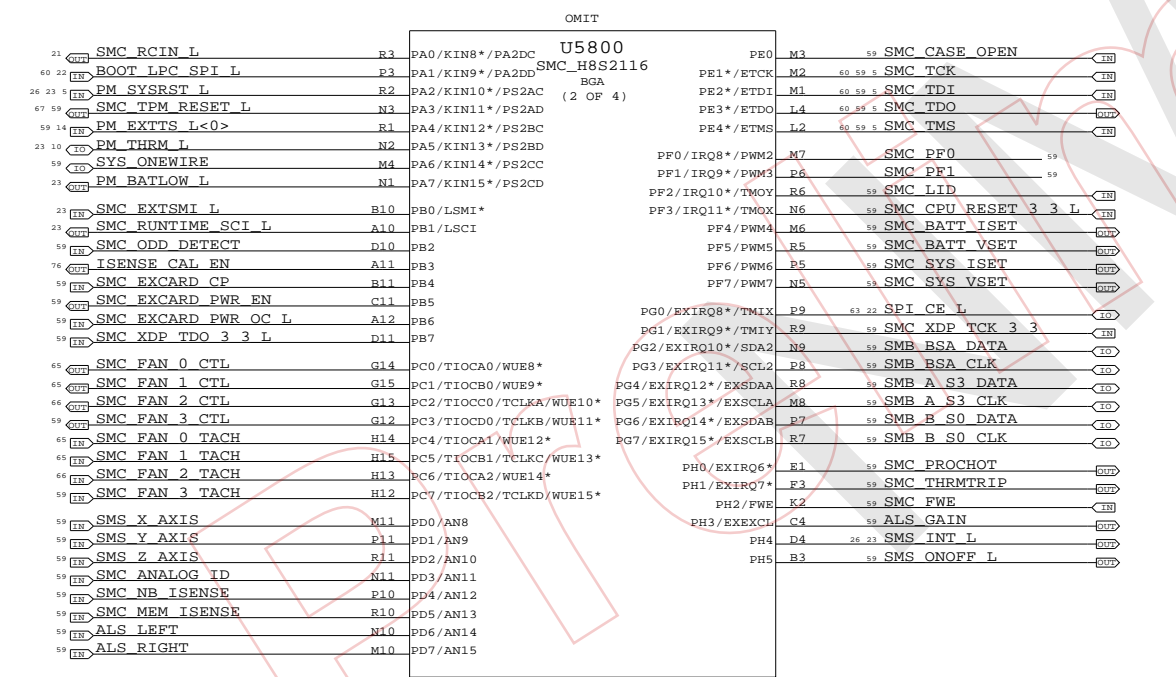
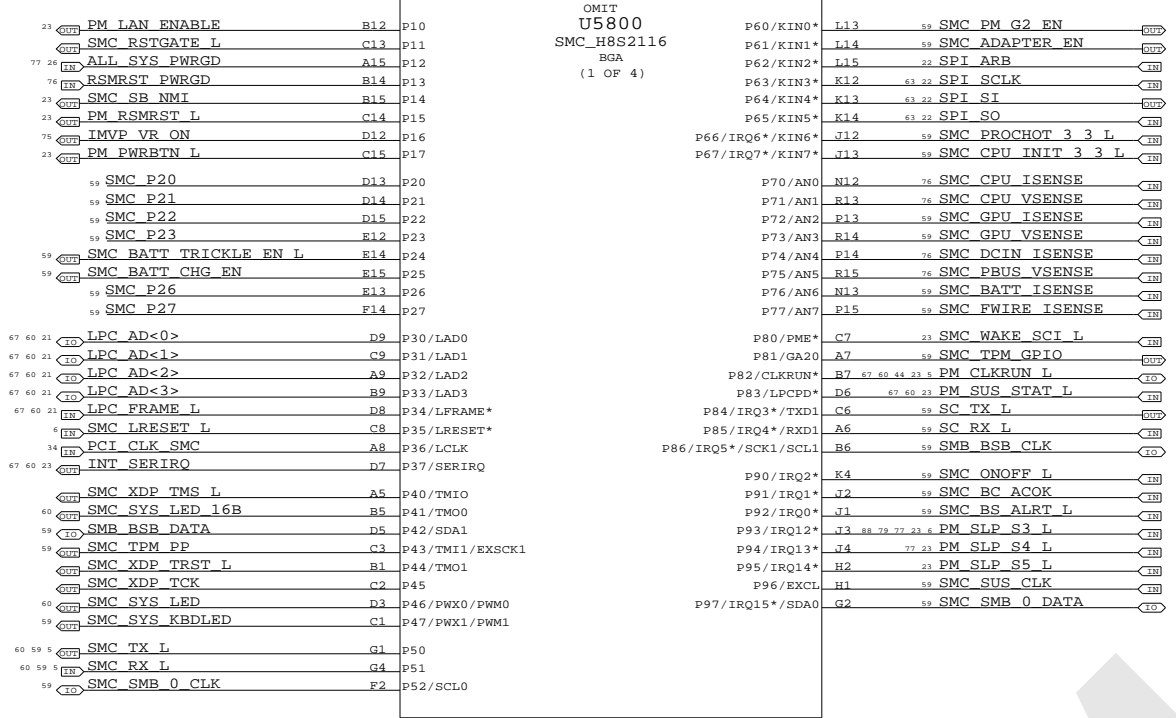
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

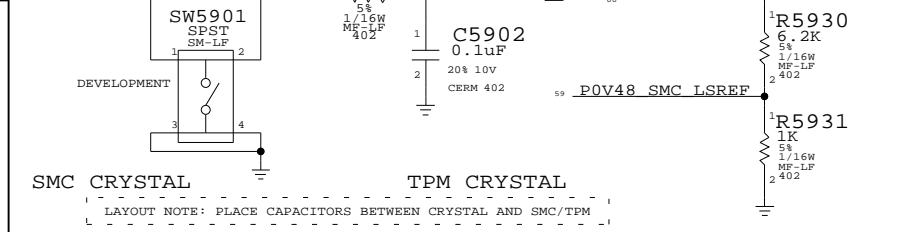
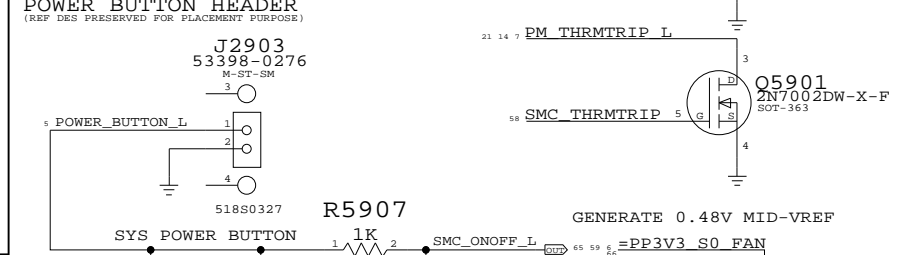
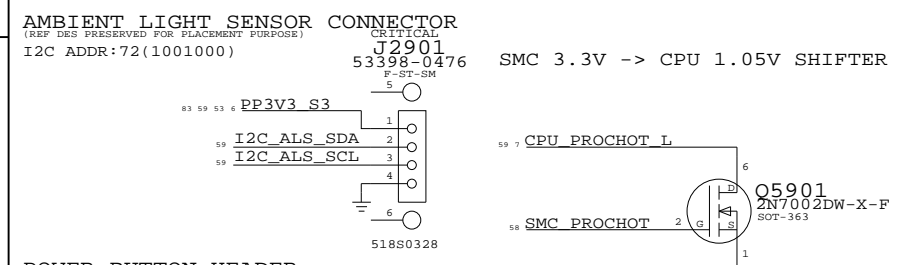
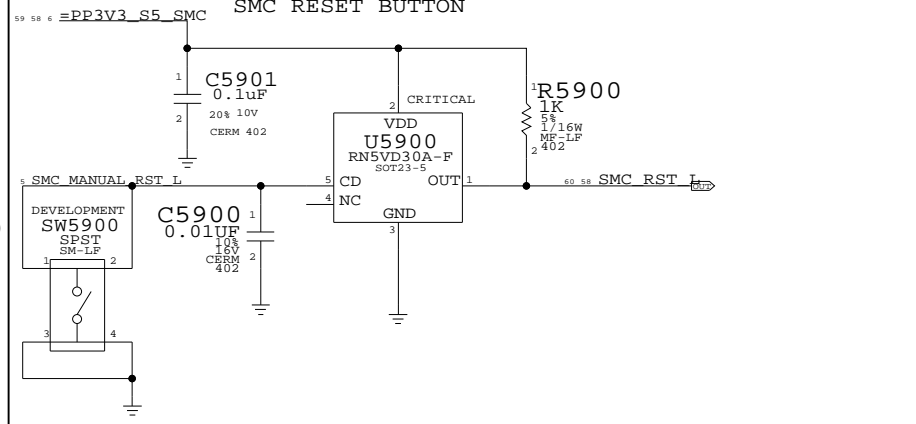
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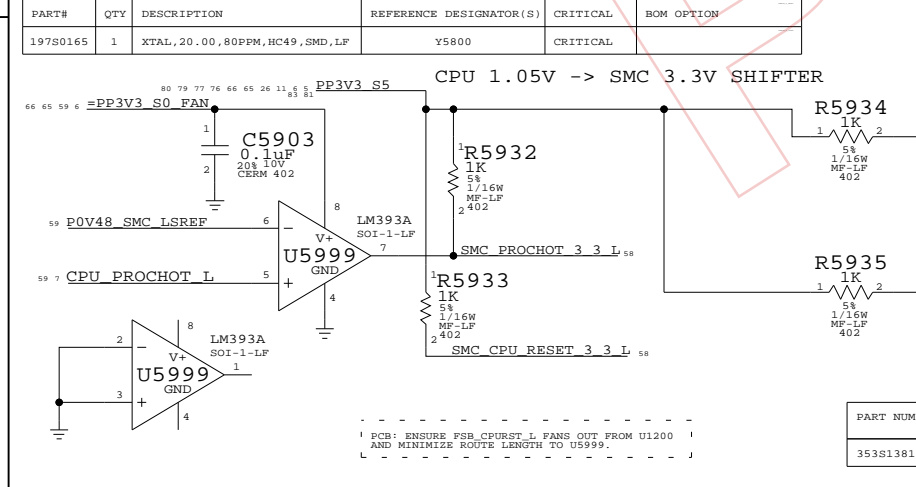
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<p>APPLE COMPUTER INC.</p>	<p>SIZE D</p>	<p>DRAWING NUMBER 051-7148</p>	<p>REV. 13</p>
	<p>SCALE NONE</p>	<p>SHT 58 OF 110</p>	

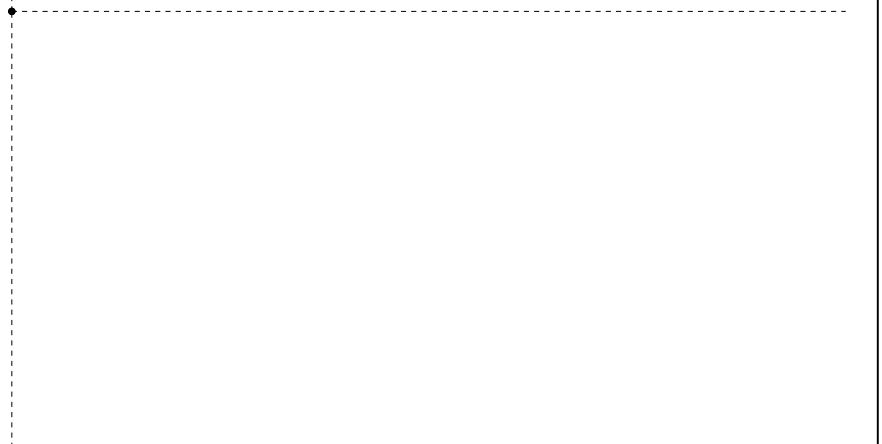
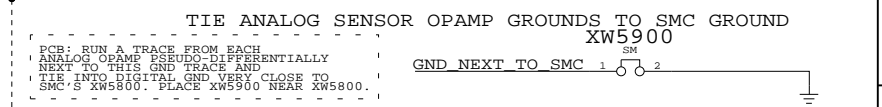
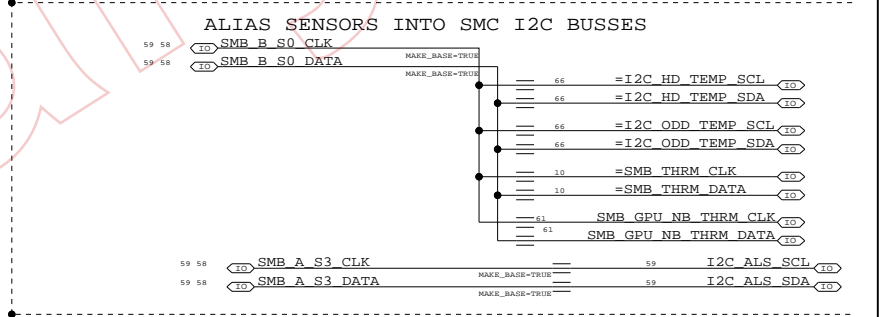
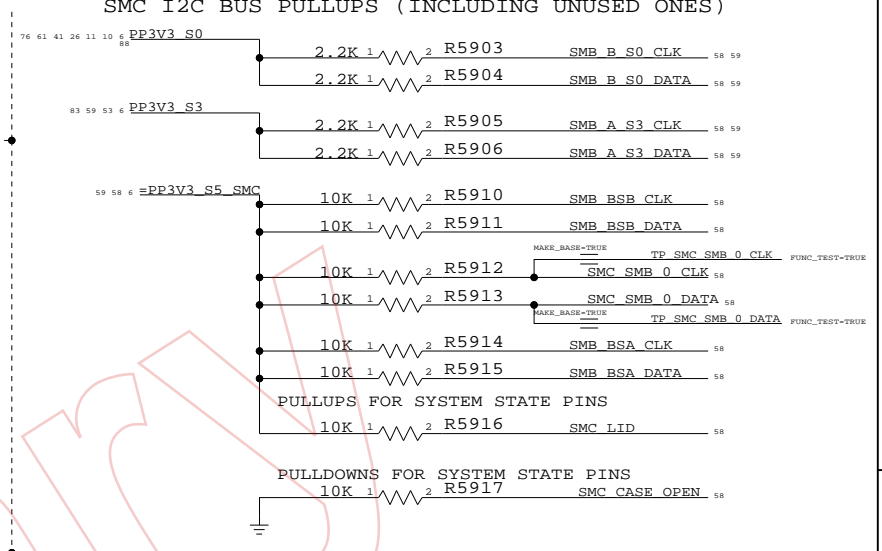
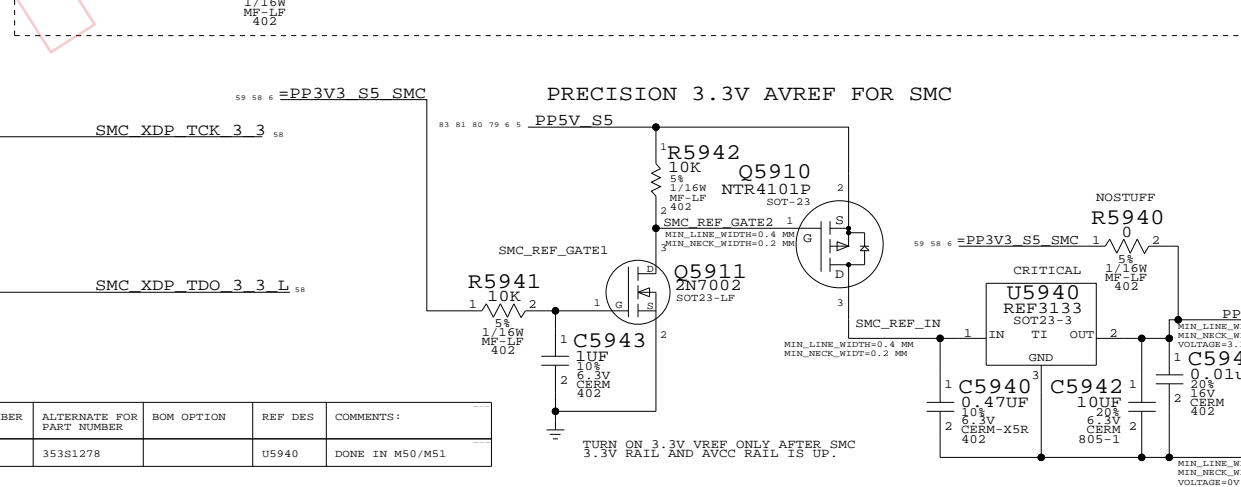
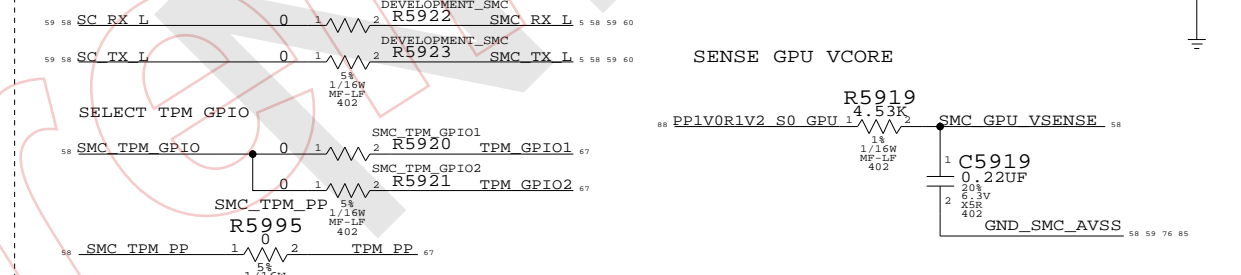
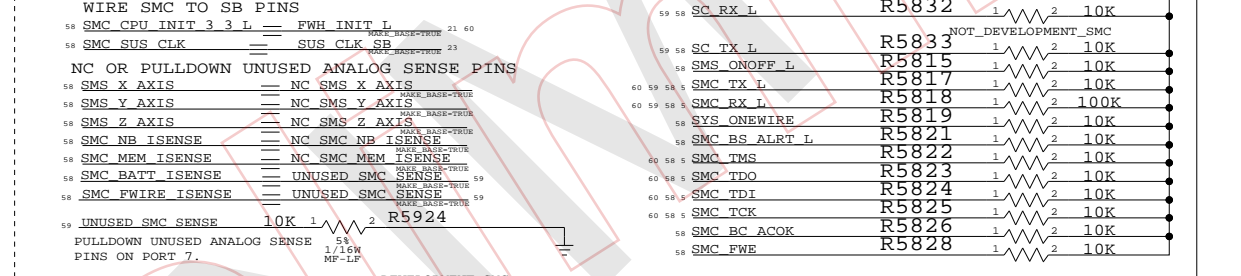
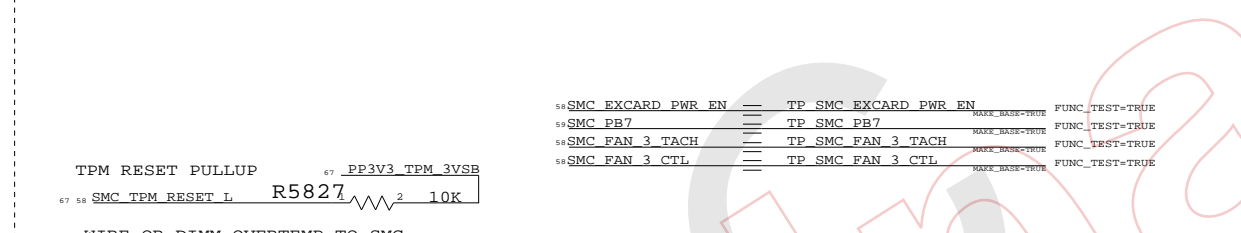


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	SMC ALIASES	TESTPOINTS	FUNCTION
58 SMC P20	NC SMC P20		
58 SMC P21	NC SMC P21		
58 SMC P22	NC SMC P22		
58 SMC P23	NC SMC P23		
58 SMC P26	NC SMC P26		
58 SMC P27	NC SMC P27		
58 SMC BATT_ISET	NC SMC BATT_ISET		
58 SMC BATT_VSET	NC SMC BATT_VSET		
58 SMC SYS_ISET	NC SMC SYS_ISET		
58 SMC SYS_VSET	NC SMC SYS_VSET		
58 SMC BATT_TRICKLE_EN_L	NC SMC BATT_TRICKLE_EN_L		
58 SMC BATT_CHG_EN	NC SMC BATT_CHG_EN		
58 SMC ANALOG_ID	NC SMC ANALOG_ID		
58 ALS_GAIN	NC ALS_GAIN		



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
35381381	35381278		U5940	DONE IN M50/M51

SMC & TPM SUPPORT

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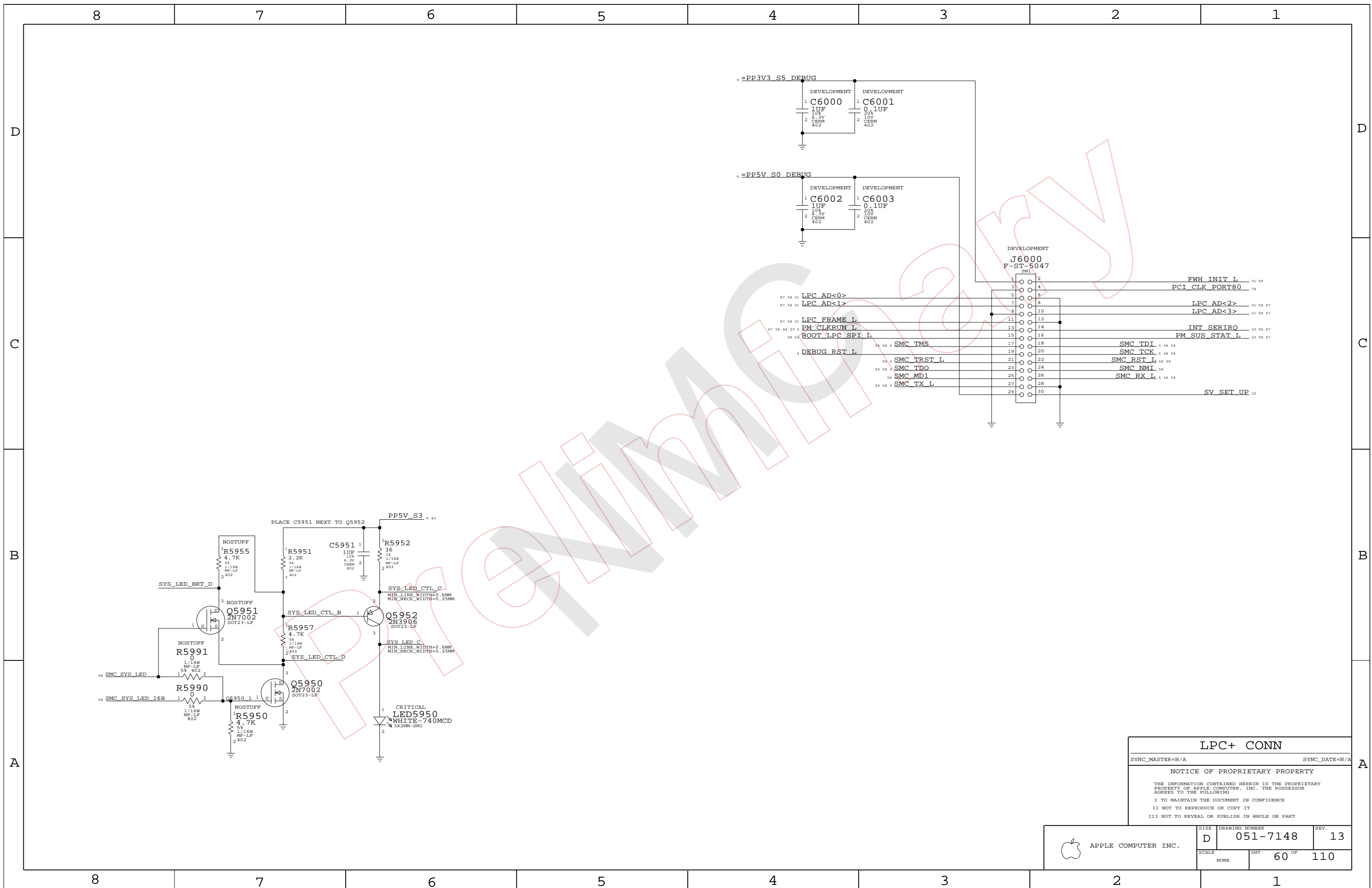
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SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE: NONE SHEET: 59 OF 110

APPLE COMPUTER INC.



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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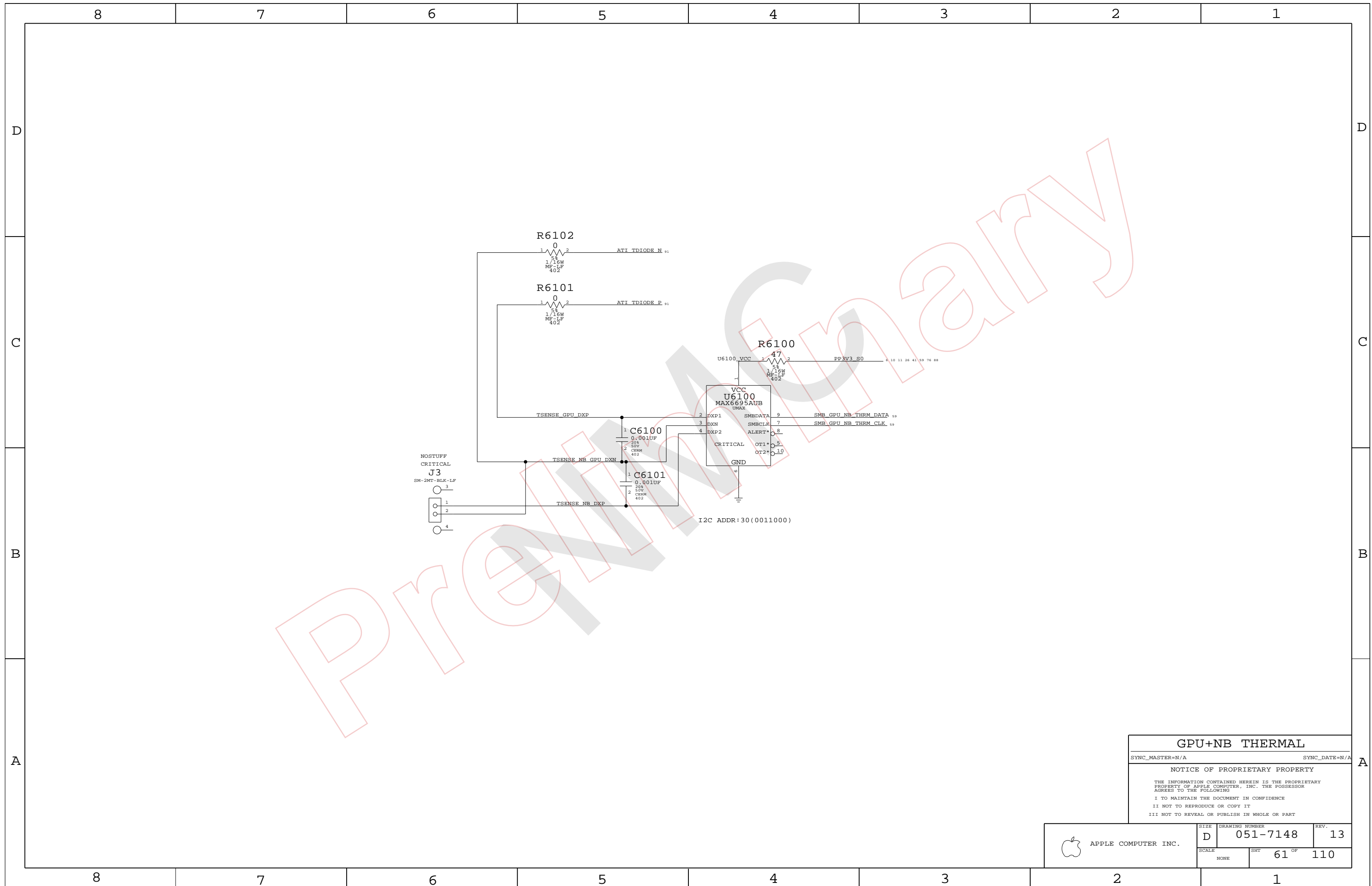
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHT 60 OF	110

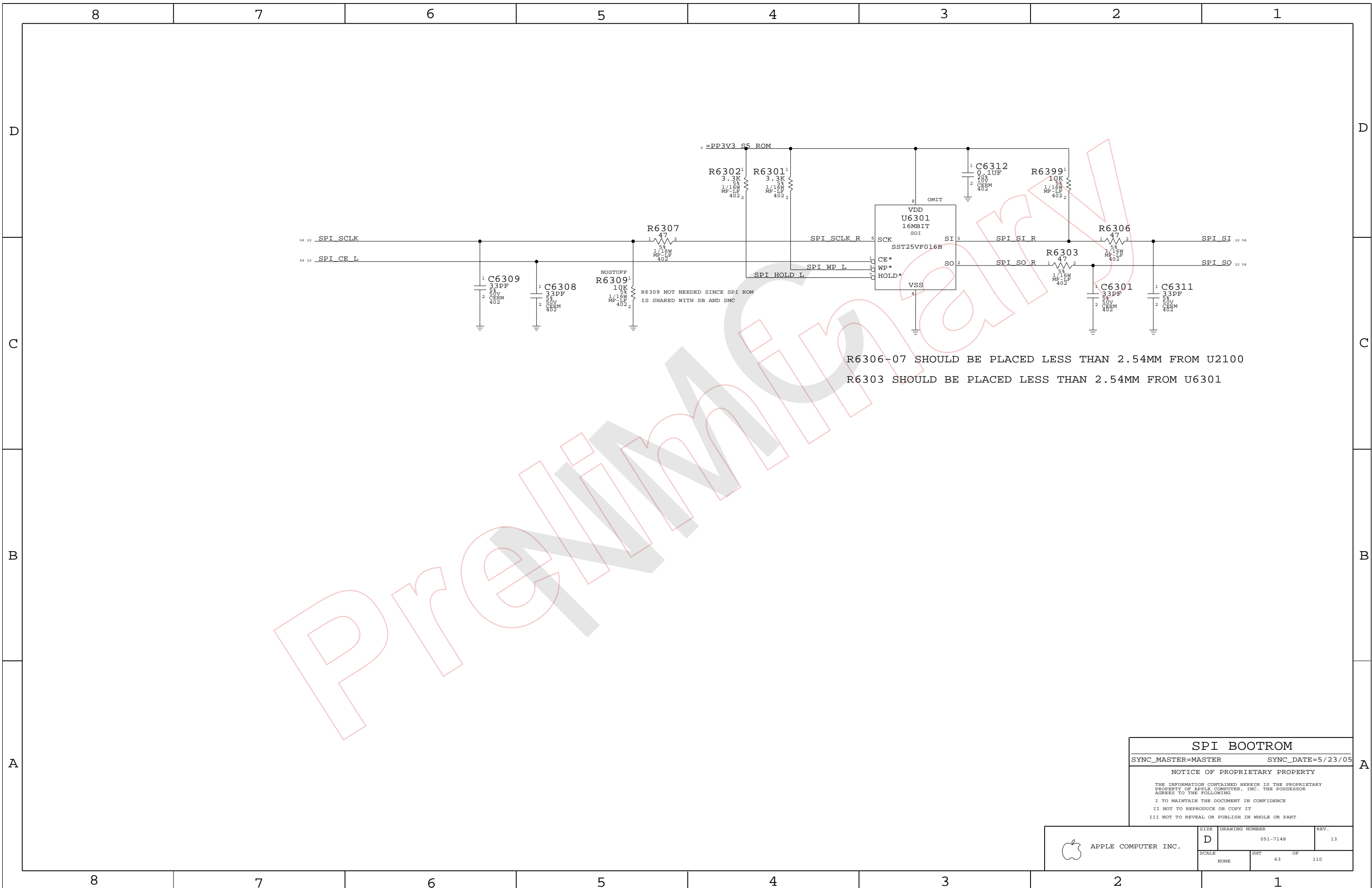


Preview

GPU+NB THERMAL

SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 61 OF 110	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

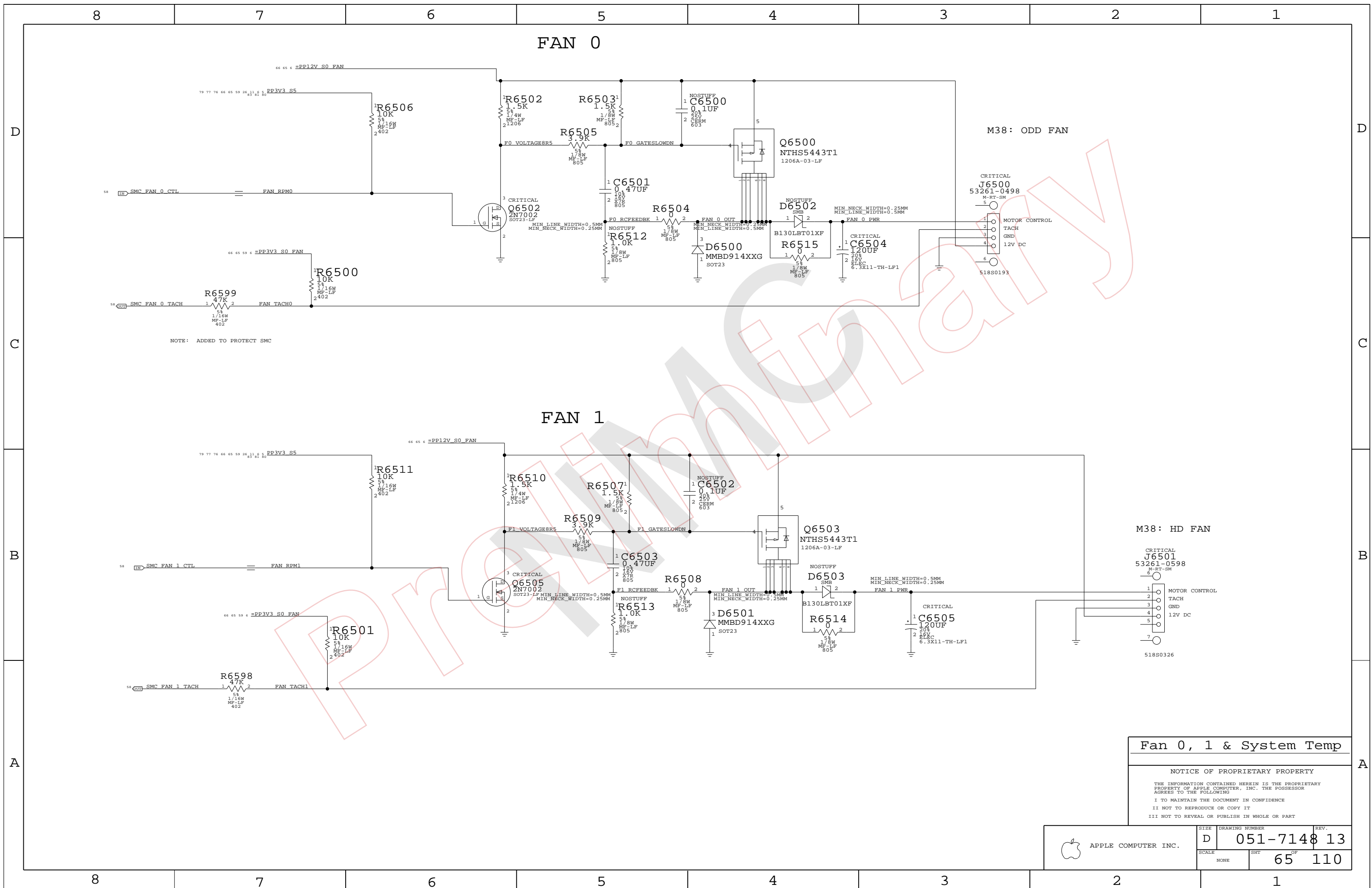
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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	SCALE NONE	SHEETS 63	OF 110

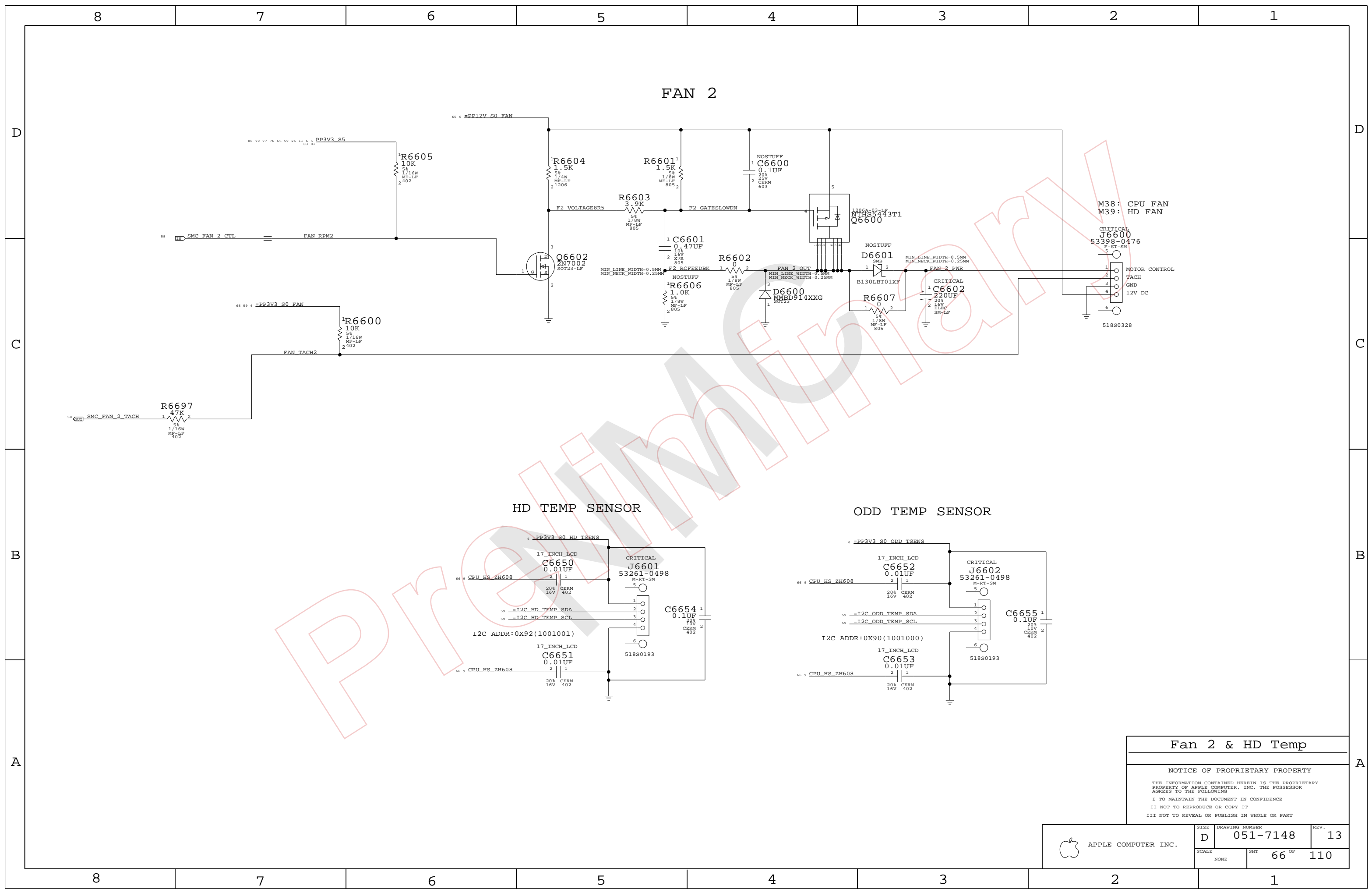


NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT	OF
		65	110



FAN 2

HD TEMP SENSOR

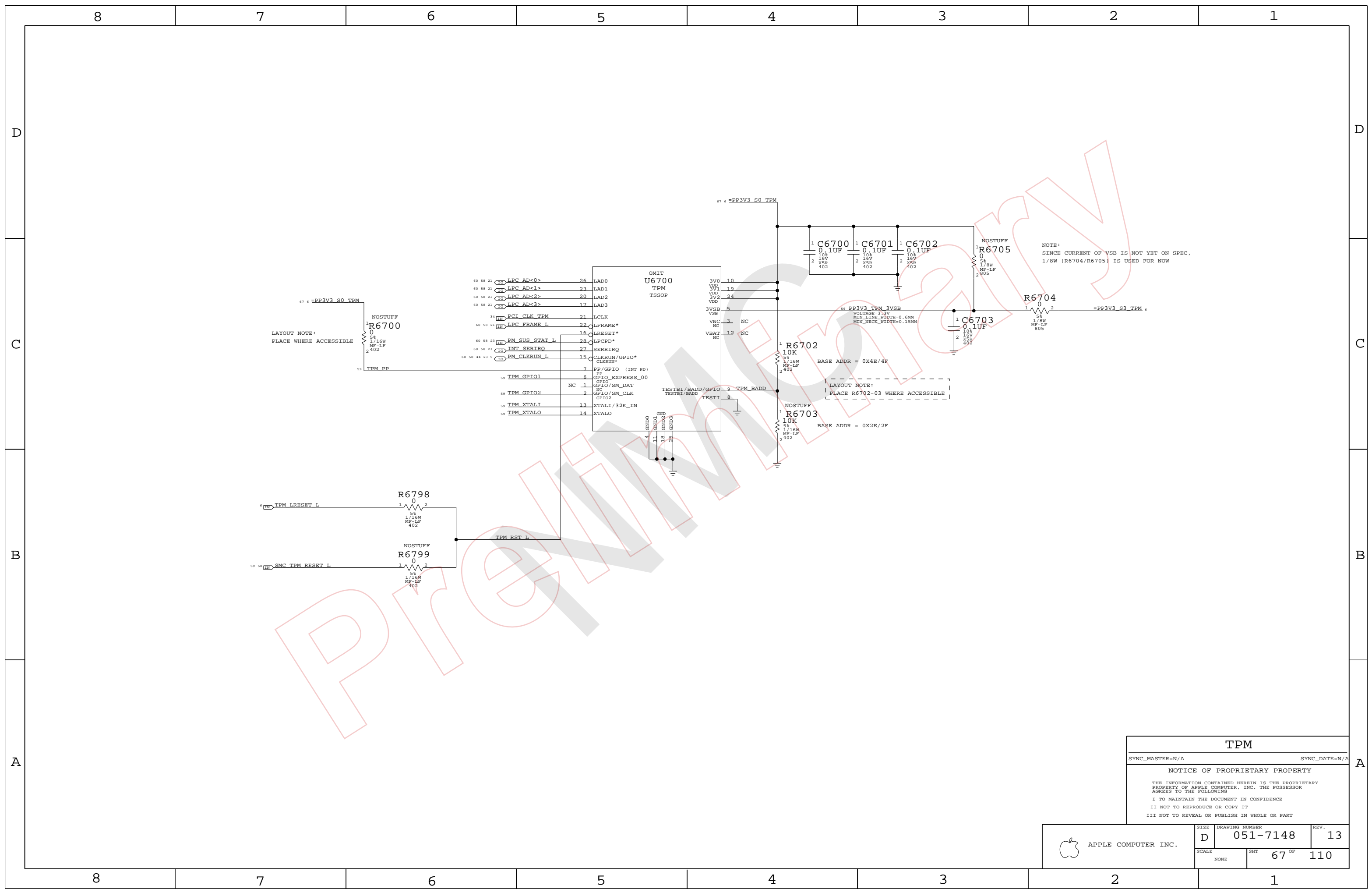
ODD TEMP SENSOR

Fan 2 & HD Temp

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	D	051-7148	13
SCALE	SHT	OF	
NONE	66	110	



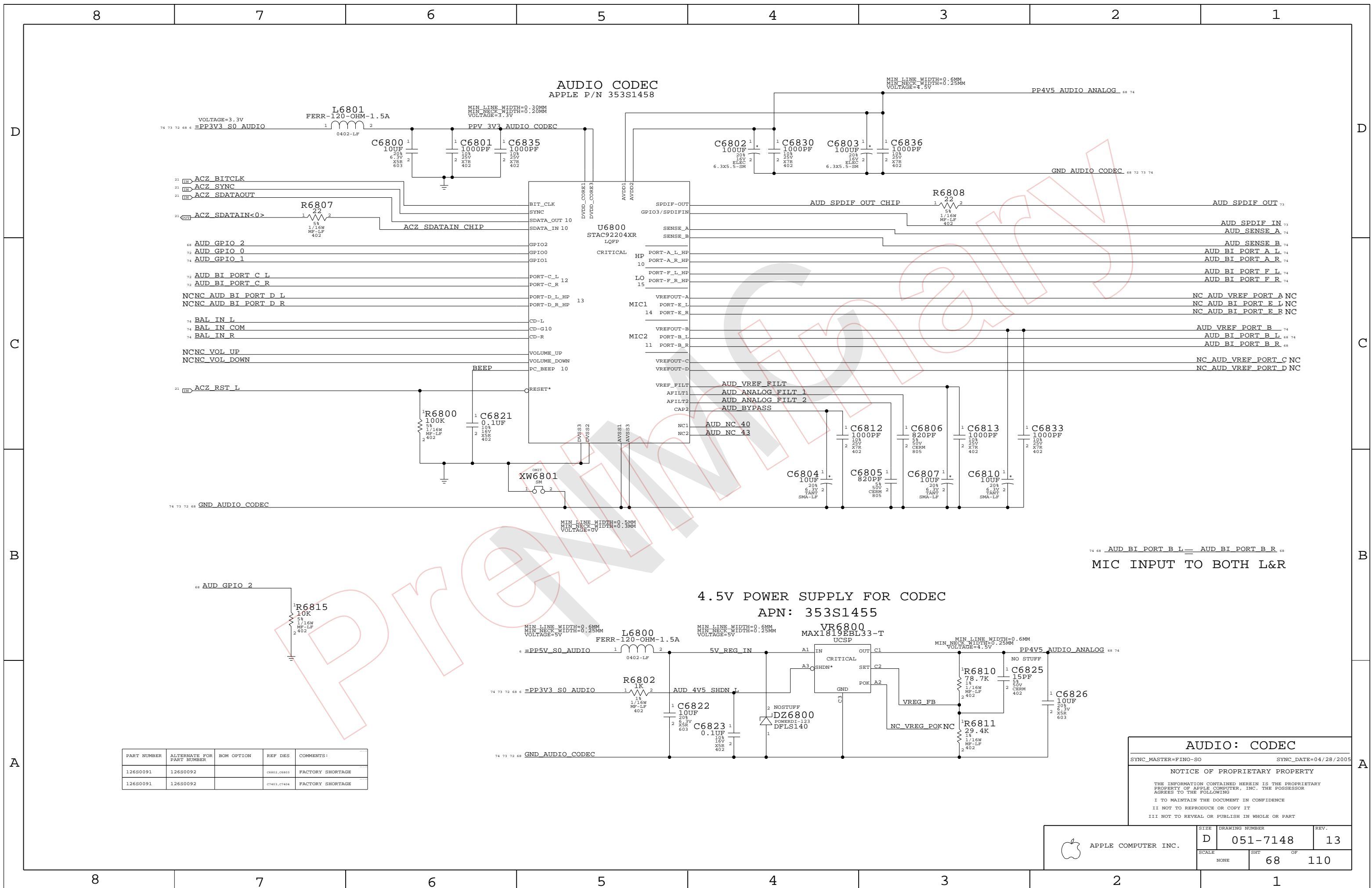
LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	67 OF	110
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C6802, C6803	FACTORY SHORTAGE
126S0091	126S0092		C7403, C7404	FACTORY SHORTAGE

AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

NOTICE OF PROPRIETARY PROPERTY

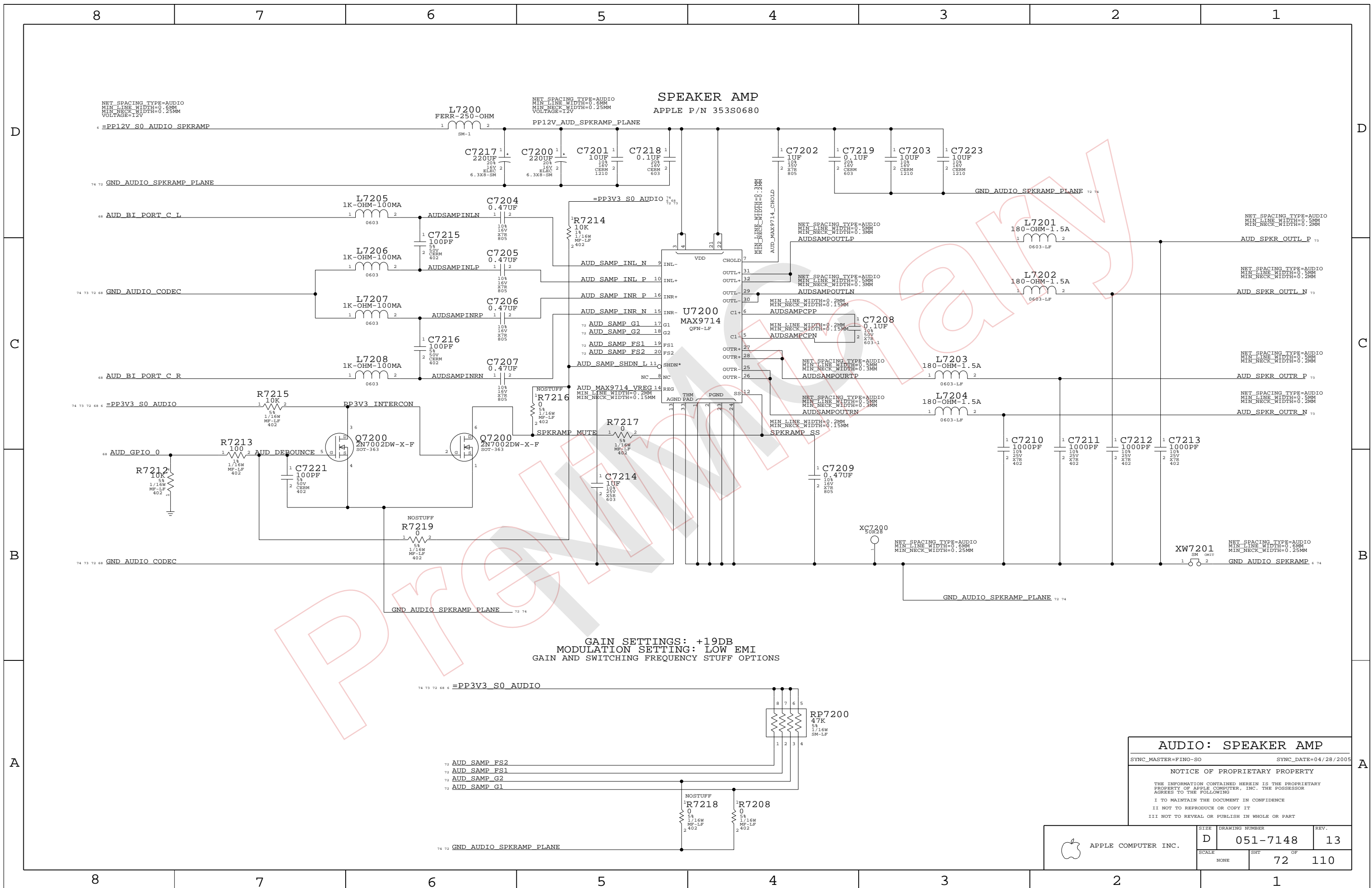
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT OF	68 110

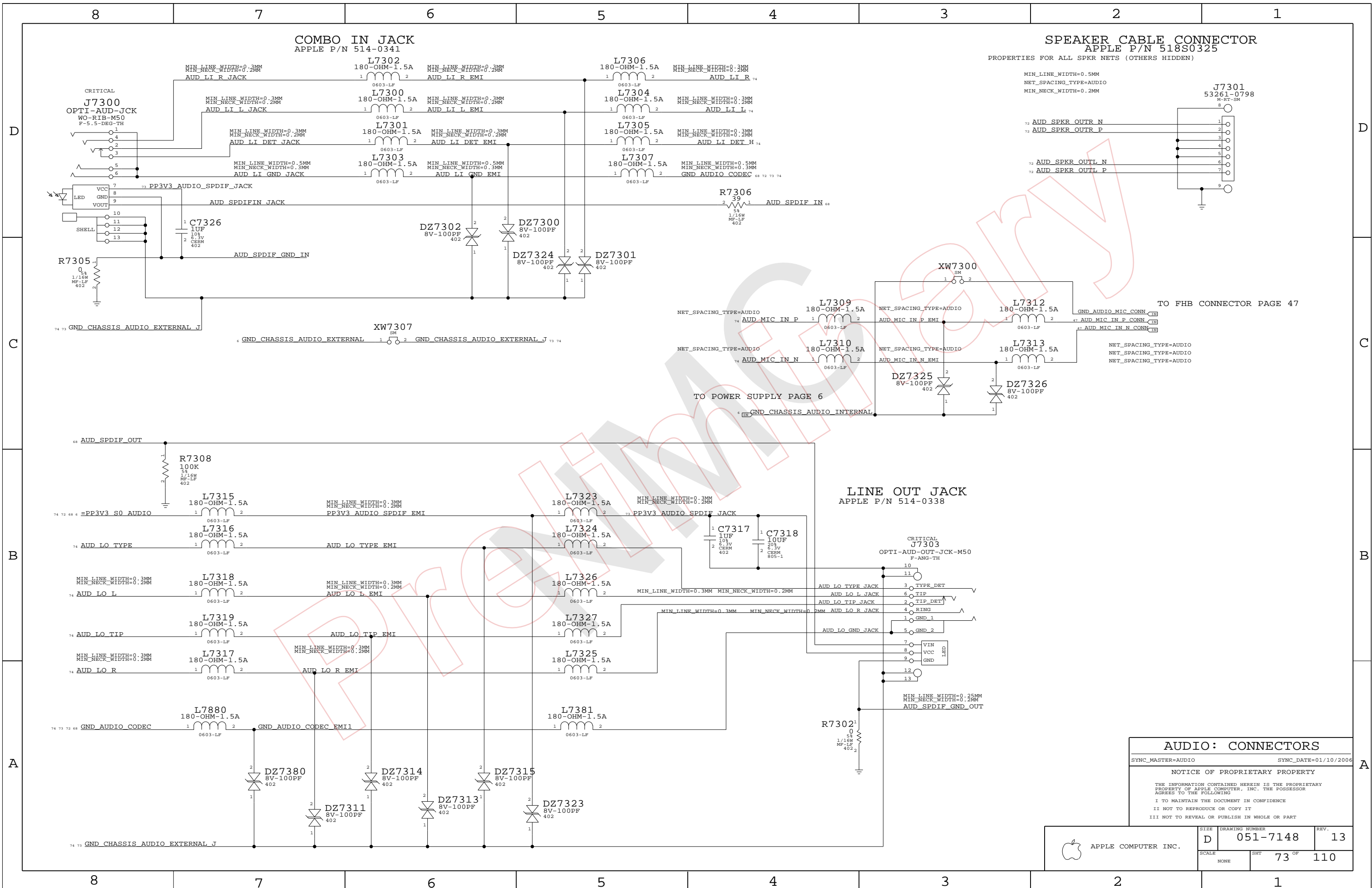


SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

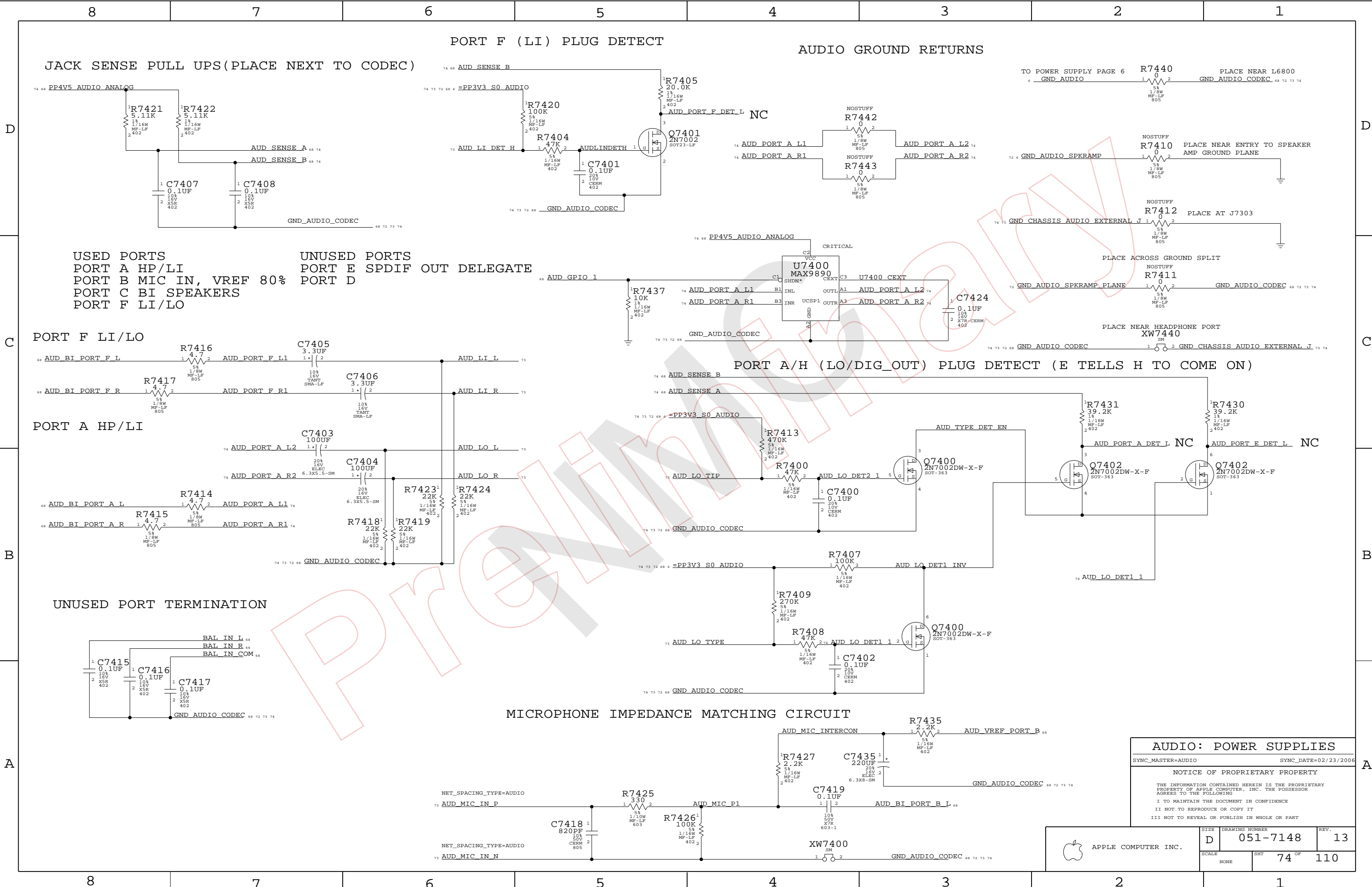
AUDIO: SPEAKER AMP
SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	NONE	SHT	OF
		72	110

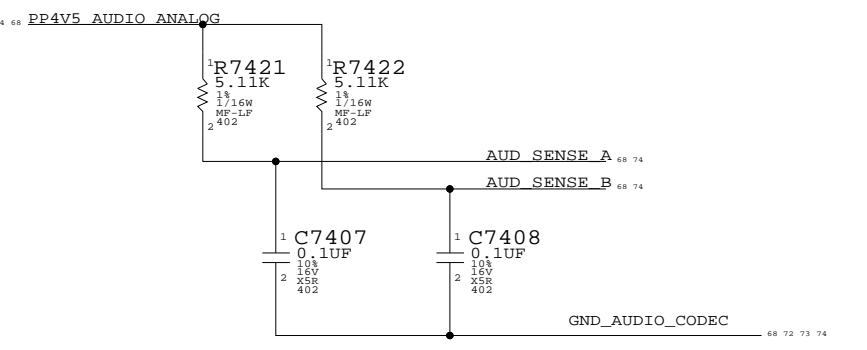


AUDIO: CONNECTORS
 SYNC_MASTER=AUDIO SYNC_DATE=01/10/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	73 OF	110
NONE			



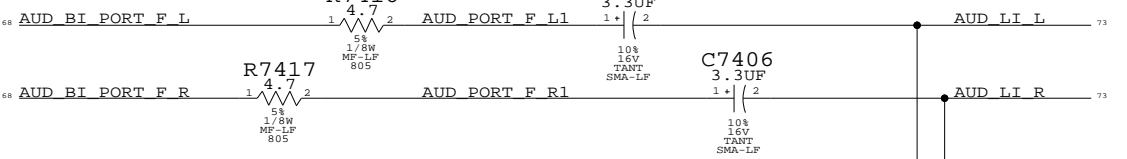
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



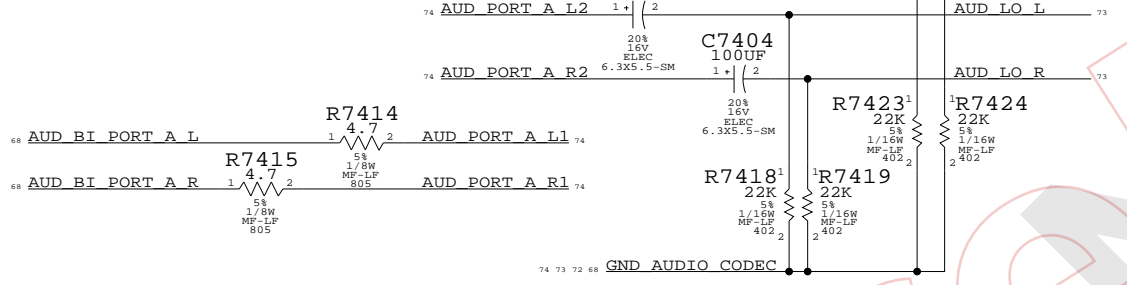
USED PORTS
 PORT A HP/LI
 PORT B MIC IN, VREF 80%
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E SPDIF OUT DELEGATE
 PORT D

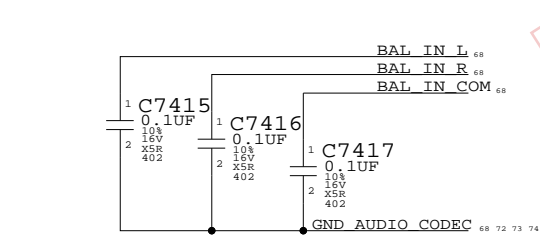
PORT F LI/LO



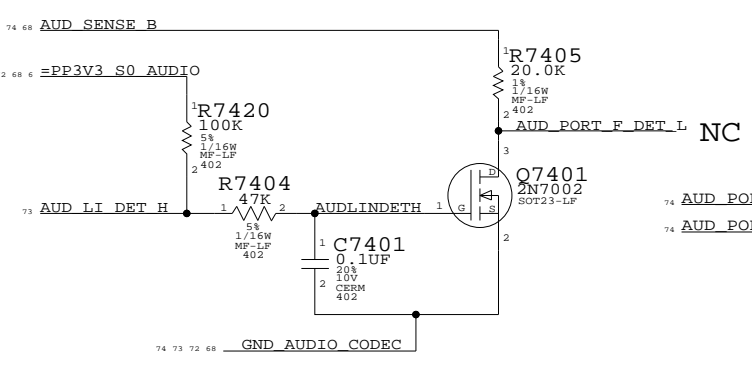
PORT A HP/LI



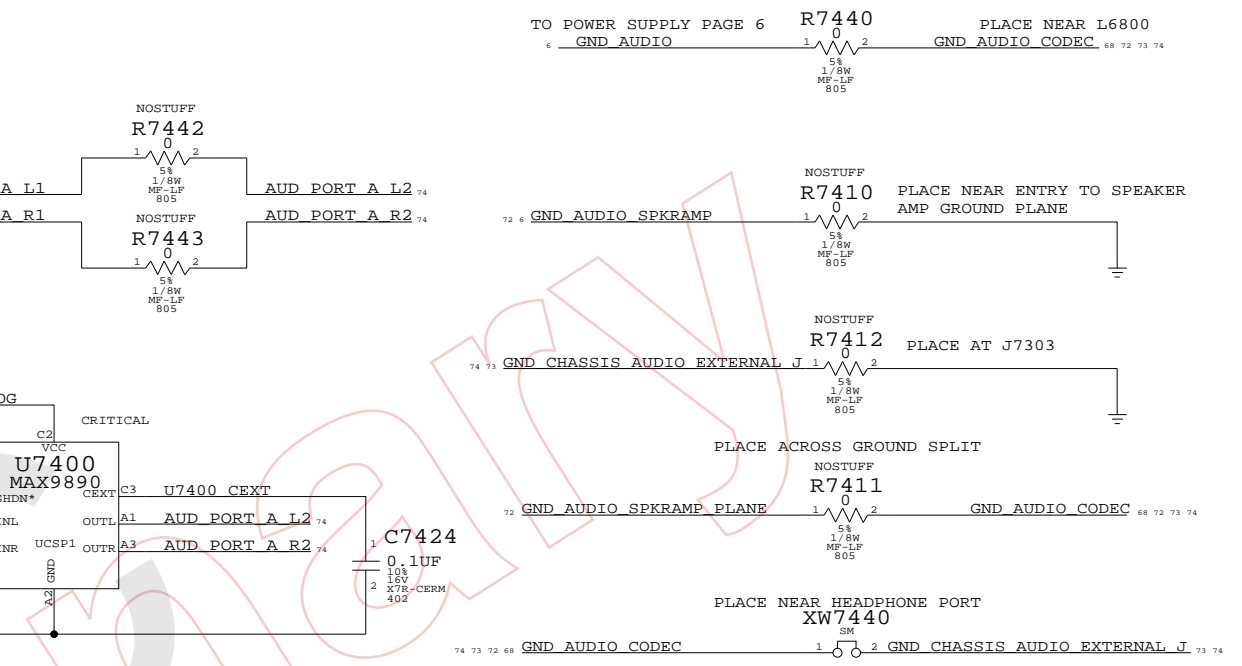
UNUSED PORT TERMINATION



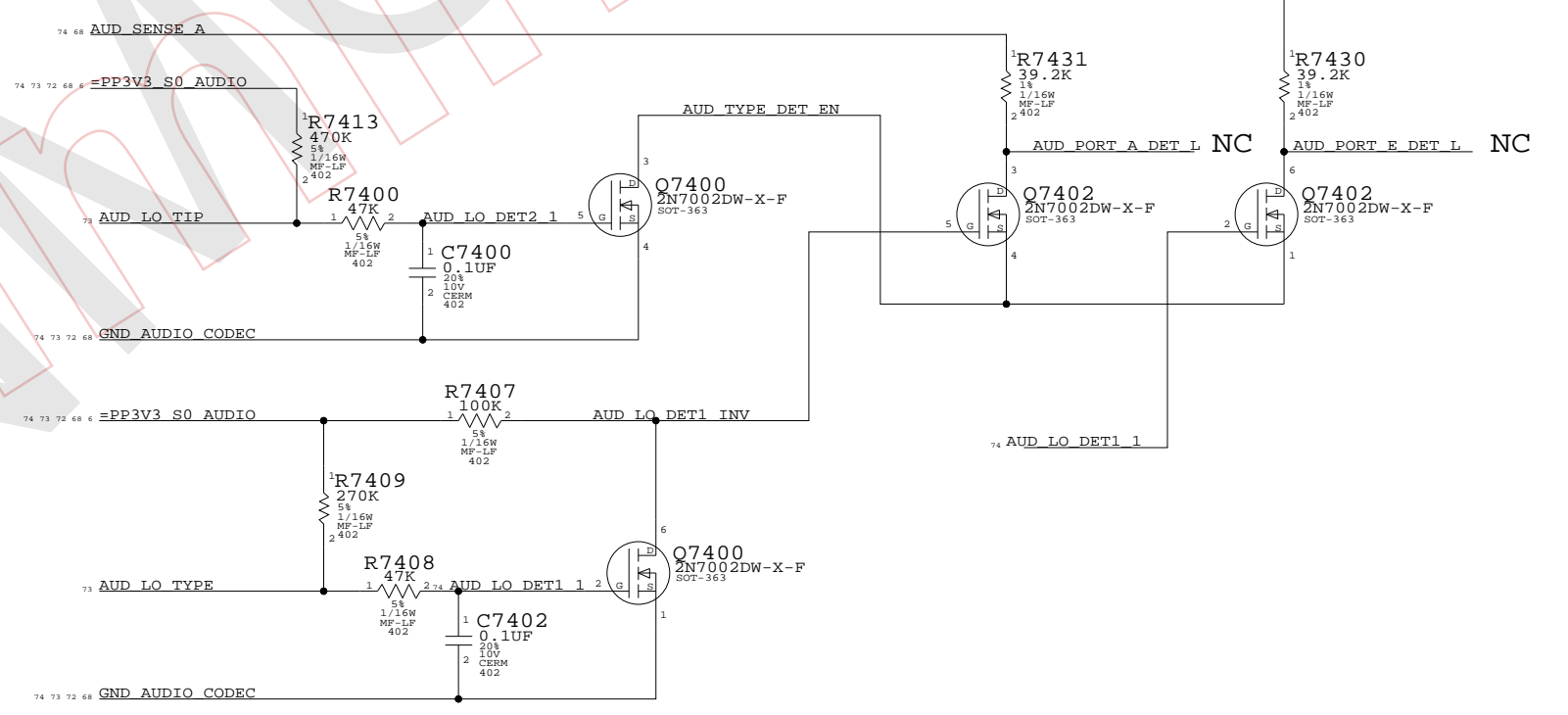
PORT F (LI) PLUG DETECT



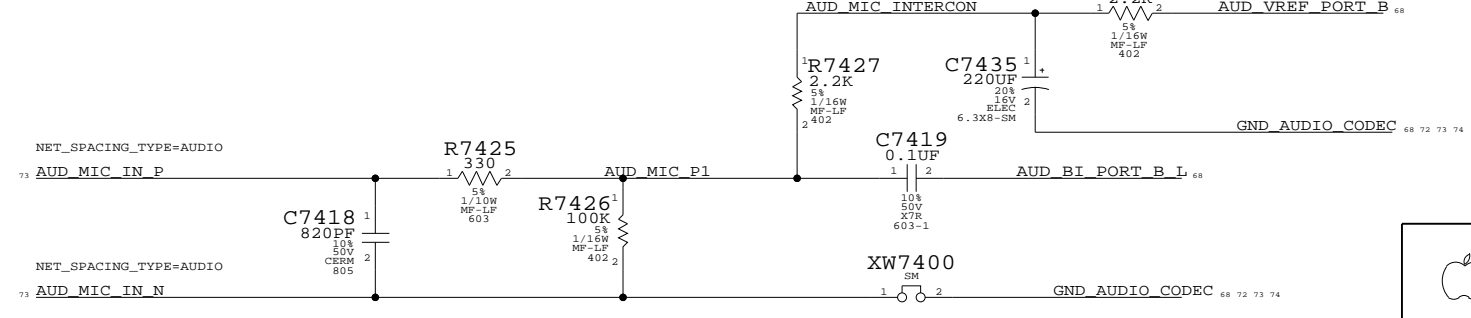
AUDIO GROUND RETURNS



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

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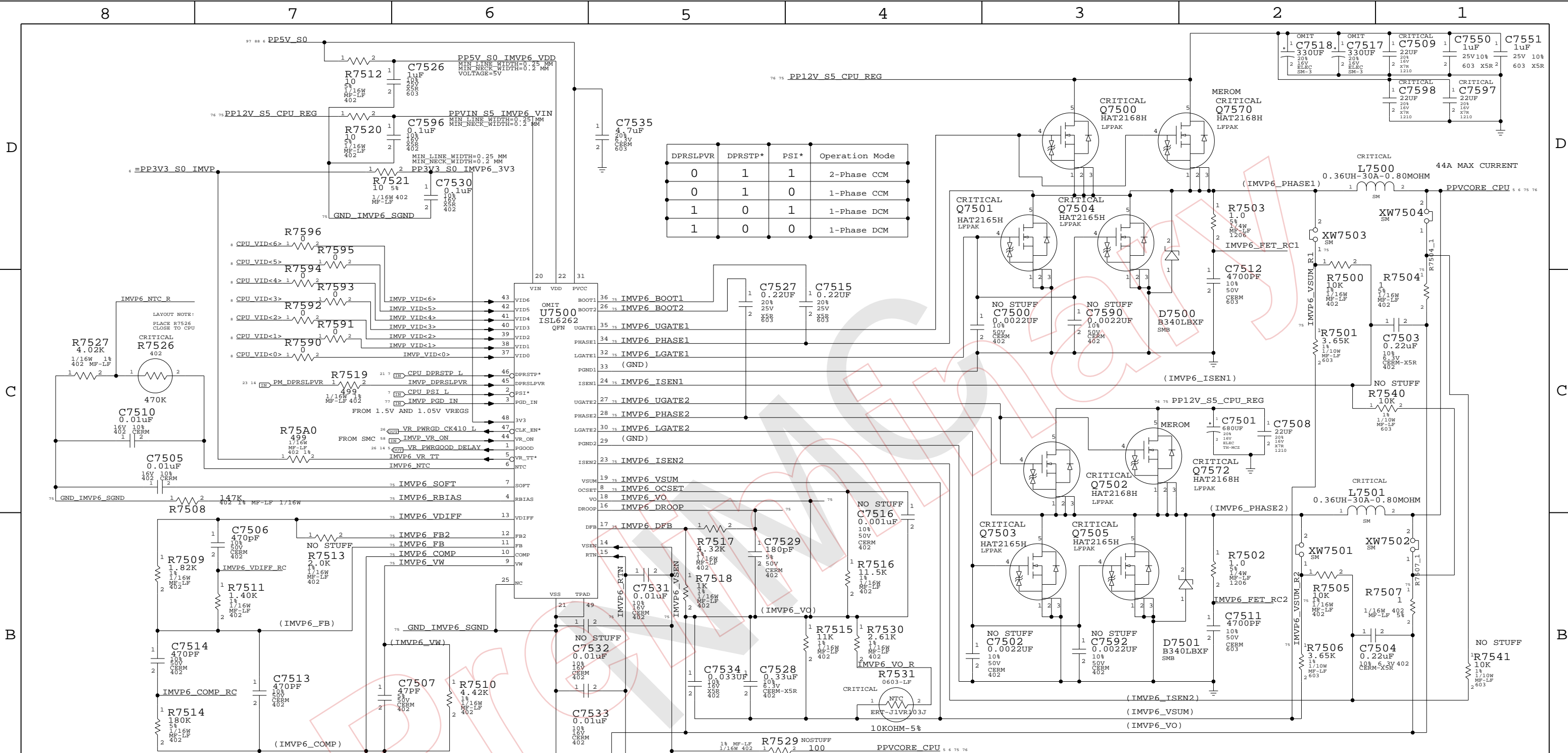
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	74 OF	110
NONE			

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

U7500	ISL6262	QFN
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
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73	73	73
74	74	74
75	75	75
76	76	76
77	77	77
78	78	78
79	79	79
80	80	80



Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

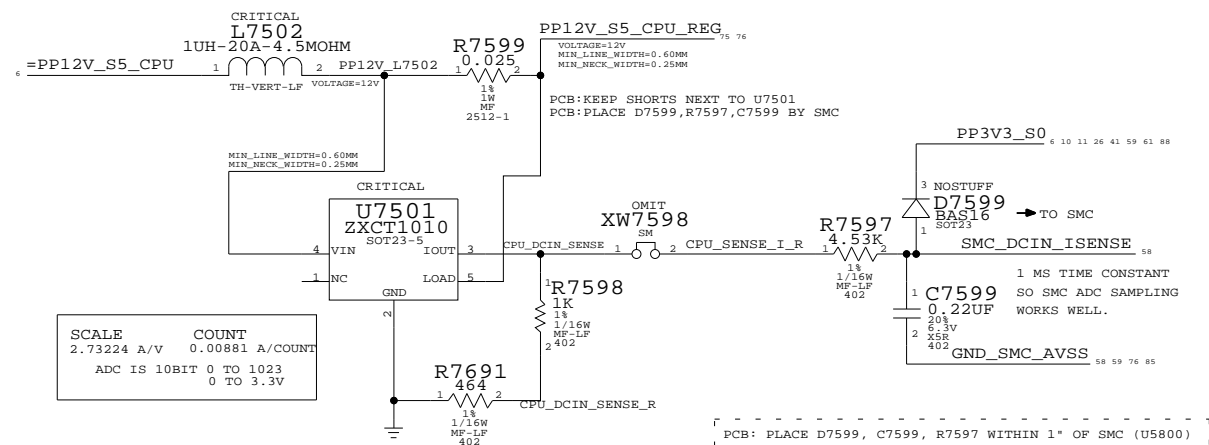
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_RBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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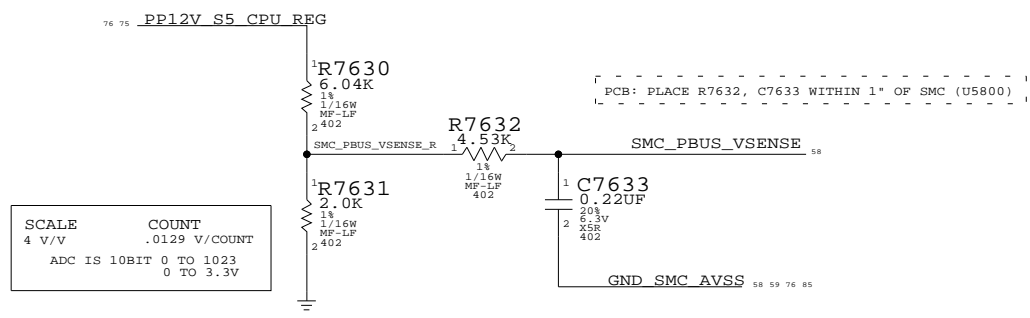
	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SIT	OF	110
NONE	75		

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



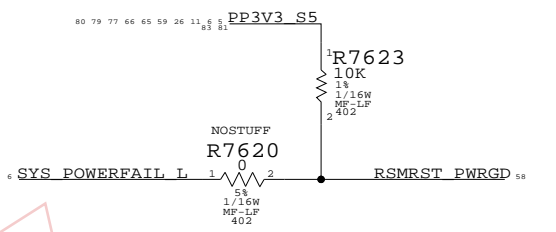
SCALE COUNT
2.73224 A/V 0.00881 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

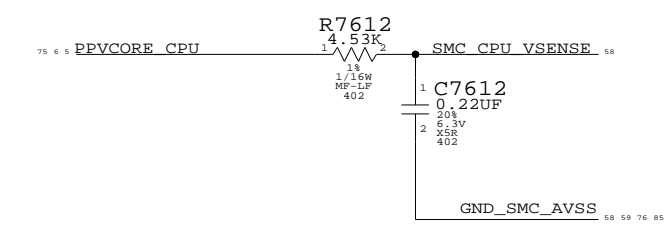


SCALE COUNT
4 V/V .0129 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

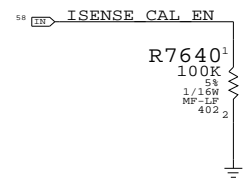
SMC PWRGD PULLUP



PROCESSOR VCORE SENSE

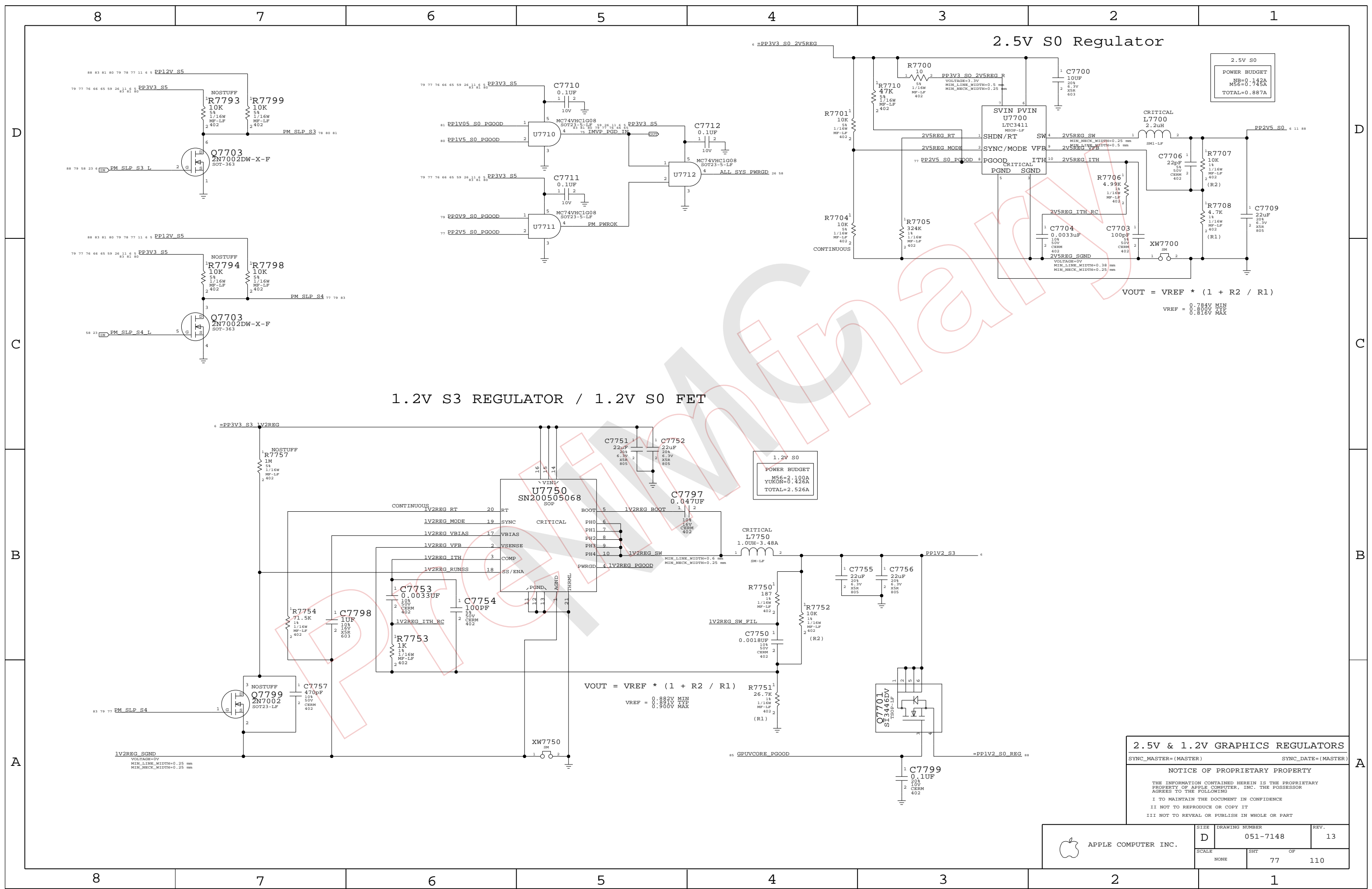


Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7148	13
SCALE	SHT	76 OF	110
NONE			



2.5V S0 Regulator

2.5V S0
POWER BUDGET
NB=0.142A
MS=0.745A
TOTAL=0.887A

$$V_{OUT} = V_{REF} * (1 + R2 / R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1.2V S3 REGULATOR / 1.2V S0 FET

1.2V S0
POWER BUDGET
MS=2.100A
YUKON=0.426A
TOTAL=2.526A

$$V_{OUT} = V_{REF} * (1 + R2 / R1)$$

VREF = 0.882V MIN
0.881V TYP
0.900V MAX

2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

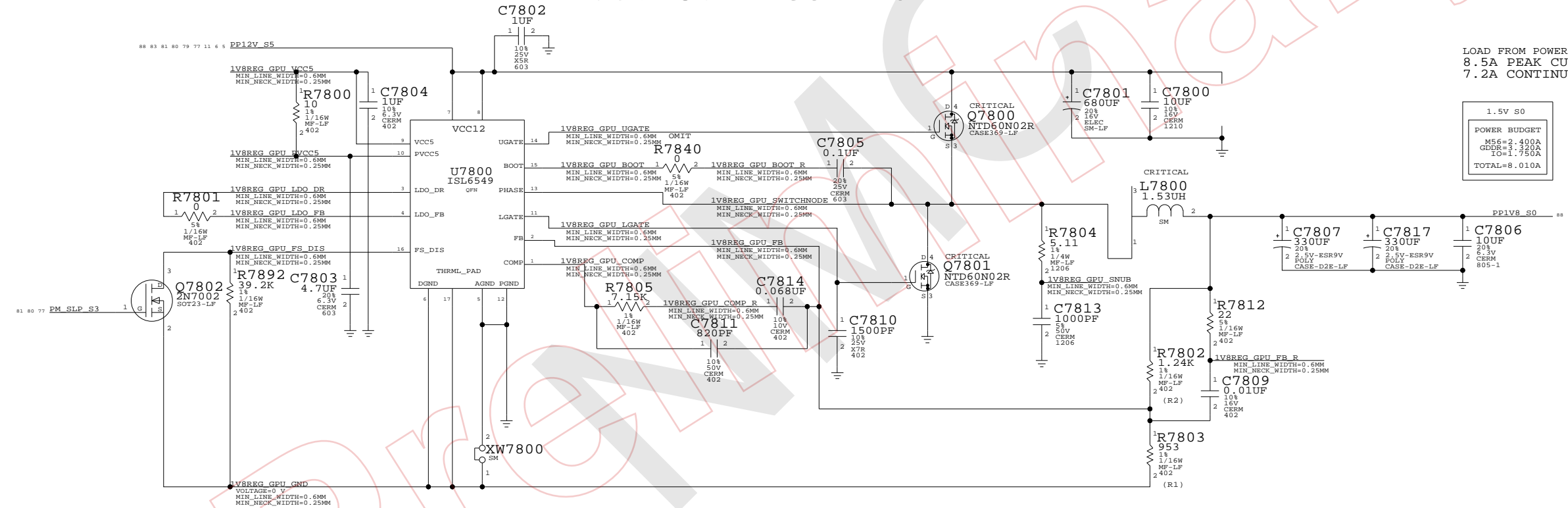
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	D	051-7148	13
SCALE	SHT	OF	
NONE	77	110	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480514	1	5.11 OHM 0402 1% 1/16W LF	R7840		

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0	
POWER BUDGET	
M56=2.400A	
GDDR=3.300A	
IO=1.750A	
TOTAL=8.010A	

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
VREF = 0.800V TYP
VREF = 0.816V MAX

1.8V GDDR REGULATOR

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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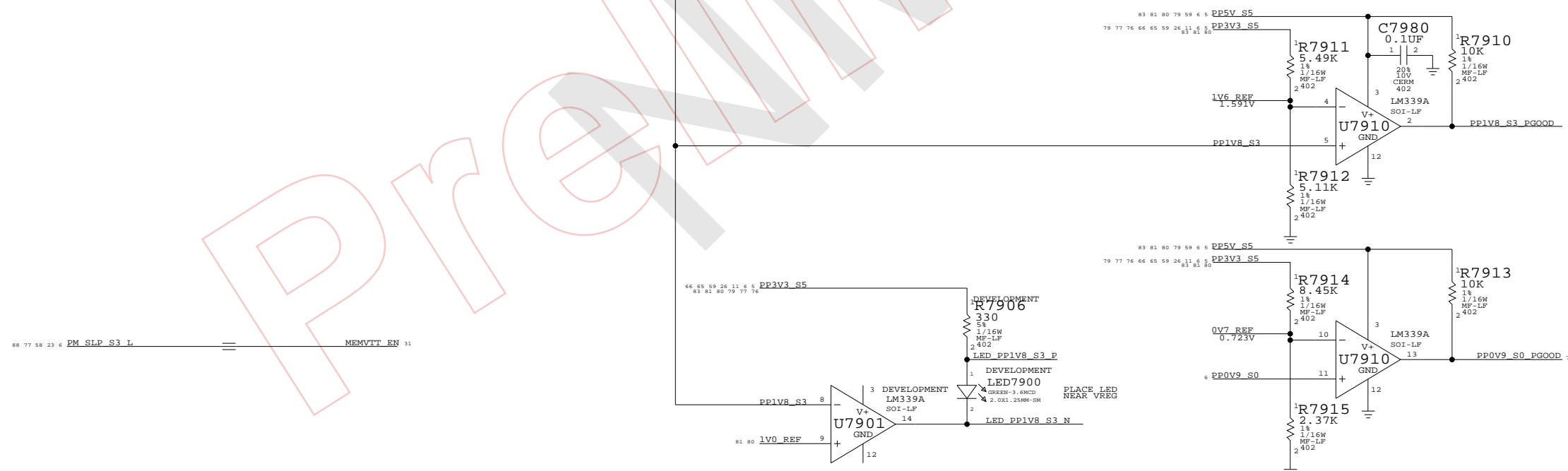
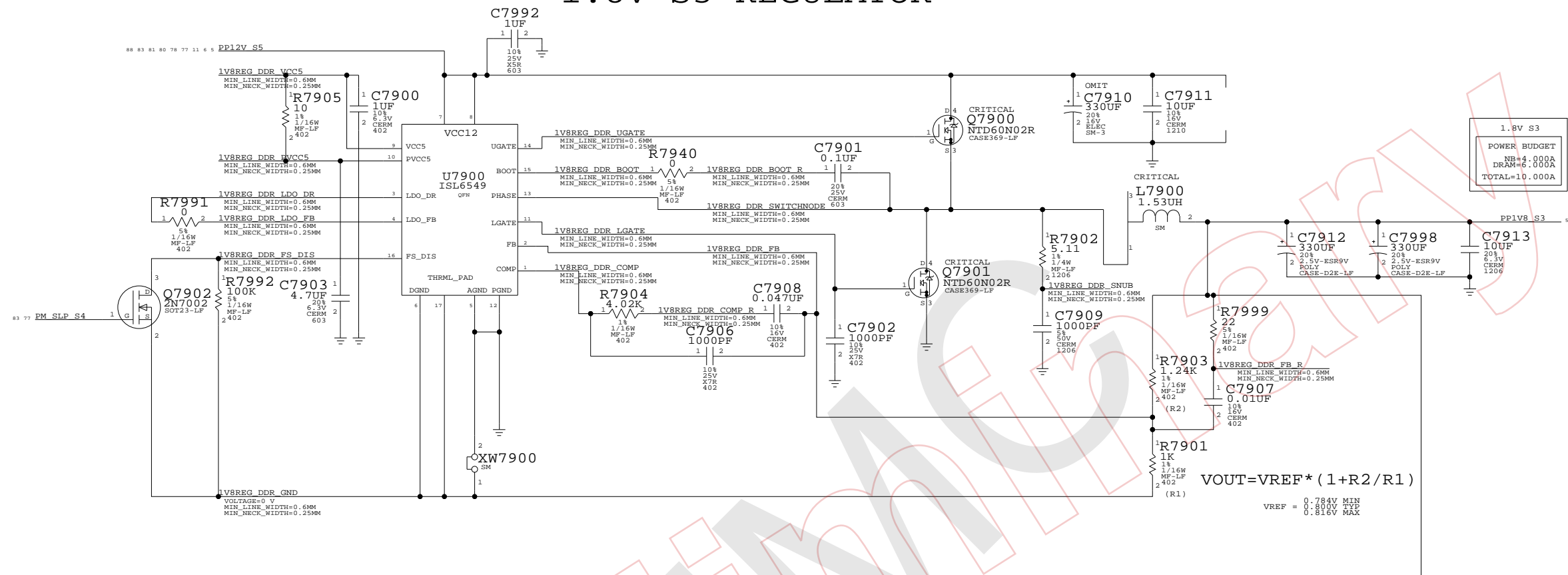
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	78 OF 110	
NONE			

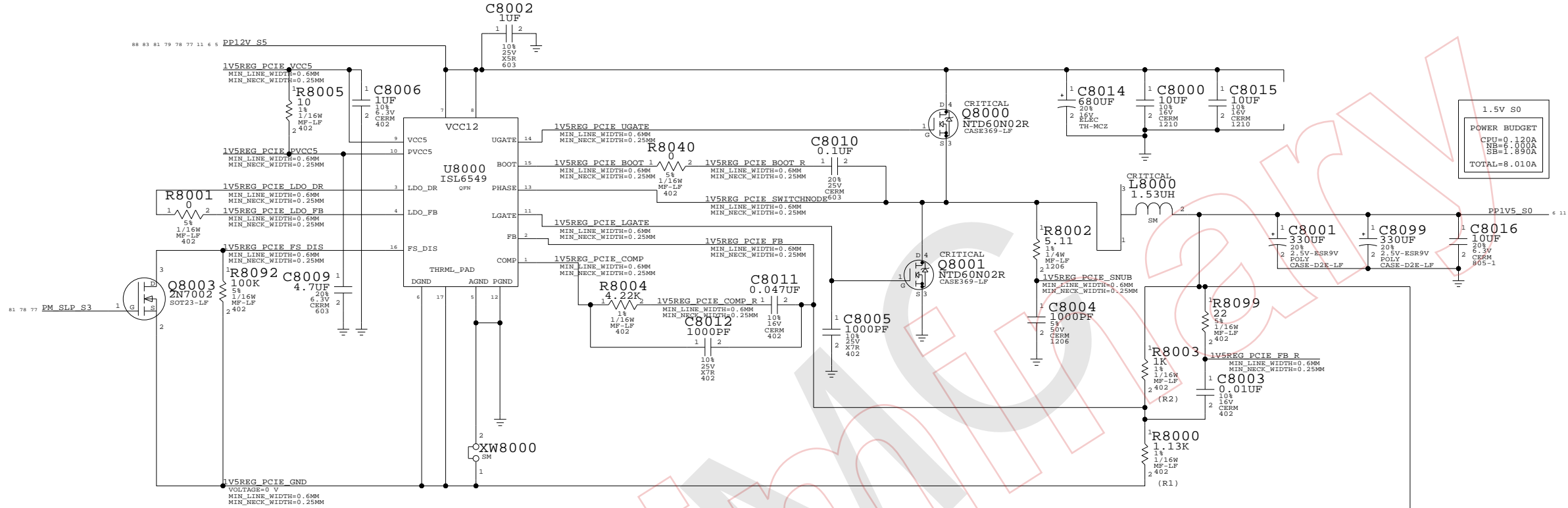
1.8V S3 REGULATOR



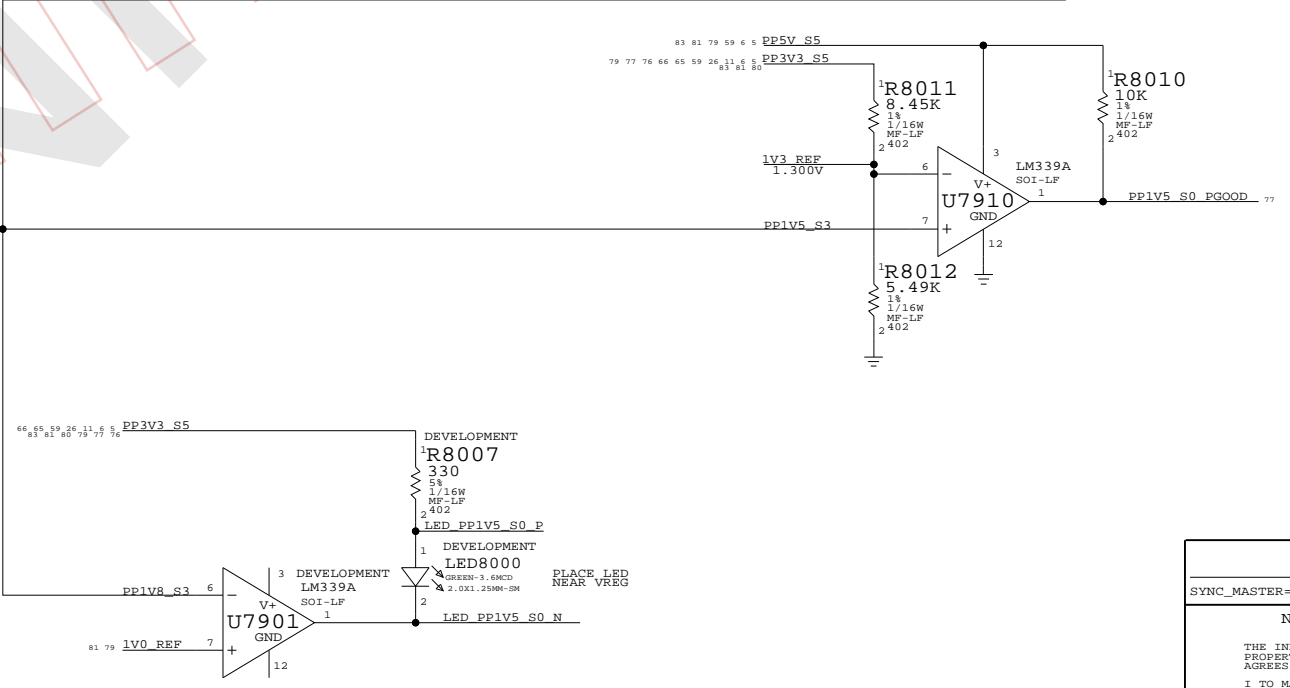
1.8V Vreg
 SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005
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	D	051-7148	13
SCALE	SHT	79 OF	110
NONE			

1.5V S0 REGULATOR



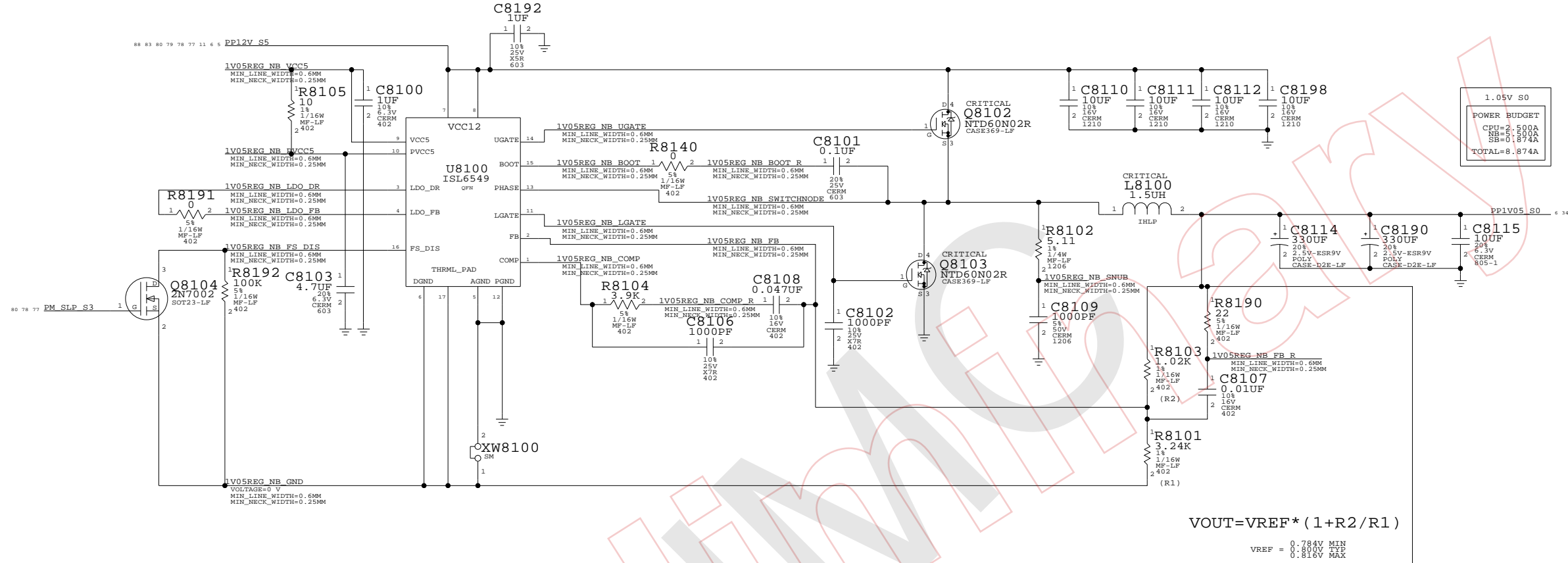
$V_{OUT} = V_{REF} * (1 + R2/R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$



1.5V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005
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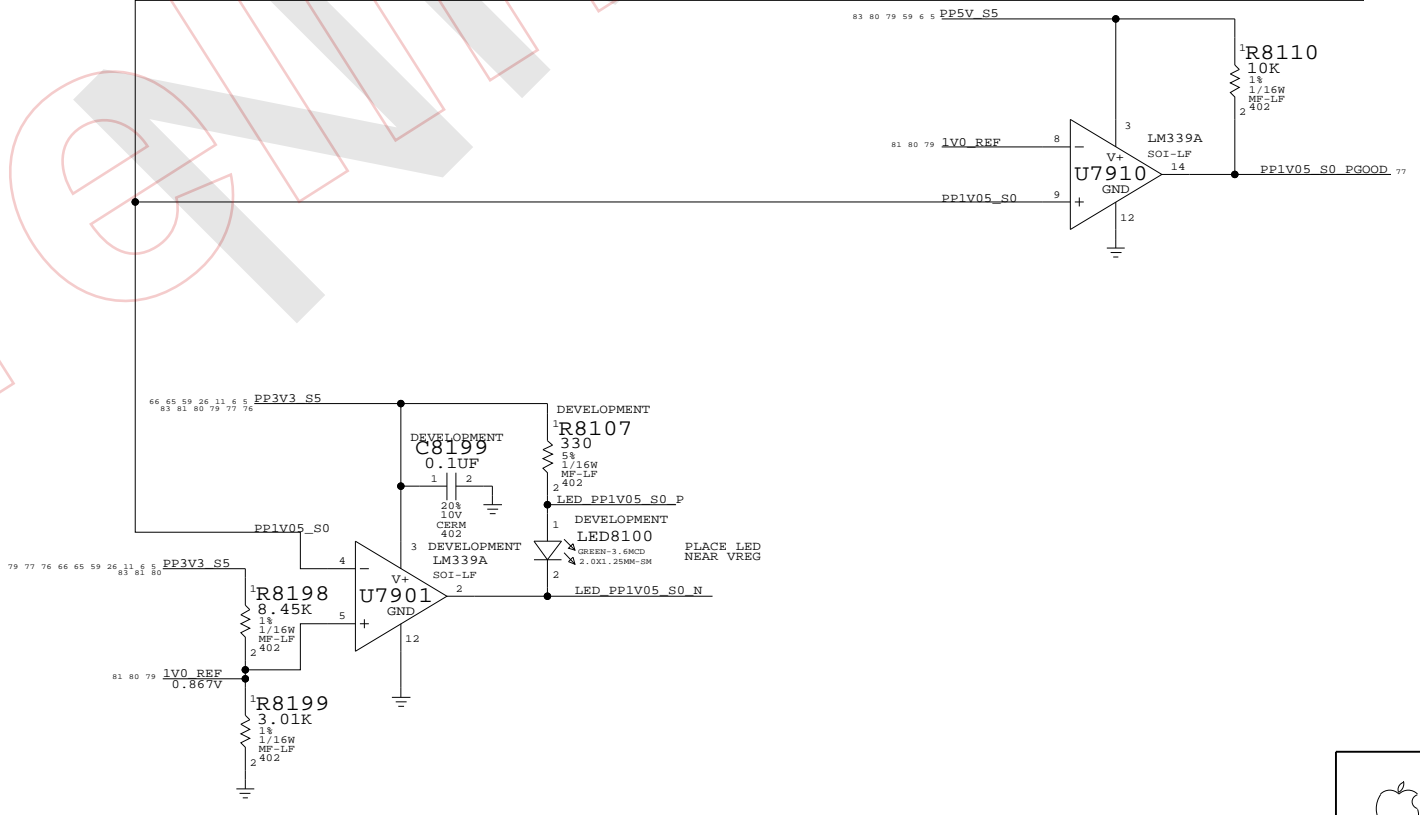
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	80 OF	110
NONE			

1.05V S0 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$



1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

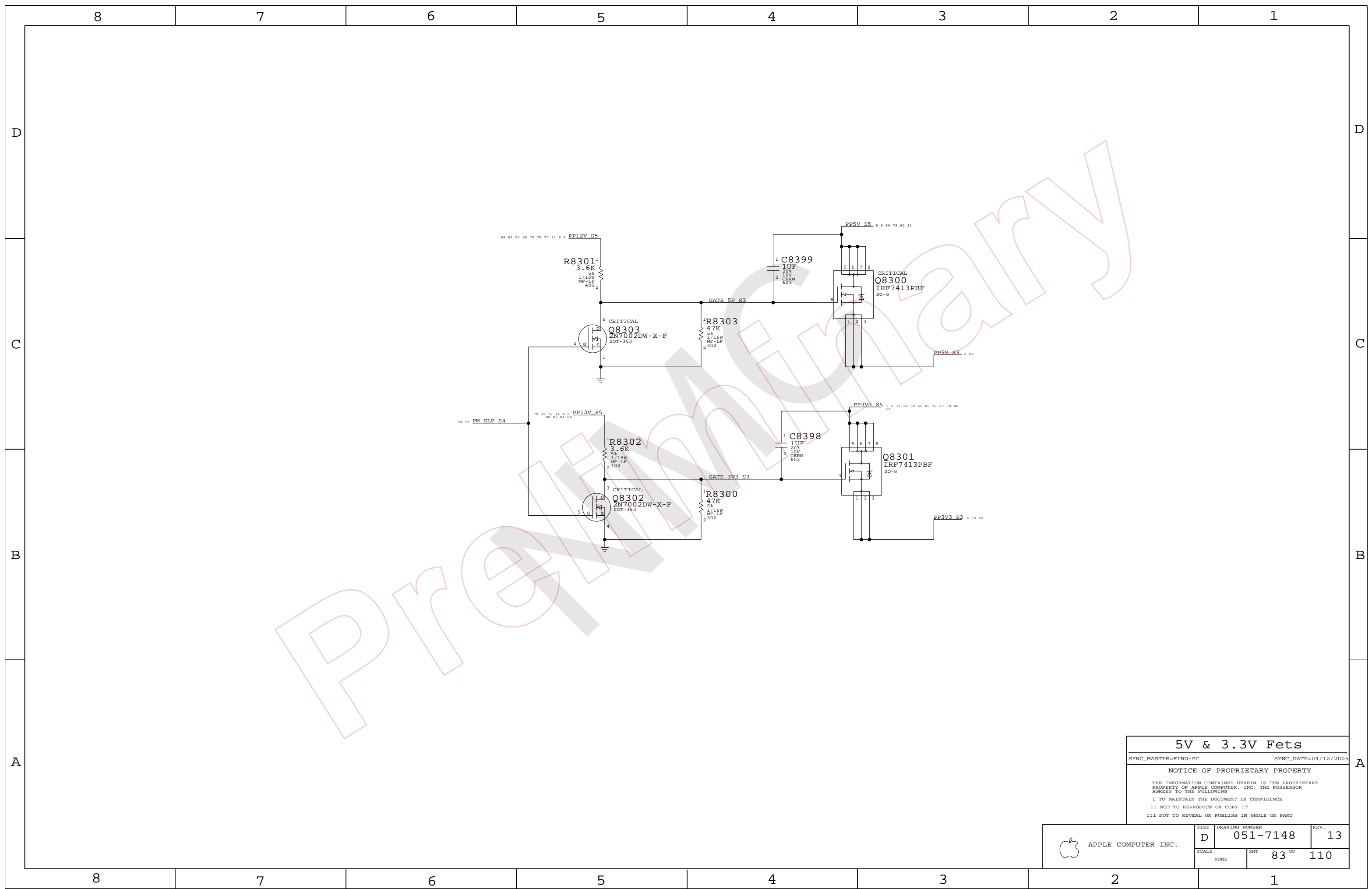
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	D	051-7148	13
SCALE	SHT	81 OF	110
NONE			




Proprietary

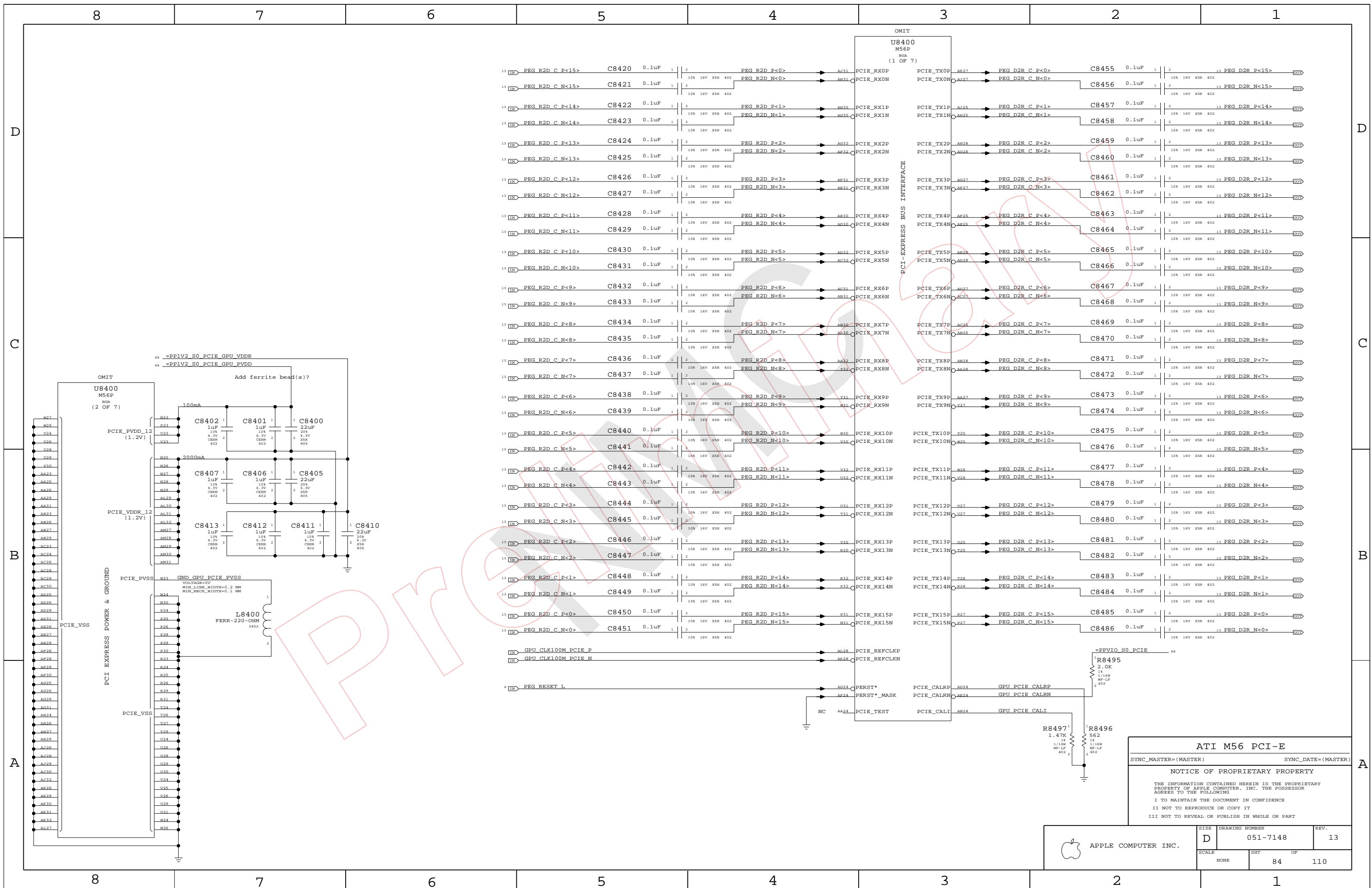
5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	83 OF 110	
NONE			



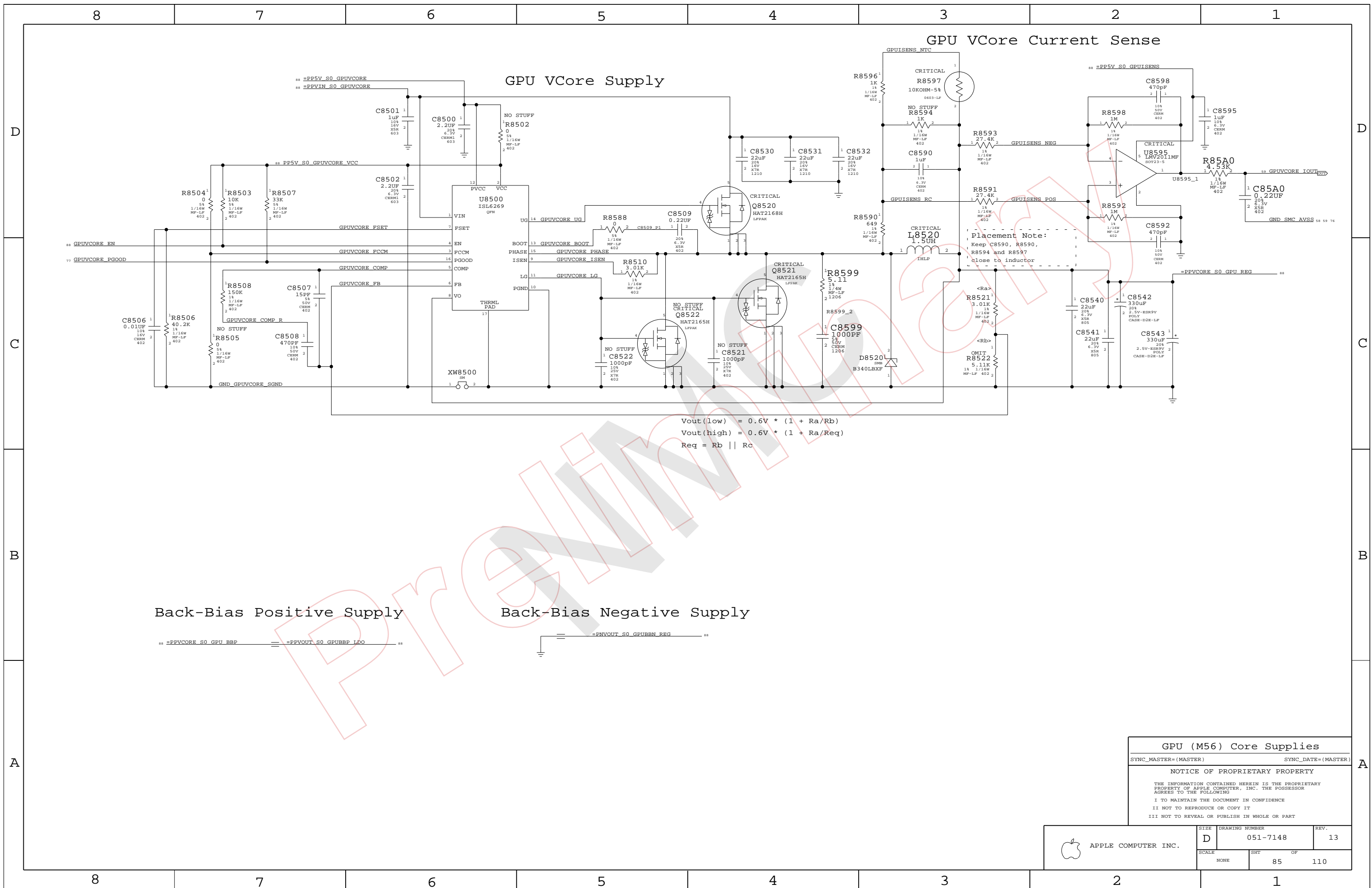
ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 84	OF 110



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

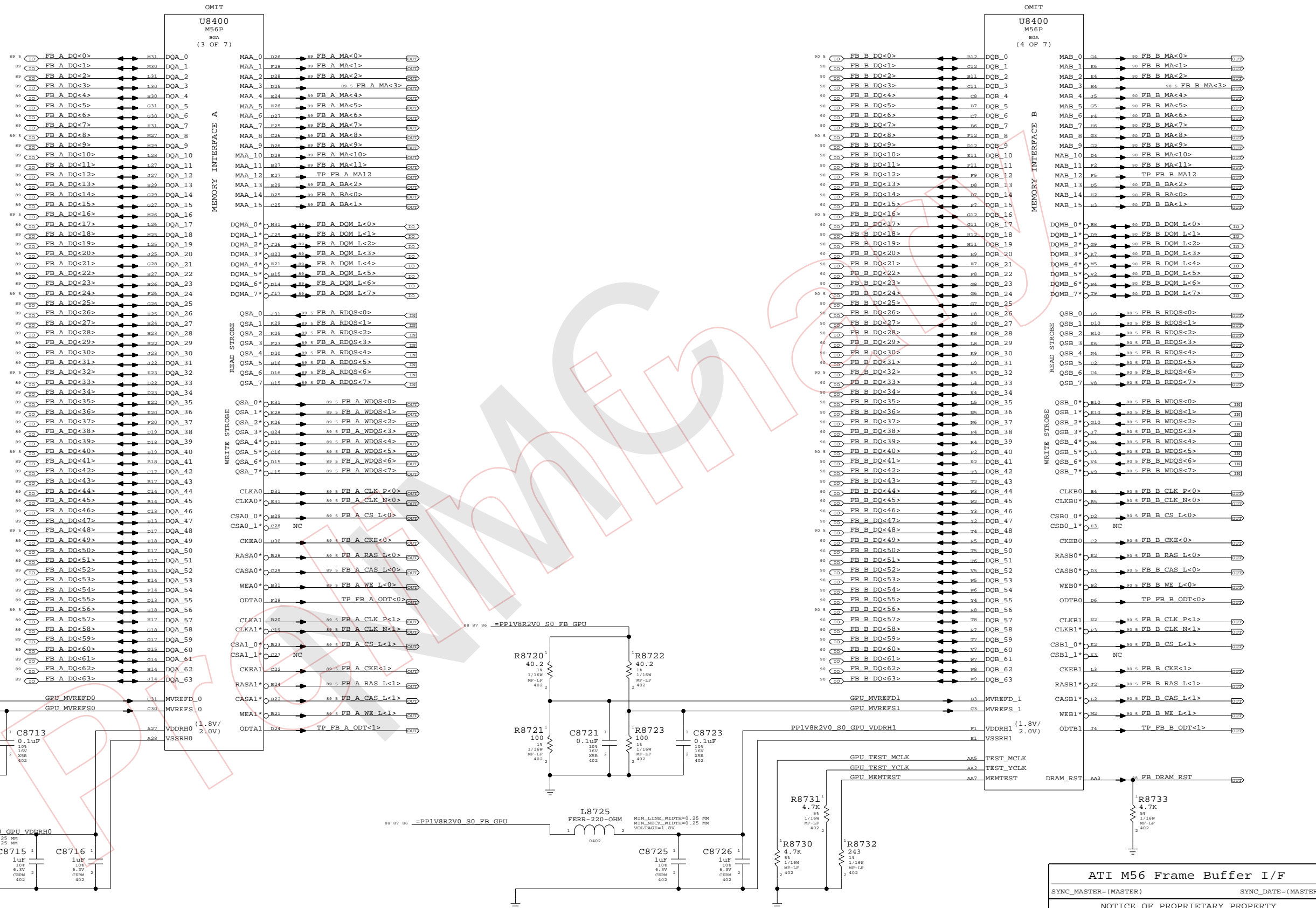
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7148	REV. 13
	SCALE NONE	SHEET 85	OF 110

Page Notes

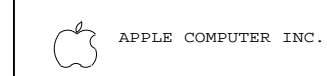
Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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Table with columns: SIZE (D), DRAWING NUMBER (051-7148), REV. (13), SCALE (NONE), SHEET (87 OF 110).



8

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"S0" GPU RAILS

ONLY ON IN RUN

59 EP1V0R1V2_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

85 PP5V_S0_GPUVCORE_VCC
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

PP1V2_GPU_IO_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

PPBB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

PNBB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.2MM
 VOLTAGE=0

76 61 59 41 26 11 10 6 PP3V3_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=3.3V

77 11 6 PP2V5_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=2.5V

PP1V8R2V0_S0_FB_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.8V

83 81 80 79 78 77 11 6 5 PP12V_S5
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=12V

6 PP12V_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=12V

97 76 6 PP5V_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

85 GPUVCORE_EN
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

97 FB_DRAM_RST
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

M56 GPIOs

94 91 GPU_GPIO_0
 GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
 GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
 GPIO 2 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_3
 GPIO 3 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_4
 GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
 GPIO 5 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_6
 GPIO 6 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

TP_GPU_GPIO_7
 MAKE_BASE=TRUE

91 GPU_GPIO_8
 GPIO 8 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

NC_GPU_GPIO_10
 MAKE_BASE=TRUE

91 GPU_GPIO_9
 GPIO 9 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_13
 GPIO 13 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_12
 GPIO 12 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_11
 GPIO 11 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

GPIO 9,13,12,11 = ROM ID CFG
 INTERNAL PULL DOWN
 0010 = 256 M APERATURE SIZE

91 GPU_GPIO_24
 GPIO 24 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_27
 GPIO 27 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_28
 GPIO 28 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_29
 GPIO 29 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

GPU_VCORE_LOW
 MAKE_BASE=TRUE

GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
 EXTERNAL PULL DOWN RECOMMENDED

=PP3V3_S0_GPU_VDDR3 88 91

TP_GPU_GPIO_14
MAKE_BASE=TRUE

TP_GPU_GPIO_17
MAKE_BASE=TRUE

TP_GPU_VGA_R
MAKE_BASE=TRUE

TP_GPU_VGA_G
MAKE_BASE=TRUE

TP_GPU_VGA_B
MAKE_BASE=TRUE

TP_GPU_VGA_HSYNC
MAKE_BASE=TRUE

TP_GPU_VGA_VSYNC
MAKE_BASE=TRUE

TP_GPU_TV_Y
MAKE_BASE=TRUE

TP_GPU_TV_COMP
MAKE_BASE=TRUE

TP_GPU_TV_C
MAKE_BASE=TRUE

TP_GPU_DDC_B_CLK
MAKE_BASE=TRUE

TP_GPU_DDC_B_DATA
MAKE_BASE=TRUE

GPU MISC

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D

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B

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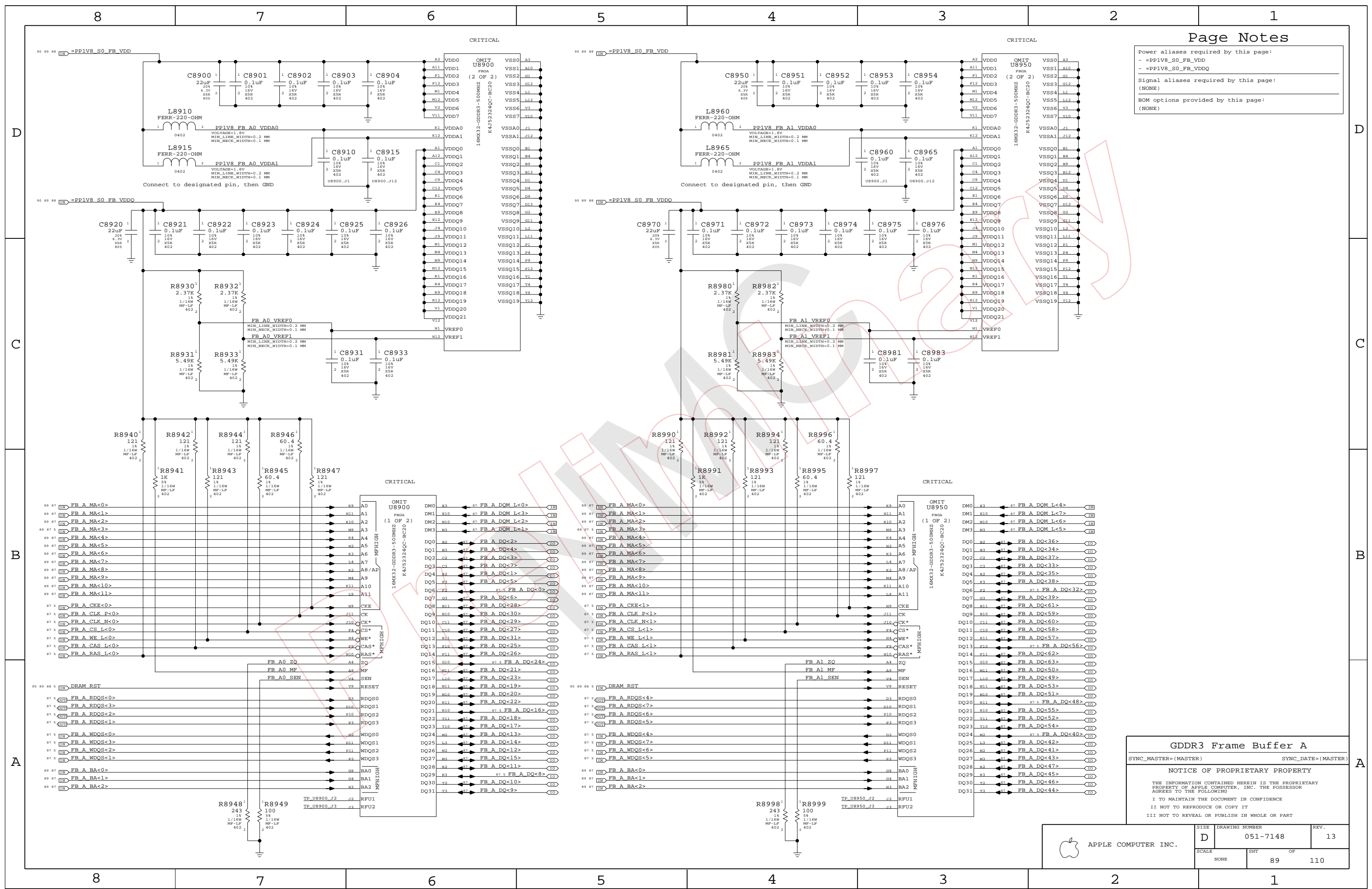
2

1

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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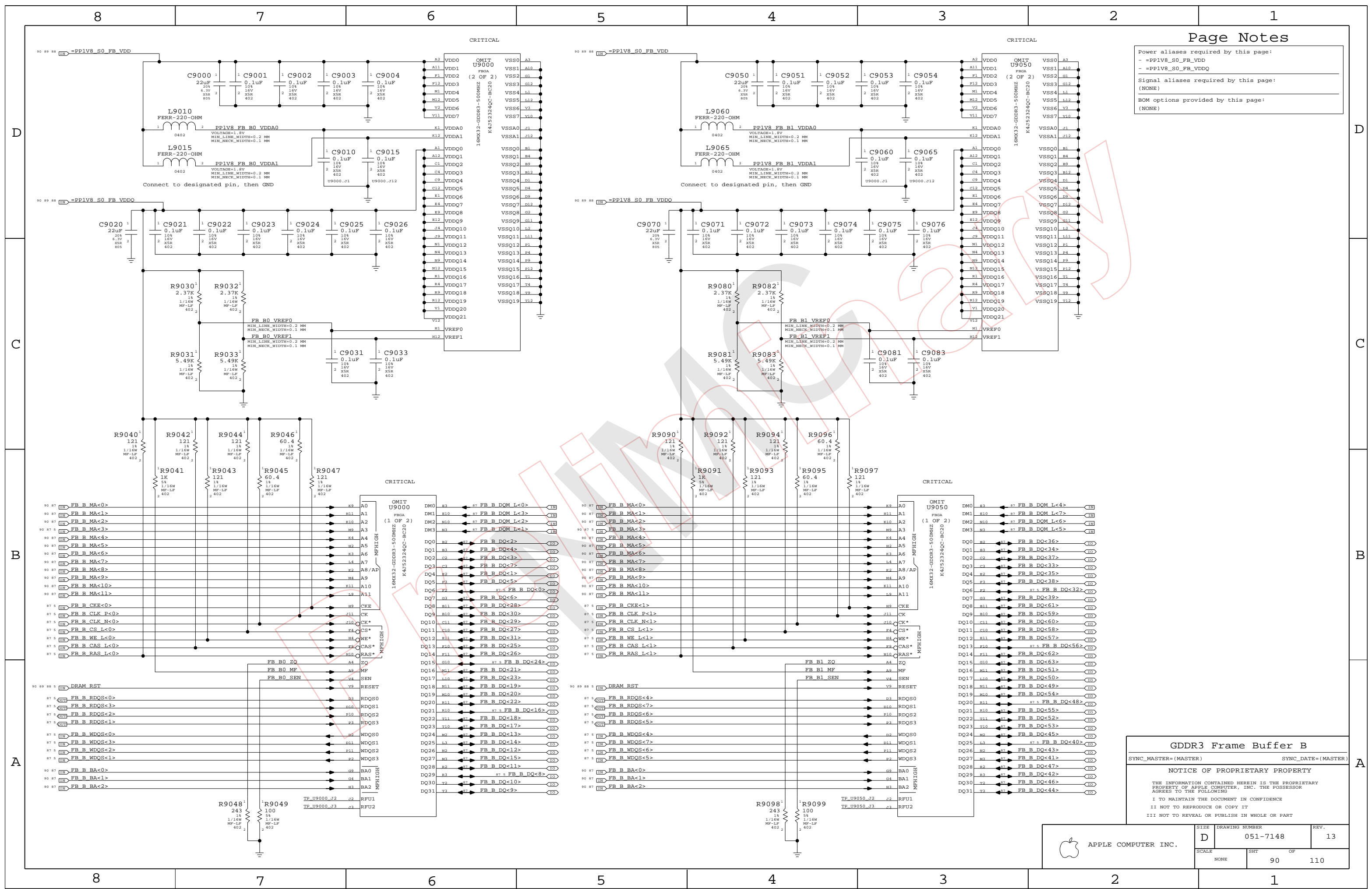
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Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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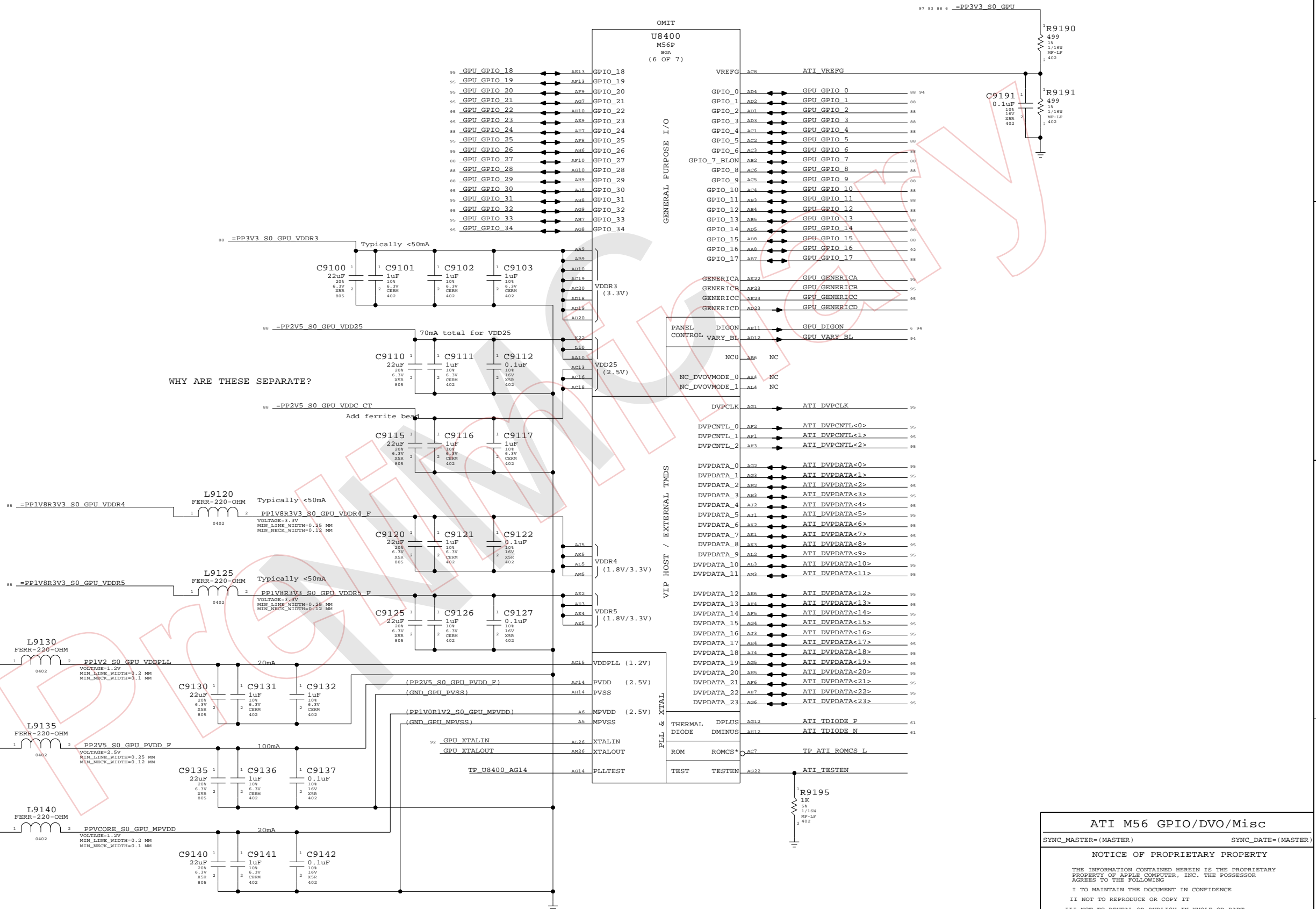
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Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)



WHY ARE THESE SEPARATE?

ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	91	110	

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Page Notes

Power aliases required by this page:

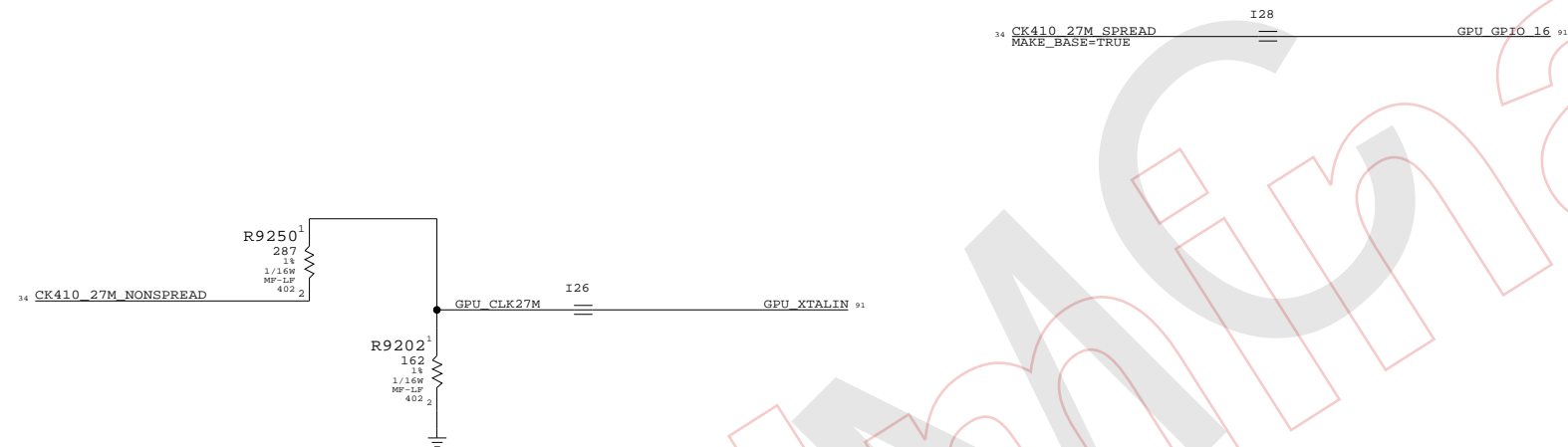
- =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- GPU_SS - GPU_LVDDR_2V8



Preview Only

GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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	D	051-7148	13
SCALE		SHT	OF
NONE		92	110

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Page Notes

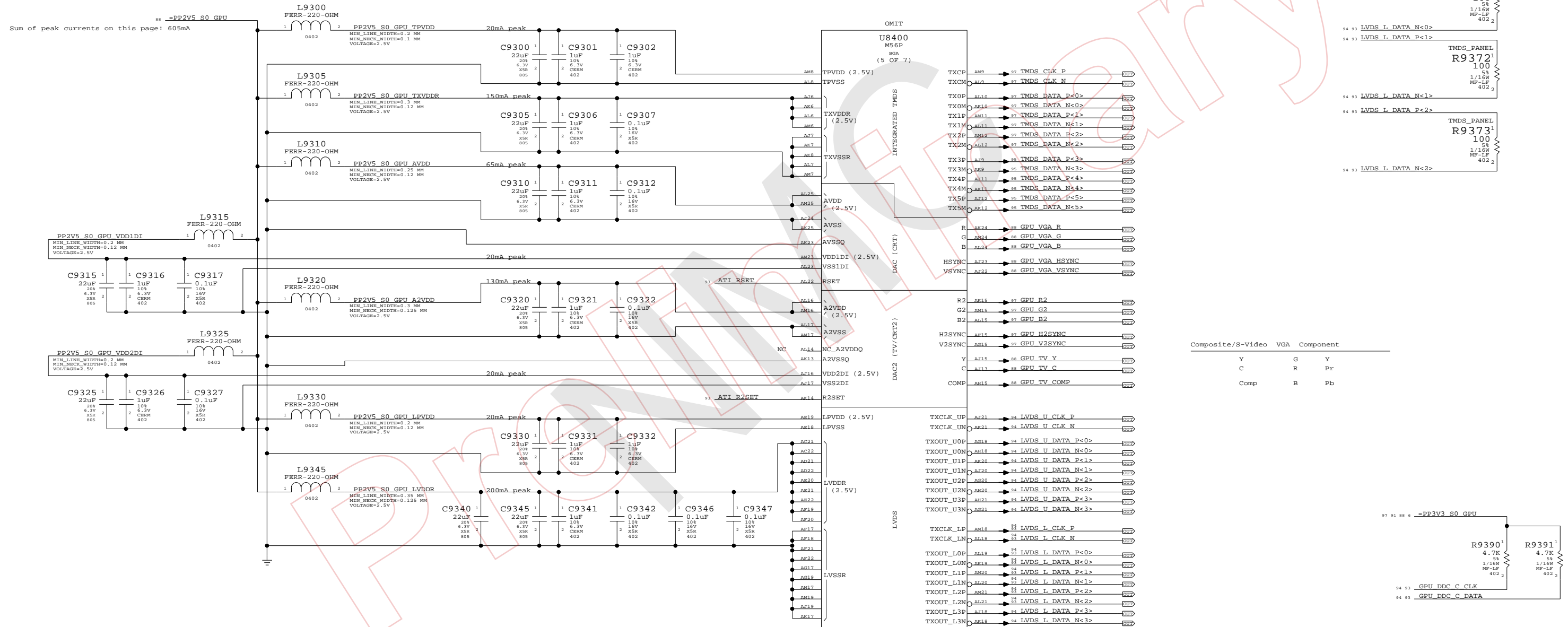
Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
 (NONE)

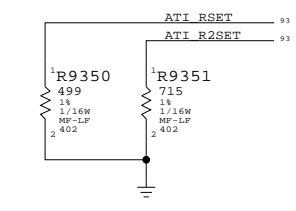
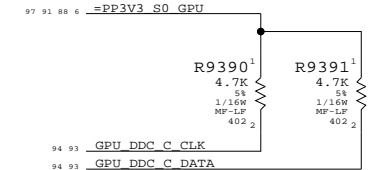
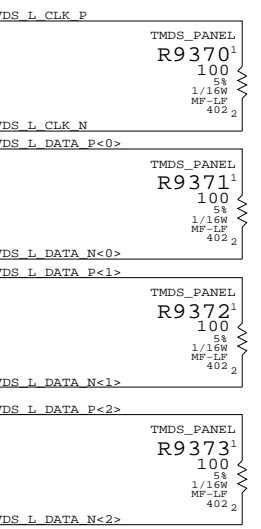
BOM options provided by this page:
 (NONE)

TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)

Sum of peak currents on this page: 605mA



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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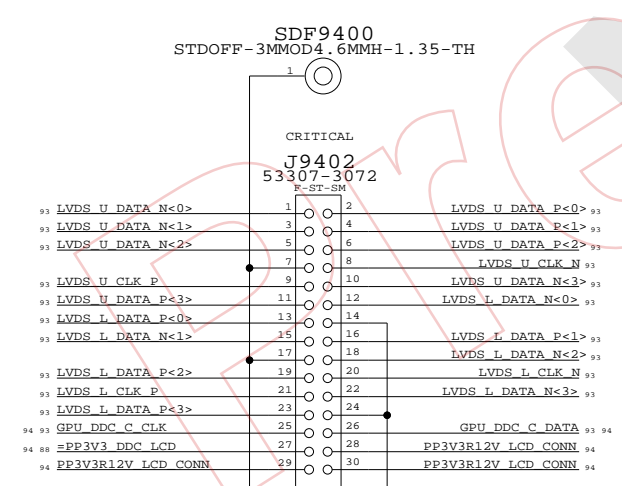
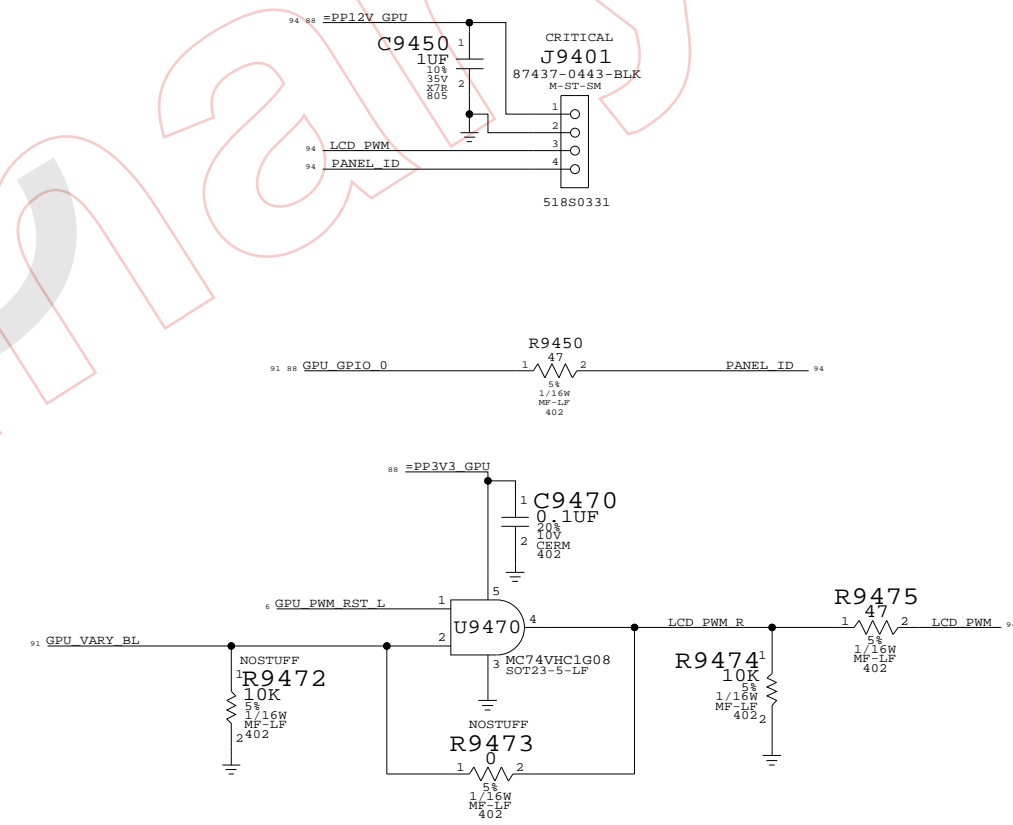
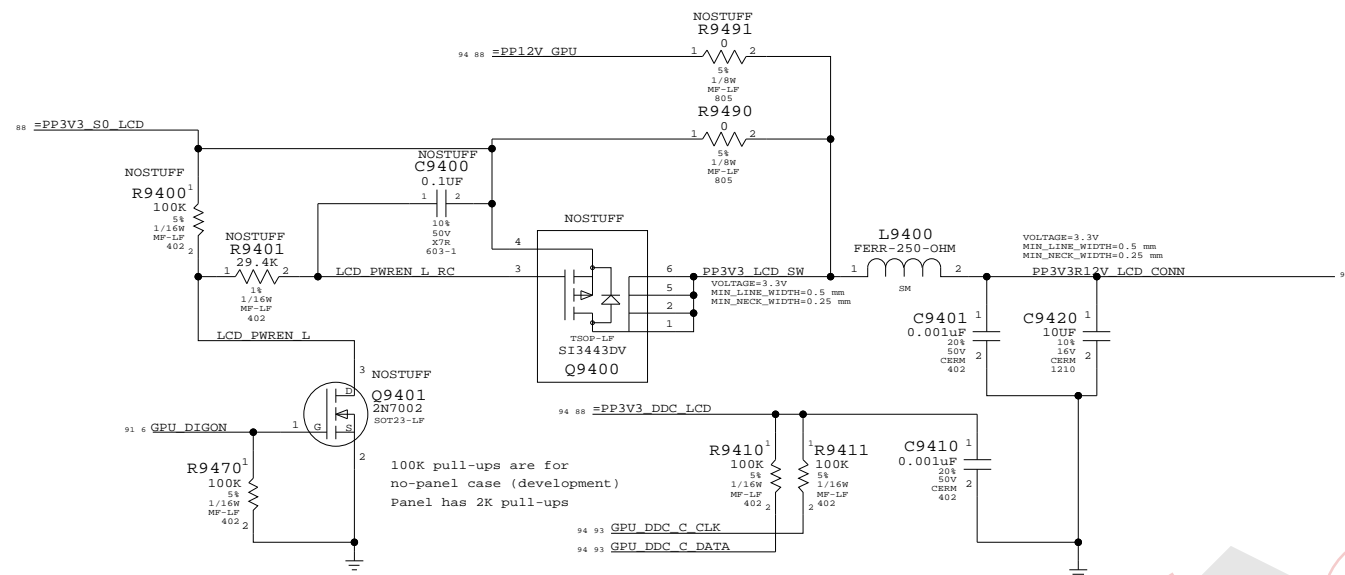
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
SCALE	SHT	OF	
NONE	93	110	

LCD (LVDS) INTERFACE

INVERTER INTERFACE



Internal Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005

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SCALE	SHT	OF	
NONE	94	110	

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C

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M56 TPS

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SCALE	SHT	OF	
NONE	95	110	

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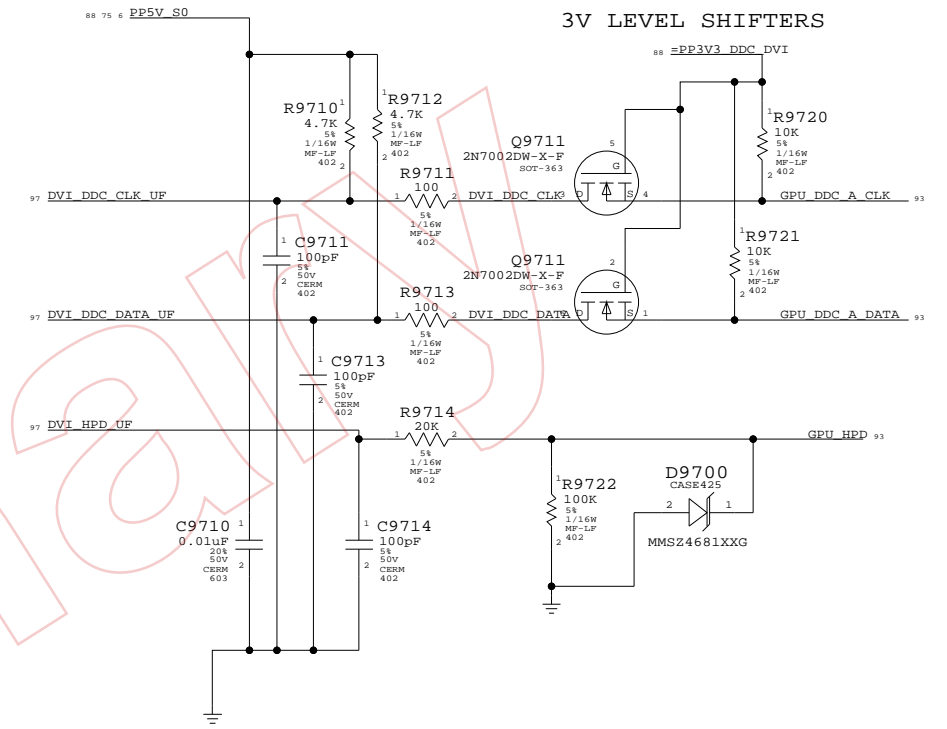
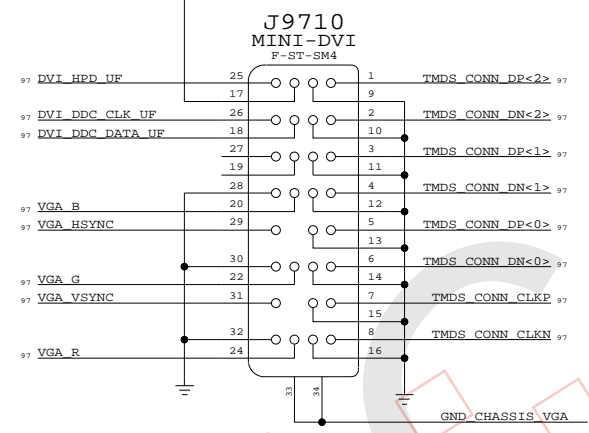
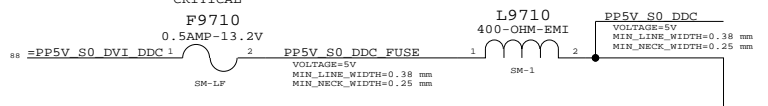
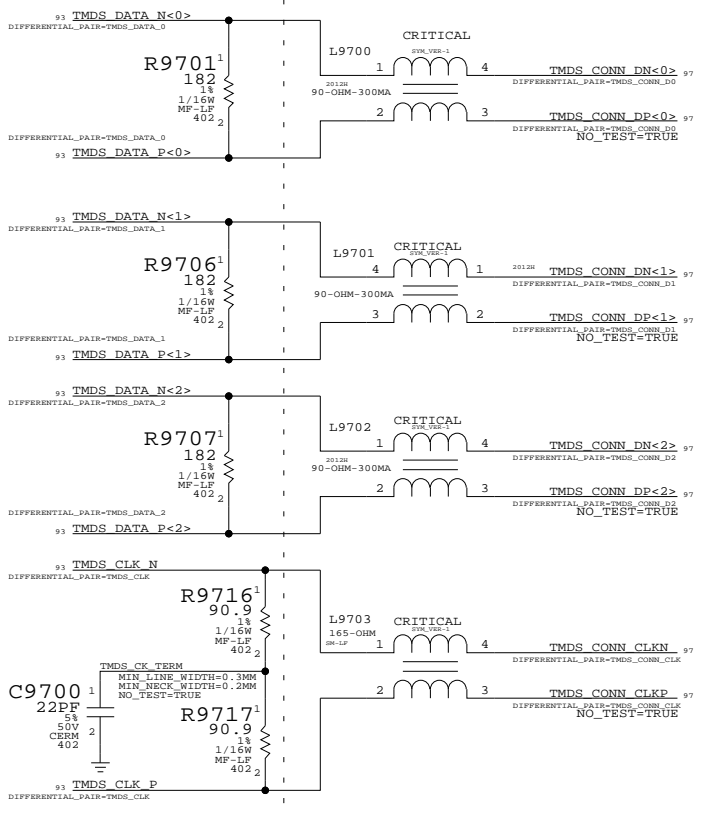
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PLACE LEFT SIDE
AS CLOSE TO GPU (U8400)
AS POSSIBLE

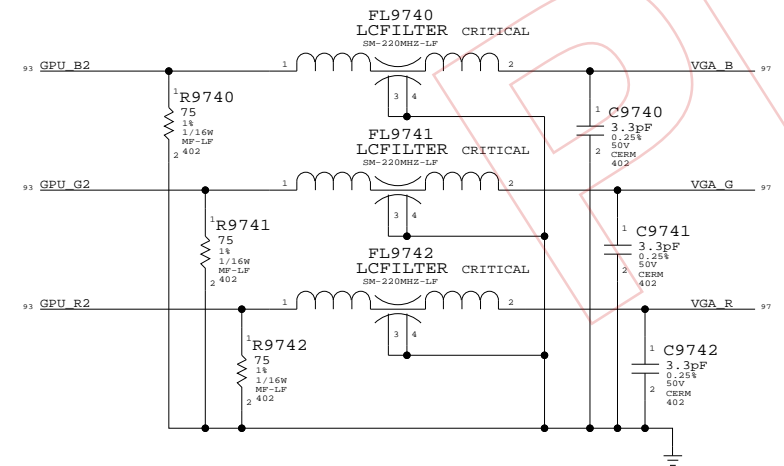
PLACE FILTER CLOSE
TO TMD5 CONNECTOR

DVI DDC CURRENT LIMIT DVI INTERFACE
(55mA requirement per DVI spec)

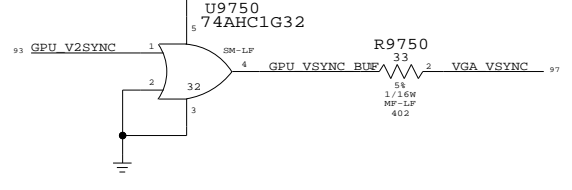
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
740S0044	740S0028		F9710	FUSE



ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS



PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

External Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

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	D	051-7148	13
SCALE	SHT	OF	
NONE	97	110	

8 7 6 5 4 3 2 1

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	Date: Jun 21 19:41:15 2006		C2505 CAP_402 m38a[25B7]	C4102 CAP_402 m38a[41D6]	C5903 CAP_402 m38a[59A8]				
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	R2101	RES_402	m38a[21C4]		R3414	RES_402	m38a[34B5]		R4713	RES_402	m38a[47C5]		R6807	RES_402	m38a[68D7]	
	R2105	RES_402	m38a[21D6]		R3415	RES_402	m38a[34B5]		R4722	RES_402	m38a[47B5]		R6808	RES_402	m38a[68D3]	
	R2107	RES_402	m38a[21C2]		R3416	RES_402	m38a[34B5]		R4723	RES_402	m38a[47B5]		R6810	RES_402	m38a[68A3]	
	R2108	RES_402	m38a[21C2]		R3417	RES_402	m38a[34B5]		R4732	RES_402	m38a[47A5]		R6811	RES_402	m38a[68A3]	
	R2110	RES_402	m38a[21C2]		R3418	RES_402	m38a[34B5]		R4733	RES_402	m38a[47A5]		R6812	RES_402	m38a[68A3]	
	R2194	RES_402	m38a[21D4]		R3419	RES_402	m38a[34A5]		R4742	RES_402	m38a[47C2]		R7208	RES_805	m38a[72A4]	
	R2195	RES_402	m38a[21C6]		R3420	RES_402	m38a[34A5]		R4743	RES_402	m38a[47C2]		R7212	RES_402	m38a[72B8]	
	R2196	RES_402	m38a[21C6]		R3421	RES_402	m38a[34A5]		R4746	RES_805	m38a[47D2]		R7213	RES_402	m38a[72B7]	

