

Avalanche Energy Rated N-Channel Power MOSFETs

2.5A and 3.0A, 350V-400V
 $r_{DS(on)} = 1.8\Omega$ and 2.5Ω

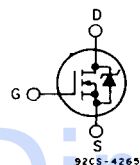
Features:

- Single pulse avalanche energy rated
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance

The IRF720R, IRF721R, IRF722R and IRF723R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

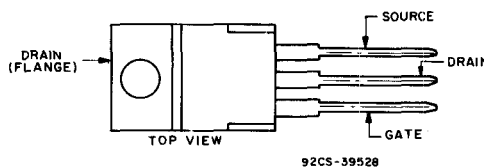
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATION



JEDEC TO-220AB

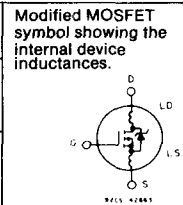
Absolute Maximum Ratings

Parameter	IRF720R	IRF721R	IRF722R	IRF723R	Units
V_{DS} Drain - Source Voltage ①	400	350	400	350	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ K}\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	3.0	3.0	2.5	2.5	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM} Pulsed Drain Current ③	12	12	10	10	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/ $^\circ\text{C}$
E_{AS} Single Pulse Avalanche Energy Rating ④	190				mj
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

**IRF720R, IRF721R
IRF722R, IRF723R**

Electrical Characteristics @ T_c = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	IRF720R IRF722R	400	—	—	V	V _{GS} = 0V I _D = 250μA
	IRF721R IRF723R	350	—	—	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _c = 125°C
I _{D(on)} On-State Drain Current ②	IRF720R IRF721R	3.0	—	—	A	V _{DS} > I _{D(on)} x R _{DS(on)max} , V _{GS} = 10V
	IRF722R IRF723R	2.5	—	—	A	
	IRF720R IRF721R IRF722R IRF723R	—	1.5	1.8	Ω	
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF720R IRF721R IRF722R IRF723R	—	1.8	2.5	Ω	V _{GS} = 10V, I _D = 1.5A
g _{fs} Forward Transconductance ②	ALL	1.0	2.0	—	S(V)	V _{DS} > I _{D(on)} x R _{DS(on)max} , I _D = 1.5A
C _{iss} Input Capacitance	ALL	—	450	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz
C _{oss} Output Capacitance	ALL	—	100	—	pF	See Fig. 10
C _{rss} Reverse Transfer Capacitance	ALL	—	20	—	pF	
t _{D(on)} Turn-On Delay Time	ALL	—	20	40	ns	V _{DD} ≈ 0.5BV _{DSS} , I _D = 1.5A, Z _θ = 50Ω
t _r Rise Time	ALL	—	25	50	ns	See Fig. 17
t _{D(off)} Turn-Off Delay Time	ALL	—	50	100	ns	(MOSFET switching times are essentially independent of operating temperature.)
t _f Fall Time	ALL	—	25	50	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	V _{GS} = 10V, I _D = 4.0A, V _{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	—	6.0	—	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
		—	4.5	—	nH	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	3.12	°C/W	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	°C/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF720R IRF721R	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF722R IRF723R	—	—	2.5	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF720R IRF721R	—	—	12	A	
	IRF722R IRF723R	—	—	10	A	
	IRF720R IRF721R	—	—	1.6	V	
V _{SD} Diode Forward Voltage ②	IRF722R IRF723R	—	—	1.5	V	T _c = 25°C, I _S = 2.5A, V _{GS} = 0V
	IRF720R IRF721R	—	—	—	—	
t _{rr} Reverse Recovery Time	ALL	—	450	—	ns	T _J = 150°C, I _F = 3.0A, dI _F /dt = 100A/μs
Q _{RR} Reverse Recovered Charge	ALL	—	3.1	—	μC	T _J = 150°C, I _F = 3.0A, dI _F /dt = 100A/μs
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ V_{DD} = 50V, starting T_J = 25°C, L = 31 mH, R_{gs} = 50Ω, I_{peak} = 3.3A. See figures 15, 16.

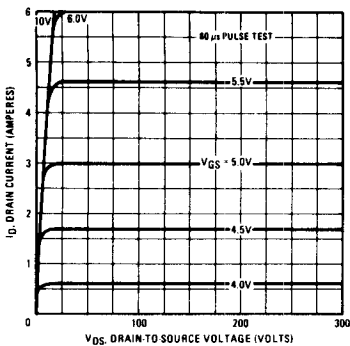


Fig. 1 - Typical Output Characteristics

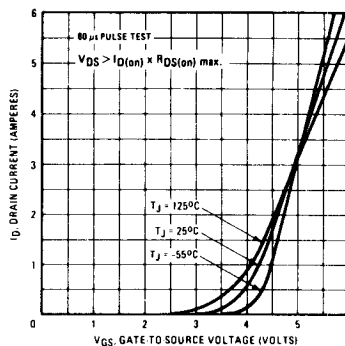


Fig. 2 - Typical Transfer Characteristics

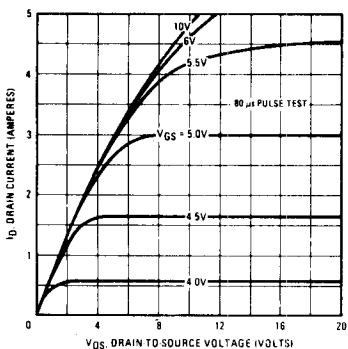


Fig. 3 - Typical Saturation Characteristics

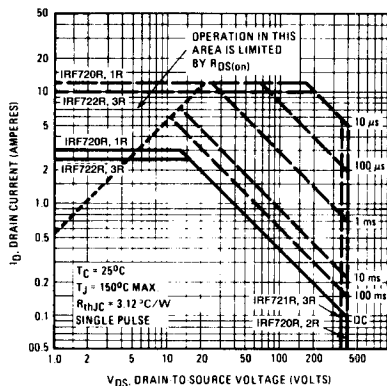


Fig. 4 - Maximum Safe Operating Area

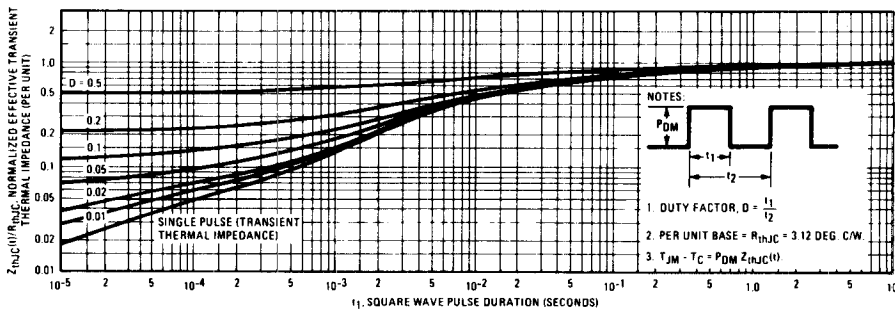


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF720R, IRF721R
IRF722R, IRF723R

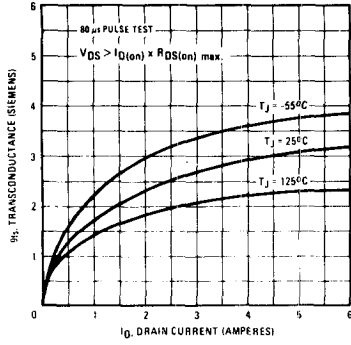


Fig. 6 - Typical Transconductance Vs. Drain Current

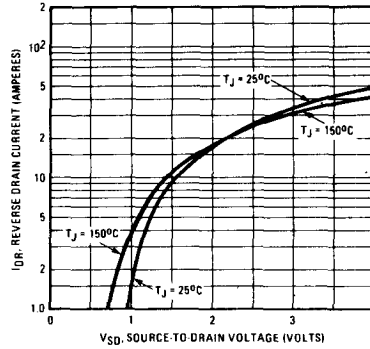


Fig. 7 - Typical Source-Drain Diode Forward Voltage

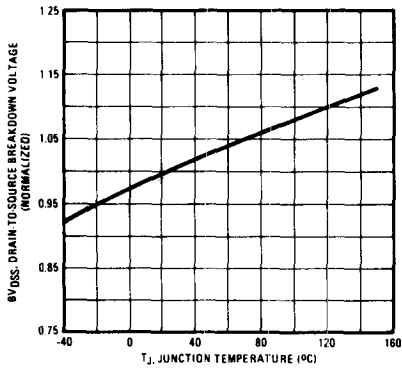


Fig. 8 - Breakdown Voltage Vs. Temperature

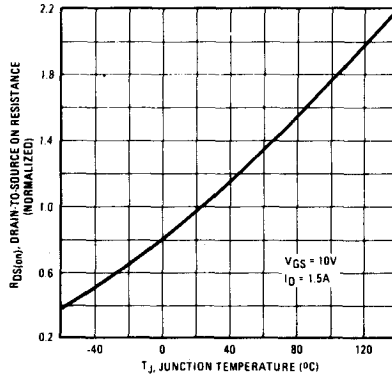


Fig. 9 - Normalized On-Resistance Vs. Temperature

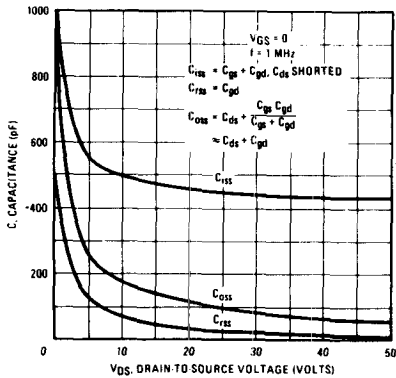


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

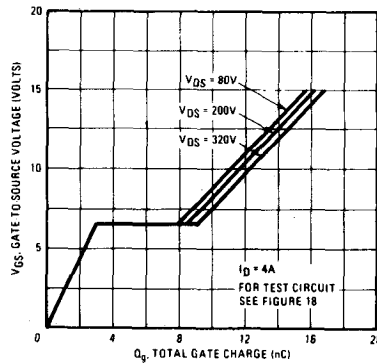


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

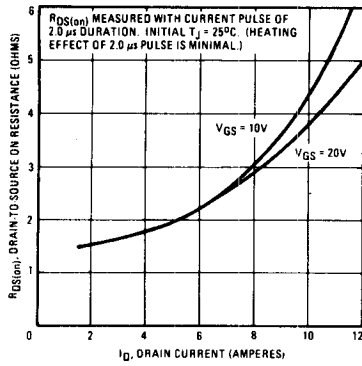


Fig. 12 - Typical On-Resistance Vs. Drain Current

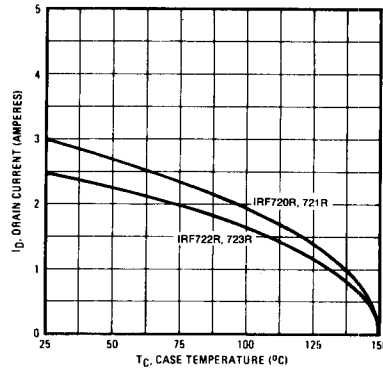


Fig. 13 - Maximum Drain Current Vs. Case Temperature

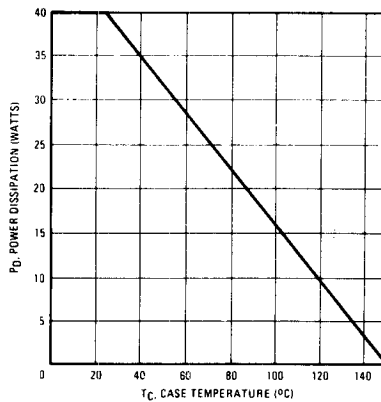


Fig. 14 - Power Vs. Temperature Derating Curve

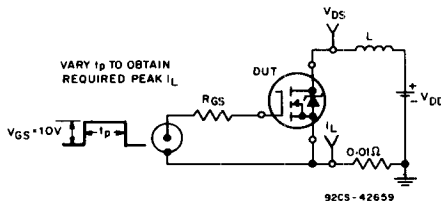


Fig. 15 - Unclamped Energy Test Circuit

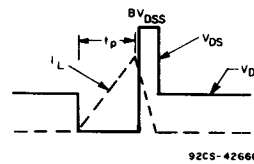


Fig. 16 - Unclamped Energy Waveforms

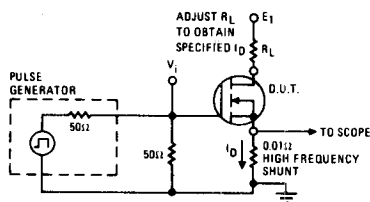


Fig. 17 - Switching Time Test Circuit

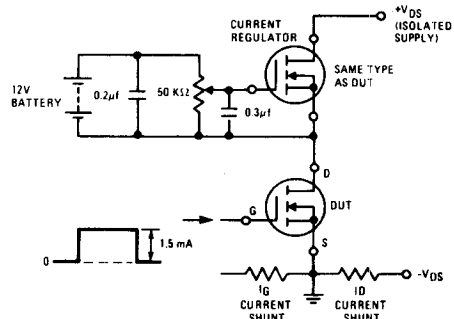


Fig. 18 - Gate Charge Test Circuit