

DDR SDRAM SODIMM

200pin Unbuffered SODIMM based on 512Mb B-die
with 64 / 72-bit (Non ECC / ECC)

Revision 1.3
October. 2003

Revision History

Revision 0.0 (Feb, 2003)

- First release

Revision 1.0 (June, 2003)

- Updated DC Characteristics

Revision 1.1 (July, 2003)

- Corrected Pin configuration table

Revision 1.2 (August, 2003)

- Corrected typo.

Revision 1.3 (October, 2003)

- Corrected typo in physical module dimension

256MB, 512MB, 1GB Unbuffered SODIMM

DDR SDRAM

200Pin Non ECC / ECC SODIMM based on 512Mb B-die (x8, x16)

Ordering Information

Part Number	Density	Organization	Component Composition	Height
M470L3324BT0-C(L)B3/A2/B0	256MB	32M x 64	32Mx16 (K4H511638B) * 4EA	1,250mil
M470L6524BT0-C(L)B3/A2/B0	512MB	64M x 64	32Mx16 (K4H511638B) * 8EA	1,250mil
M470L2923BN0-C(L)B3/A2/B0	1GB	128M x 64	64Mx8 (K4H510838B) * 16EA	1,250mil
M485L3324BT0-C(L)B3/A2/B0	256MB	32M x 72	32Mx16 (K4H511638B) * 5EA	1,250mil
M485L6523BT0-C(L)B3/A2/B0	512MB	64M x 72	64Mx8 (K4H510838B) * 9EA	1,400mil
M485L2829BT0-C(L)B3/A2/B0	1GB	128M x 72	st.128Mx8 (K4H1G0738B) * 9EA	1,400mil

Operating Frequencies

	B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)
Speed @CL2	133MHz	133MHz	100MHz
Speed @CL2.5	166MHz	133MHz	133MHz
CL-tRCD-tRP	2.5-3-3	2-3-3	2.5-3-3

Feature

- Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe [DQ] (x4,x8) & [L(U)DQS] (x16)
- Differential clock inputs(CK and \overline{CK})
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1250 (mil), single (256MB), double(512MB, 1GB) sided

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Rev. 1.3 October 2003

256MB, 512MB, 1GB Unbuffered SODIMM

DDR SDRAM

Pin Configurations (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back		
1	VREF	67	DQ27	135	DQ34	2	VREF	68	DQ31	136	DQ38		
3	VSS	69	VDD	137	VSS	4	VSS	70	VDD	138	VSS		
5	DQ0	71	CB0	139	DQ35	6	DQ4	72	CB4	140	DQ39		
7	DQ1	73	CB1	141	DQ40	8	DQ5	74	CB5	142	DQ44		
9	VDD	75	VSS	143	VDD	10	VDD	76	VSS	144	VDD		
11	DQS0	77	DQS8	145	DQ41	12	DM0	78	DM8	146	DQ45		
13	DQ2	79	CB2	147	DQS5	14	DQ6	80	CB6	148	DM5		
15	VSS	81	VDD	149	VSS	16	VSS	82	VDD	150	VSS		
17	DQ3	83	CB3	151	DQ42	18	DQ7	84	CB7	152	DQ46		
19	DQ8	85	DU	153	DQ43	20	DQ12	86	*DU/(RESET)	154	DQ47		
21	VDD	87	VSS	155	VDD	22	VDD	88	VSS	156	VDD		
23	DQ9	89	CK2	157	VDD	24	DQ13	90	VSS	158	/CK1		
25	DQS1	91	/CK2	159	VSS	26	DM1	92	VDD	160	CK1		
27	VSS	93	VDD	161	VSS	28	VSS	94	VDD	162	VSS		
29	DQ10	95	CKE1	163	DQ48	30	DQ14	96	CKE0	164	DQ52		
31	DQ11	97	DU	165	DQ49	32	DQ15	98	DU(BA2)	166	DQ53		
33	VDD	99	A12	167	VDD	34	VDD	100	A11	168	VDD		
35	CK0	101	A9	169	DQS6	36	VDD	102	A8	170	DM6		
37	/CK0	103	VSS	171	DQ50	38	VSS	104	VSS	172	DQ54		
39	VSS	105	A7	173	VSS	40	VSS	106	A6	174	VSS		
KEY			107	A5	175	DQ51	KEY			108	A4	176	DQ55
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60		
43	DQ17	111	A1	179	VDD	44	DQ21	112	A0	180	VDD		
45	VDD	113	VDD	181	DQ57	46	VDD	114	VDD	182	DQ61		
47	DQS2	115	A10/AP	183	DQS7	48	DM2	116	BA1	184	DM7		
49	DQ18	117	BA0	185	VSS	50	DQ22	118	/RAS	186	VSS		
51	VSS	119	/WE	187	DQ58	52	VSS	120	/CAS	188	DQ62		
53	DQ19	121	/CS0	189	DQ59	54	DQ23	122	/CS1	190	DQ63		
55	DQ24	123	*DU(A13)	191	VDD	56	DQ28	124	DU	192	VDD		
57	VDD	125	VSS	193	SDA	58	VDD	126	VSS	194	SA0		
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1		
61	DQS3	129	DQ33	197	VDDSPD	62	DM3	130	DQ37	198	SA2		
63	VSS	131	VDD	199	VDDID	64	VSS	132	VDD	200	DU		
65	DQ26	133	DQS4			66	DQ30	134	DM4				

Note 1. *: These pins are not used in this module.

2. Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are not used on x64(M470~) module, & used on x72(M485 ~) module.

Pin 95,122 are NC for 1Row module & used for 2Row module (M470L6524BT0, M470L2923BN0, M485L2829BT0).

Pin Description

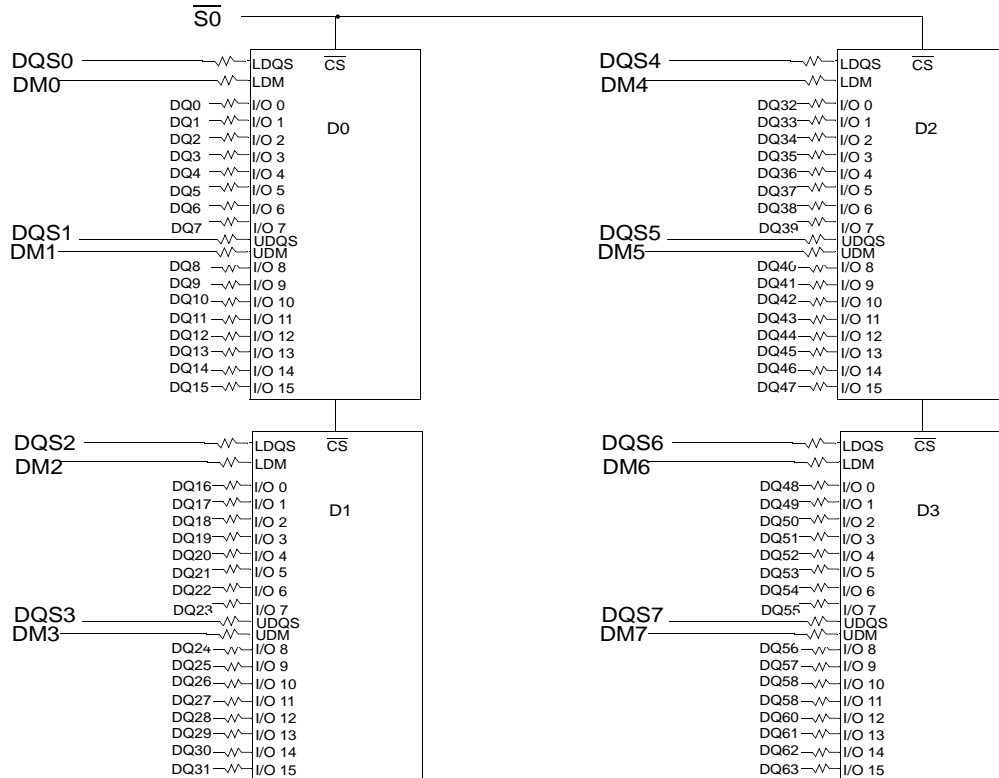
Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DM0 ~ DM7, DM8(for ECC)	Data - in mask
BA0 ~ BA1	Bank Select Address	VDD	Power supply (2.5V)
DQ0 ~ DQ63	Data input/output	VDDQ	Power Supply for DQS(2.5V)
DQS0 ~ DQS8	Data Strobe input/output	VSS	Ground
CK0,CK0 ~ CK2, CK2	Clock input	VREF	Power supply for reference
CKE0~CKE1	Clock enable input	VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
CS0~CS1	Chip select input	SDA	Serial data I/O
RAS	Row address strobe	SCL	Serial clock
CAS	Column address strobe	SA0 ~ 2	Address in EEPROM
WE	Write enable	NC	No connection
CB0 ~ CB7 (for x72)	Check bit(Data-in/data-out)		

256MB, 512MB, 1GB Unbuffered SODIMM

DDR SDRAM

256MB, 32M x 64 Non ECC Module (M470L3324BT0) (Populated as 1 bank of x16 DDR SDRAM Module)

FUNCTIONAL BLOCK DIAGRAM



BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D3

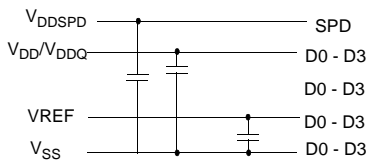
A0 - A12 → A0-A12: DDR SDRAMs D0 - D3

\overline{RAS} → \overline{RAS} : SDRAMs D0 - D3

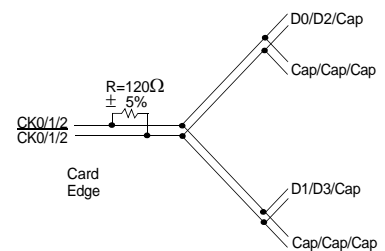
\overline{CAS} → \overline{CAS} : SDRAMs D0 - D3

CKE0 → CKE: SDRAMs D0 - D3

\overline{WE} → \overline{WE} : SDRAMs D0 - D3

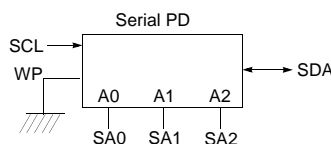


Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	2 SDRAMs
CK1/CK1	2 SDRAMs
CK2/CK2	NC



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.

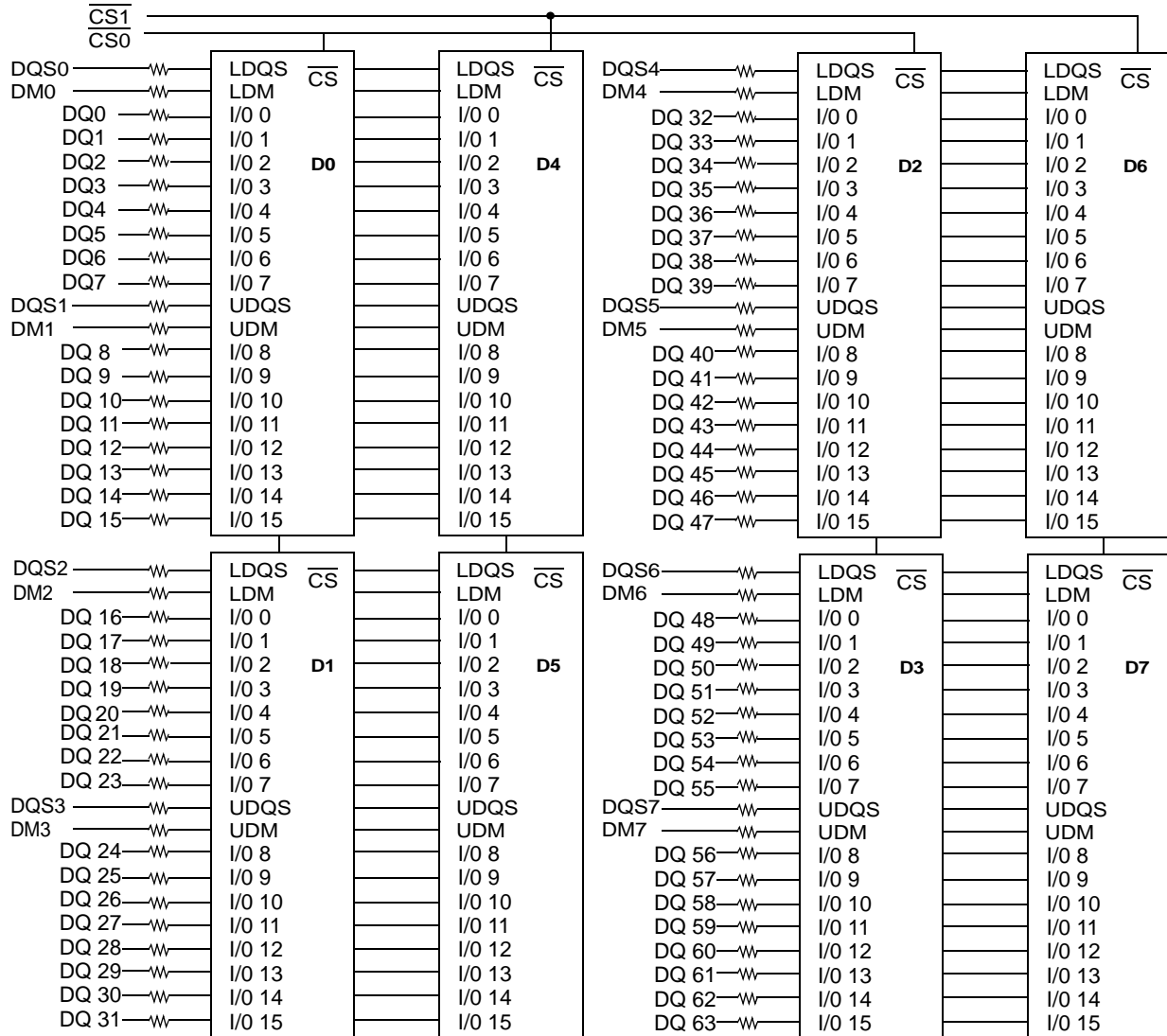


256MB, 512MB, 1GB Unbuffered SODIMM

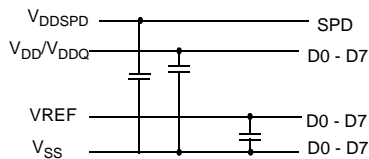
DDR SDRAM

512MB, 64M x 64 Non ECC Module (M470L6524BT0) (Populated as 2 bank of x16 DDR SDRAM Module)

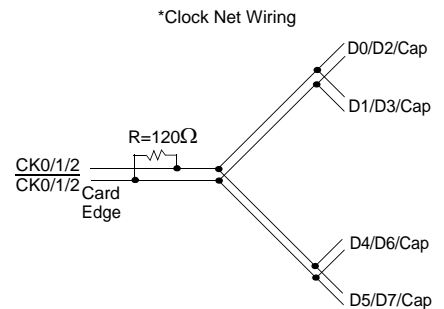
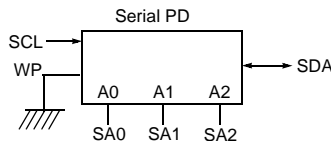
Functional Block Diagram



- BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D7
- A0 - A12 → A0-A12: DDR SDRAMs D0 - D7
- $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMs D0 - D7
- $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMs D0 - D7
- CKE0 → CKE: SDRAMs D0 - D3
- CKE1 → CKE: SDRAMs D4 - D7
- $\overline{\text{WE}}$ → $\overline{\text{WE}}$: SDRAMs D0 - D7



Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	4 SDRAMs
CK1/CK1	4 SDRAMs
CK2/CK2	NC



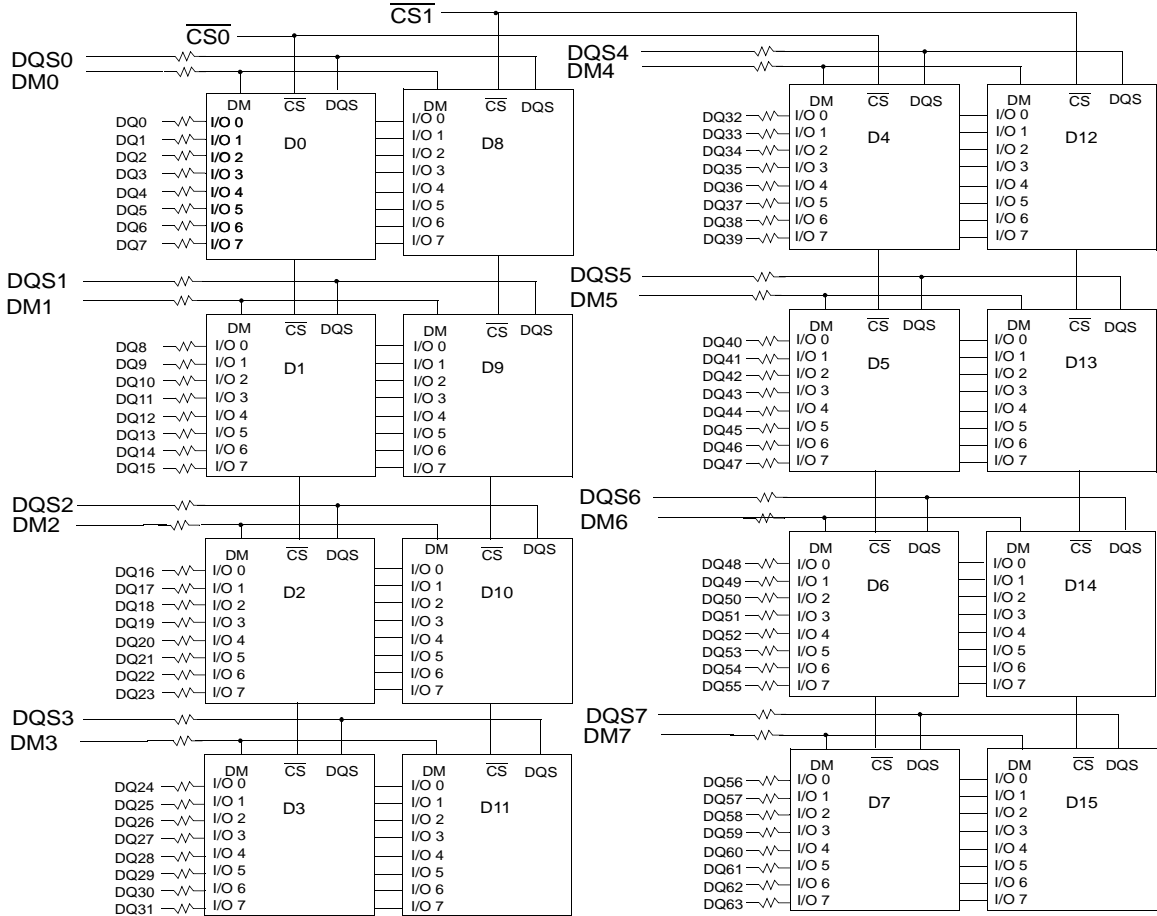
- Notes:
- DQ-to-I/O wiring is shown as recommended but may be changed.
 - DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
 - DQ, DQS, DM/DQS resistors: 22 Ohms.

256MB, 512MB, 1GB Unbuffered SODIMM

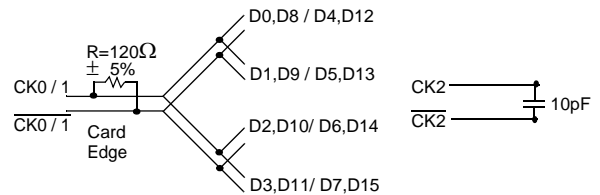
DDR SDRAM

1GB, 128M x 64 Non ECC Module (M470L2923BN0) (Populated as 2 bank of x8 DDR SDRAM Module)

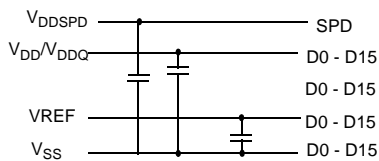
FUNCTIONAL BLOCK DIAGRAM



- BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D15
- A0 - A12 → A0-A12: DDR SDRAMs D0 - D15
- RAS → RAS: DDR SDRAMs D0 - D15
- CAS → CAS: DDR SDRAMs D0 - D15
- CKE1 → CKE: DDR SDRAMs D8 - D15
- CKE0 → CKE: DDR SDRAMs D0 - D7
- WE → WE: DDR SDRAMs D0 - D15



*Clock Net Wiring



Notes :

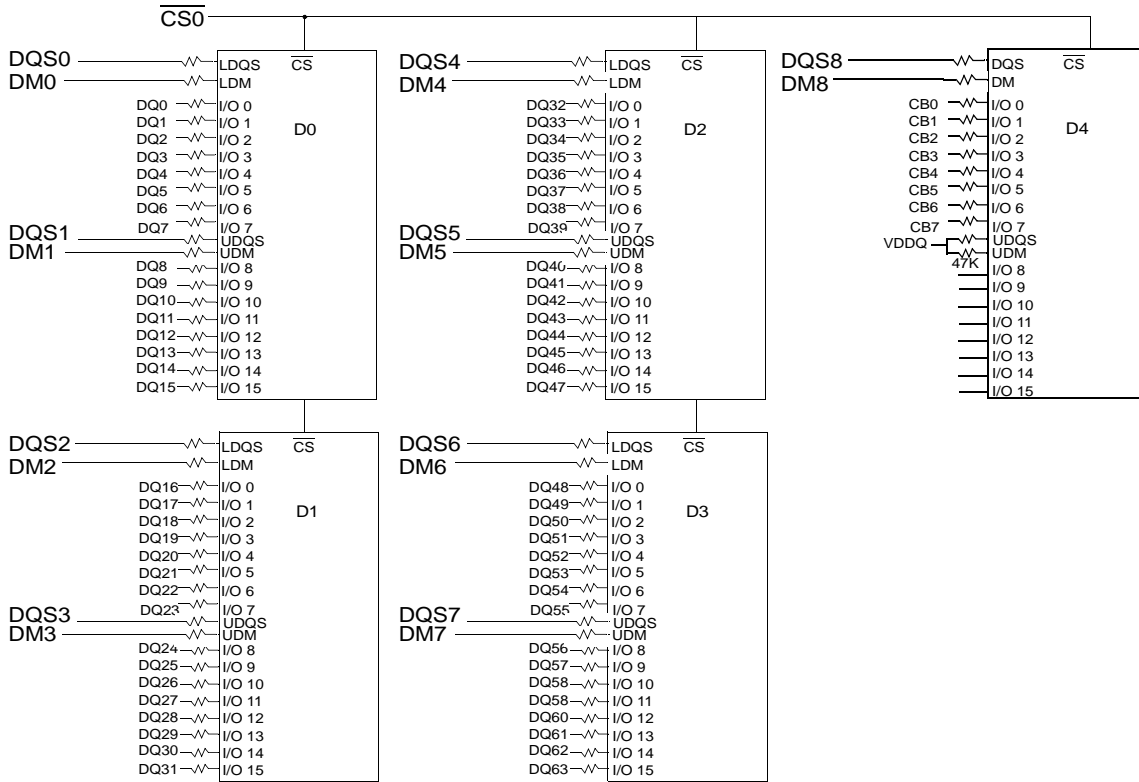
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown
3. DQ, DQS, DM/DQS resistors: 22 Ohm.

256MB, 512MB, 1GB Unbuffered SODIMM

DDR SDRAM

256MB, 32M x 72 ECC Module (M485L3324BT0) (Populated as 1 bank of x16 DDR SDRAM Module)

Functional Block Diagram



BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D4

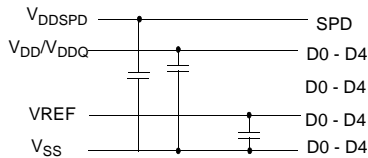
A0 - A12 → A0-A12: DDR SDRAMs D0 - D4

$\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMs D0 - D4

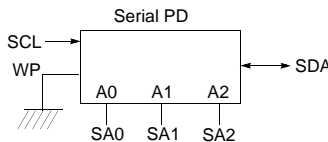
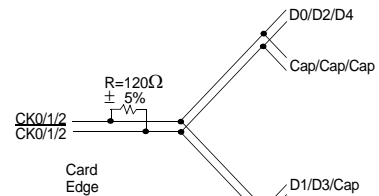
$\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMs D0 - D4

CKE0 → CKE: SDRAMs D0 - D4

$\overline{\text{WE}}$ → $\overline{\text{WE}}$: SDRAMs D0 - D4



Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	2 SDRAMs
CK1/CK1	2 SDRAMs
CK2/CK2	1 SDRAMs



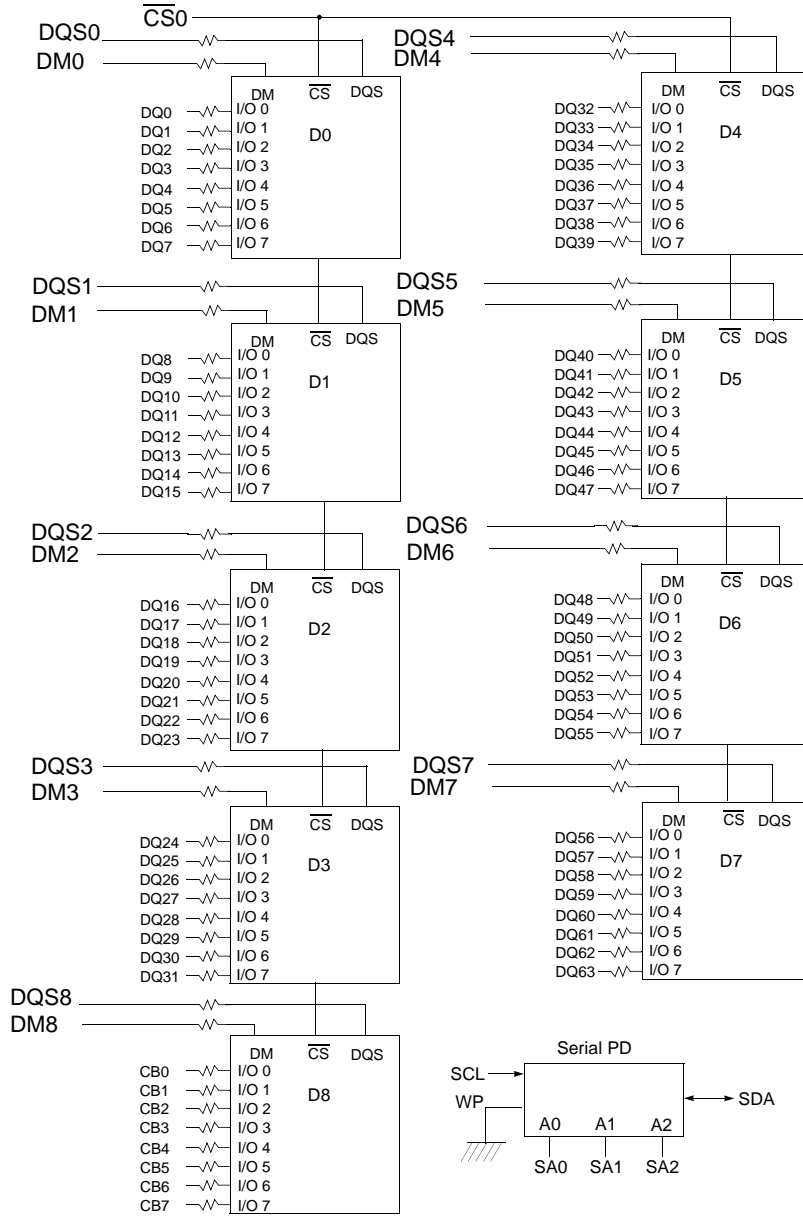
- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
 3. DQ, DQS, DM/DQS resistors: 22 Ohms.

256MB, 512MB, 1GB Unbuffered SODIMM

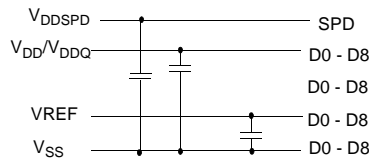
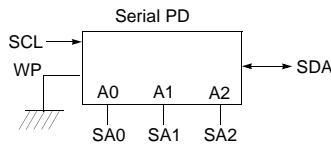
DDR SDRAM

512MB, 64M x 72 ECC Module (M485L6523BT0) (Populated as 1 bank of x8 DDR SDRAM Module)

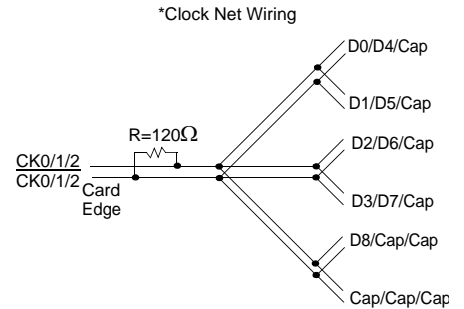
Functional Block Diagram



- BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D8
- A0 - A12 → A0-A12: DDR SDRAMs D0 - D8
- $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: DDR SDRAMs D0 - D8
- $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: DDR SDRAMs D0 - D8
- CKE0 → CKE: DDR SDRAMs D0 - D8
- $\overline{\text{WE}}$ → $\overline{\text{WE}}$: DDR SDRAMs D0 - D8



* Clock Wiring	
Clock Input	DDR SDRAMs
CK0/CK0	5 DDR SDRAMs
CK1/CK1	4 DDR SDRAMs



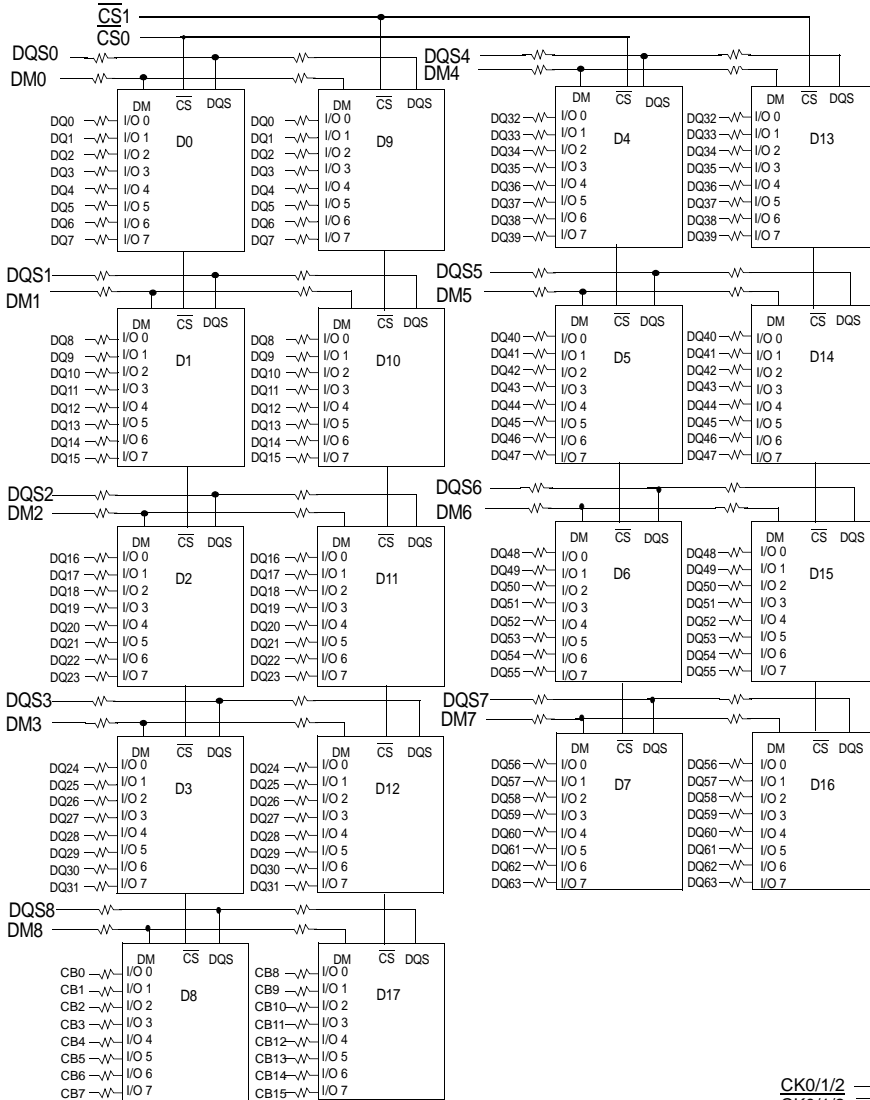
- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/ $\overline{\text{CS}}$ relationships must be maintained as shown.
 3. DQ, DQS, DM/DQS resistors: 22 Ohms \pm 5%.

256MB, 512MB, 1GB Unbuffered SODIMM

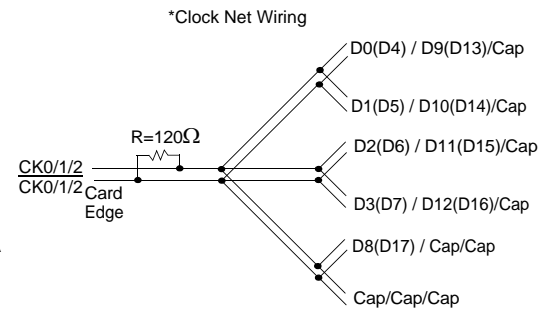
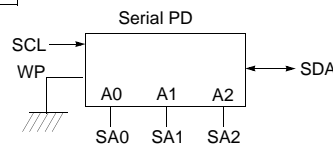
DDR SDRAM

1GB, 128M x 72 ECC Module (M485L2829BT0) (Populated as 2 bank of x8 DDR SDRAM Module)

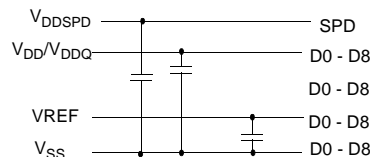
Functional Block Diagram



* Clock Wiring	
Clock Input	DDR SDRAMs
CK0/ $\overline{\text{CK0}}$	10 DDR SDRAMs
CK1/ $\overline{\text{CK1}}$	8 DDR SDRAMs



- BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D8
- A0 - A12 → A0-A12: DDR SDRAMs D0 - D8
- $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: DDR SDRAMs D0 - D8
- $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: DDR SDRAMs D0 - D8
- CKE0/1 → CKE: DDR SDRAMs D0 - D8
- $\overline{\text{WE}}$ → $\overline{\text{WE}}$: DDR SDRAMs D0 - D8



- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/ $\overline{\text{CS}}$ relationships must be maintained as shown.
 3. DQ, DQS, DM/DQS resistors: 22 Ohms \pm 5%.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD}	-1.0 ~ 3.6	V
Voltage on V _{DDQ} supply relative to Vss	V _{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	PD	1.5 * # of component	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Power & DC Operating Conditions (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V _{DD} of 2.5V)	V _{DD}	2.3	2.7		
I/O Supply voltage	V _{DDQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	V _{DDQ} /2-50mV	V _{DDQ} /2+50mV	V	1
I/O Termination voltage(system)	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{DDQ} +0.3	V	4
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	4
Input Voltage Level, CK and \overline{CK} inputs	V _{IN} (DC)	-0.3	V _{DDQ} +0.3	V	
Input Differential Voltage, CK and \overline{CK} inputs	V _{ID} (DC)	0.3	V _{DDQ} +0.6	V	3
Input leakage current	I _I	-2	2	uA	
Output leakage current	I _{OZ}	-5	5	uA	
Output High Current(Normal strength driver) ;V _{OUT} = V _{TT} + 0.84V	I _{OH}	-16.8		mA	
Output High Current(Normal strength driver) ;V _{OUT} = V _{TT} - 0.84V	I _{OL}	16.8		mA	
Output High Current(Half strength driver) ;V _{OUT} = V _{TT} + 0.45V	I _{OH}	-9		mA	
Output High Current(Half strength driver) ;V _{OUT} = V _{TT} - 0.45V	I _{OL}	9		mA	

Notes 1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.
 2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
 3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
 4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.

M470L3324BT0 (32M x 64, 256MB Module)

(VDD=2.7V, T = 10°C)

Symbol	B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0	500	440	440	mA	
IDD1	620	560	560	mA	
IDD2P	20	20	20	mA	
IDD2F	120	120	120	mA	
IDD2Q	100	80	80	mA	
IDD3P	120	120	120	mA	
IDD3N	200	200	200	mA	
IDD4R	780	680	680	mA	
IDD4W	860	760	760	mA	
IDD5	1,000	960	960	mA	
IDD6	Normal	20	20	mA	
	Low power	12	12	mA	Optional
IDD7A	1,620	1,440	1,440	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

M470L6524BT0 (64M x 64, 512MB Module)

(VDD=2.7V, T = 10°C)

Symbol	B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0	700	640	640	mA	
IDD1	820	760	760	mA	
IDD2P	40	40	40	mA	
IDD2F	240	240	240	mA	
IDD2Q	200	160	160	mA	
IDD3P	240	240	240	mA	
IDD3N	400	400	400	mA	
IDD4R	980	880	880	mA	
IDD4W	1,060	960	960	mA	
IDD5	1,200	1,160	1,160	mA	
IDD6	Normal	40	40	mA	
	Low power	24	24	mA	Optional
IDD7A	1,820	1,640	1,640	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

M470L2923BN0 (128M x 64, 1GB Module)(V_{DD}=2.7V, T = 10°C)

Symbol		B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0		1,400	1,280	1,280	mA	
IDD1		1,600	1,480	1,480	mA	
IDD2P		80	80	80	mA	
IDD2F		480	480	480	mA	
IDD2Q		400	400	400	mA	
IDD3P		480	480	480	mA	
IDD3N		800	800	800	mA	
IDD4R		1,840	1,600	1,600	mA	
IDD4W		1,880	1,640	1,640	mA	
IDD5		2,400	2,320	2,320	mA	
IDD6	Normal	80	80	80	mA	
	Low power	48	48	48	mA	Optional
IDD7A		3,520	3,120	3,120	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

M485L3324BT0 (32M x 72, 256MB Module)(V_{DD}=2.7V, T = 10°C)

Symbol		B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0		625	550	550	mA	
IDD1		775	700	700	mA	
IDD2P		25	25	25	mA	
IDD2F		150	150	150	mA	
IDD2Q		125	100	100	mA	
IDD3P		150	150	150	mA	
IDD3N		250	250	250	mA	
IDD4R		975	850	850	mA	
IDD4W		1,075	950	950	mA	
IDD5		1,250	1,200	1,200	mA	
IDD6	Normal	25	25	25	mA	
	Low power	15	15	15	mA	Optional
IDD7A		2,025	1,800	1,800	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

256MB, 512MB, 1GB Unbuffered SODIMM

DDR SDRAM

DDR SDRAM IDD spec table

M485L6523BT0 (64M x 72, 512MB Module)

(V_{DD}=2.7V, T = 10°C)

Symbol	B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0	1,125	990	990	mA	
IDD1	1,350	1,215	1,215	mA	
IDD2P	45	45	45	mA	
IDD2F	270	270	270	mA	
IDD2Q	225	180	180	mA	
IDD3P	270	270	270	mA	
IDD3N	450	450	450	mA	
IDD4R	1,620	1,350	1,350	mA	
IDD4W	1,665	1,395	1,395	mA	
IDD5	2,250	2,160	2,160	mA	
IDD6	Normal	45	45	mA	
	Low power	27	27	mA	Optional
IDD7A	3,510	3,060	3,060	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

M485L2829BT0 (st.128M x 72, 1GB Module)

(V_{DD}=2.7V, T = 10°C)

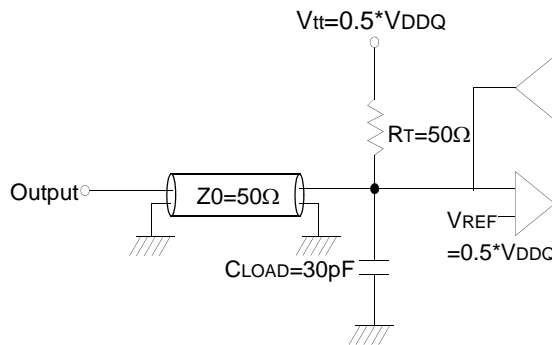
Symbol	B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0	1,575	1,440	1,440	mA	
IDD1	1,800	1,665	1,665	mA	
IDD2P	90	90	90	mA	
IDD2F	540	540	540	mA	
IDD2Q	450	360	360	mA	
IDD3P	540	540	540	mA	
IDD3N	900	900	900	mA	
IDD4R	2,070	1,800	1,800	mA	
IDD4W	2,115	1,845	1,845	mA	
IDD5	2,700	2,610	2,610	mA	
IDD6	Normal	90	90	mA	
	Low power	54	54	mA	Optional
IDD7A	3,960	3,510	3,510	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V _{IH} (AC)	V _{REF} + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V _{IL} (AC)		V _{REF} - 0.31	V	3
Input Differential Voltage, CK and CK inputs	V _{ID} (AC)	0.7	V _{DDQ} +0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V _{IX} (AC)	0.5*V _{DDQ} -0.2	0.5*V _{DDQ} +0.2	V	2

- Note 1. V_{ID} is the magnitude of the difference between the input level on CK and the input on \overline{CK} .
 2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
 3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.



Output Load Circuit (SSTL_2)

Input/Output Capacitance

(VDD=2.5V, VDDQ=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	M470L3324BT0		M470L6524BT0		M470L2923BN0		Unit
		Min	Max	Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1,RAS,CAS,WE)	CIN1	41	45	49	57	65	81	pF
Input capacitance(CKE0, CKE1)	CIN2	34	38	42	50	42	50	pF
Input capacitance($\overline{CS0}$, CS1)	CIN3	34	38	42	50	42	50	pF
Input capacitance(CLK0, CLK1,CLK2)	CIN4	25	30	25	30	28	34	pF
Input capacitance(DM0~DM7)	CIN5	6	7	6	7	10	12	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	6	7	6	7	10	12	pF

Input/Output Capacitance

(VDD=2.5V, VDDQ=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	M485L3324BT0		M485L6523BT0		M485L2829BT0		Unit
		Min	Max	Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1,RAS,CAS,WE)	CIN1	43	48	51	60	69	87	pF
Input capacitance(CKE0, CKE1)	CIN2	36	41	44	53	44	53	pF
Input capacitance($\overline{CS0}$, CS1)	CIN3	36	41	44	53	44	53	pF
Input capacitance(CLK0, CLK1,CLK2)	CIN4	25	30	25	30	28	34	pF
Input capacitance(DM0~DM7, DM8(for ECC))	CIN5	6	7	6	7	10	12	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	6	7	6	7	10	12	pF
Data input/output capacitance (CB0~CB7)	Cout2	6	7	6	7	10	12	pF

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DDR SDRAM

AC Timing Parameters & Specifications

Parameter	Symbol	B3 (DDR333@CL=2.5)		A2 (DDR266@CL=2.0)		B0 (DDR266@CL=2.5)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	60		65		65		ns		
Refresh row cycle time	tRFC	72		75		75		ns		
Row active time	tRAS	42	70K	45	120K	45	120K	ns		
RAS to CAS delay	tRCD	18		20		20		ns		
Row precharge time	tRP	18		20		20		ns		
Row active to Row active delay	tRRD	12		15		15		ns		
Write recovery time	tWR	15		15		15		ns		
Last data in to Read command	tWTR	1		1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		1		tCK		
Clock cycle time	tCK	CL=2.0	7.5	12	7.5	12	10	12	ns	
		CL=2.5	6	12	7.5	12	7.5	12	ns	
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSK	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns		
Output data access time from CK/CK	tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns		
Data strobe edge to output data edge	tDQSQ	-	0.45	-	0.5	-	0.5	ns	12	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		0		ns	3	
DQS-in hold time	tWPRE	0.25		0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time(fast)	tIS	0.75		0.9		0.9		ns	i,5,7-9	
Address and Control Input hold time(fast)	tIH	0.75		0.9		0.9		ns	i,5,7-9	
Address and Control Input setup time(slow)	tIS	0.8		1.0		1.0		ns	i, 6-9	
Address and Control Input hold time(slow)	tIH	0.8		1.0		1.0		ns	i, 6-9	
Data-out high impedance time from CK/CK	tHZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	1	
Data-out low impedance time from CK/CK	tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	1	
Input Slew Rate(for input only pins)	tSL(I)	0.5		0.5		0.5		V/ns		
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		0.5		V/ns		
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns		
Output Slew Rate(x16)	tSL(O)	0.7	5	0.7	5	0.7	5	V/ns		
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5			

Parameter	Symbol	B3 (DDR333@CL=2.5))		A2 (DDR266@CL=2.0)		B0 (DDR266@CL=2.5))		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	12		15		15		ns	
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		ns	j, k
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		ns	j, k
Control & Address input pulse width	tIPW	2.2		2.2		2.2		ns	8
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		ns	8
Power down exit time	tPDEX	6		7.5		7.5		ns	
Exit self refresh to non-Read command	tXSNR	75		75		75		ns	
Exit self refresh to read command	tXSRD	200		200		200		tCK	
Refresh interval time	tREFI		7.8		7.8		7.8	us	4
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	11
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	10, 11
Data hold skew factor	tQHS		0.55		0.75		0.75	ns	11
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	2
Active to Read with Auto precharge command	tRAP	18		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	13

System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333, DDR266 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR333		DDR266			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Units	Notes
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	TBD	TBD	TBD	TBD	V/ns	a, m

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tIS	tIH	Units	Notes
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tDS	tDH	Units	Notes
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	tDS	tDH	Units	Notes
+/- 0.0 V/ns	0	0	ps	j
+/- 0.25 V/ns	+50	+50	ps	j
+/- 0.5 V/ns	+100	+100	ps	j

Table 5 : Output Slew Rate Characteristic (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g,h

Table 6 : Output Slew Rate Characteristic (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g,h

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS	DDR333		DDR266		Notes
	MIN	MAX	MIN	MAX	
Output Slew Rate Matching Ratio (Pullup to Pulldown)	TBD	TBD	TBD	TBD	e,m

Component Notes

1. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
2. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
3. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
4. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
5. For command/address input slew rate ≥ 1.0 V/ns
6. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
7. For CK & $\overline{\text{CK}}$ slew rate ≥ 1.0 V/ns
8. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
9. Slew Rate is measured between VOH(ac) and VOL(ac).
10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
11. tQH = tHP - tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. tDQSQ
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
13. tDAL = (tWR/tCK) + (tRP/tCK)
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns tDAL = (15 ns / 7.5 ns) + (20 ns/ 7.5ns) = (2) + (3)
tDAL = 5 clocks

System Notes :

a. Pullup slew rate is characterized under the test conditions as shown in Figure 1.

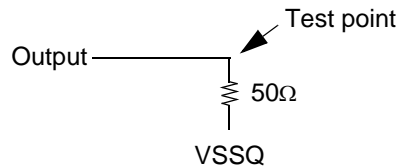


Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

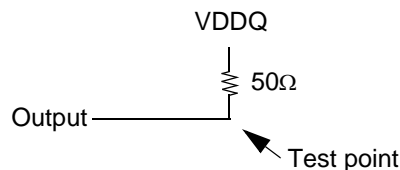


Figure 2 : Pulldown slew rate test load

- c. Pullup slew rate is measured between $(VDDQ/2 - 320 \text{ mV} \pm 250 \text{ mV})$
 Pulldown slew rate is measured between $(VDDQ/2 + 320 \text{ mV} \pm 250 \text{ mV})$
 Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example : For typical slew rate, DQ0 is switching

For minimum slew rate, all DQ bits are switching from either high to low, or low to high.
 The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions

Typical : 25 °C (T Ambient), VDDQ = 2.5V, typical process

Minimum : 70 °C (T Ambient), VDDQ = 2.3V, slow - slow process

Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOP11 package devices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates determined by either $V_{IH}(AC)$ to $V_{IL}(AC)$ or $V_{IH}(DC)$ to $V_{IL}(DC)$, similarly for rising transitions.

j. A derating factor will be used to increase t_{DS} and t_{DH} in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either $V_{IH}(AC)$ to $V_{IL}(AC)$ or $V_{IH}(DC)$ to $V_{IL}(DC)$, similarly for rising transitions.

The delta rise/fall rate is calculated as: $\{1/(\text{Slew Rate1})\} - \{1/(\text{Slew Rate2})\}$

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in t_{DS} and t_{DH} of 100 ps.

k. Table 3 is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC - AC slew rate and the DC- DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either $V_{IH}(ac)$ to $V_{IL}(ac)$ or $V_{IH}(DC)$ to $V_{IL}(DC)$, and similarly for rising transitions.

m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotony.

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0,1	A10/AP	A0 ~ A9, A11, A12	Note
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh	H	H	L	L	L	L	H	X		3
			L								3
	Self Refresh	Exit	L	H	L	H	H	H	X		3
					H	X	X	X			3
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable	H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable								H		4
Write & Column Address	Auto Precharge Disable	H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable								H		4, 6
Burst Stop		H	X	L	H	H	L	X			7
Precharge	Bank Selection	H	X	L	L	H	L	V	L	X	
	All Banks							X	H		5
Active Power Down	Entry	H	L	H	X	X	X	X			
				L	V	V	V				
	Exit	L	H	X	X	X	X				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			
				L	H	H	H				
	Exit	L	H	H	X	X	X				
				L	V	V	V				
DM		H	X					X			8
No operation (NOP) : Not defined		H	X	H	X	X	X	X			9
				L	H	H	H			9	

Note : 1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at trP after the end of burst.

7. Burst stop command is valid at every burst length.

8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

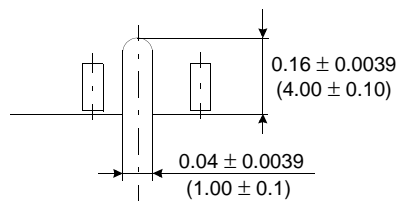
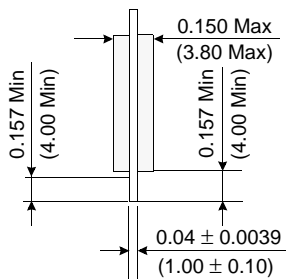
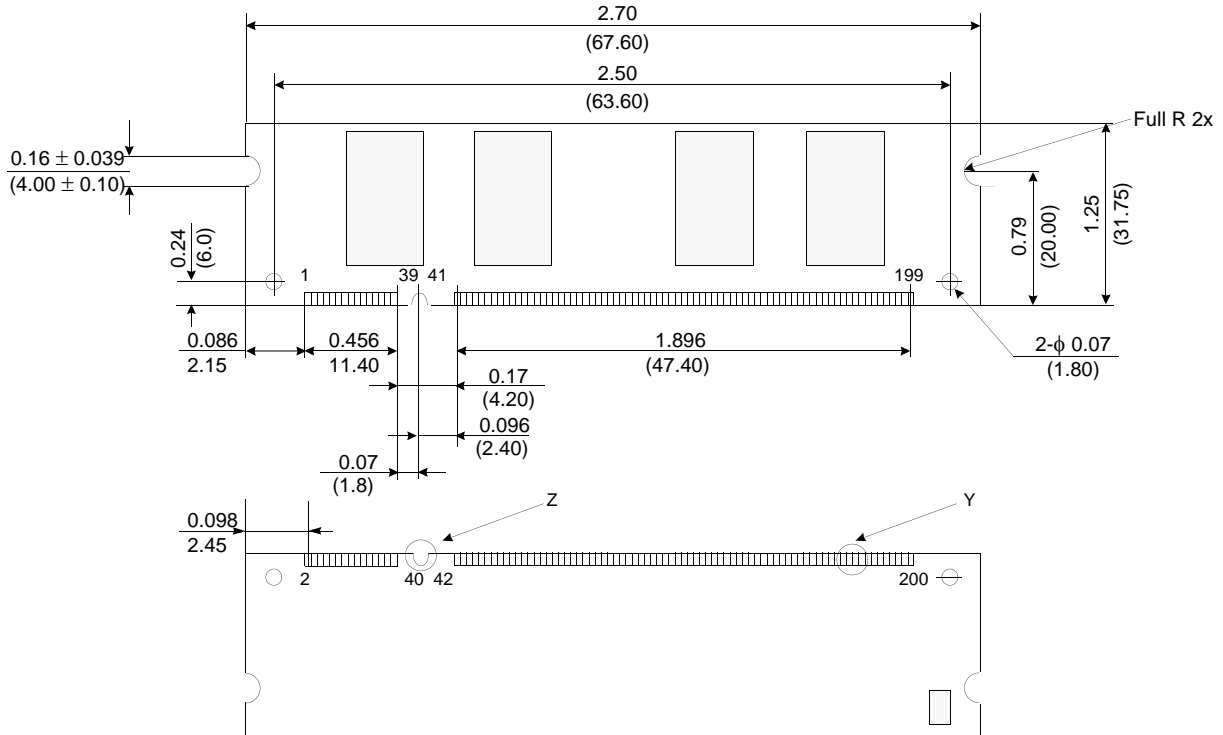
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

256MB, 512MB, 1GB Unbuffered SODIMM

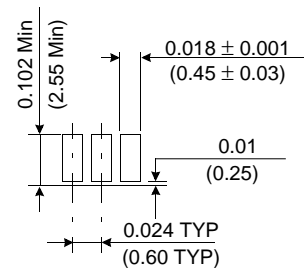
DDR SDRAM

Physical Dimensions : 32M x64 (M470L3324BT0)

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±.006(.15) unless otherwise specified

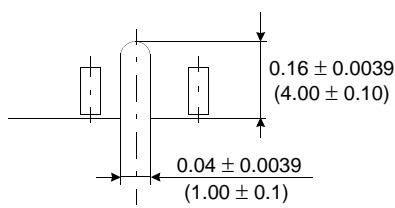
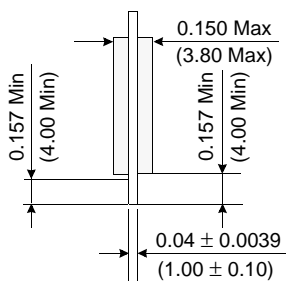
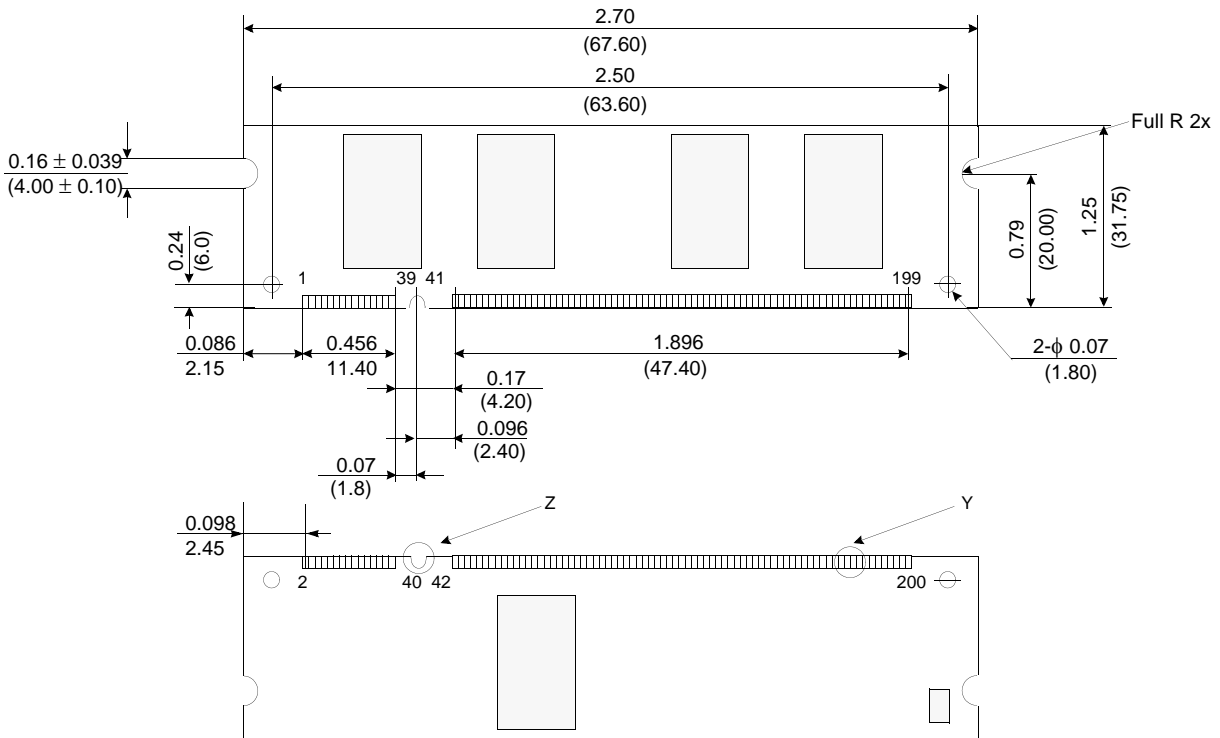
The used device is 32Mx16 SDRAM, TSOP11
SDRAM Part No. : K4H511638B-T***

256MB, 512MB, 1GB Unbuffered SODIMM

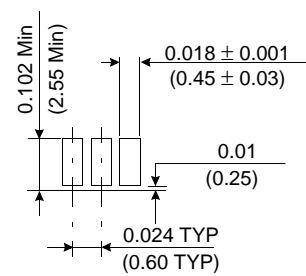
DDR SDRAM

Physical Dimensions : 32M x72 (M485L3324BT0)

Units : Inches (Millimeters)



Detail Z



Detail Y

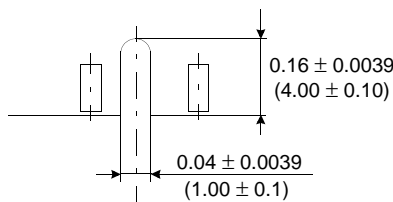
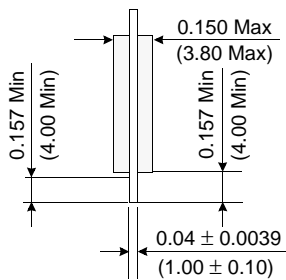
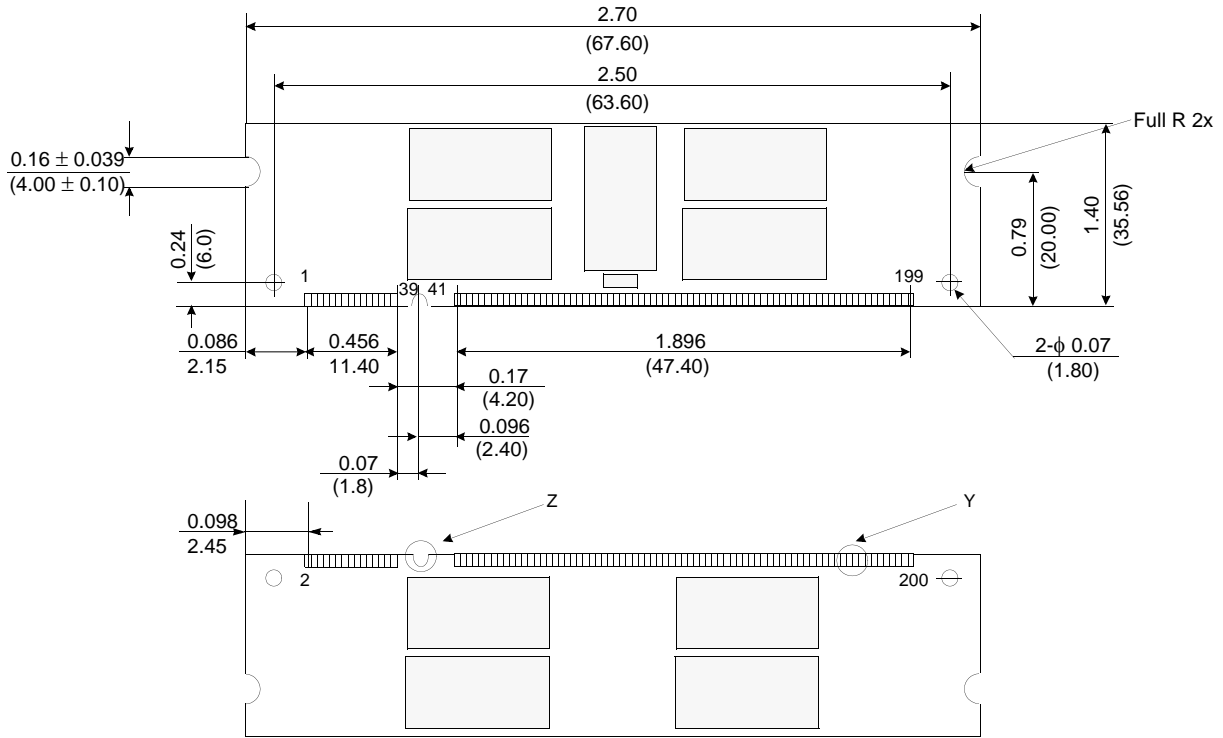
Tolerances : $\pm 0.006(.15)$ unless otherwise specified
 The used device is 32Mx16 DDR SDRAM, TSOP11
 DDR SDRAM Part No. : K4H511638B-T***

256MB, 512MB, 1GB Unbuffered SODIMM

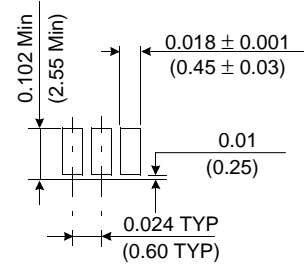
DDR SDRAM

Physical Dimensions : 64M x72 (M485L6523BT0)

Units : Inches (Millimeters)



Detail Z



Detail Y

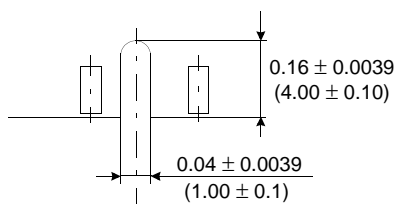
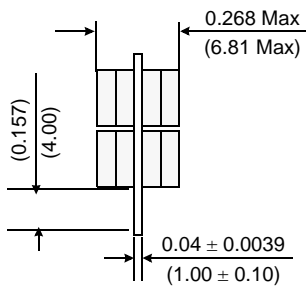
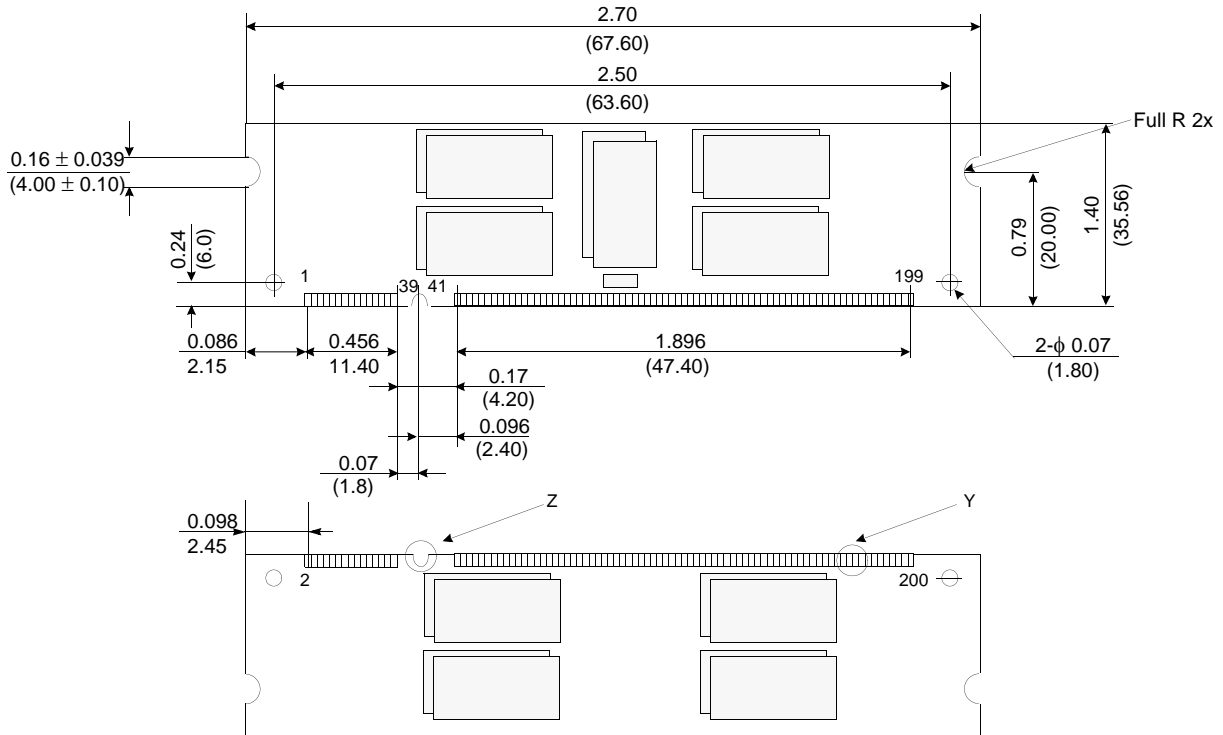
Tolerances : ±.006(.15) unless otherwise specified
 The used device is 64Mx8 DDR SDRAM, TSOPII
 DDR SDRAM Part No. : K4H510838B-T***

256MB, 512MB, 1GB Unbuffered SODIMM

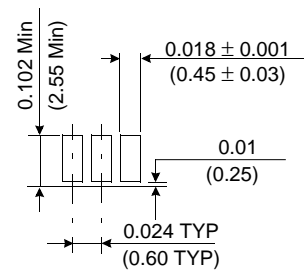
DDR SDRAM

Physical Dimensions : st.128M x72 (M485L2829BT0)

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : $\pm 0.006(.15)$ unless otherwise specified
 The used device is stacked 128Mx8 DDR SDRAM, TSOPII
 DDR SDRAM Part No. : K4H1G0738B-T***