

300 kHz N-Channel FET Synchronous PWM Buck Controller

DESCRIPTION

SiP12205 is a synchronous step down controller designed for use in DC-to-DC converter circuits requiring output currents as high as 10 Amperes. SiP12205 is designed to require a minimum number of external components, simplifying design and layout. It accepts input voltages from 5.5 V to 26.0 V, providing an adjustable output with voltage ranging from 0.6 V to 20 V. SiP12205 uses two N-Channel switching MOSFETs architecture to eliminate the expensive high power P-Channel MOSFET.

SiP12205 features a combination of frequency compensation and shutdown pin. The featured protections include under-voltage lockout, converter output short circuit protection, converter output over-voltage protection and thermal shutdown. SiP12205 senses the current of low-side MOSFET for converter output short circuit protection to eliminate the need of additional current sense resistor.

SiP12205 is available in a lead (Pb)-free MLP33-10 PowerPAK package and is specified to operate over the range of - 40 °C to 85 °C.

FEATURES

- 5.5 V to 26.0 V Wide Input Voltage Range
- Adjustable Output Voltage - 0.6 V to 20 V
- Optimized for 1.8 V and 10 A Output
- High Efficiency up to 93 %
- Drive N-Channel External Switching MOSFETs
- Constant 300 kHz Frequency Operation
- Internal Staircase Soft-Start
- Combination of Shutdown and Compensation Pin
- Output Short Circuit Protection
- No External Sense Resistor Required
- Minimum External Components
- Compact MLP33-10 PowerPAK® Package



RoHS
COMPLIANT

APPLICATIONS

- Distributed Power
- Desktop and Notebook Computers
- Battery Operated Equipment
- Point of Load Regulation
- DSP Cores
- Automotive Entertainment

Datasheet.Directory

TYPICAL APPLICATION CIRCUIT

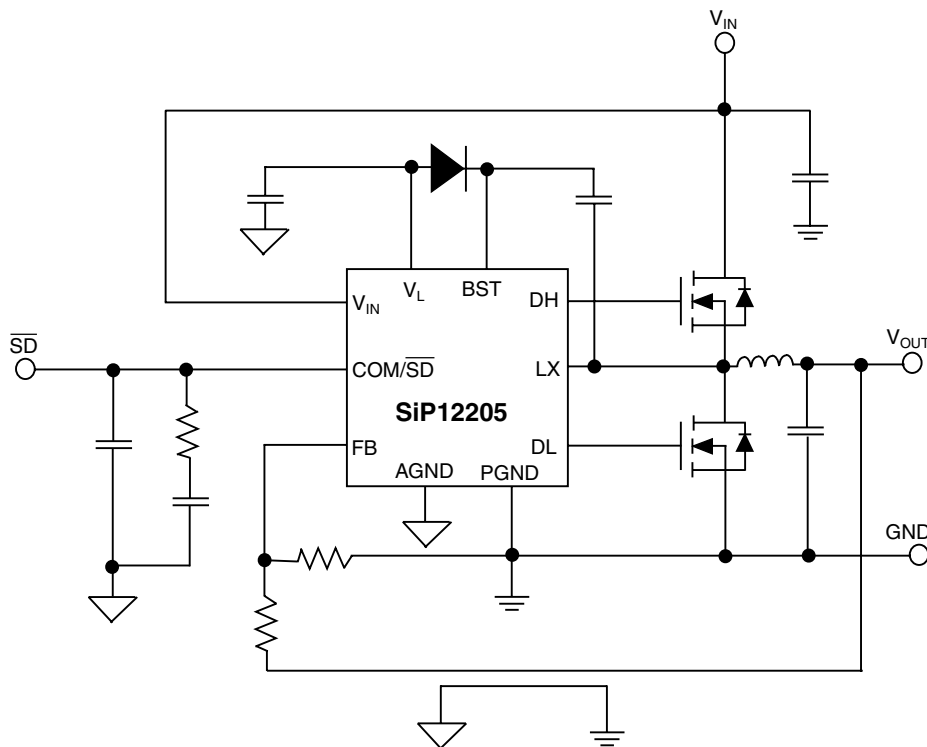


Figure 1.



ABSOLUTE MAXIMUM RATINGS		
Parameter	Limit	Unit
V_{IN} , LX to GND	29	V
BST to LX	6	
FB, COMP/ \overline{SD} to GND	- 0.3 to 6	
Power Dissipation ^{a, b}	1100	mW
Maximum Junction Temperature	125	°C
Storage Temperature	- 55 to + 150	

Notes:

a. Device mounted with all leads soldered or welded to PC board

b. Derate 20 mW/°C above + 70 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE		
Parameter	Limit	Unit
Input Voltage Range	5.5 to 26.0	V
Output Voltage Adjustment Range	0.6 to 20	
Operating Temperature Range	- 40 to + 85	°C

SPECIFICATIONS ^a						
Parameter	Symbol	Test Condition Unless Specified $V_{IN} = 5.5 \text{ V to } 26 \text{ V}$	Limits - 40 to 85 °C			Unit
			Min ^a	Typ ^b	Max ^a	
Controller						
Input Voltage	V_{IN}		5.5		26.0	V
Quiescent Current		Non switching		850	1250	μA
Internal Supply Voltage	V_L		4.8		5.5	V
Oscillator Frequency	f_{OSC}		240	300	360	kHz
Oscillator Ramp Amplitude	ΔV_{OSC}			1		V
Maximum Duty Cycle	DC		85	91		%
Feedback Voltage	V_{FB}	$T_A = 25 \text{ °C}$	0.591	0.600	0.609	V
			0.585		0.615	
FB Input Bias Current	I_{FB}				100	nA
Transconductance	GM			1		mA/V
Soft-Start				8		ms
Inputs and Outputs						
\overline{SD} Input Voltage	V_{IL}				0.15	V
Shutdown Current	I_{SD}			120	225	μA
MOSFET Drivers						
Break-Before-Make Time	t_{BBM}			10		ns
Highside Driver						
Output Voltage	V_{DH}		4.5			V
On-Resistance	$R_{DS_{HH}}$	$V_{IN} = V_{BST} = V_{LX} = 4.5 \text{ V}$		1.4	2.0	Ω
	$R_{DS_{HL}}$	$V_{IN} = V_{BST} = V_{LX} = 4.5 \text{ V}$		1.0	1.8	
Rise Time	t_{rH}	$V_{IN} = V_L = V_{BST} = 5 \text{ V}, C_L = 2.7 \text{ nF}$		10		ns
Fall Time	t_{fH}	$V_{IN} = V_L = V_{BST} = 5 \text{ V}, C_L = 2.7 \text{ nF}$		8		

SPECIFICATIONS ^a						
Parameter	Symbol	Test Condition Unless Specified $V_{IN} = 5.5\text{ V to }26\text{ V}$	Limits - 40 to 85 °C			Unit
			Min ^a	Typ ^b	Max ^a	
Lowside Driver						
Output Voltage	V_{DL}		4.5			V
On-Resistance	$R_{DS_{LH}}$	$V_{IN} = V_L = 4.5\text{ V}$		2.5	3.9	Ω
	$R_{DS_{LL}}$	$V_{IN} = V_L = 4.5\text{ V}$		0.85	1.4	
Rise Time	t_{rL}	$V_{IN} = V_L = 5\text{ V}, C_L = 2.7\text{ nF}$		18		ns
Fall Time	t_{fL}	$V_{IN} = V_L = 5\text{ V}, C_L = 2.7\text{ nF}$		8		
Protection						
Under Voltage Lockout	V_{UVLO}	Rising		3.6	3.9	V
UVLO-Hysteresis				0.180		
Thermal Shutdown Temperature		Rising		165		°C
Thermal Hysteresis				20		
Over Current Limit						
MOSFET On-Voltage Sense Threshold	V_{DL}		- 250	- 190	- 130	mV

Notes:

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

PIN CONFIGURATION

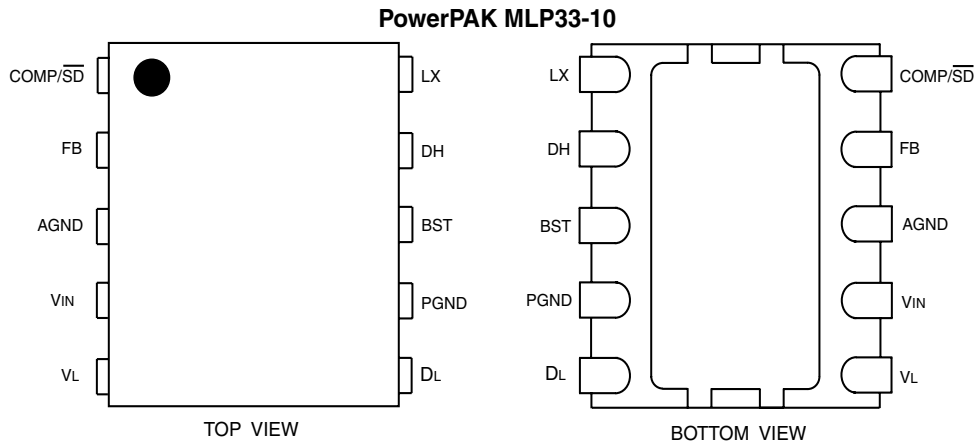


Figure 2.

PIN DESCRIPTION		
Pin Number	Name	Function
1	COMP/SD	Combination of Compensation and Shut Down Pin
2	FB	Feedback Input
3	AGND	Analog Ground
4	V_{IN}	Input Voltage
5	V_L	Internal Supply Voltage
6	DL	Low-Side Gate Drive
7	PGND	Power Ground
8	BST	Connection for the Bootstrap Capacitor
9	DH	High-Side Gate Drive
10	LX	Connection for the Inductor Node
	PowerPAK	Thermal Pad, Connect to Analog Ground Only or Floating

ORDERING INFORMATION

Part Number	Temperature Range	Package
SiP12205DMP-T1-E3	- 40 to 85 °C	MLP33-10 PowerPAK
Eval Kit	Temperature Range	Board
SiP12205DB	- 40 to 85 °C	Surface Mount

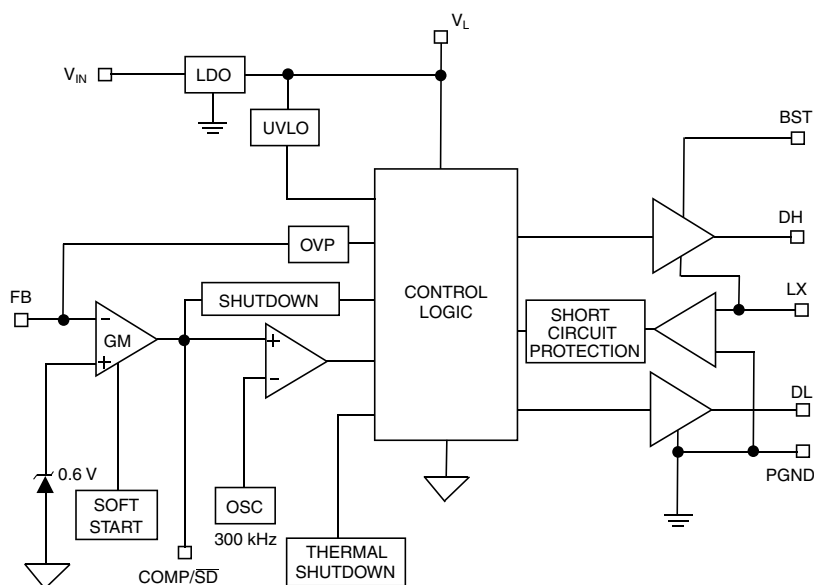
FUNCTIONAL BLOCK DIAGRAM


Figure 3.

DETAILED OPERATIONAL DESCRIPTION
Enable/ON State:

The COMP/ $\overline{\text{SD}}$ pin has 10 μA pull-up current to ensure auto start-up as soon as the pin is released by the external pull-down MOS. When the internal reference is ready, a current clamp at COMP/ $\overline{\text{SD}}$ is activated to ensure the COMP/ $\overline{\text{SD}}$ pin will not go below 600 mV due to the amplifier excursion or noise. The COMP/ $\overline{\text{SD}}$ has to go above 600 mV to enable the SiP12205 fully.

Disable/Shutdown/Off State:

To disable SiP12205, the COMP/ $\overline{\text{SD}}$ pin has to go below 150 mV typically and the external pull-down MOSFET has to be able to sink at least 250 μA . Once the pin reaches a voltage below the 150 mV, SiP12205 will go into shutdown mode with only essential circuitry active and the current bias of the SiP12205 will be reduced to 120 μA typically. Both high-side and low-side gate drivers are off.

UVLO:

SiP12205 enters into under-voltage lockout when V_L is below 3.4 V typical. Both high-side and low-side gate drivers will be turned off. SiP12205 will go out of UVLO mode when V_L is above 3.6 V typical.

Soft Start:

Once SiP12205 is out of shutdown and UVLO mode, the soft-start is initiated. The soft-start is accomplished by ramping up the internal reference voltage. During soft-start mode, SiP12205 cannot enter into fault mode. If there is an over current condition (current limit condition), the high-side gate driver will be turned off and the low-side gate driver will be turned on. Once the soft-start timing elapses, SiP12205 enters into a normal state of operation.

Output Over Voltage State:

When the output voltage goes above 1.083 times normal output voltage, the over-voltage protection circuit will act as a high speed clamp to turn off the high-side gate driver and turn on the low-side gate driver. The condition will persist until the output voltage drops below the trigger voltage minus a hysteresis.

Output Over Current State:

SiP12205 will enter a cycle-by-cycle over-current condition whenever the low-side MOSFET is turned on and the LX voltage falls 190 mV below power ground. If this condition remains for seven consecutive cycles, SiP12205 will go into a fault state. If the over-current condition is removed before seven consecutive cycles, SiP12205 will revert to normal operation mode.

Fault State:

SiP12205 can only enter fault mode after the soft-start mode has ended and seven consecutive over-current condition cycles has occurred. Once SiP12205 enters the fault mode with the high-side gate driver off and the low-side gate driver on, any occurring over-current condition will be ignored. The fault mode will last for seven soft-start cycles. After SiP12205 enter soft-start mode, SiP12205 will operate normally if the over-current condition is removed, otherwise the over-current sequence will be repeated. This fault scheme minimizes the thermal stress on the external power MOSFET switches.

Over Temperature Protection:

When the temperature of SiP12205 goes above 165 °C, SiP12205 enters into over-temperature shutdown. The high-side gate driver will be off and the low-side gate driver will be on. Once the temperature of SiP12205 drops below 145 °C, SiP12205 enters into the normal operation mode.

Duty-Factor Limitations for Low V_{OUT}/V_{IN} Ratios:

The SiP12205 output voltage is adjustable down to 0.6 V. However, the minimum duty factor may limit the ability to supply low voltage outputs from high voltage inputs. With high-input voltages, the required duty factor is approximately:

$$\left(\frac{V_{OUT} + R_{DS(ON)} \times I_{LOAD}}{V_{IN}} \right)$$

where $R_{DS(ON)} \times I_{LOAD}$ is the voltage drop across the synchronous rectifier. The SiP12205 minimum duty factor is 10 %, so the maximum input voltage ($V_{IN(MAX)}$) that can supply a given output voltage is:

$$V_{IN(MAX)} \leq 10 \times (V_{OUT} + R_{DS(ON)} \times I_{LOAD})$$

If the SiP12205 converter cannot attain the required duty factor dictated by the input and output voltages, the output voltage still remains in regulation. However, there may be intermittent or continuous half-frequency operations as the controller attempts to lower the average duty factor by deleting pulses. This can increase output voltage ripple and inductor current ripple, which increases noise and reduces efficiency. Furthermore, the stability of SiP12205 converter is not guaranteed.

Setting the Output Voltage:

Connecting FB pin to a resistive divider between output of the converter and GND can configure an output voltage between 0.6 V and 20 V. Select resistor R_2 in the range of 1 kΩ to 10 kΩ. R_1 is then given by:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where $V_{FB} = 0.6 \text{ V}$.

The maximum output voltage of SiP12205 converter is $0.9 \times V_{IN}$ if the input voltage of SiP12205 converter is in the range of 5.5 V to 6 V.

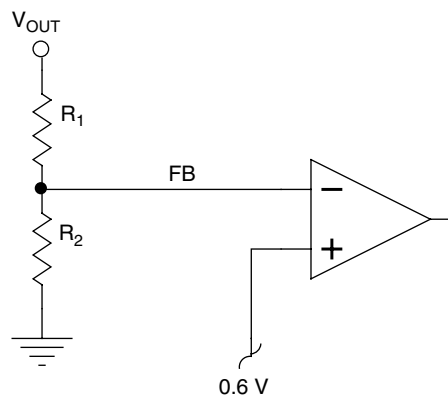
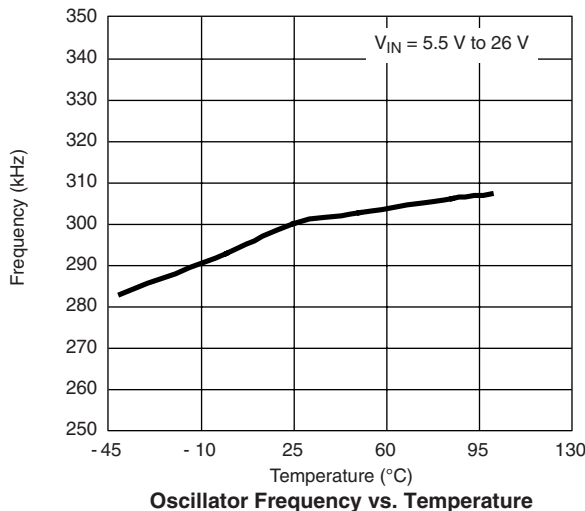
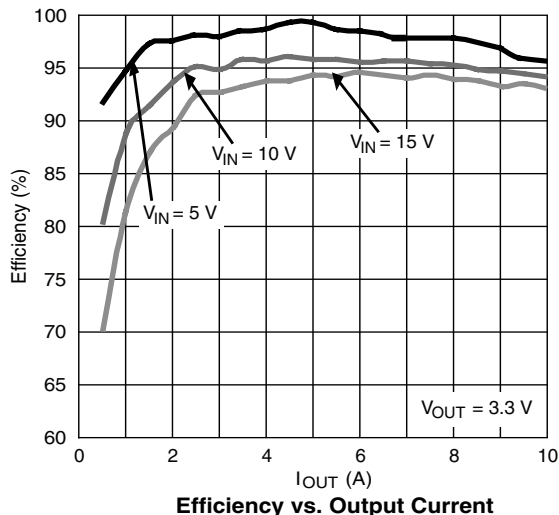


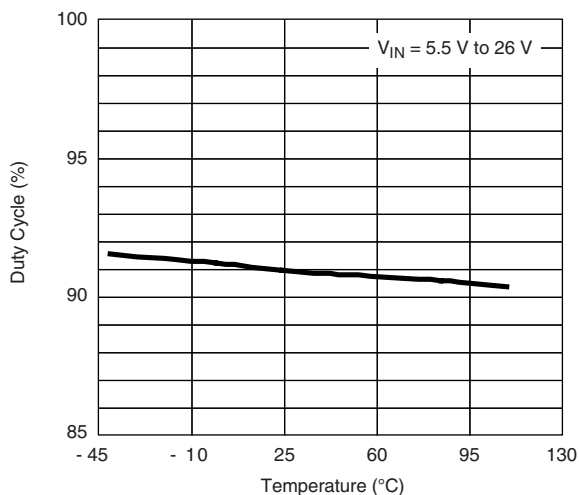
Figure 4.

TYPICAL CHARACTERISTICS

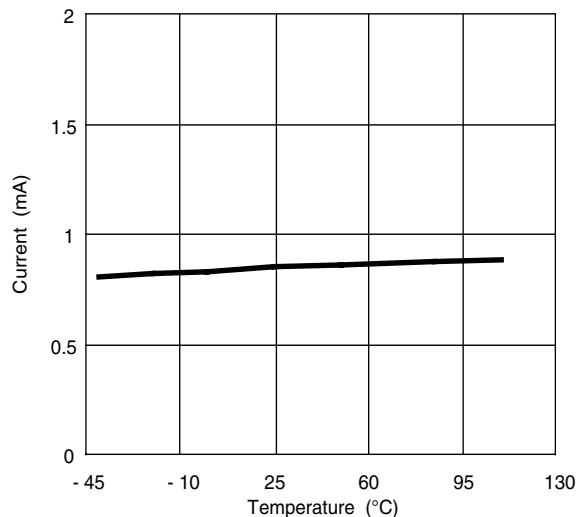




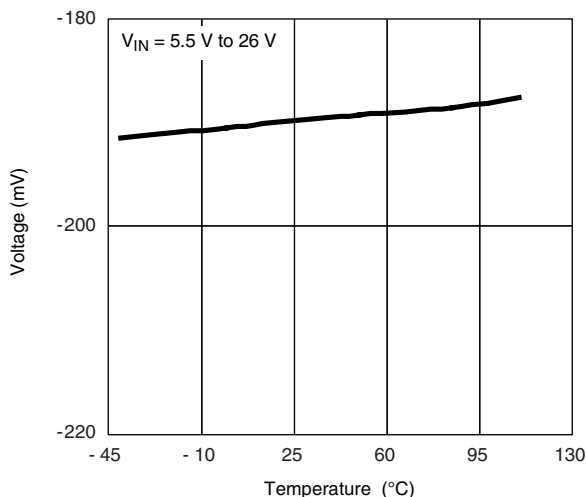
TYPICAL CHARACTERISTICS



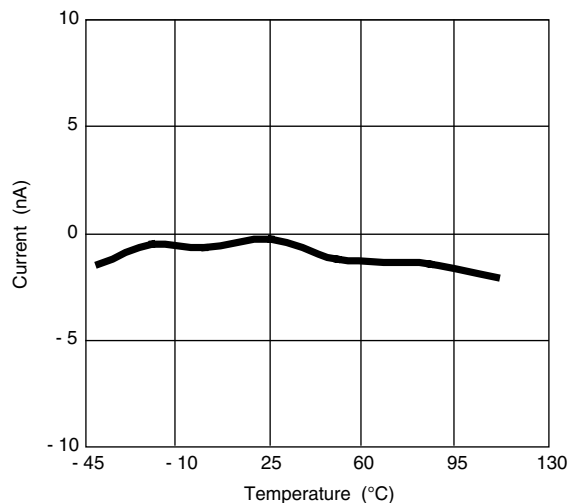
Maximum Duty Cycle vs. Temperature



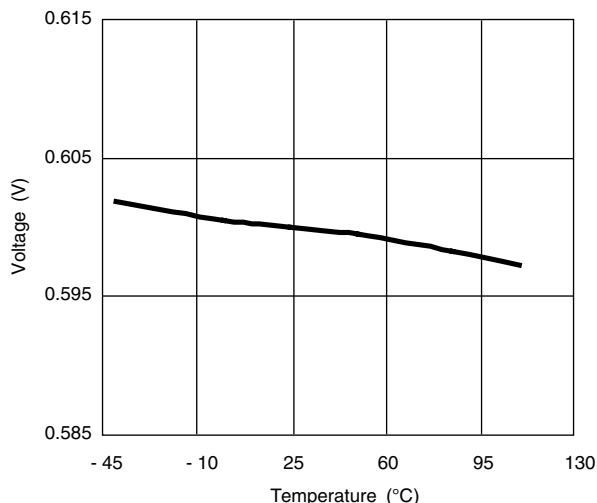
Quiescent Current vs. Temperature



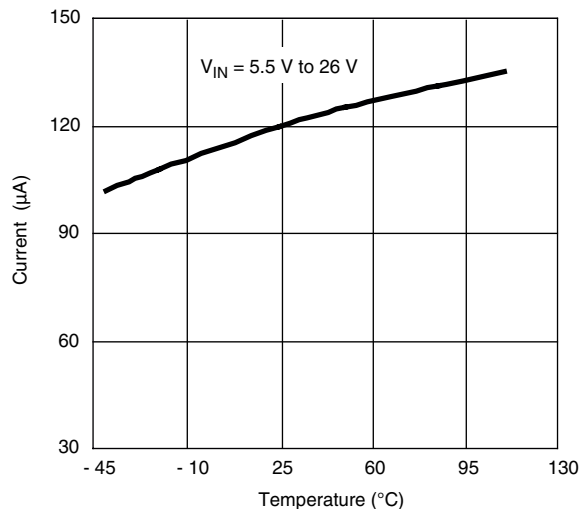
Current Sense Voltage vs. Temperature



FB Input Bias Current vs. Temperature



Feedback Reference Voltage vs. Temperature



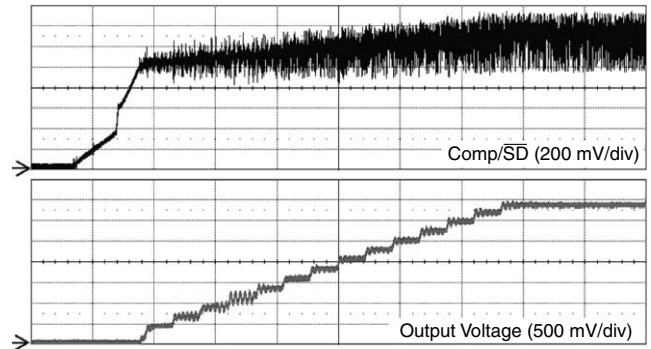
Shutdown Current vs. Temperature



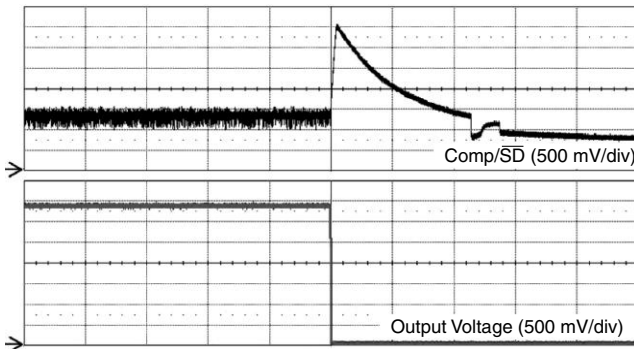
TYPICAL WAVEFORMS



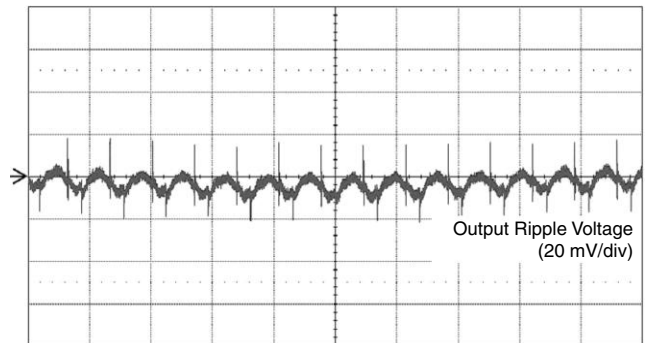
2 μ s/div
 $V_{IN} = 12$ V, $V_{OUT} = 3.3$ V, Load Current = 10 A, $L = 2.2$ μ H,
 $C_{OUT} = 100$ μ F x 3
Typical Switching Waveform



2 ms/div
 $V_{IN} = 12$ V, $V_{OUT} = 3.3$ V, Load Current = 10 A, $L = 2.2$ μ H,
 $C_{OUT} = 100$ μ F x 3
Typical Soft Start Waveform



100 ms/div
 $V_{IN} = 12$ V, $V_{OUT} = 3.3$ V, Load Current = 10 A, $L = 2.2$ μ H,
 $C_{OUT} = 100$ μ F x 3
Typical Input Power Shut Down Waveform



5 μ s/div
 $V_{IN} = 12$ V, $V_{OUT} = 3.3$ V, Load Current = 10 A, $L = 2.2$ μ H,
 $C_{OUT} = 100$ μ F x 3
Typical Output Ripple Voltage Waveform

APPLICATION NOTES

Inductor Selection:

An inductor is one of the energy storage component in a converter. Choosing an inductor means specifying its size, structure, material, inductance, saturation level, DC-resistance (DCR), and core loss. Fortunately, there are many inductor vendors that offer wide selections with ample specifications and test data, such as Vishay Dale.

The following are some key parameters that users should focus on. In PWM mode, inductance has a direct impact on the ripple current. The peak-to-peak inductor ripple current can be calculated as

$$I_{P-P} = \frac{V_{OUT} (V_{IN} - V_{OUT})}{V_{IN} L f}$$

where f = Switching Frequency.

Higher inductance means lower ripple current, lower RMS current, lower voltage ripple on both input and output, and higher efficiency, unless the resistive loss of the inductor dominates the overall conduction loss. However, higher inductance also means a bigger inductor size and a slower response to transients. In PSM mode, inductance affects inductor peak current, and consequently impacts the load capability and switching frequency. For fixed line and load conditions, higher inductance results in a lower peak current for each pulse, a lower load capability, and a higher switching frequency.

The saturation level is another important parameter in choosing inductors. Note that the saturation levels specified in data sheets are maximum currents. For a DC-to-DC converter operating in PWM mode, it is the maximum peak inductor current that is relevant, and which can be calculated using these equations:

$$I_{PK} = I_{OUT} + \frac{I_{P-P}}{2}$$

This peak current varies with inductance tolerance and other errors, and the rated saturation level varies over temperature. So a sufficient design margin is required when choosing current ratings.

A high-frequency core material, such as ferrite, should be chosen, the core loss could lead to serious efficiency penalties. The DCR should be kept as low as possible to reduce conduction losses.

Input Capacitor Selection:

To minimize current pulse induced ripple caused by the step-down controller and interference of large voltage spikes from other circuits, a low-ESR input capacitor is required to filter the input voltage. The input capacitor should be rated for the maximum RMS input current:

$$I_{RMS} = I_{LOAD(max)} \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

It is common practice to rate for the worst-case RMS ripple that occurs when the duty cycle is at 50 %:

$$I_{RMS} = \frac{I_{LOAD(max)}}{2}$$

Output Capacitor Selection:

The selection of the output capacitor is primarily determined by the ESR required to minimize voltage ripple and current ripple. The desired output ripple ΔV_{OUT} can be calculated by:

$$\Delta V_{OUT} = (I_{max} - I_{min}) \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Current ripple can be calculated by:

$$(I_{max} - I_{min}) = \frac{T}{L} \frac{V_{OUT}}{V_{IN}} (V_{IN} - V_{OUT})$$

Where: ΔV_{OUT} = Desired Output Ripple Voltage

f = Switching Frequency

I_{max} = Maximum Inductor Current

I_{min} = Minimum Inductor Current

T = Switching Period

Multiple capacitors placed in parallel may be needed to meet the ESR requirements. However if the ESR is too low it can cause instability problems.

MOSFET Selection:

The key selection criteria for the MOSFETs include maximum specifications for on-resistance, drain-source voltage, gate source, current, and total gate charge Q_g . While the voltage ratings are fairly straightforward, it is important to carefully balance on-resistance and gate charge. In typical MOSFETs, the lower the on-resistance, the higher the gate charge. The power loss of a MOSFET consists of conduction, gate charge, and crossover losses. For lower-current applications, gate charge losses become a significant factor, so low gate charge MOSFETs, such as Vishay Siliconix's LITTLE FOOT family of PWM-optimized devices, are desirable.

Frequency Compensation:

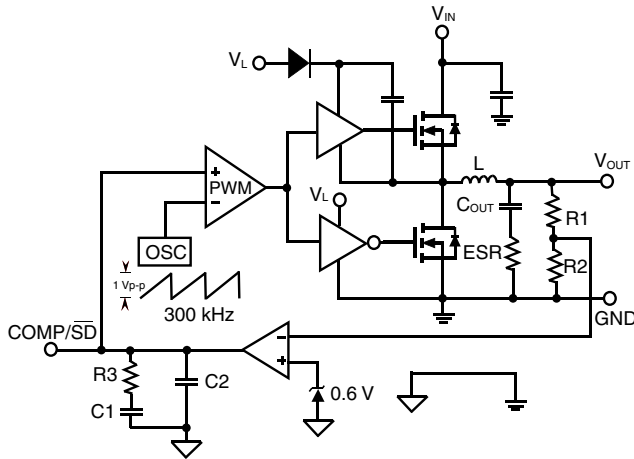


Figure 5.

The SiP12205 uses voltage mode control in conjunction with a high frequency transconductance error amplifier. The voltage feedback loop is compensated at the COMP/SD pin, which is the output node of the error amplifier. The feedback loop is generally compensated with an one pole, one zero network from comp to GND. Loop stability is affected by the values of the inductor, the output capacitor, the output capacitor ESR, and the error amplifier compensation network. The simplified schematics is shown in Figure 5.

The ideal Bode plot for a compensated system would be gain that rolls off at a slope of - 20 dB/decade, crossing 0 dB at the desired bandwidth. The phase margin should be greater than 40° for all frequencies at the 0 dB crossing.

The compensation network used with the error amplifier must provide enough phase margin at the 0 dB crossover frequency for the overall close-loop feedback system to be stable.

The major design objectives for the compensation network are the following:

1. Increase the low frequency loop gain to eliminate the output voltage steady state error.
2. Limit the loop bandwidth to eliminate the output high frequency ripple voltage and noise.
3. Introduce a phase boost in the crossover frequency to increase the phase margin to improve the stability.

To achieve the design objective above, the following design principles are need to applied.

1. The crossover frequency must be less than half of the switching frequency to ensure the stability. The typical cross frequency is about one-fifth of the switching frequency.
2. The crossover frequency should be high enough to make sure the converter respond fast enough to transient line/load condition.
3. The gain of the loop must cross the crossover frequency with - 20 dB and at least 6 dB gain phase.

4. The phase boost must be introduced to increase the phase margin.
5. The low frequency zero is typically placed at the one-tenth of the crossover frequency.
6. The high frequency pole is typically placed at 10 times of the crossover frequency.

The following guidelines will calculate the compensation pole and zero to stabilize the SiP12205.

1. Determine the double pole and zero for the output power filter. The inductor and output capacitor values are usually determined by efficiency, voltage and current ripple requirements. The inductor and the output capacitor create a double pole at the frequency, which will introduce the - 40 dB/decade slop and - 180° phase.

$$f_p(LC_{OUT}) = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

The ESR of the output capacitor and the output capacitor value form a zero at the frequency.

$$f_z(ESR) = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The power filter circuit and related Bode Plot is illustrated in Figure 6a and Figure 6b.

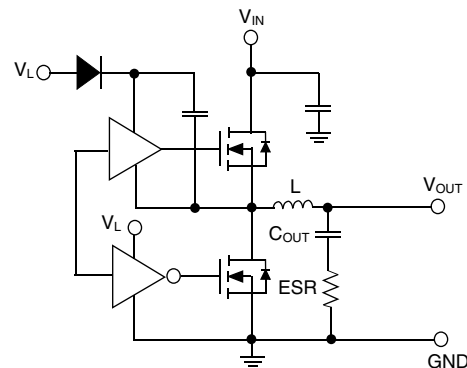


Figure 6a.

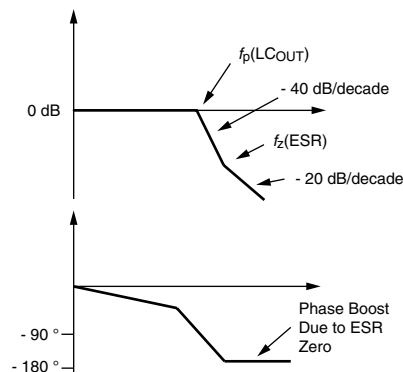


Figure 6b.

SiP12205

Vishay Siliconix



The Bode Plot above is just for the LC filter of the buck converter only. Due to the reason of LC filter is just passive components. The Bode Plot shows the gain of the LC filter is 0 dB. - 40 dB/decade roll off cause the phase approach - 180°.

The simplified transfer function is following:

$$G_{\text{filter}} = \frac{1 + s \times \text{ESR} \times C_{\text{OUT}}}{1 + s^2 \times L \times C_{\text{OUT}}} = \frac{s + \frac{1}{\text{ESR} \times C_{\text{OUT}}}}{\left(s - j \times \frac{1}{\sqrt{L \times C_{\text{OUT}}}}\right) \times \left(s + j \times \frac{1}{\sqrt{L \times C_{\text{OUT}}}}\right)}$$

This transfer function can be used to plot the Bode Plot of the power output filter. The pole and zero can be figured out from the pole/zero format of the transfer function.

2. Determine the attenuation caused by the output voltage-sampling divider.

The output voltage sampling divider resistors R_1 and R_2 contribute attenuation according to its sampling ratio

$$\frac{R_2}{R_1 + R_2}$$

The gain of the output voltage sampling divider is

$$20 \log \left(\frac{V_{\text{REF}}}{V_{\text{OUT}}} \right) \text{ dB.}$$

Because the output voltage is always greater than the reference voltage and the divider resistor is passive component, the gain value is negative value. After modification by the output voltage sampling resistor divider, the Bode Plot of LC filter and resistor divider is illustrated in Figure 7b and the open loop circuit is shown in Figure 7a.

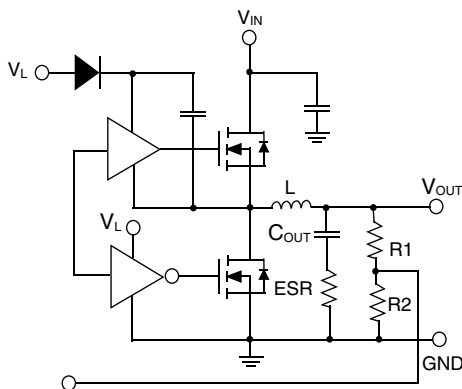


Figure 7a.

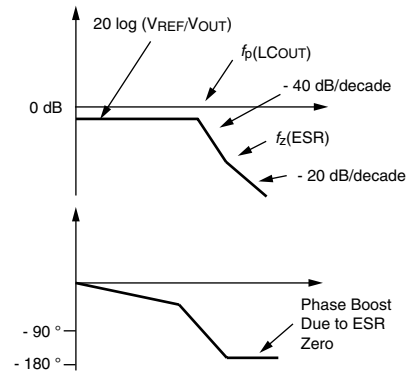


Figure 7b.

The transfer function of the combination is shown as following:

$$G_{\text{filter}} \times G_{\text{divider}} = \frac{V_{\text{REF}}}{V_{\text{OUT}}} \times \frac{1 + s \times \text{ESR} \times C_{\text{OUT}}}{1 + s^2 \times L \times C_{\text{OUT}}} = \frac{V_{\text{REF}}}{V_{\text{OUT}}} \times \frac{s + \frac{1}{\text{ESR} \times C_{\text{OUT}}}}{\left(s - j \times \frac{1}{\sqrt{L \times C_{\text{OUT}}}}\right) \times \left(s + j \times \frac{1}{\sqrt{L \times C_{\text{OUT}}}}\right)}$$

3. Determine the gain of the SiP12205 and the crossover frequency. The crossover frequency is typically one-fifth of the switching frequency. The switching frequency of SiP12205 is 300 kHz. The crossover frequency is about 60 kHz or less. So the gain of the SiP12205 should shape the gain of the Bode Plot, which makes the gain of the plot cross over the 0 dB at 60 kHz. The gain of SiP12205 is the combination of the gain of error amplifier and PWM.

The gain of PWM is calculated as following:

$$A_{\text{PWM}} = 20 \log \left(\frac{V_{\text{INPUT}}}{V_{\text{P-P}}} \right)$$

Where:

V_{INPUT} is the input voltage of the SiP12205 buckconverter.
 $V_{\text{P-P}}$ is the peak-to-peak value of the oscillator output.

The gain of the error amplifier can be calculated as following:

$$\text{GM} \times R_3 = 10 \frac{A_{\text{EA}}}{20}$$

or

$$A_{\text{EA}} = 20 \log (\text{GM} \times R_3)$$

Where:

A_{EA} is absolute value of the open loop gain of the output LC filter and output voltage sampling resistor divider at crossover frequency. GM is the tranconductance of the error amplifier.

The total gain of SiP12205 can be figured out as following:

$$A_{\text{SiP12205}} = A_{\text{EA}} + A_{\text{PWM}}$$

A_{SiP12205} is the required gain to shift the gain of plot up to cross over 0 dB at 60 kHz or the desired crossover frequency. The value of R_3 can be figured out by the formula above.

The required gain $A_{SiP12205}$ to move the gain of Bode Plot up to meet the desired crossover frequency can be figured out by substituting the desired cross over frequency into the following formula, which is also the absolute value of $G_{filter} \times G_{divider}$ at the desired crossover frequency:

$$A_{SiP12205} = 20 \log (G_{filter} \times G_{divider}) = 20 \log \left(\frac{V_{REF}}{V_{OUT}} \times \frac{1 + 2\pi \times f_{crossover} \times ESR \times C_{OUT}}{1 + (2\pi \times f_{crossover})^2 \times L \times C_{OUT}} \right) =$$

$$20 \log \left(\frac{V_{REF}}{V_{OUT}} \times \frac{2\pi \times f_{crossover} + \frac{1}{ESR \times C_{OUT}}}{\left(2\pi \times f_{crossover} - j \times \frac{1}{\sqrt{L \times C_{OUT}}} \right) \times \left(2\pi \times f_{crossover} + j \times \frac{1}{\sqrt{L \times C_{OUT}}} \right)} \right)$$

4. Combine the SiP12205 controller with open loop of the LC filter + output voltage sampling divider. The open loop gain shift up due to the active device of SiP12205. The close loop system and its related Bode Plot are illustrated in Figure 8a and Figure 8b.

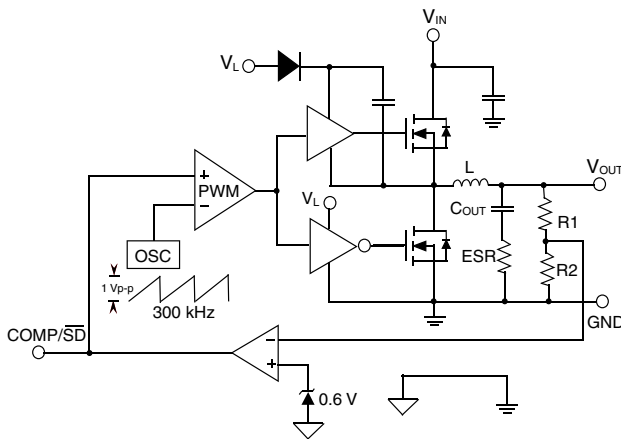


Figure 8a.

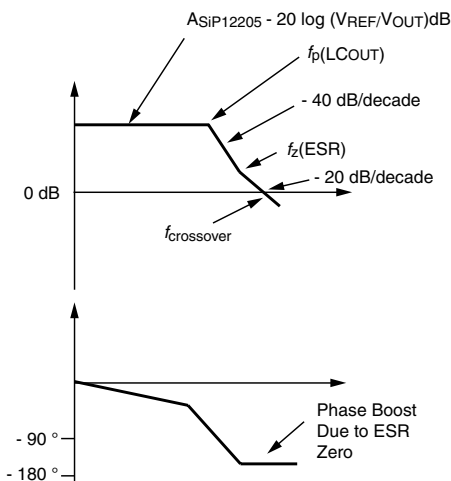


Figure 8b.

5. Introduce the low frequency zero to increase the low frequency gain and boost up the phase margin. Then introduce high frequency pole to eliminate the high frequency noise by limiting the bandwidth. The low frequency zero is typical placed at one-tenth of the crossover frequency and the high frequency pole is placed at 10 times of the crossover frequency.

$$f_z = \frac{1}{2\pi \times R_3 \times C_1} = \frac{f_{CROSSOVER}}{10}$$

$$f_p = \frac{1}{2\pi \times R_3 \times C_2} = 10 \times f_{CROSSOVER}$$

Where: $f_{crossover}$ is the crossover frequency at 0 dB.

The total phase introduce by the ESR zero, compensation zero and compensation pole is

$$\theta_{TOTAL} = 180^\circ + 90^\circ - \tan^{-1} \left(\frac{f_{crossover}}{f_z(ESR)} \right) - \tan^{-1} \left(\frac{f_{crossover}}{f_z} \right) + \tan^{-1} \left(\frac{f_{crossover}}{f_p} \right)$$

Where:

θ_{TOTAL} is the total phase in degree.

180° is the phase lag due to LC filter of the buck converter.
90° is the phase lag due to pole at the origin introduced by the compensation network.

The final close loop circuit is illustrated in Figure 5 after frequency compensation. The related Bode Plot is shown in Figure 9.

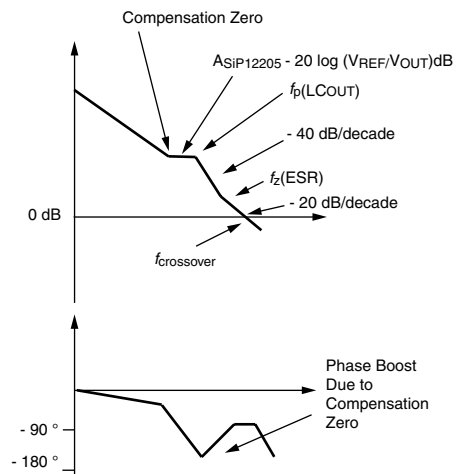


Figure 9.

Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations, all suggest a more practical empirical method.

This can be done by injecting at the load a variable frequency small signal voltage between the output and feedback network and using an RC network box to iterate toward the final values; or by obtaining the optimum loop response using a network analyzer to measure the loop gain and phase.

Layout Consideration:

As in the design of any switching DC-to-DC converter, driver careful layout will ensure that there is a successful transition from design to production.

One of the few drawbacks of switching DC-to-DC converters is the noise induced by their high frequency switching. Parasitic inductance and capacitance may become significant when a converter is switching at 300 kHz. However, noise levels can be minimized by properly laying out the components.

Here are some general guidelines for laying out a step-down converter with the SiP12205. Since power traces in step down converters carry pulsating current, energy stored in trace inductance during the pulse can cause high-frequency ringing with input and output capacitors. Minimizing the

length of the power traces will minimize the parasitic inductance in the trace. The same pulsating currents can cause voltage drops due to the trace resistance and cause effects such as ground bounce. Increasing the width of the power trace, which increases the cross sectional area, will minimize the trace resistance.

In all DC-to-DC converters the decoupling capacitors should be placed as close as possible to the pins being decoupled to reduce the noise. The connections to both terminals should be as short as possible with low-inductance (wide) traces. In the SiP12205 converters, the V_{IN} is decoupled to PGND. It may be necessary to decouple V_L to AGND, with the decoupling capacitor being placed adjacent to the pin. AGND and PGND traces should be isolated from each other and only connected at a single node such as a "star ground".

DEMO BOARD CIRCUIT WITH BILLS OF MATERIALS

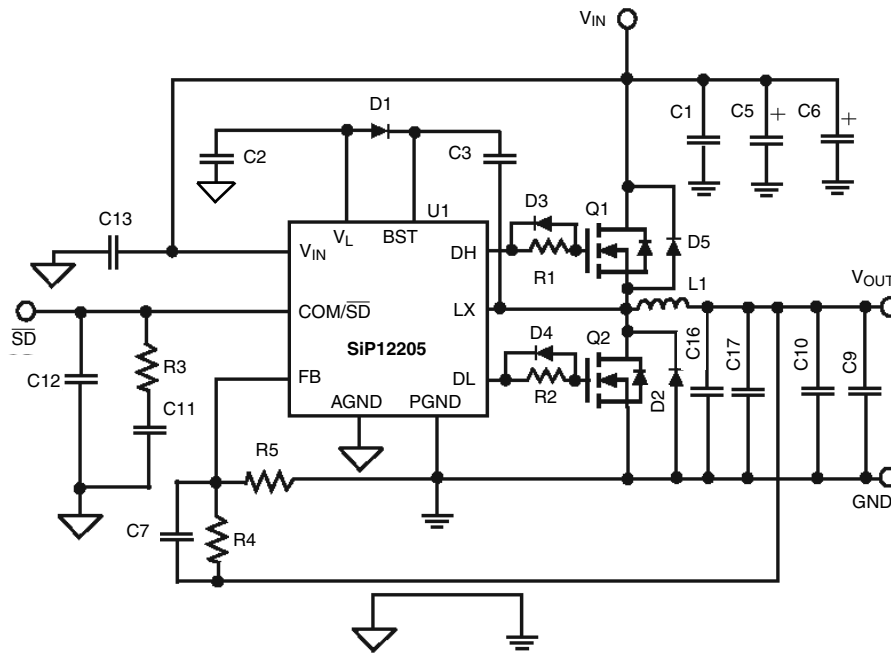
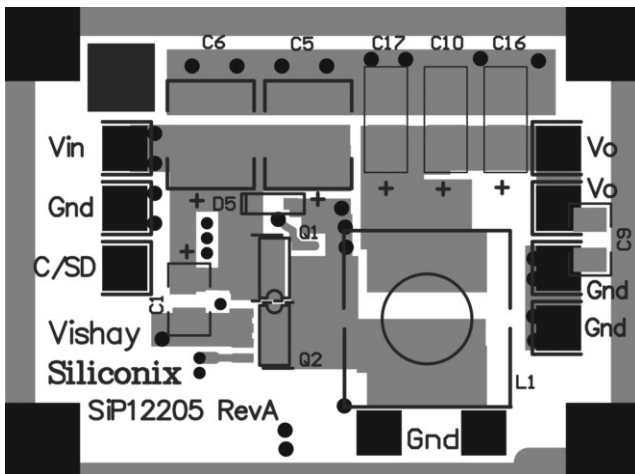


Figure 10.

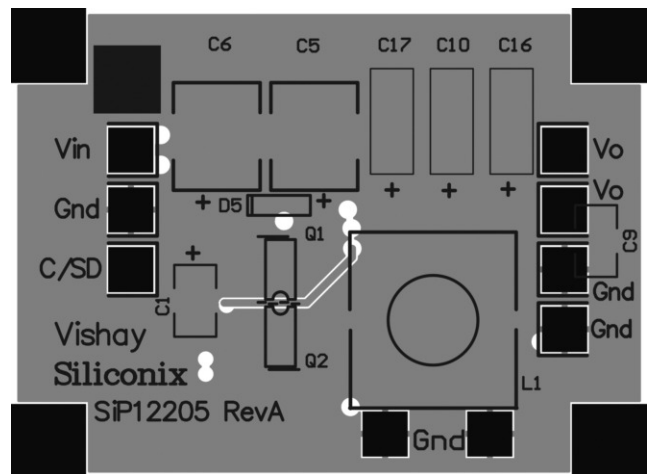
Item	Qty	Designator	Part Type	Description	Footprint	Manufacturer
1	1	R3	CRCW08056811RF	Resistor 1 % 6.81 k Ω	0805	VISHAY/ DALE
2	1	R4		Resistor 1 % 16.2 k Ω 2.5 V output Resistor 1 % 25.3 k Ω 3.3 V output Resistor 1 % 37.4 k Ω 5.0 V output	0805	MULTI-SOURCE
3	1	R5	CRCW08055111RF	Resistor 1 % 5.11 K Ω	0805	VISHAY/DALE
4	2	C1, C9	VJ1206V105MXAC	CAP, CER, 1 μ F 50 V 20 %	1206	VISHAY/VITRAMON
5	1	C2	VJ1206V105MXXC	CAP, CER, 1 μ F 25 V 20 %	1206	VISHAY/VITRAMON
6	1	C3	VJ0603Y104MXAC	CAP, CER, 0.1 μ F 50 V 20 %	0603	VISHAY/VITRAMON
7	1	C11	VJ0805Y153KXAC	CAP, CER, 15 nF 50 V 10 %	0805	VISHAY/VITRAMON
8	1	C12	VJ0805A4R7DXAC	CAP, CER, 4.7 pF 50 V 10 %	0805	VISHAY/VITRAMON
9	1	C7		CAP, CER, 560 pF 50 V 10 %	0805	MULTI-SOURCE
9	1	C13	VJ0805Y104MXAC	CAP, CER, 0.1 μ F 50 V 20 %	0805	VISHAY/VITRAMON
10	6	C5, C6	594D336X_035R2T	CAP, TAN, 33 μ F 35 V	595D_R	VISHAY/SPRAGUE

Item	Qty	Designator	Part Type	Description	Footprint	Manufacturer
11	3	C10, C16, C17		CAP, CERAMIC, 100 μ F 6.3 V	1812	MULTI-SOURCE
12	1	L1	IHLP5050CEER2R2M01	2.2 μ H Power Inductor	IHLP	VISHAY/DALE
13	1	D1	MBR0540T1	Schottky Diode 0.5 A 40 V	SOD-123	ON SEMICONDUCTOR
14	2	R1, R2		Resistor 1 % 0 Ω	0805	MULTI-SOURCE
15	1	Q2	Si7336ADP	N-FET 30 V 30 A	PowerPAK-SO8	VISHAY/SILICONIX
16	1	Q1	Si4336DY	N-FET 30 V 25 A	SO8	VISHAY/SILICONIX
17	1	U1	SiP12205DMP-T1-E3	POWER IC	MLP33-10 PowerPAK	VISHAY/SILICONIX
Other optional components - not required or inserted						
18	1	D2	SS36	Schottky Diode 3 A 60 V	SMC	VISHAY SEMICONDUCTOR
19	2	D3, D4, D5	MBR0540T1	Schottky Diode 0.5 A 40 V	SOD-123	ON SEMICONDUCTOR

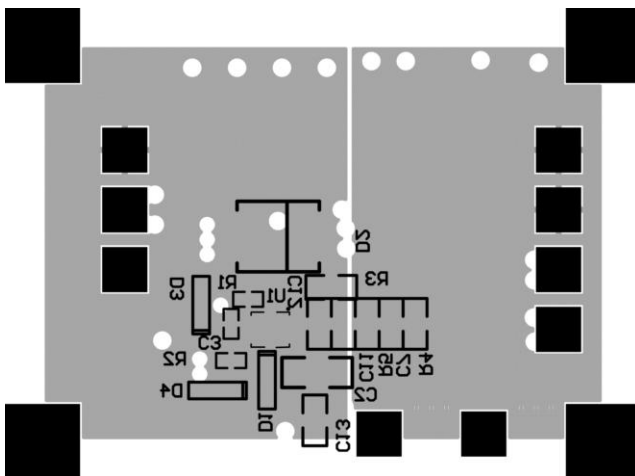
PCB LAYEROUT



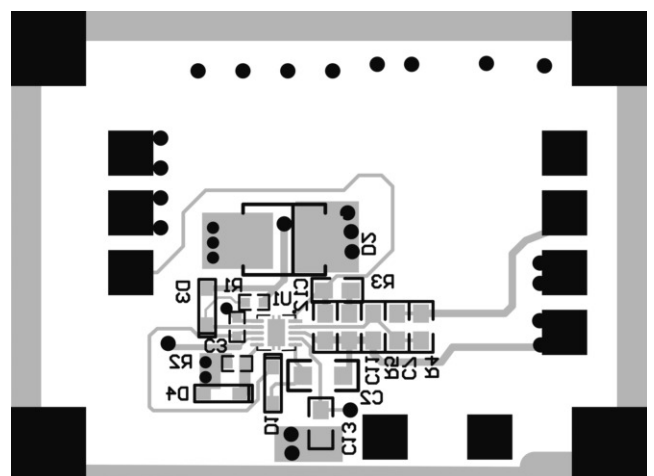
Top Power Layer



Mid-Power Ground Layer



Mid-Shielding Layer



Bottom Controller Layer

Figure 11.

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