

IMG5 20" REV F

11/01/05

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

			DESCRIPTION OF CHANGE	CK APPD	ENG APPD
REV	ZONE	ECN		DATE	DATE
F		408133	PRODUCTION RELEASED	11/01/05	?

D

D

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C

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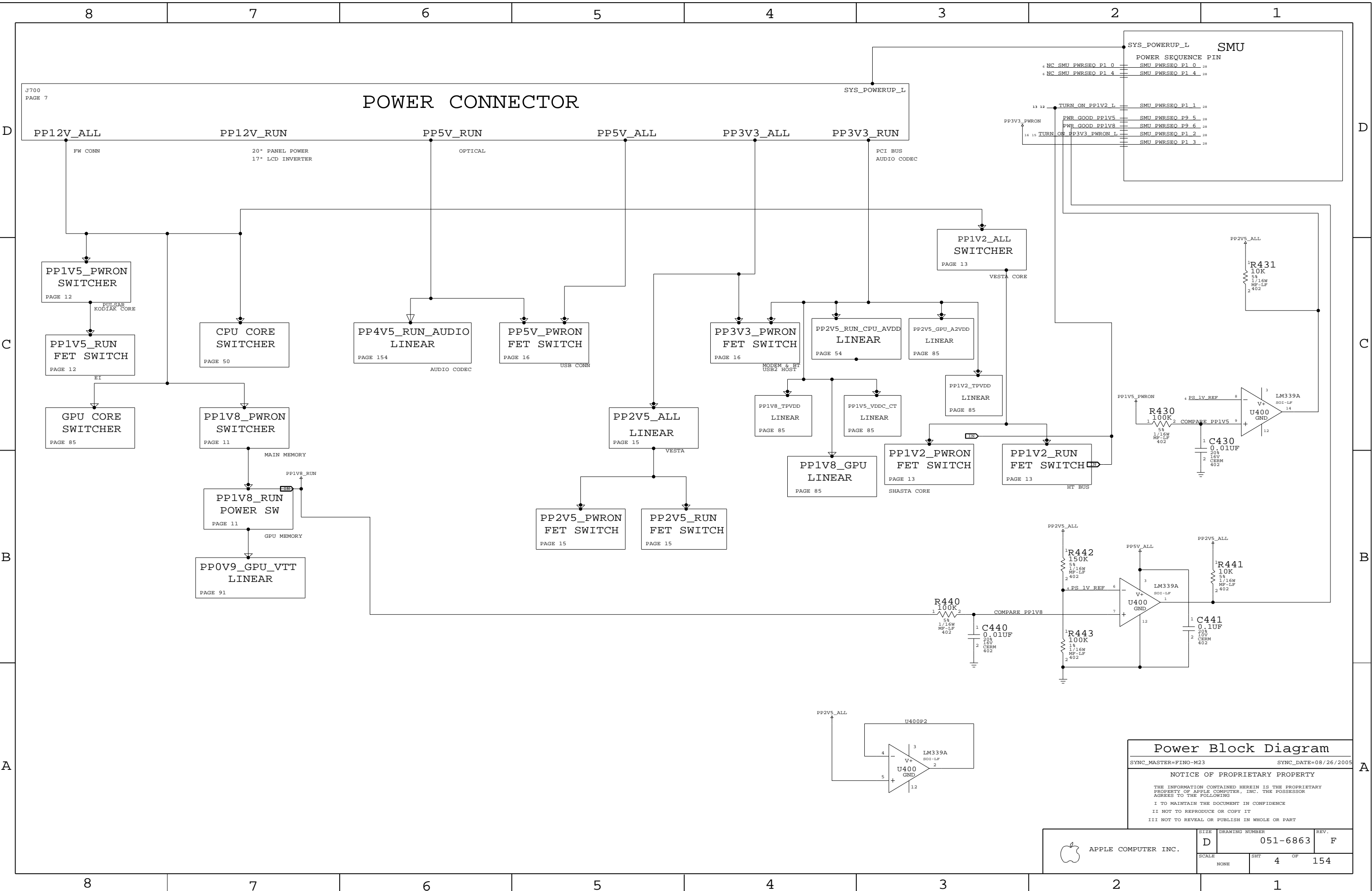
B

B

A

A

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX: _____</p> <p>X.XX: _____</p> <p>X.XXX: _____</p> <p>ANGLES: _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	<p>Apple Computer Inc.</p> <p style="font-size: x-small;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small;">II NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <p style="font-size: large; font-weight: bold;">SCH, MLB, IMG5, 20</p> <p style="font-size: x-small;">DRAWING NUMBER 051-6863 REV. F</p> <p style="font-size: x-small; text-align: right;">SHT 1 OF 154</p>
<p>DRAPTER</p> <p>ENG APPD</p> <p>QA APPD</p> <p>RELEASE</p> <p>MATERIAL/FINISH NOTED AS APPLICABLE</p>	<p>DESIGN CK</p> <p>MFG APPD</p> <p>DESIGNER</p> <p>SCALE</p> <p>SIZE D</p>	



Power Block Diagram
 SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT	4 OF	154
NONE			

8

7

6

5

4

3

2

1

PROCESSORS

NEED TO UPDATED BIN CODES AS NOTES

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION	
337S3224	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,1.9G,85C	1.9GHZ	1.10V	45W	50MV	U4300	17_INCH_LCD	CRITICAL
337S3220	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.1G,85C	2.1GHZ	1.10V	45W	50MV	U4300	20_INCH_LCD	CRITICAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3225	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.15V
337S3226	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.20V
337S3227	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.25V
337S3228	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.15V
337S3229	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.20V
337S3230	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.25V
337S3231	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.30V
337S3221	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.15V
337S3222	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.20V
337S3223	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
343S0379	1	IC,KODIAK,V1.2,PBGA,200MM	U1900		CRITICAL
343S0377	1	IC,ASIC,SHASTA,V1.1,PBGA,LF	U2300		CRITICAL
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U1701		CRITICAL
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500		CRITICAL

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
051-6790	1	PCB,SCHM,MLB,M23	SCH1	17_INCH_LCD	
051-6863	1	PCB,SCHM,MLB,M33	SCH1	20_INCH_LCD	
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD	CRITICAL
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD	CRITICAL
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VFP1		
825-6447	1	BARCODE LABEL, MLB	LBL1		
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500		CRITICAL
341T1752	1	PURCH ASSY, SMU BIG	U2800		CRITICAL
603-7318	1	M23 CPU HEATSINK	MECH1	OMIT	CRITICAL
603-7321	1	M33 CPU HEATSINK	MECH1	OMIT	CRITICAL
603-7319	1	M23 GPU HEATSINK	MECH2	OMIT	CRITICAL HEATSINKS ARE NOW ON THE PD BOM
603-7322	1	M33 GPU HEATSINK	MECH2	OMIT	CRITICAL
603-7320	1	M23 NB HEATSINK	MECH3	OMIT	CRITICAL
603-7323	1	M33 NB HEATSINK	MECH3	OMIT	CRITICAL
875-1905	1	CPU GAP FILLER	GAP1		
875-2429	1	LED COVER TAPE	TAPE1	17_INCH_LCD	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0140	378S0141		LED700,LED700	KINGBRIGHT LED
343S0388	343S0356		U1701	VESTA A4
126S0078	126S0086		C722	EL CAP
126S0068	126S0088		CF000	EL CAP
353S1321	353S1105		U400	LM339
138S0558	138S0547			10UF CAP ALL LOC.
124-0338	124-0333			PANASONIC CAPS

Table Items

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE	SHT	OF
NONE	5	154

8

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4

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2

1

D

C

B

A

D

C

B

A

NO TEST XW NETS

Table of test points for NO TEST XW NETS, columns 8 and 7.

Table of test points for NO TEST XW NETS, columns 6 and 5.

Table of test points for NO TEST XW NETS, columns 4 and 3.

EE IDENTIFIED NO TEST NETS

Table of test points for EE IDENTIFIED NO TEST NETS, columns 8 and 7.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 6 and 5.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 4 and 3.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 8 and 7.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 6 and 5.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 4 and 3.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 8 and 7.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 6 and 5.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 4 and 3.

Table of test points for FUNC TEST NETS, columns 4 and 3.

Table of test points for FUNC TEST NETS, columns 4 and 3.

Table of test points for FUNC TEST NETS, columns 4 and 3.

Table of test points for FUNC TEST NETS, columns 4 and 3.

Table of test points for FUNC TEST NETS, columns 4 and 3.

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE FOR PP3V3_ALL AND GND PLACE WITHIN 1 INCH OF EACH OTHER USE FAT TRACES

Table of test points for FUNC TEST NETS, columns 2 and 1.

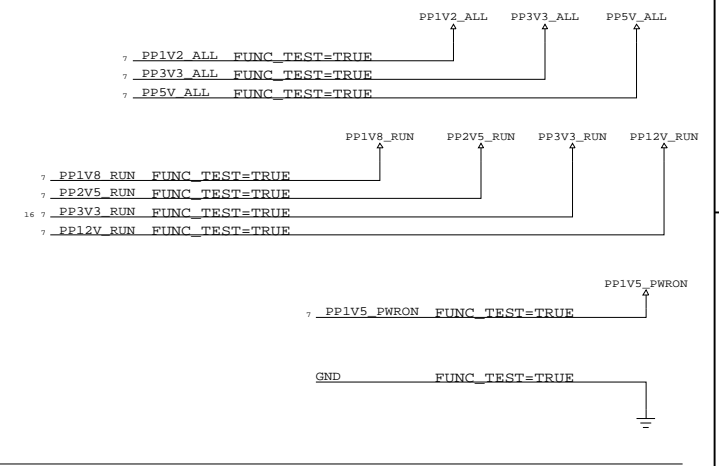
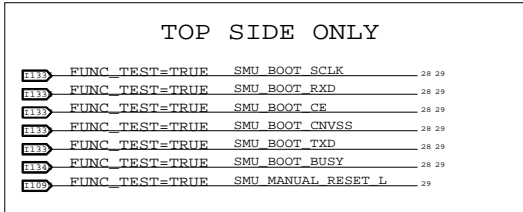


Table of test points for FUNC TEST NETS, columns 2 and 1.

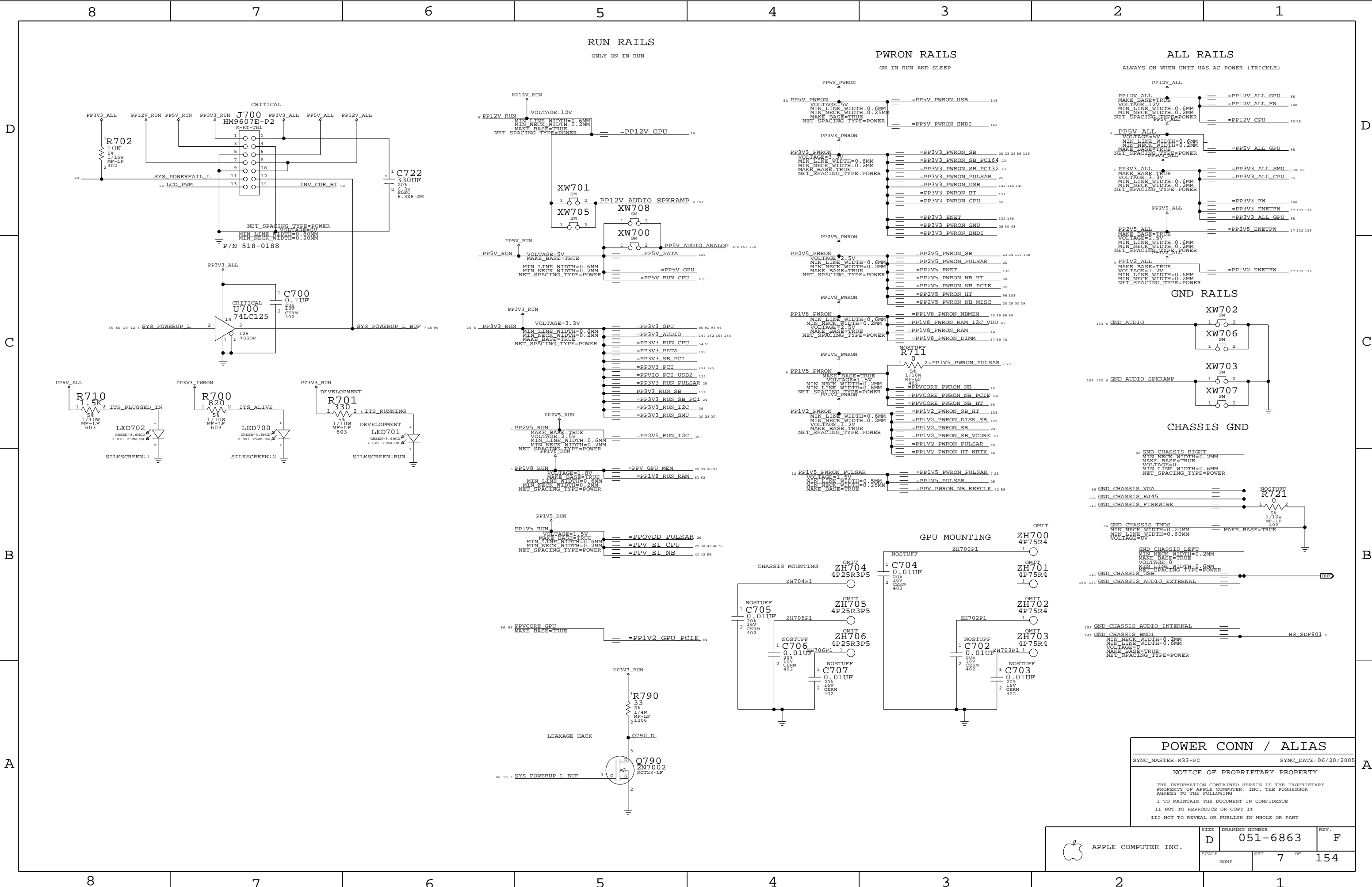
FUNC TEST 1 OF 2

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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POWER CONN / ALIAS

SYNC_MASTER=M33-PC SYNC_DATE=06/20/2005

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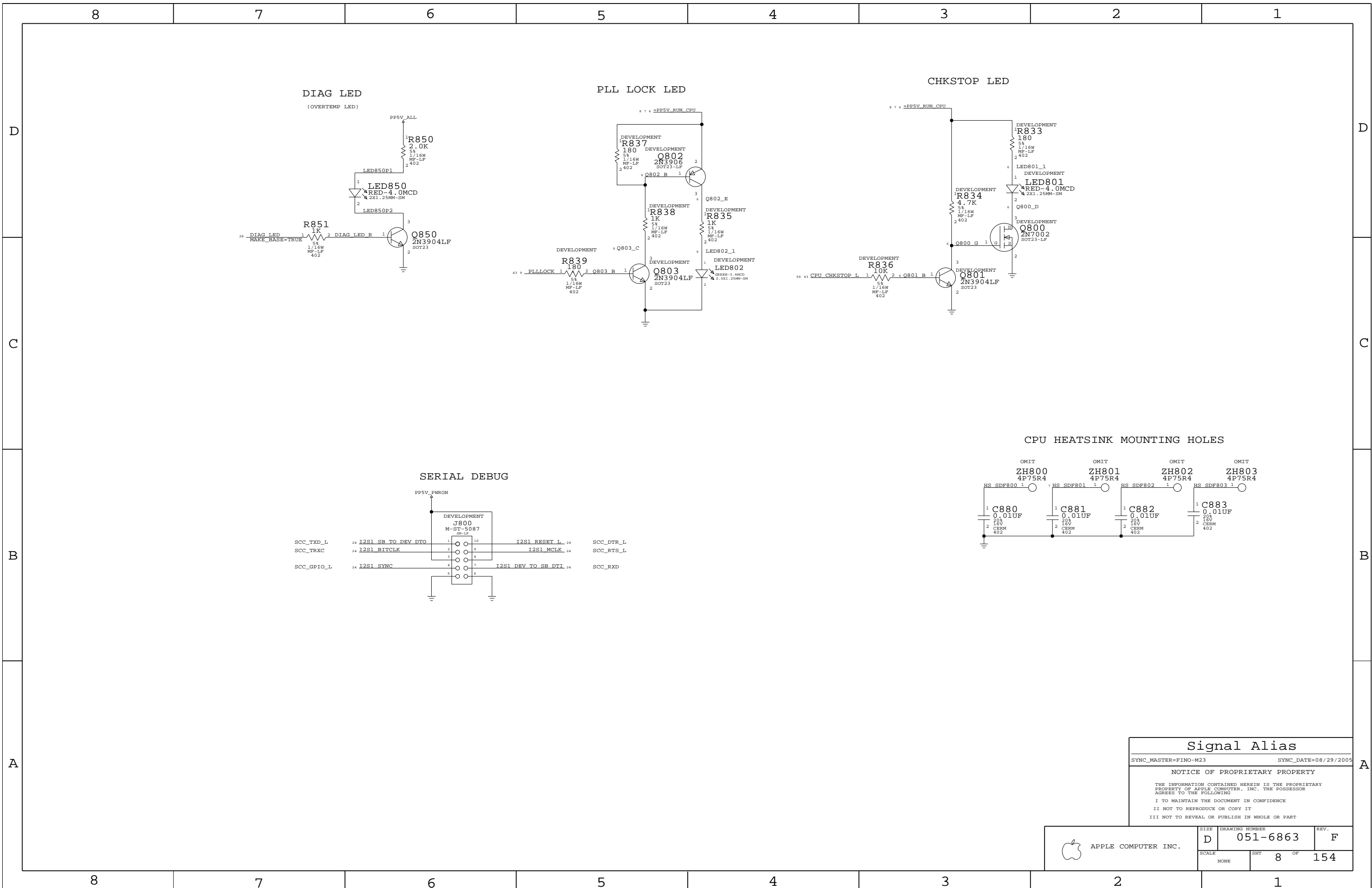
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	SCALE NONE	SHEET 7 OF 154	



Signal Alias

SYNC_MASTER=FINO-M23 SYNC_DATE=08/29/2005

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	SCALE NONE	SHT 8	OF 154

THE FOLLOWING NETS ARE USED ONLY WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

THE FOLLOWING NETS DO NOT HAVE TEST POINT BECAUSE OF ROUTING DENSITY AND SIGNAL INTEGRITY. TEST COVERAGE WILL BE BY FCT NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

Table of test points and nets for development BOM option, including items like ENET_TXD_R<7>, TP_VESTA_TVCO_24, TP_VESTA_TXC_RXC_DELAY, etc.

Table of test points and nets for routing density and signal integrity, including items like Q803_C, PLLLOCK, LED_PPIV8_RUN_P, etc.

THE FOLLOWING PULSAR NETS WILL BE TESTED VIA TEST JET... ADDING NO_TEST TO ALL PCIE NETS TO AVOID STUBS WILL GET COVERAGE IN FCT WITH A DIAG THAT CHECKS THAT THE BUS IS 16 LANES WIDE

JTAG TEST POINTS NEED TO BE ON THE BOTTOM OF THE BOARD ADDING FUNC_TEST=TRUE TO THESE NETS

Table of JTAG test points and nets, including items like TP_JTAG_SB_TCK, TP_JTAG_SB_TDI, TP_JTAG_SB_TDO, etc.

Table of JTAG test points and nets, including items like JTAG_CPU_TCK, JTAG_CPU_TDI, JTAG_CPU_TDO, etc.

FUNC TEST 2 OF 2

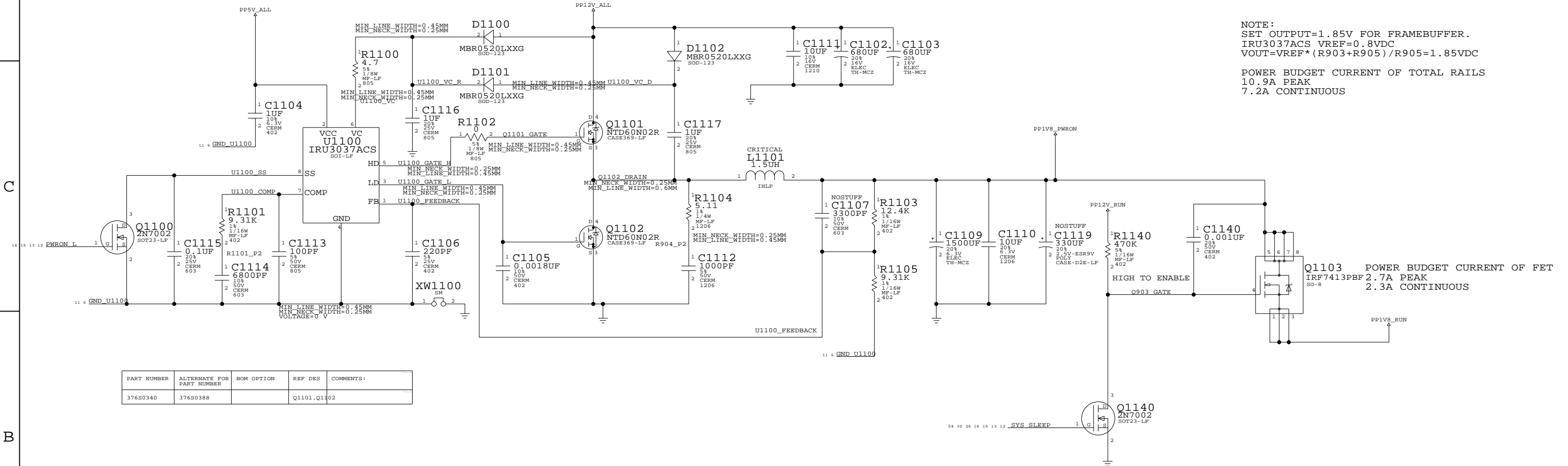
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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Apple Computer Inc. logo and drawing information: DRAWING NUMBER 051-6863, SCALE NONE, SHEET 9 OF 154, REV. F

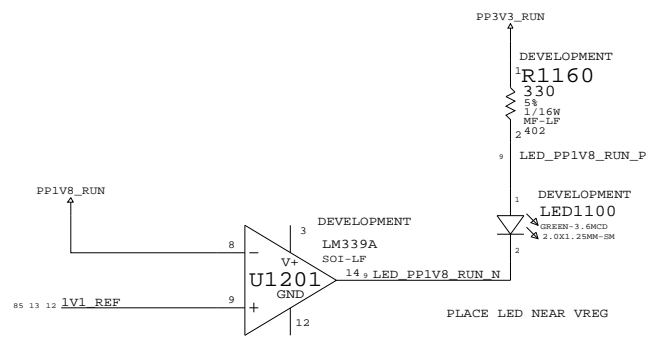
1.8V VOLTAGE REGULATOR



NOTE:
 SET OUTPUT=1.85V FOR FRAMEBUFFER.
 IRU3037ACS VREF=0.8VDC
 $V_{OUT}=V_{REF} * (R_{903}+R_{905})/R_{905}=1.85VDC$
 POWER BUDGET CURRENT OF TOTAL RAILS
 10.9A PEAK
 7.2A CONTINUOUS

POWER BUDGET CURRENT OF FET
 IRF7413PBF 2.7A PEAK
 2.3A CONTINUOUS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1101, Q1102	



1.8V VREG
 SYNC_MASTER=M33-PC SYNC_DATE=06/20/2005
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SCALE	SHT	11 OF	154
NONE			

KODIAK CORE VOLTAGE REGULATOR

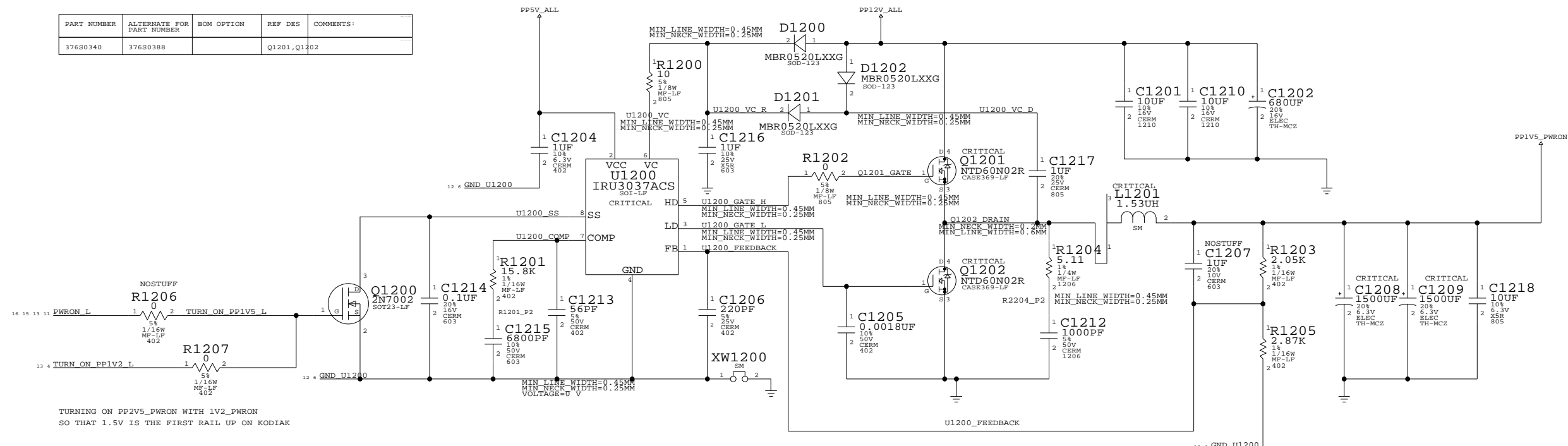
NOTE:

IRU3037ACS VREF=0.8VDC
 $V_{OUT} = V_{REF} * (R_{1203} + R_{1205}) / R_{1205} = 1.25VDC$

LOAD FROM POWER BUDGET
 8.5A PEAK CURRENT DRAW
 7.2A CONTINUOUS CURRENT DRAW

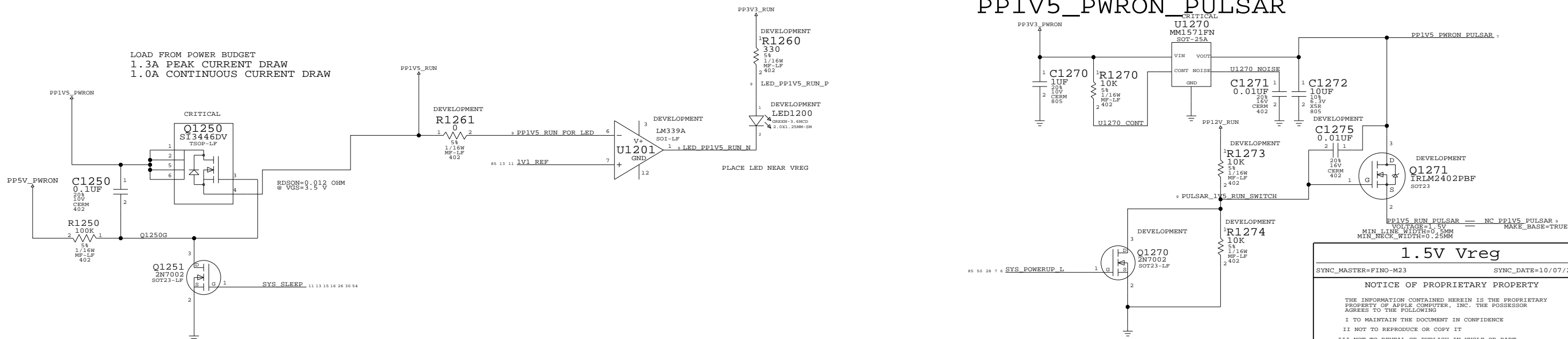
1.35V R1205=2.87K
 1.30V R1205=3.24K
 1.25V R1205=3.65K

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1201, Q1202	



TURNING ON PP2V5_PWRON WITH 1V2_PWRON
 SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

PP1V5_PWRON_PULSAR

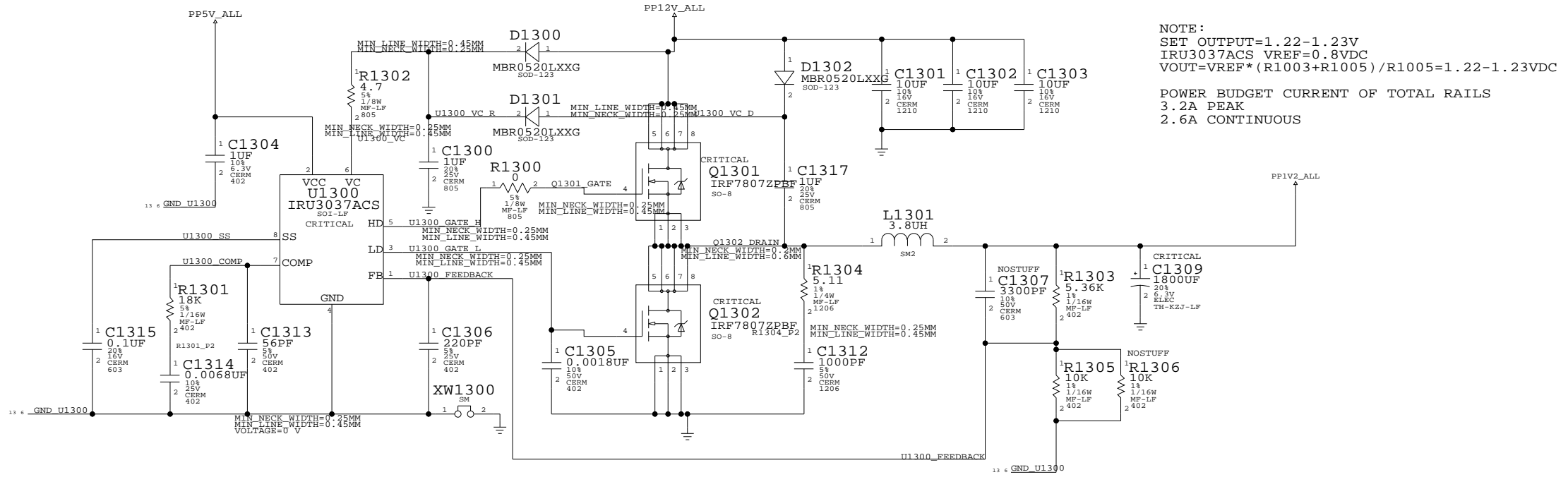


LOAD FROM POWER BUDGET
 1.3A PEAK CURRENT DRAW
 1.0A CONTINUOUS CURRENT DRAW

1.5V Vreg
 SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005
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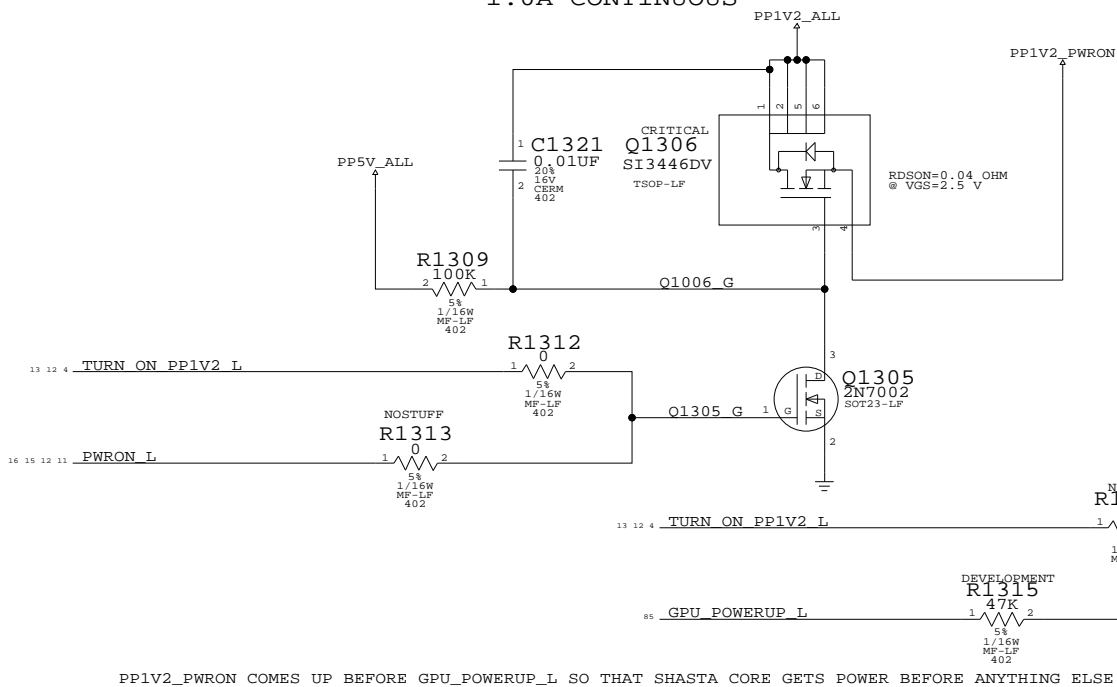
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT	12 OF	154
NONE			

PP1V2_ALL VOLTAGE REGULATOR



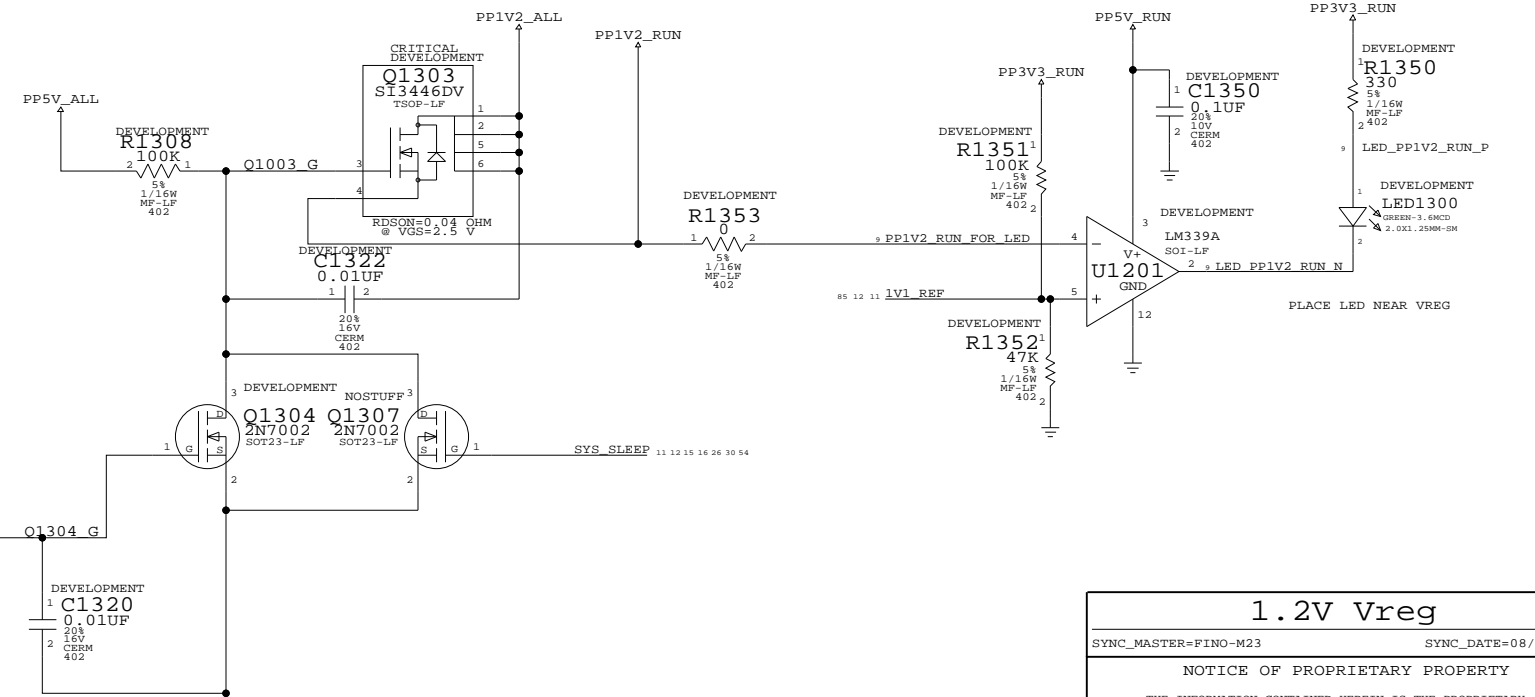
PP1V2_PWRON FET SWITCH

PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



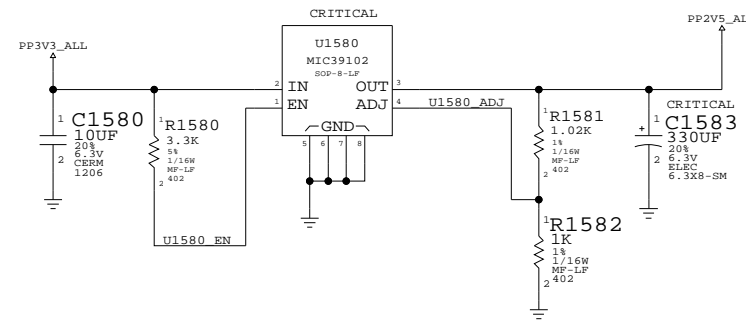
1.2V Vreg

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005
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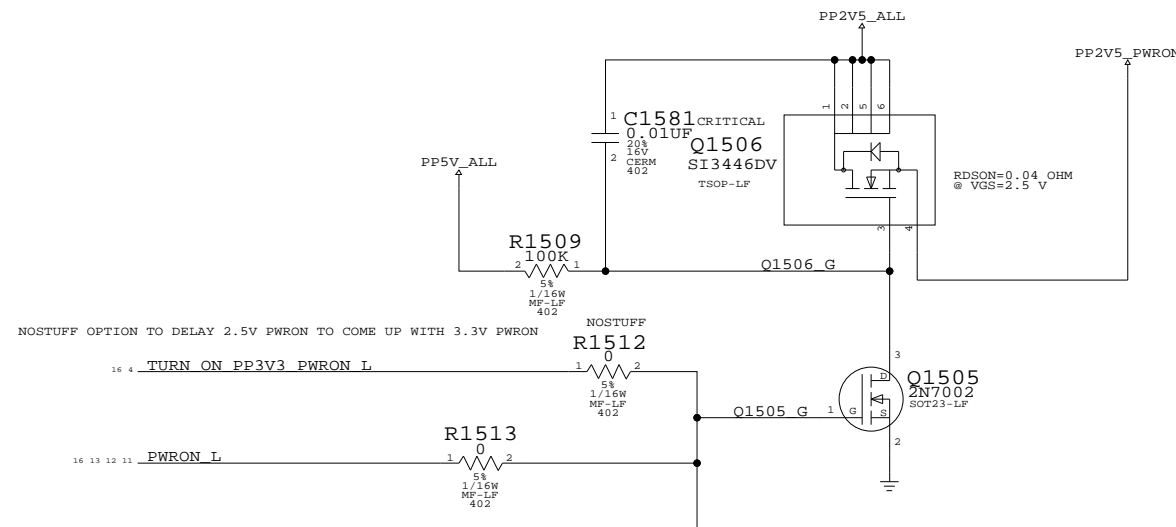
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT	13 OF	154
NONE			

PP2V5_ALL VOLTAGE REGULATOR

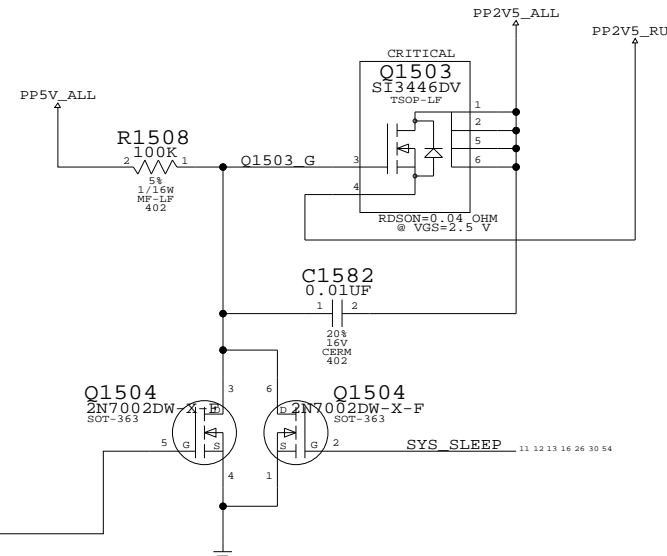
NOTE:
 SET OUTPUT=2.5V
 IRU3037CS VREF=1.24VDC
 $V_{OUT} = V_{REF} * (R_{1581} + R_{1582}) + 1 = 5.505VDC$
 POWER BUDGET CURRENT OF TOTAL RAILS
 0.2A PEAK
 0.1A CONTINUOUS



PP2V5_PWRON FET SWITCH PEAK CURRENT 0.1A



PP2V5_RUN FET SWITCH PEAK CURRENT 0.1A



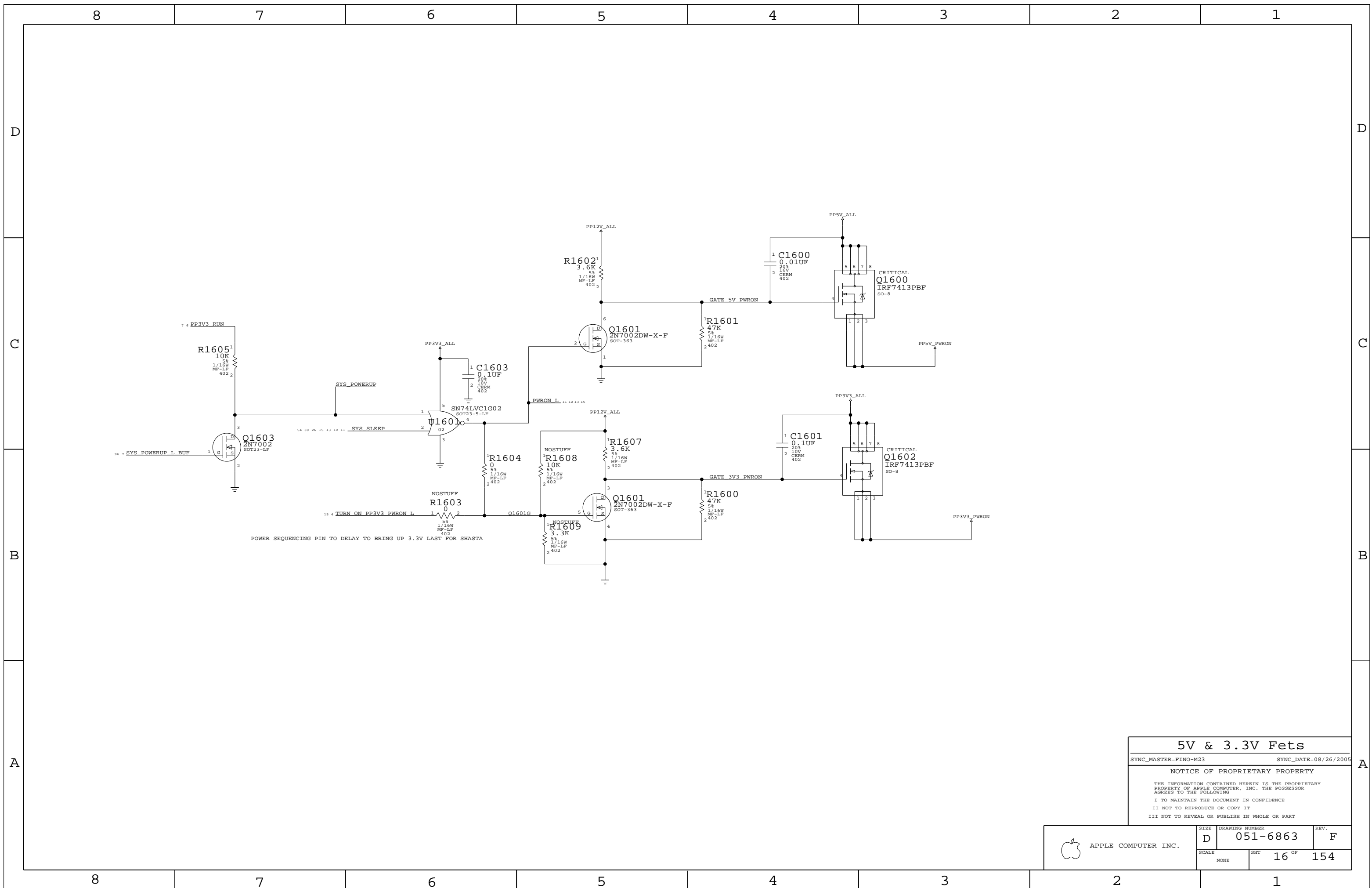
2.5V Vreg

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5V & 3.3V Fets

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	SCALE NONE	SHT 16 OF	154

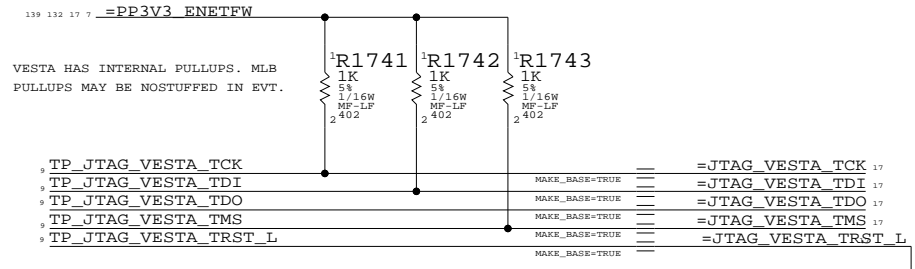
Page Notes

Power aliases required by this page:

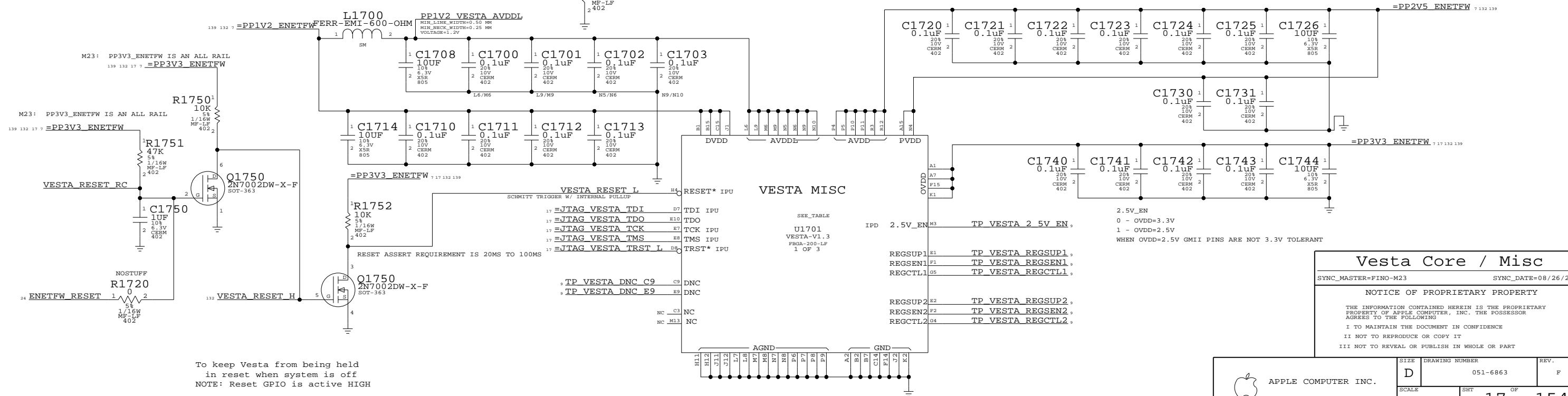
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG



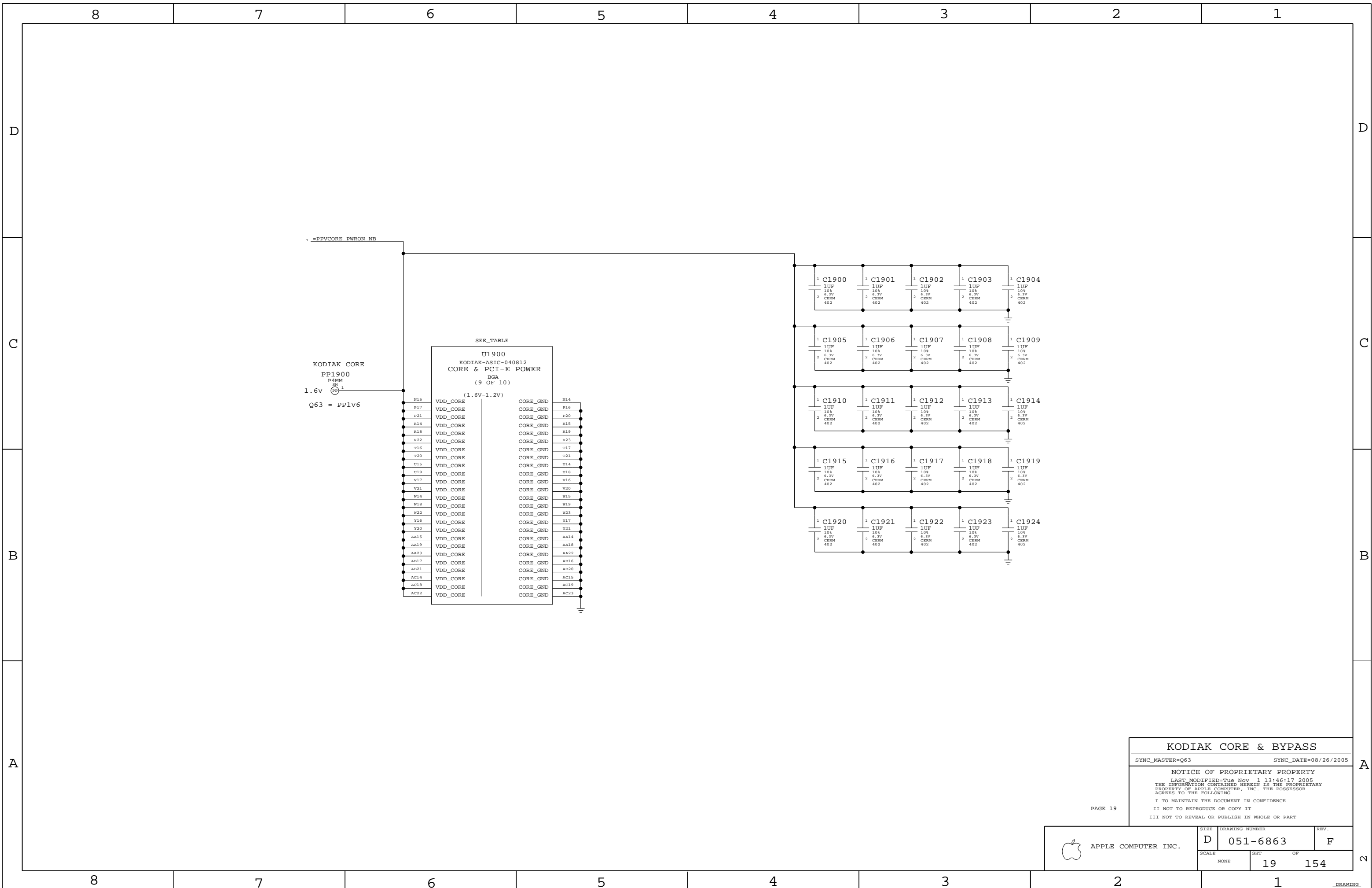
M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS



To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

Vesta Core / Misc		
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	D	051-6863	F
SCALE	SHT	OF	REV.
NONE	17	154	



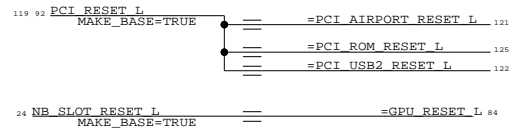
KODIAK CORE & BYPASS
 SYNC_MASTER=Q63 SYNC_DATE=08/26/2005
 NOTICE OF PROPRIETARY PROPERTY
 LAST MODIFIED=Tue Nov 1 13:46:17 2005
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PAGE 19

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	NONE	SHT OF	19 OF 154

SHASTA ALIASES

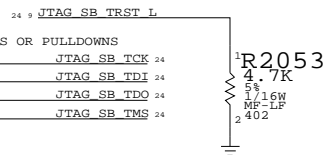
PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)



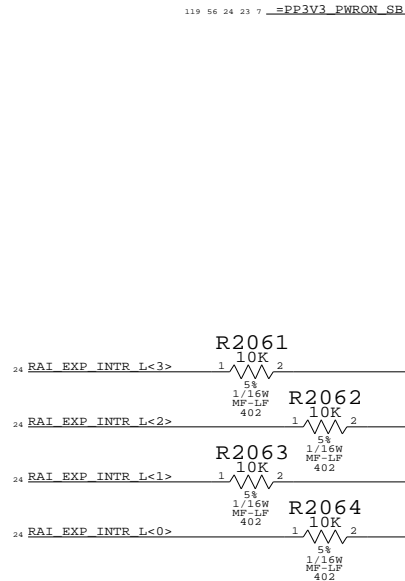
SHASTA JTAG

THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS

TP JTAG SB_TCK == JTAG SB_TCK 24
MAKE_BASE=TRUE == JTAG SB_TDI 24
TP JTAG SB_TDI == JTAG SB_TDI 24
TP JTAG SB_TDO == JTAG SB_TDO 24
MAKE_BASE=TRUE == JTAG SB_TMS 24
TP JTAG SB_TMS == JTAG SB_TMS 24
MAKE_BASE=TRUE



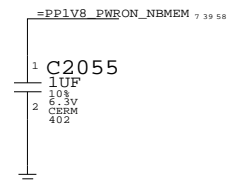
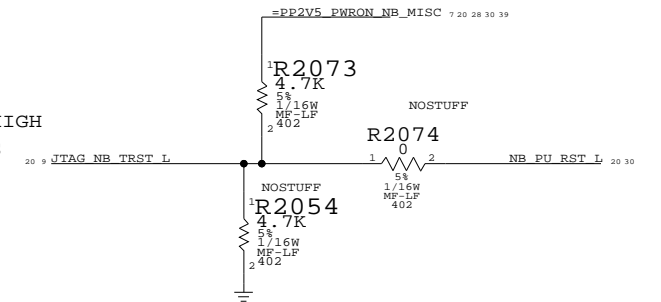
SHASTA GPIO TERMINATIONS
(SOME OF THESE ARE NOSTUFF
ON PAGE 24)



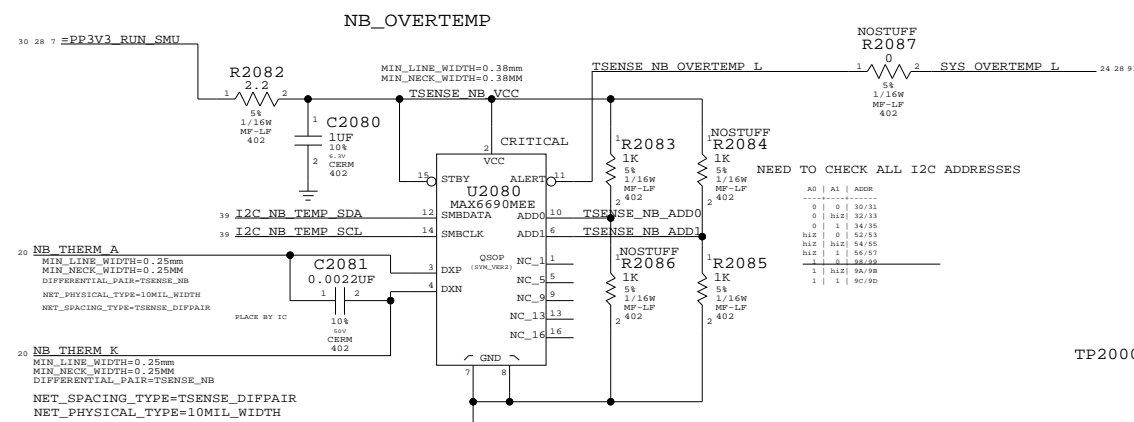
KODIAK ALIASES

NC PMR_CLK_DIS_L == MAKE_BASE=TRUE == PMR_CLK_DIS_L 20

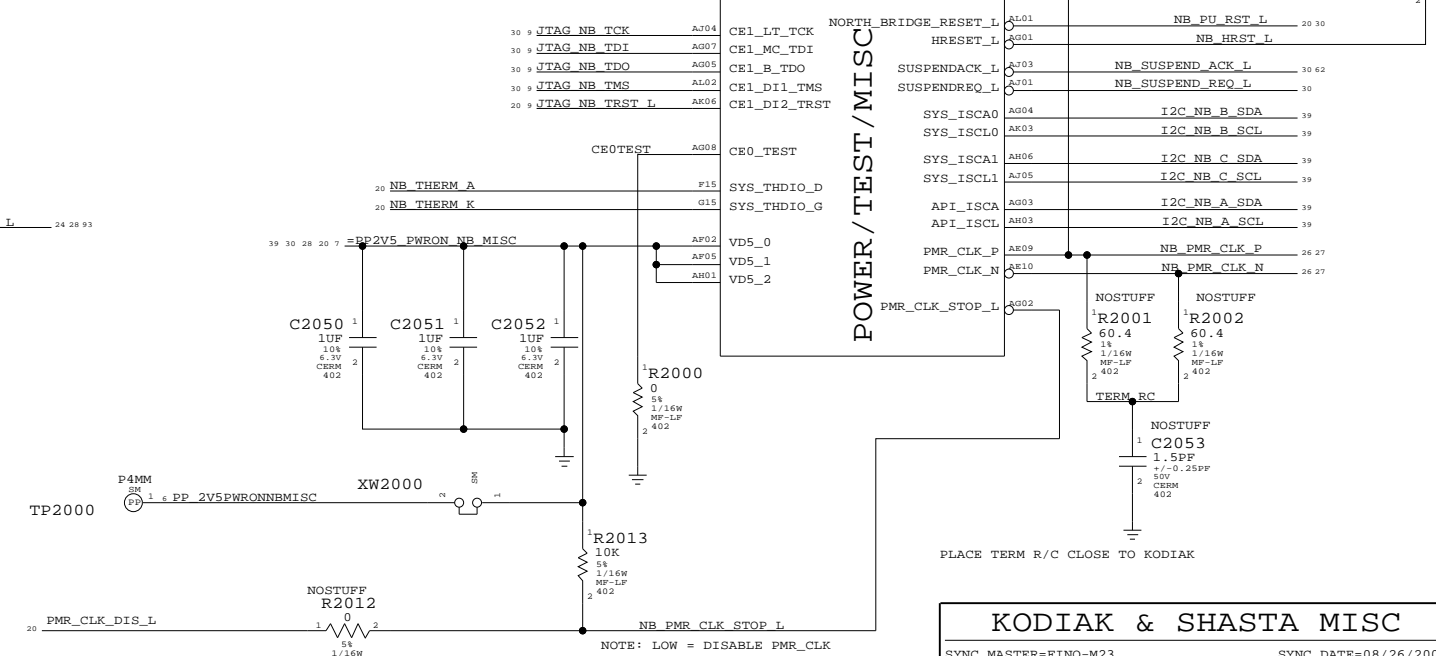
KODIAK JTAG_TRST PULLED HIGH
TO ALLOW SMU DEBUG ACCESS



C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP



NEED TO CHECK ALL I2C ADDRESSES



NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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SCALE	SHEET OF		
NONE	20		154

Page Notes

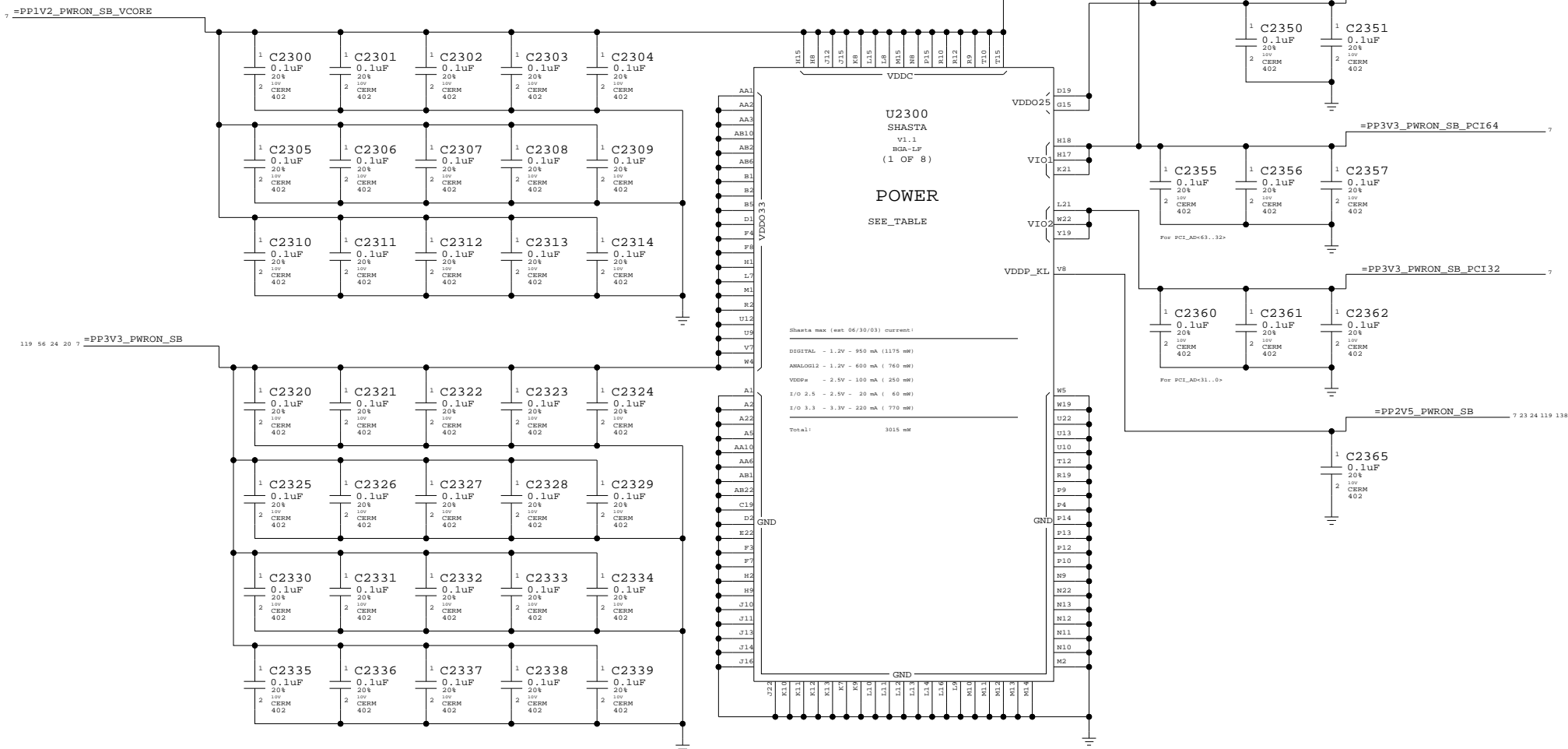
Power aliases required by this page:
 - =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
 - =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
 - =PP3V3_PWRON_SB
 - =PP2V5_PWRON_SB
 - =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Power Sequencing:
 Must power Shasta VCore rail before any other Shasta supplies.



Shasta Core Power

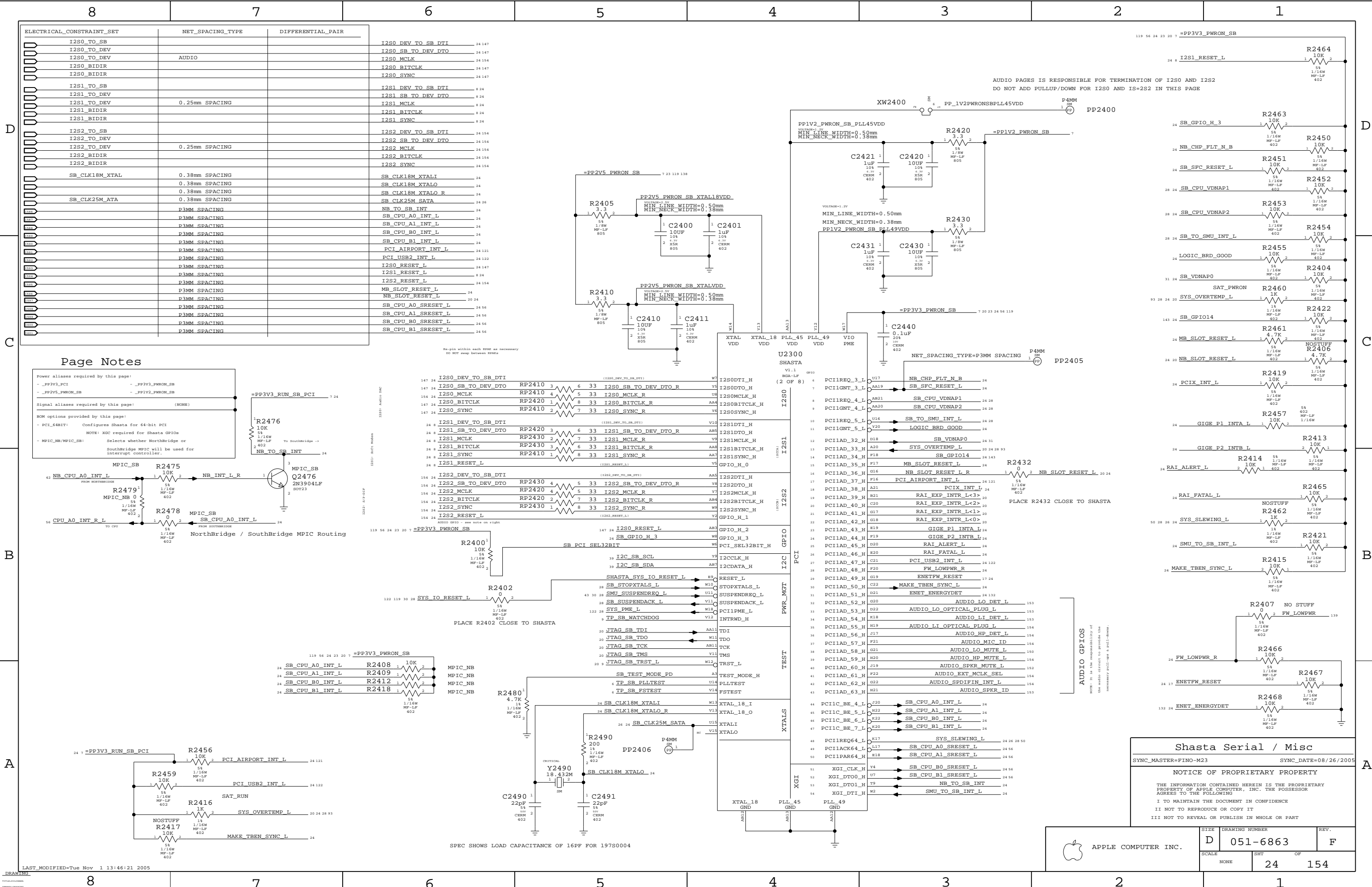
SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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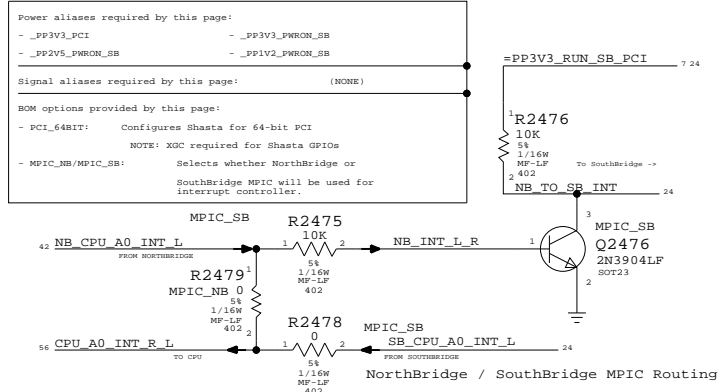
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NONE	23 OF 154		



Page Notes



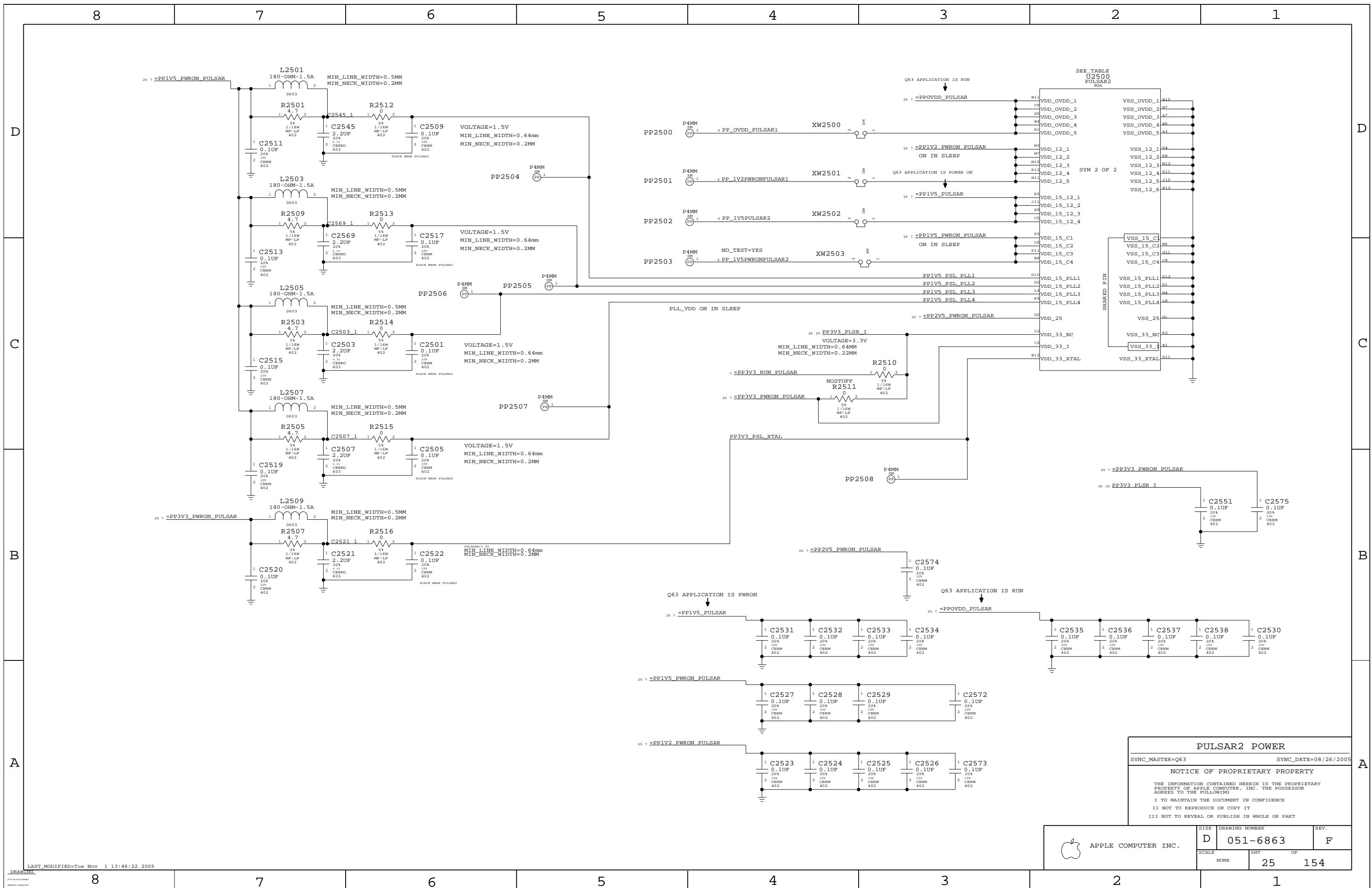
B

A

AUDIO GPIOs
 NOTE: It is the responsibility of the audio circuit to provide the necessary pull-up & pull-down.

Shasta Serial / Misc
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DRAWING NUMBER	051-6863	REV.	F		
	SCALE		NONE	SHT	24



PULSAR2 POWER

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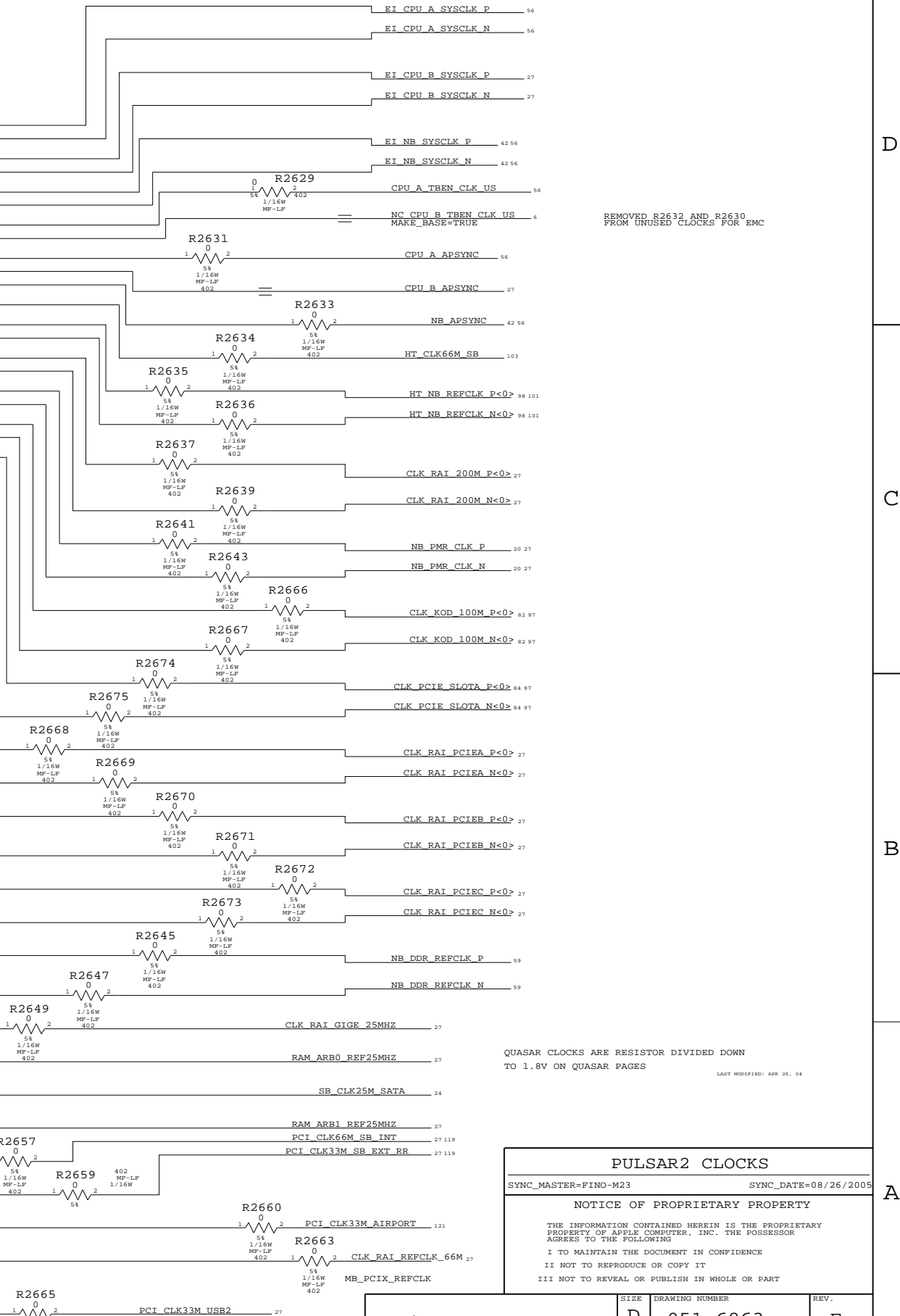
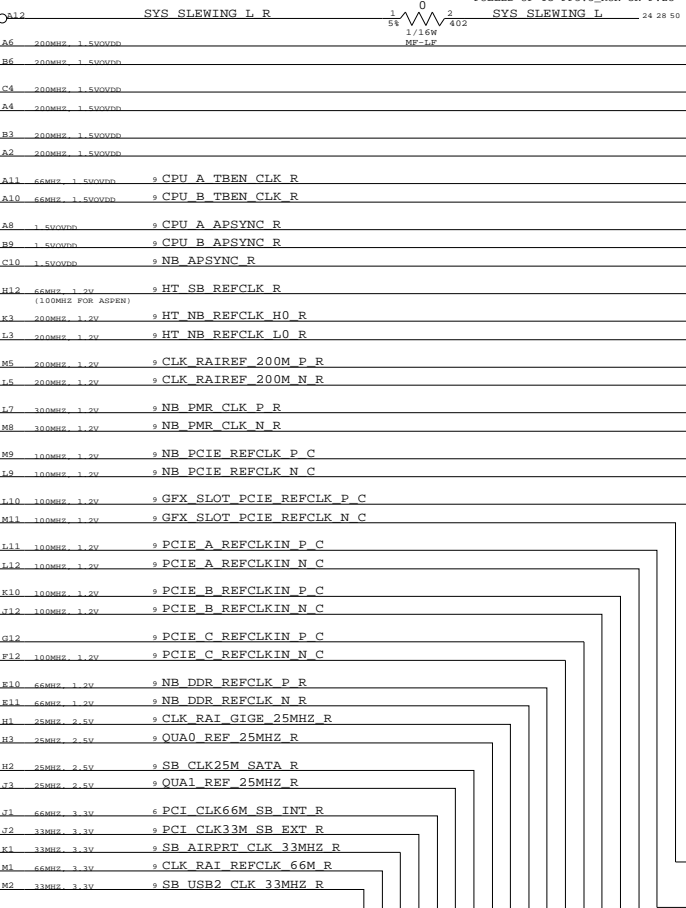
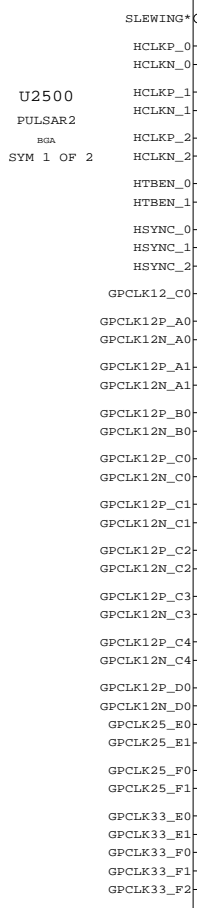
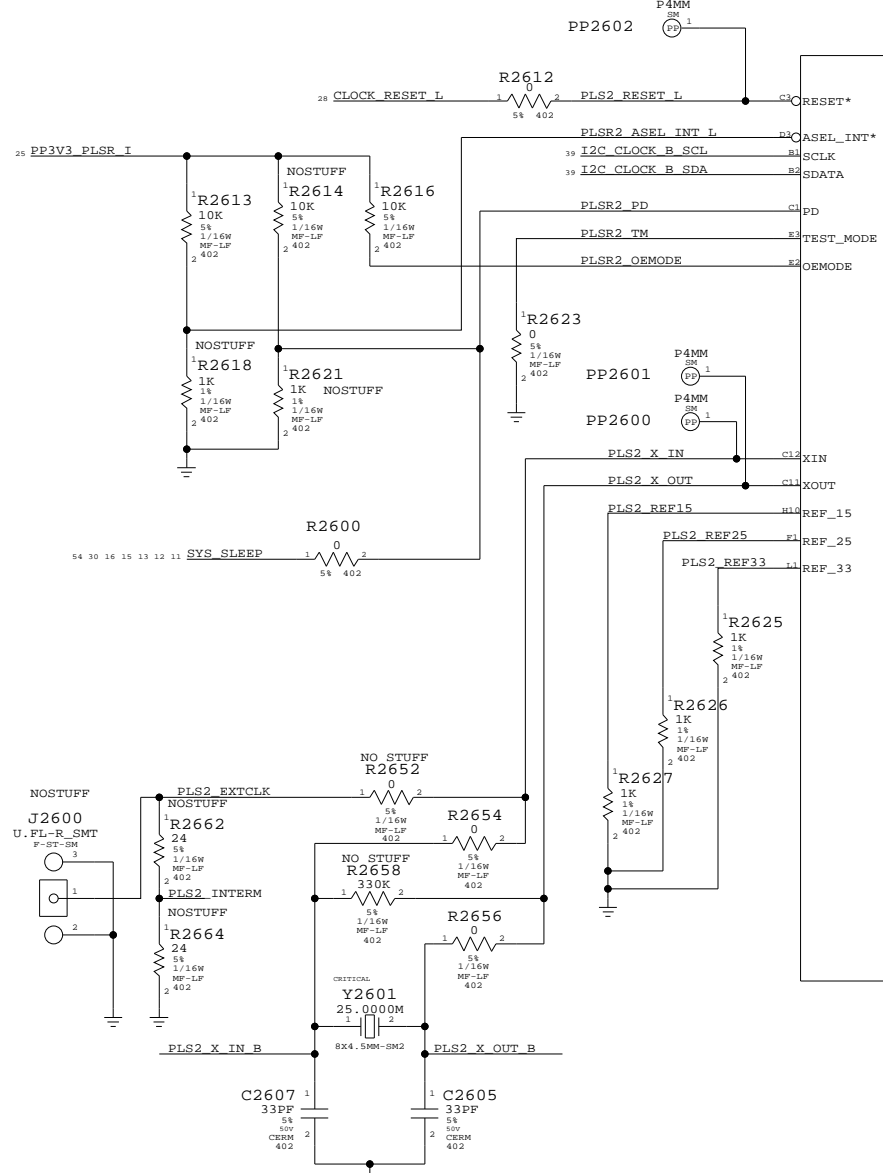
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PLACE ALL 0-OHM SERIES RESISTORS
ON THIS PAGE NEAR PULSAR



QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN TO 1.8V ON QUASAR PAGES
LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS
 SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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	D	051-6863	F
SCALE	NONE	SHT	OF
		26	154

N/C ALIASES

N/C RAINIER CLOCKS

NC_CLK_RAI_REFCLK_66M == CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

NC_CLK_RAI_GIGE_25MHZ == CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

NC_CLK_RAI_200M_P<0> == CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_200M_N<0> == CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEA_P<0> == CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEA_N<0> == CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEB_P<0> == CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEB_N<0> == CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEC_P<0> == CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEC_N<0> == CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

NC_EI_CPU_B_SYSCLK_P == EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

NC_EI_CPU_B_SYSCLK_N == EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

NC_CPU_B_APSYNC == CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

NC_RAM_ARB0_REF25MHZ == RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

NC_RAM_ARB1_REF25MHZ == RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTRAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	499
26 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	499
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM_SPACING	PCI_CLK_SB	499
119 26 PCI_CLK33M_SB_EXT RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB_CAP	499

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 == =PCI_CLK33M_USB2 122
MAKE_BASE=TRUE

Pulsar Aliases

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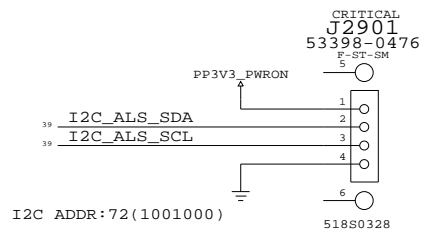
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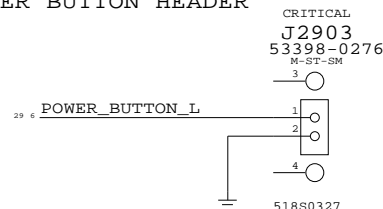
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE	SHT	27 OF 154
NONE		

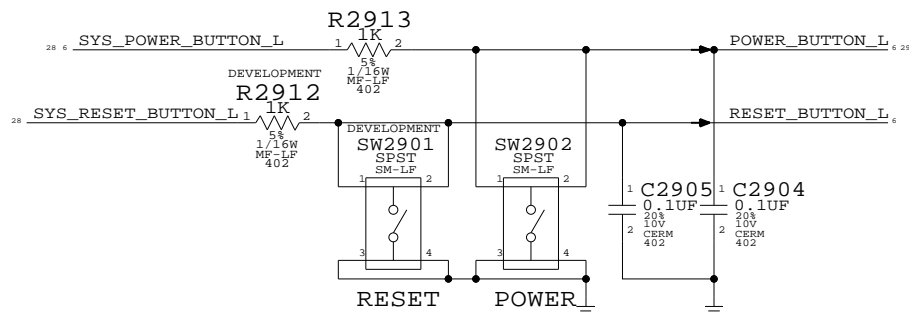
AMBIENT LIGHT SENSOR CONNECTOR



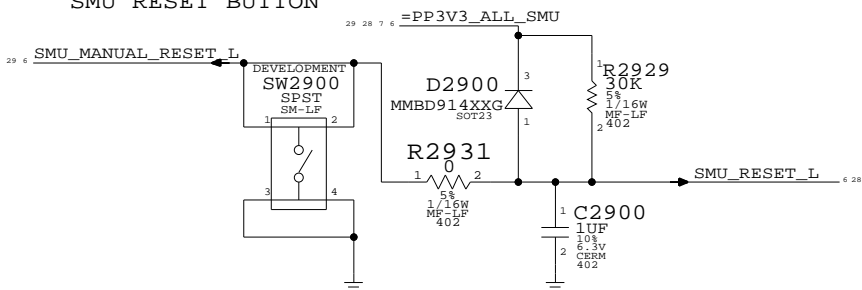
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

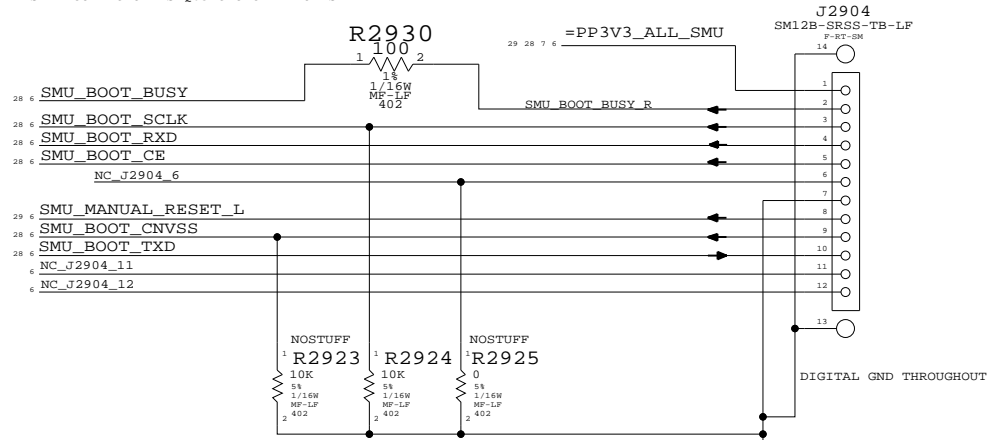


SMU RESET BUTTON



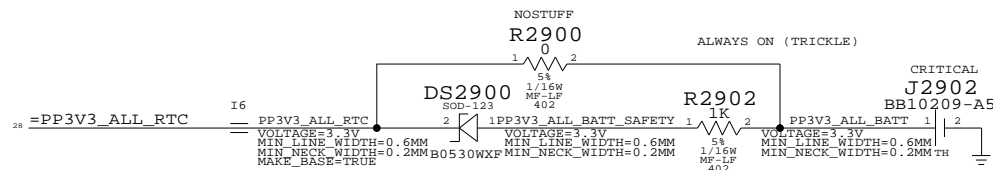
SMU DEBUG/DOWNLOAD CONNECTOR

SAME CONNECTOR AS Q63 CPU CARD FOR SAT

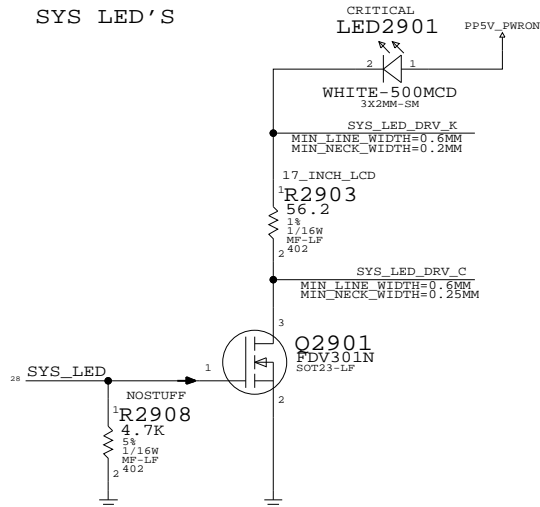


R2930, R2931, J2904 SHOULD BE MOVED BACK TO THE DEVELOPMENT BOM POST-RAMP

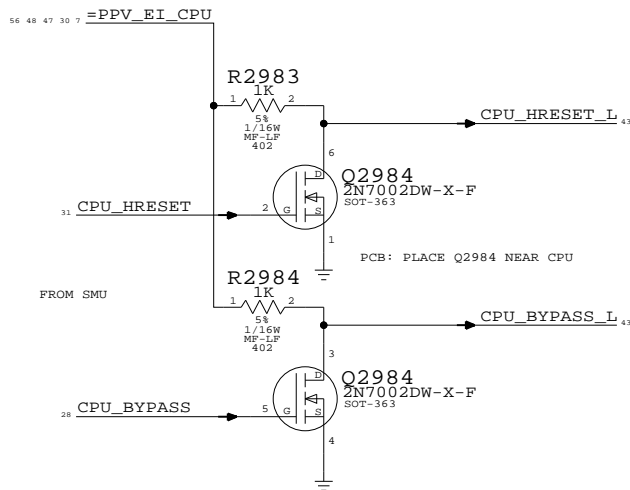
RTC BATTERY



SYS LED'S



DRIVE STRONG HRESET AND BYPASS TO CPU



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

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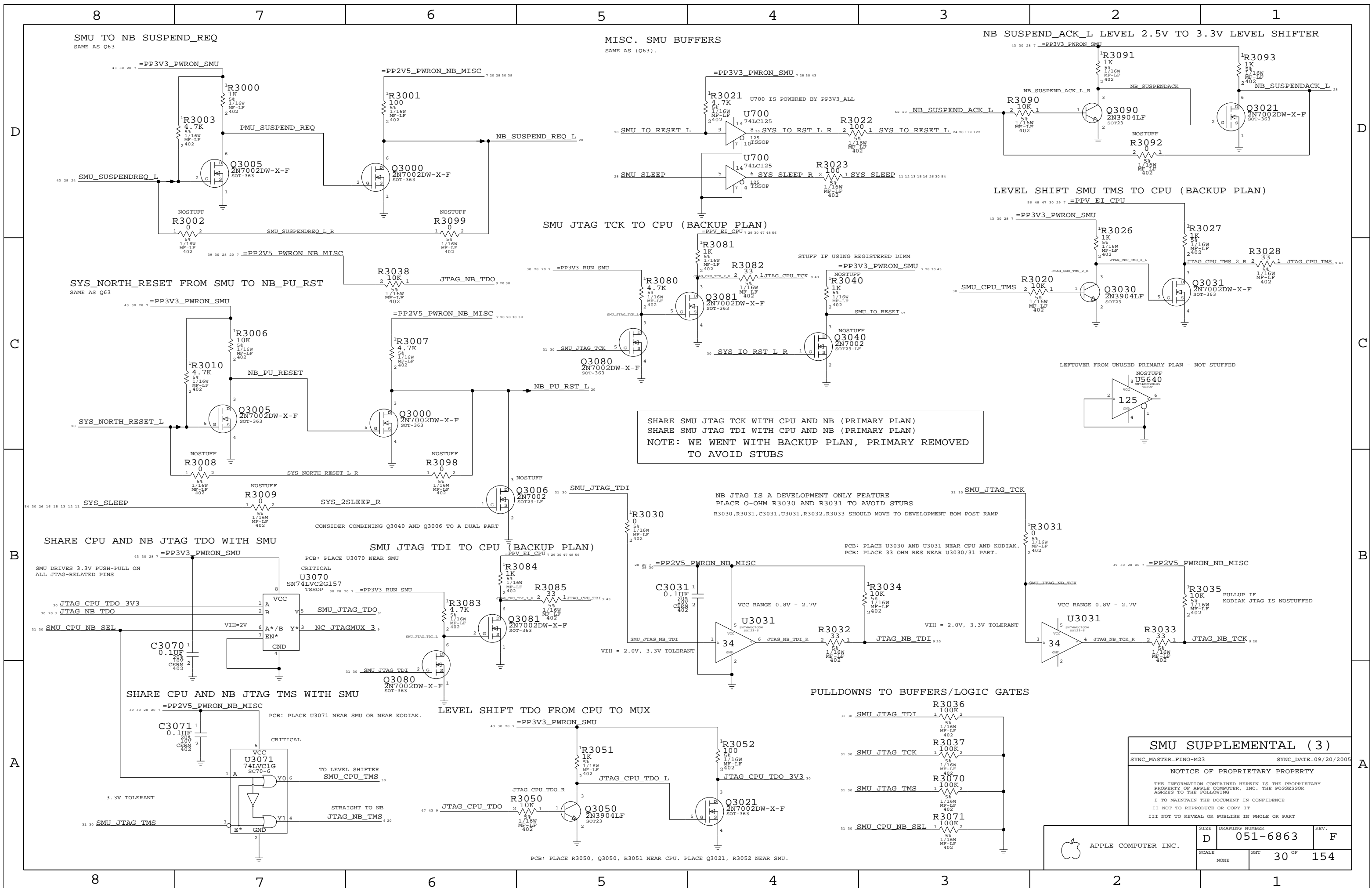
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SCALE	SHT	OF
NONE	29	154



SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

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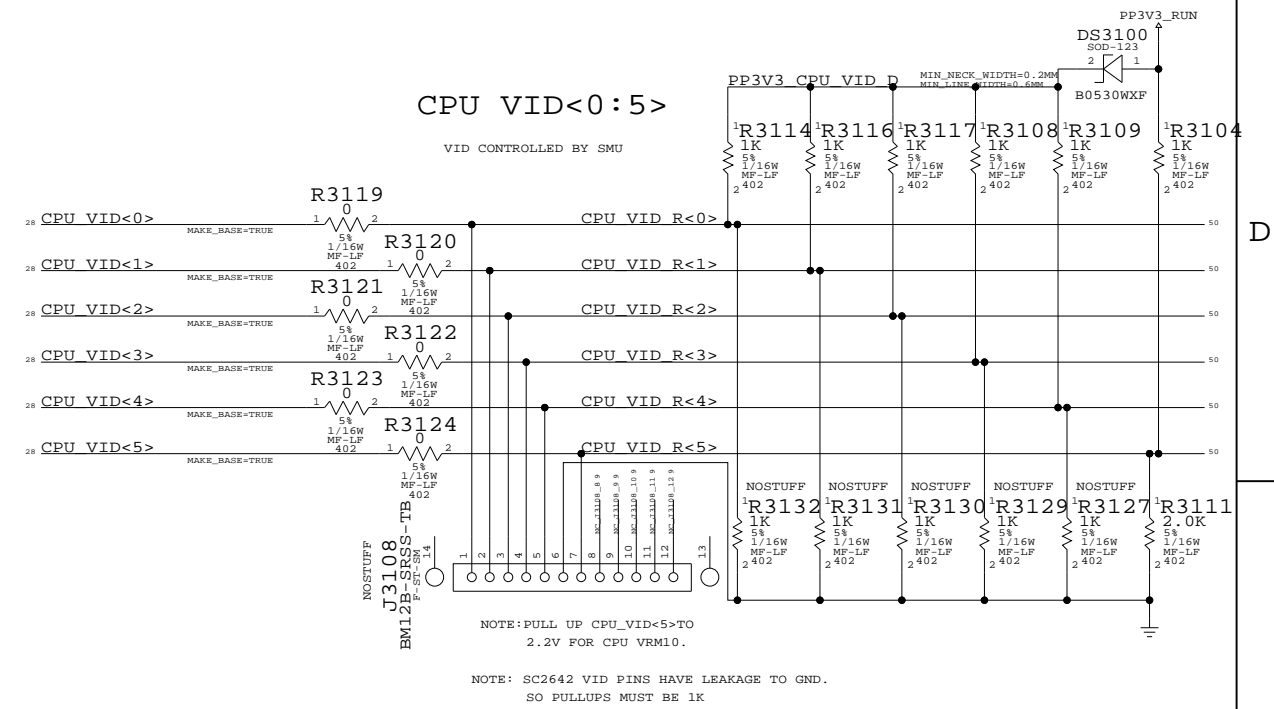
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	D	051-6863	F
SCALE	SHT	30 OF 154	
NONE			

SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION	Q63 NET NAME (SHARED PAGE)
Q63 NC'S THESE AS IT USES A SAT.		CPU_SENSE_I0 P0.0	
		CPU_SENSE_V0 P0.1	
		CPU_TEMP0 P0.2	
		CPU_BYPASS P0.3	
M23/M33 DOESN'T HAVE THOSE FANS.	NC_SMU_FAN_RPM3	FAN_CNTRL0_4 P0.4	SMU_FAN_RPM3
	NC_SMU_FAN_RPM4	FAN_CNTRL0_5 P0.5	SMU_FAN_RPM4
	NC_SMU_FAN_RPM5	FAN_CNTRL0_6 P0.6	SMU_FAN_RPM5
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE. M23/M33 DOESN'T USE. P1.0 NC ON PG 7.	NC_SMU_SER_SEL	SMU_SCCL_SEL P0.7	SMU_SER_SEL
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_SENSE_I1 P1.0	
		CPU_SENSE_V1 P1.1	
		CPU_TEMP1 P1.2	
		PS1_3 P1.3	
		PS1_4 P1.4	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		POWERFAIL* P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE. CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR? CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE. M23/M33 DOESN'T HAVE THIS FAN.	NC_SMU_CPU_VID_LE0	CPU_VID_LE0 P1.6	SMU_FAN_TACH9
	NC_SYS_DOOR_AJAR_L	DOOR_AJAR* P1.7	SYS_DOOR_AJAR_L
	NC_SMU_CPU_VID_LE1	CPU_VID_LE1 P2.0	SMU_FAN_TACH6
	NC_SMU_FAN_TACH7	FAN_TACH2_1 P2.1	SMU_FAN_TACH7
		FAN_TACH2_2 P2.2	
		FAN_TACH2_3 P2.3	
		FAN_TACH2_4 P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7. M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	NC_SMU_FAN_TACH3	FAN_TACH2_5 P2.5	SMU_FAN_TACH3
	NC_SMU_FAN_TACH4	FAN_TACH2_6 P2.6	SMU_FAN_TACH4
	NC_SMU_FAN_TACH5	FAN_TACH2_7 P2.7	SMU_FAN_TACH5
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	I2C_SMU_A_SDA	IIC_A_DAT P3.0	I2C_SMU_A_SDA_IN
	I2C_SMU_A_SCL	IIC_A_CLK P3.1	I2C_SMU_A_SDA_OUT_L
	SMU_JTAG_TDI	TDI P3.2	I2C_SMU_A_SCL_IN
	SMU_JTAG_TCK	TCK P3.3	I2C_SMU_A_SCL_OUT_L
		IIC_E_DAT P3.4	
		IIC_E_CLK P3.5	
		DIAG_LED P3.6	
		OVERTEMP* P3.7	
		CPU_VID[0] P6.0	
		CPU_VID[1] P6.1	
		CPU_VID[2] P6.2	
		CPU_VID[3] P6.3	
		CPU_VID[4] P6.4	
		CPU_VID[5] P6.5	
		DEBUG_RXD P6.6	
		DEBUG_TXD P6.7	
		IIC_B_DAT P7.0	
		IIC_B_CLK P7.1	
Q63 USE OF P7.2 IS PWM FAN SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	SMU_CPU_NB_SEL	CPU_TMS P7.2	I2C_SMU_CPU_SDA_IN
		FAN_CNTRL7_3 P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4) M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.	NC_I2C_SMU_CPU_SCL_IN	FAN_CNTRL7_4 P7.4	I2C_SMU_CPU_SCL_IN
		FAN_CNTRL7_5 P7.5	
		VDNAP2 P7.6	
		FAN_CNTRL7_7 P7.7	
		SYSTEM_LED P8.0	
		NB_RESET* P8.1	
		PME* P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	SB_VDNAP0	VDNAP0 P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF
		SLEWING* P8.4	
	SMU_JTAG_TMS	DR_5 P8.5	I2C_SMU_CPU_SDA_OUT_L
		POWERUP* P8.6	
		SLEEP P8.7	
		CLK_RESET* P9.0	
Q63 USE OF P9.1 IS TACH 8.	CPU_HRESET	CPU_HRESET P9.1	SMU_FAN_TACH8
		SMU_DOORBELL* P9.2	
		STOP_XTAL* P9.3	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7. M23/M33 HAS NO SLOTS.	NC_SLOT_TOTAL_PWR	PS9_5 P9.5	SYS_SLOT_PWR
		PS9_6 P9.6	
		VDNAP1 P10.0	
		IO_RESET* P10.1	
		SUSPEND_ACK* P10.2	
		SUSPEND_IO_ACK* P10.3	
		SUSPEND_REQ* P10.4	
		PWR_BUTTON* P10.5	
		RST_BUTTON* P10.6	
	SMU_JTAG_TDO	TDO P10.7	I2C_SMU_CPU_SCL_OUT_L



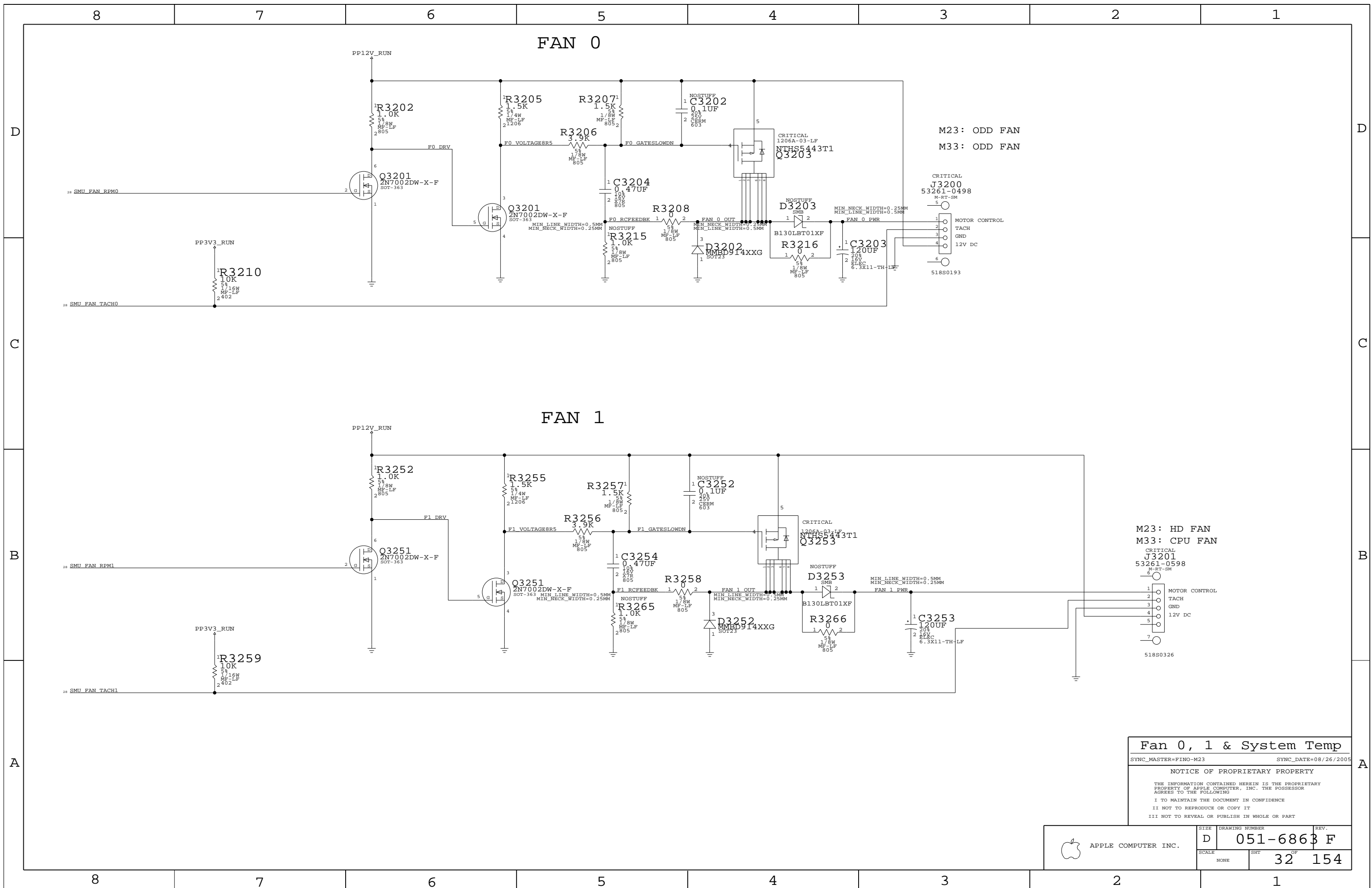
SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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	D	051-6863	F
SCALE	SHT	31 OF 154	
NONE			



Fan 0, 1 & System Temp

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	NONE	D 051-6863 F	
SCALE		SHT	OF
NONE		32	154

SMU AND NB I2C A BUS

SB I2C BUS

SMU I2C B BUS

SMU I2C E BUS

NB I2C C BUS

NB I2C B BUS

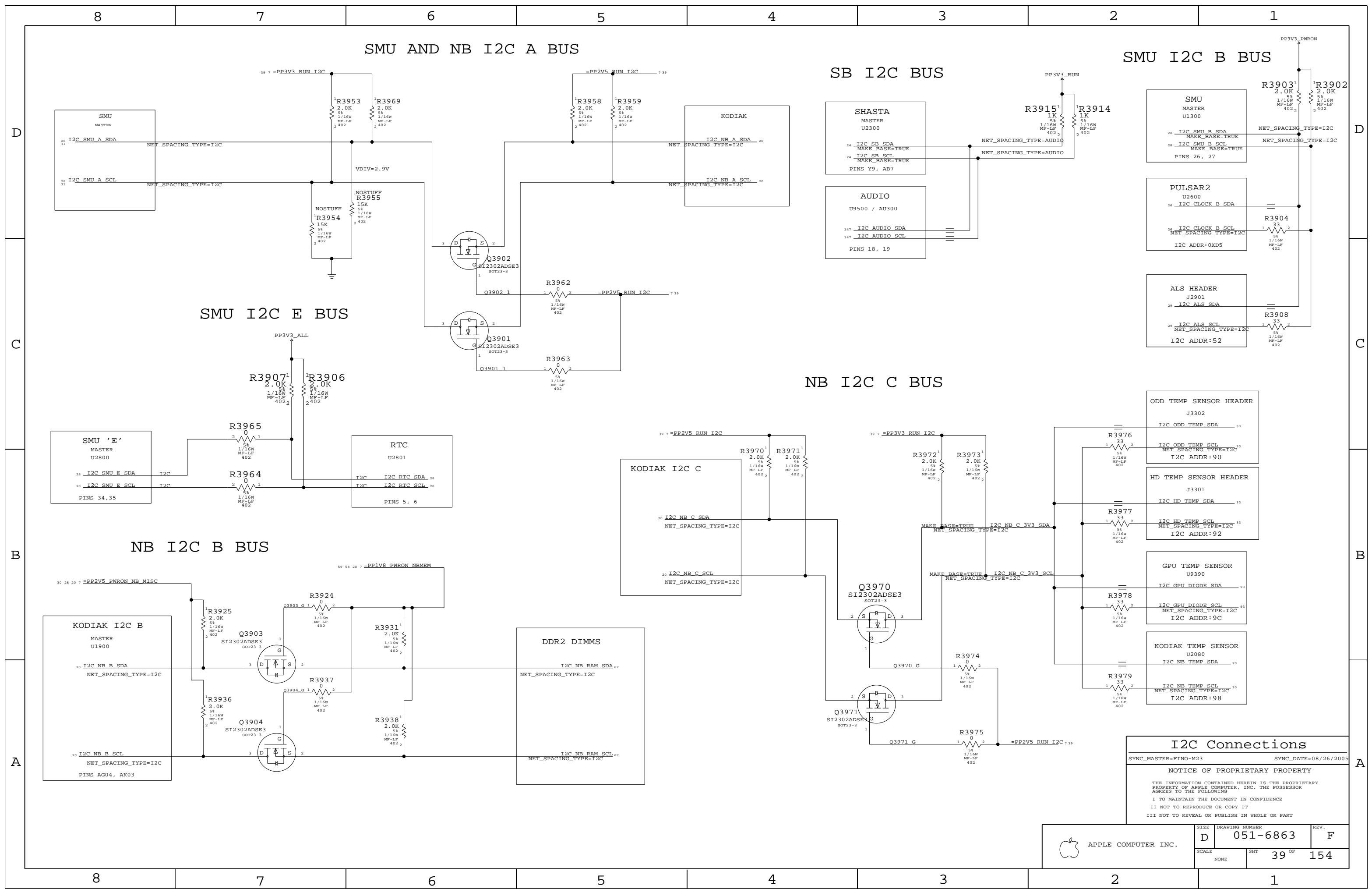
I2C Connections

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NONE			



SMU MASTER
 U1300
 I2C SMU A SDA
 I2C SMU A SCL

KODIAK
 I2C NB A SDA
 I2C NB A SCL

SHASTA MASTER
 U2300
 I2C SB SDA
 I2C SB SCL

AUDIO
 U9500 / AU300
 I2C AUDIO SDA
 I2C AUDIO SCL

SMU MASTER
 U1300
 I2C SMU B SDA
 I2C SMU B SCL

PULSAR2
 U2600
 I2C CLOCK B SDA
 I2C CLOCK B SCL

ALS HEADER
 J2901
 I2C ALS SDA
 I2C ALS SCL

SMU 'E' MASTER
 U2800
 I2C SMU E SDA
 I2C SMU E SCL

RTC
 U2801
 I2C RTC SDA
 I2C RTC SCL

KODIAK I2C C
 I2C NB C SDA
 I2C NB C SCL

KODIAK I2C C
 I2C NB C SDA
 I2C NB C SCL

ODD TEMP SENSOR HEADER
 J3302
 I2C ODD TEMP SDA
 I2C ODD TEMP SCL

HD TEMP SENSOR HEADER
 J3301
 I2C HD TEMP SDA
 I2C HD TEMP SCL

GPU TEMP SENSOR
 U9390
 I2C GPU DIODE SDA
 I2C GPU DIODE SCL

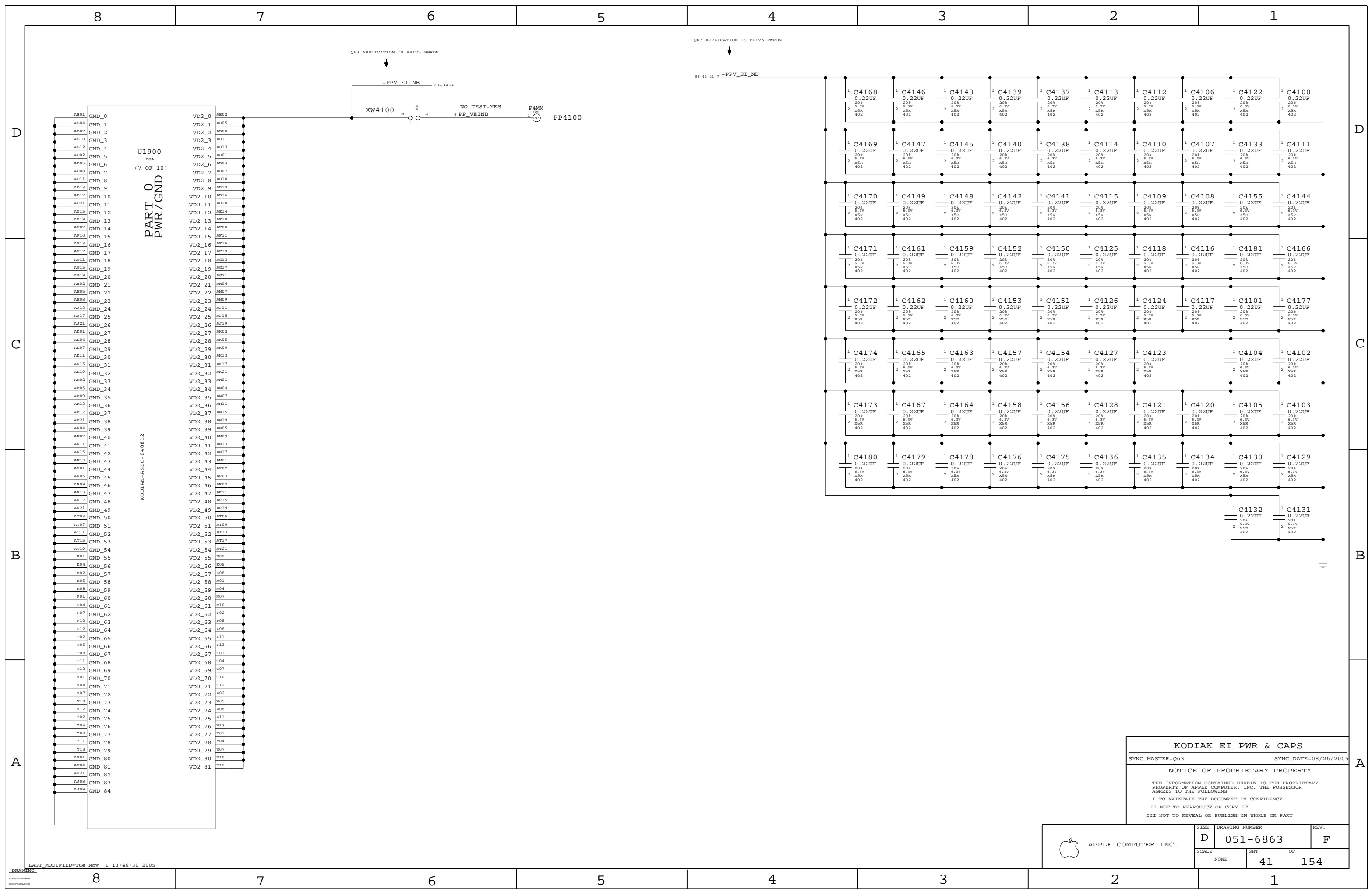
KODIAK TEMP SENSOR
 U2080
 I2C NB TEMP SDA
 I2C NB TEMP SCL

KODIAK I2C B MASTER
 U1900
 I2C NB B SDA
 I2C NB B SCL

DDR2 DIMMS
 I2C NB RAM SDA
 I2C NB RAM SCL

I2C Connections	
SYNC_MASTER=FINO-M23	SYNC_DATE=08/26/2005
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NONE			



KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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SCALE	SHT OF		
NONE	41 OF		154

D

D

C

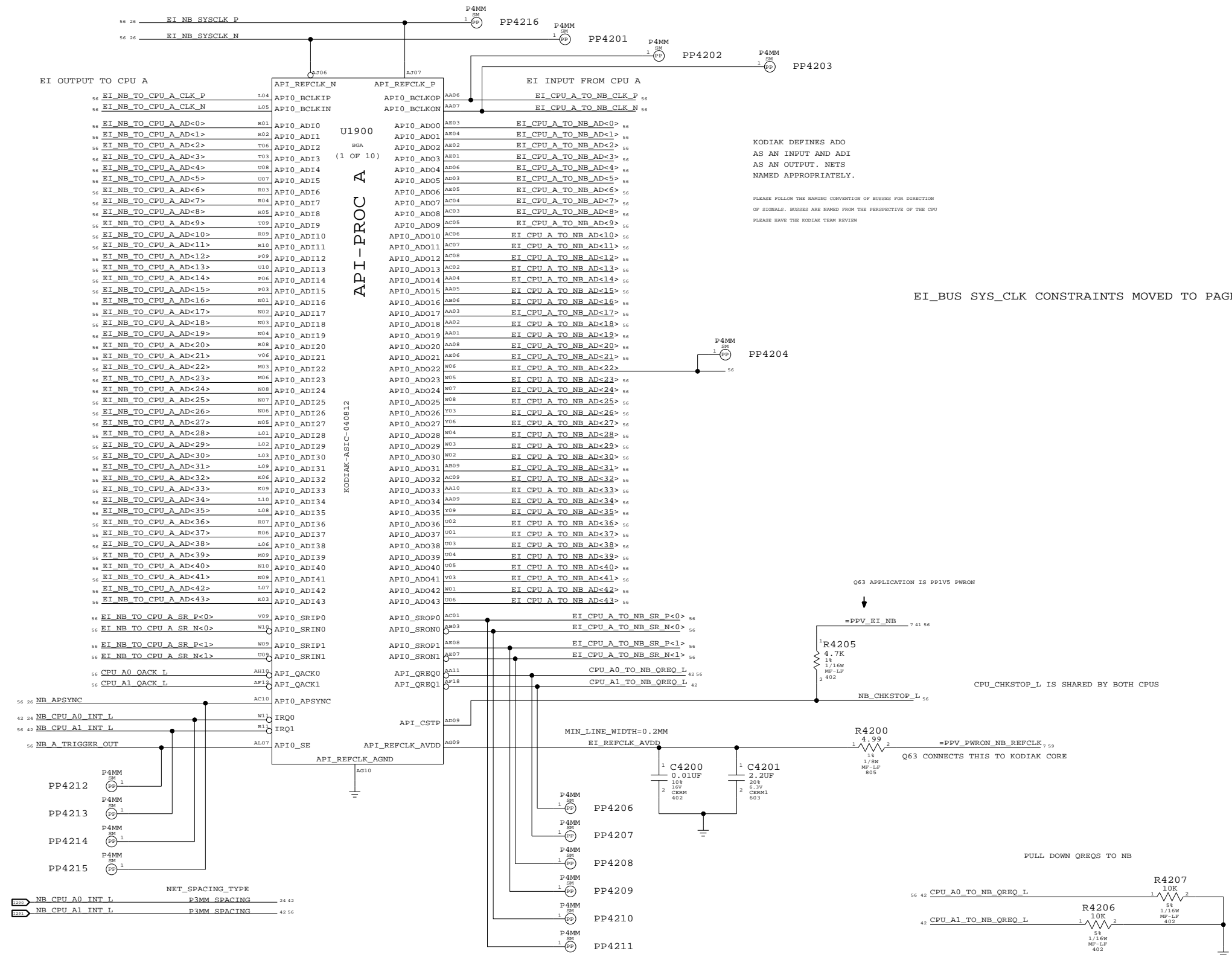
C

B

B

A

A



KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

PLEASE FOLLOW THE NAMING CONVENTION OF BUSES FOR DIRECTION OF SIGNALS. BUSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU PLEASE HAVE THE KODIAK TEAM REVIEW

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

Q63 APPLICATION IS PP1VS PWRON

=PPV_EI_NB 7 41 56

CPU_CHKSTOP_L IS SHARED BY BOTH CPUS

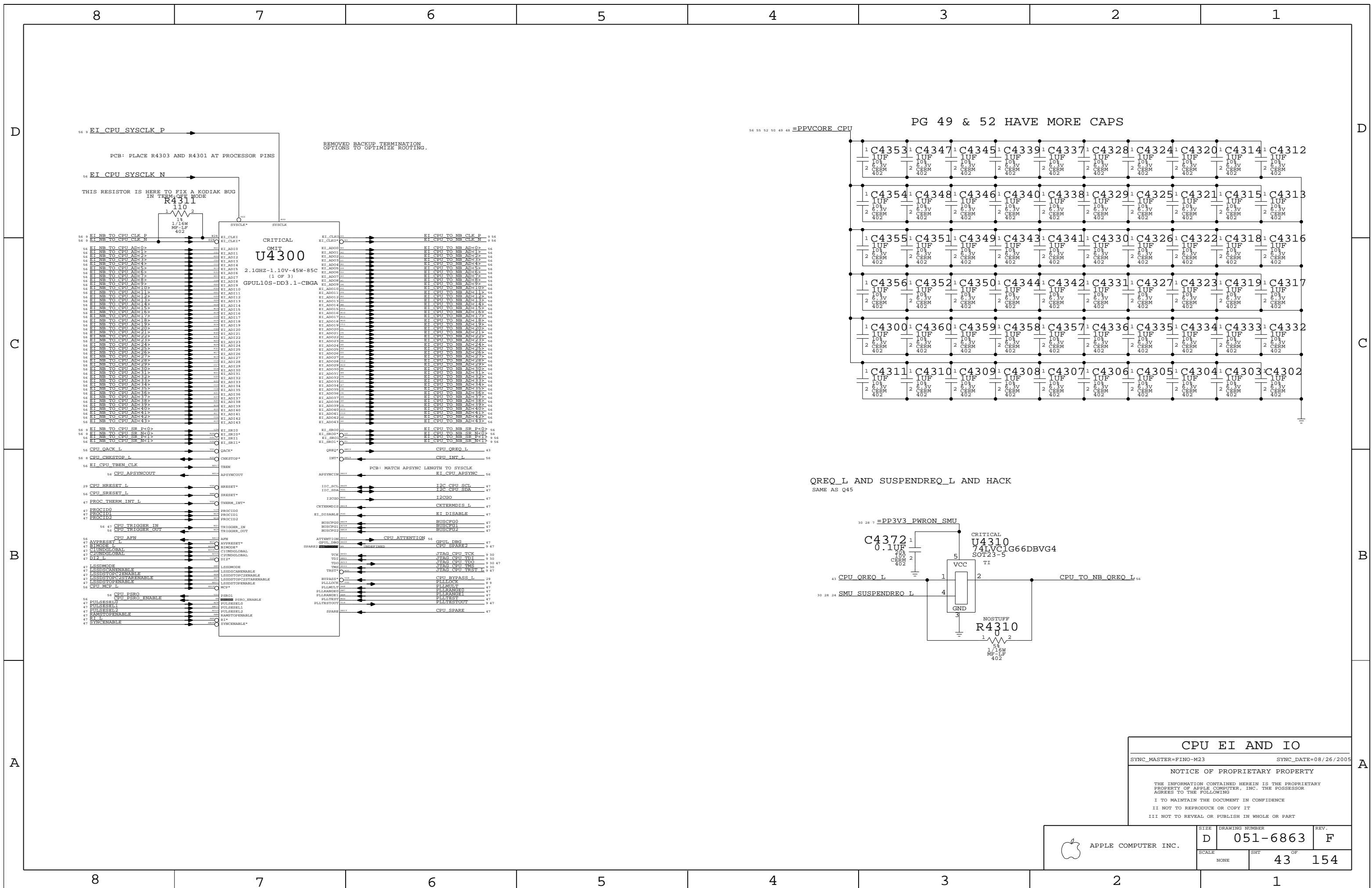
NB_CHKSTOP_L 56

Q63 CONNECTS THIS TO KODIAK CORE

PULL DOWN QREQS TO NB

KODIAK EI A		
SYNC_MASTER=Q63	SYNC_DATE=08/26/2005	
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SCALE	SHT	OF	
NONE	42	154	



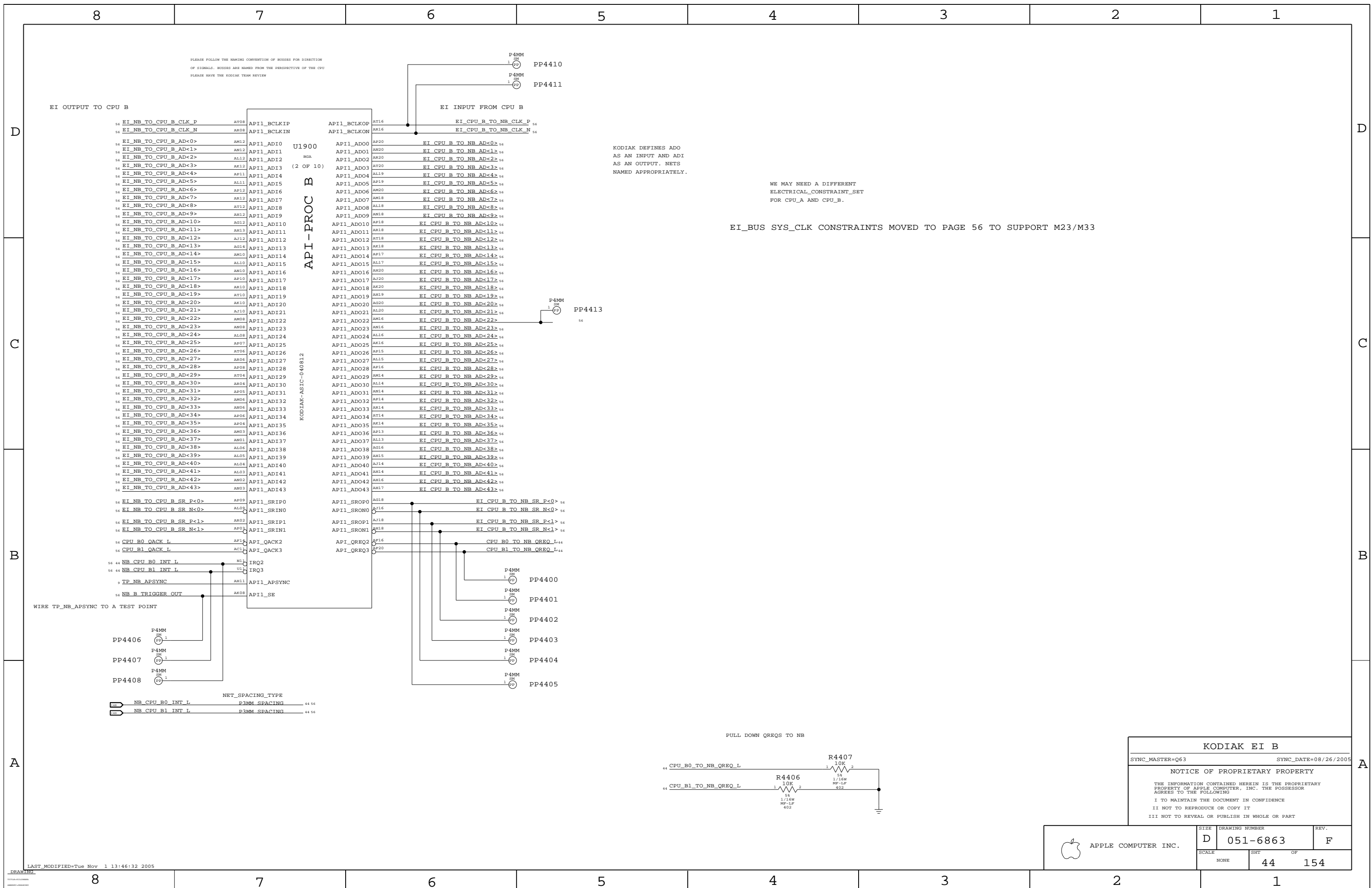
CPU EI AND IO

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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	D	051-6863	F
SCALE	NONE	SHT	OF
		43	154



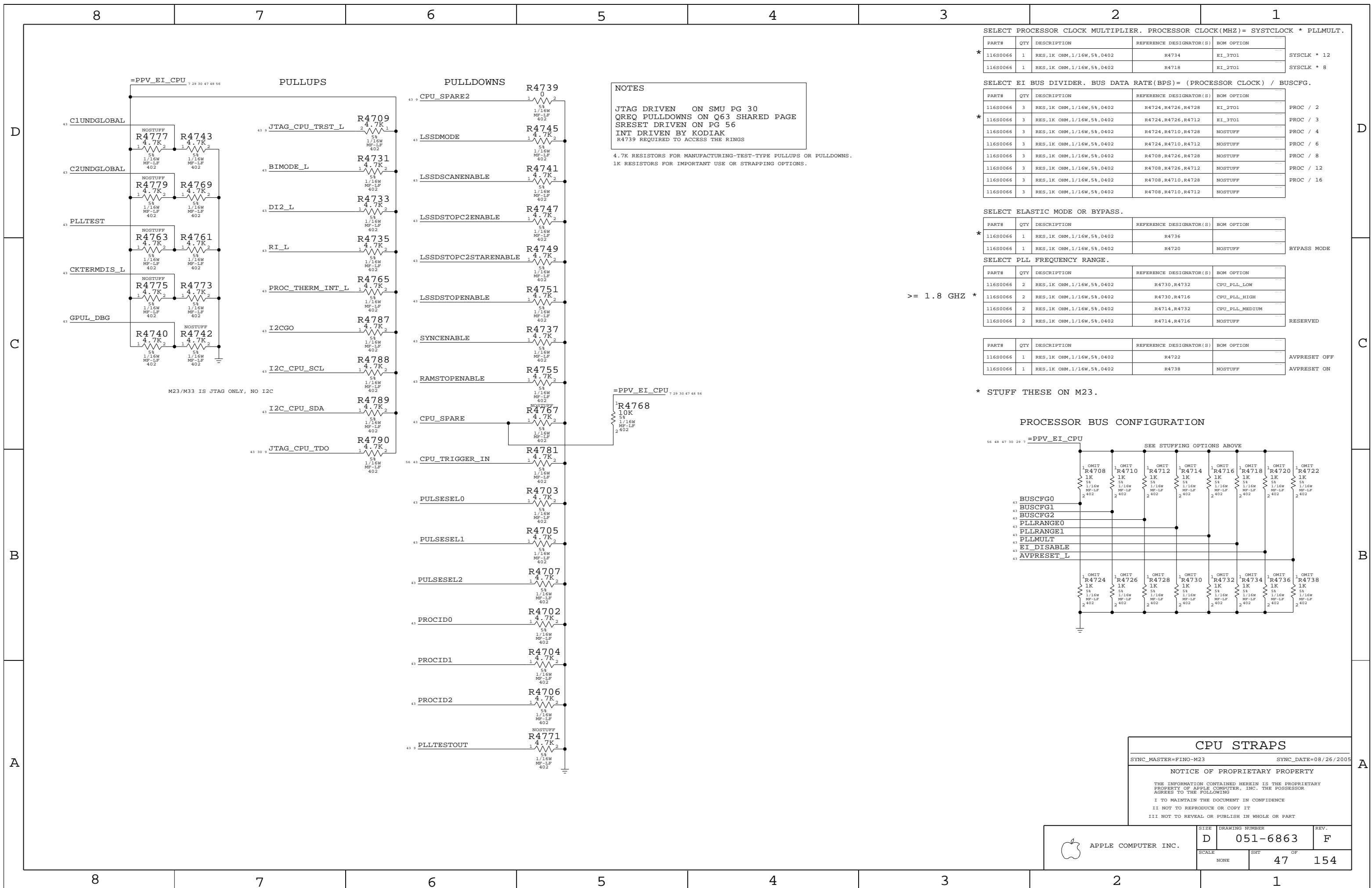
KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT ELECTRICAL_CONSTRAINT_SET FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

KODIAK EI B
 SYNC_MASTER=Q63 SYNC_DATE=08/26/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	NONE	SHT OF	44 154



NOTES

JTAG DRIVEN ON SMU PG 30
 QREQ PULLDOWNS ON Q63 SHARED PAGE
 SRESET DRIVEN ON PG 56
 INT DRIVEN BY KODIAK
 R4739 REQUIRED TO ACCESS THE RINGS

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
 1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
* 116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3T01
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2T01

SYSCLK * 12
 SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2T01
* 116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3T01
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF

PROC / 2
 PROC / 3
 PROC / 4
 PROC / 6
 PROC / 8
 PROC / 12
 PROC / 16

SELECT ELASTIC MODE OR BYPASS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
* 116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736	
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF

BYPASS MODE

SELECT PLL FREQUENCY RANGE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW
* 116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF

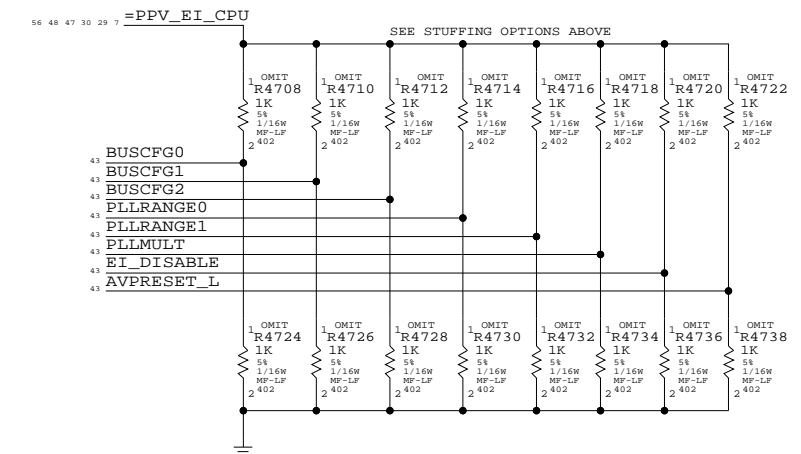
RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722	AVPRESET OFF
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	AVPRESET ON

AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



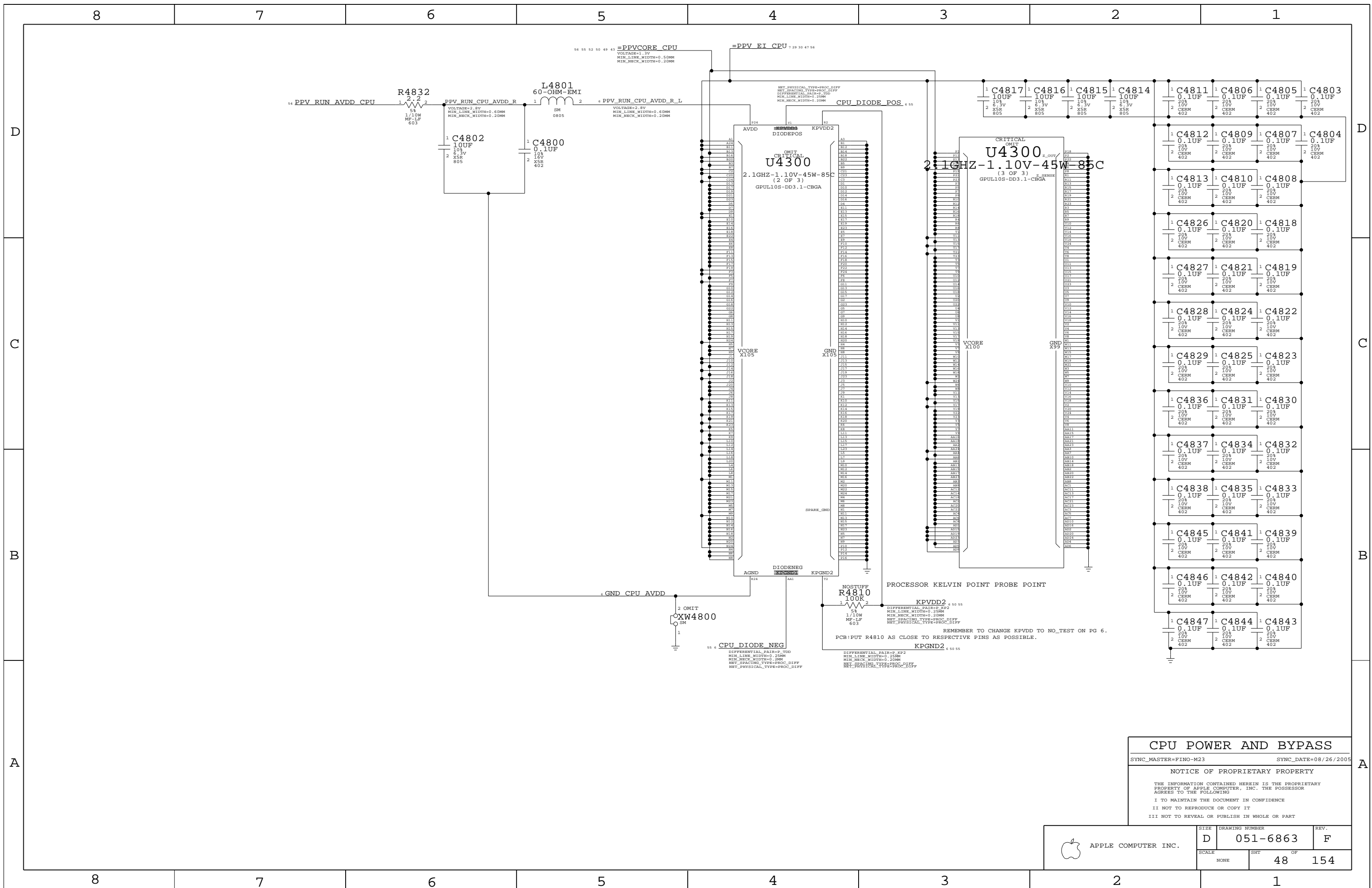
CPU STRAPS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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SCALE	SHEET OF		
NONE	47 OF		154



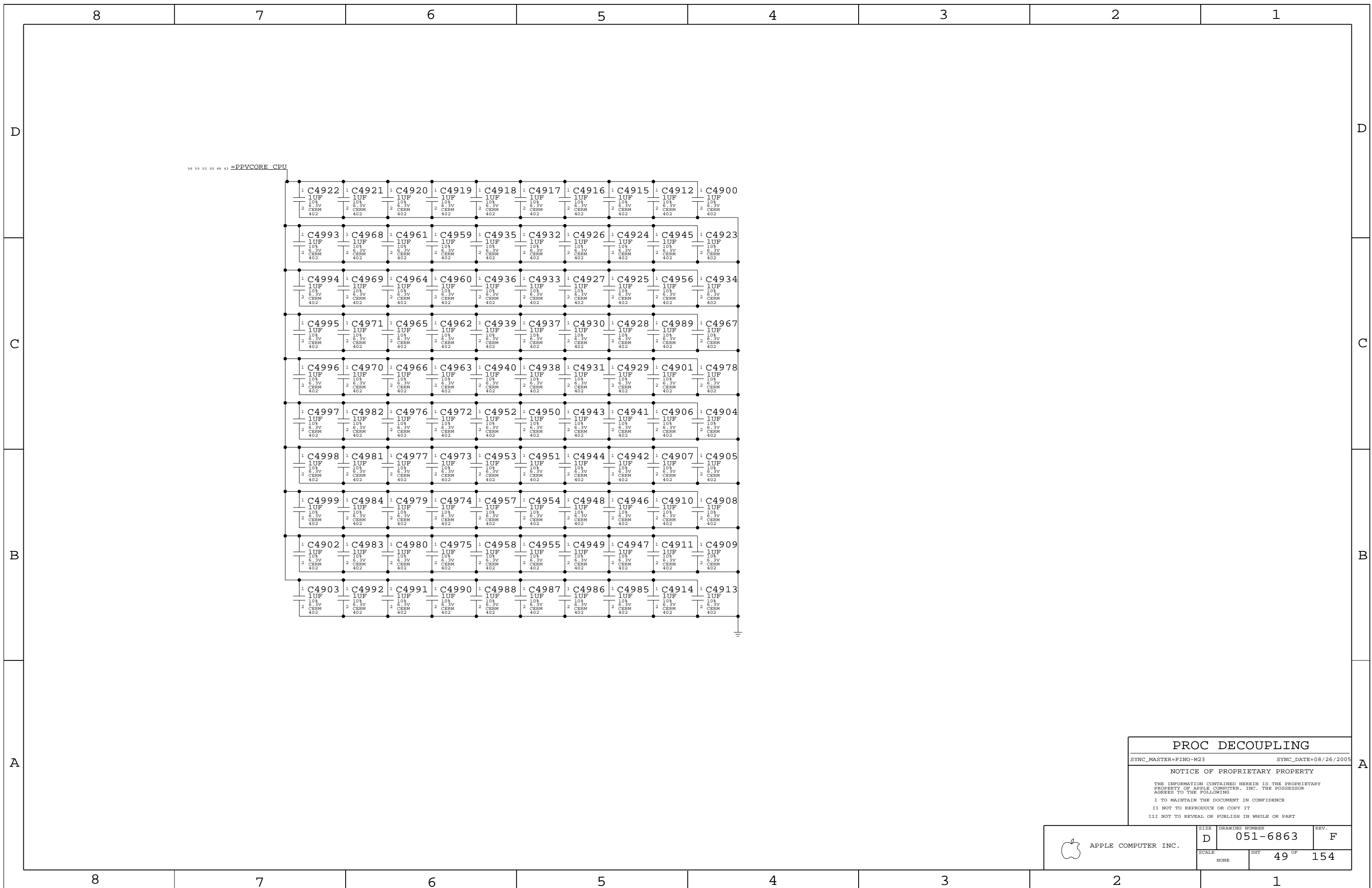
CPU POWER AND BYPASS

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SCALE	NONE	SHT	OF
		48	154



PROC DECOUPLING

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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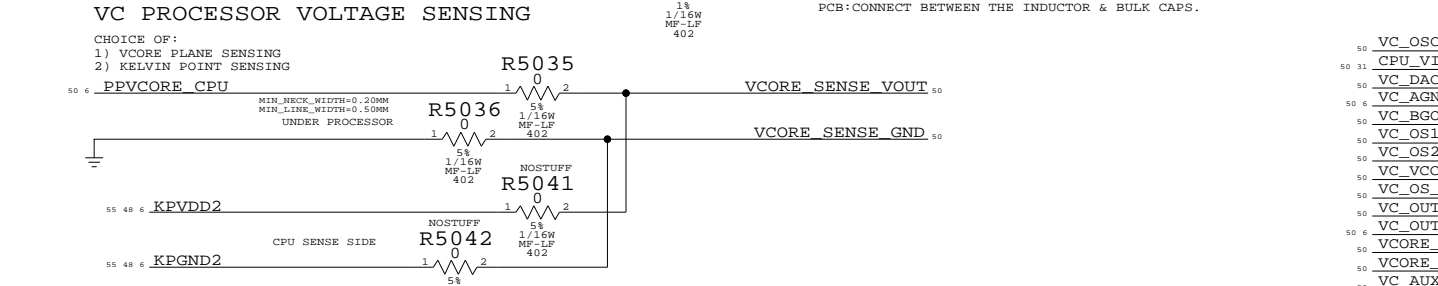
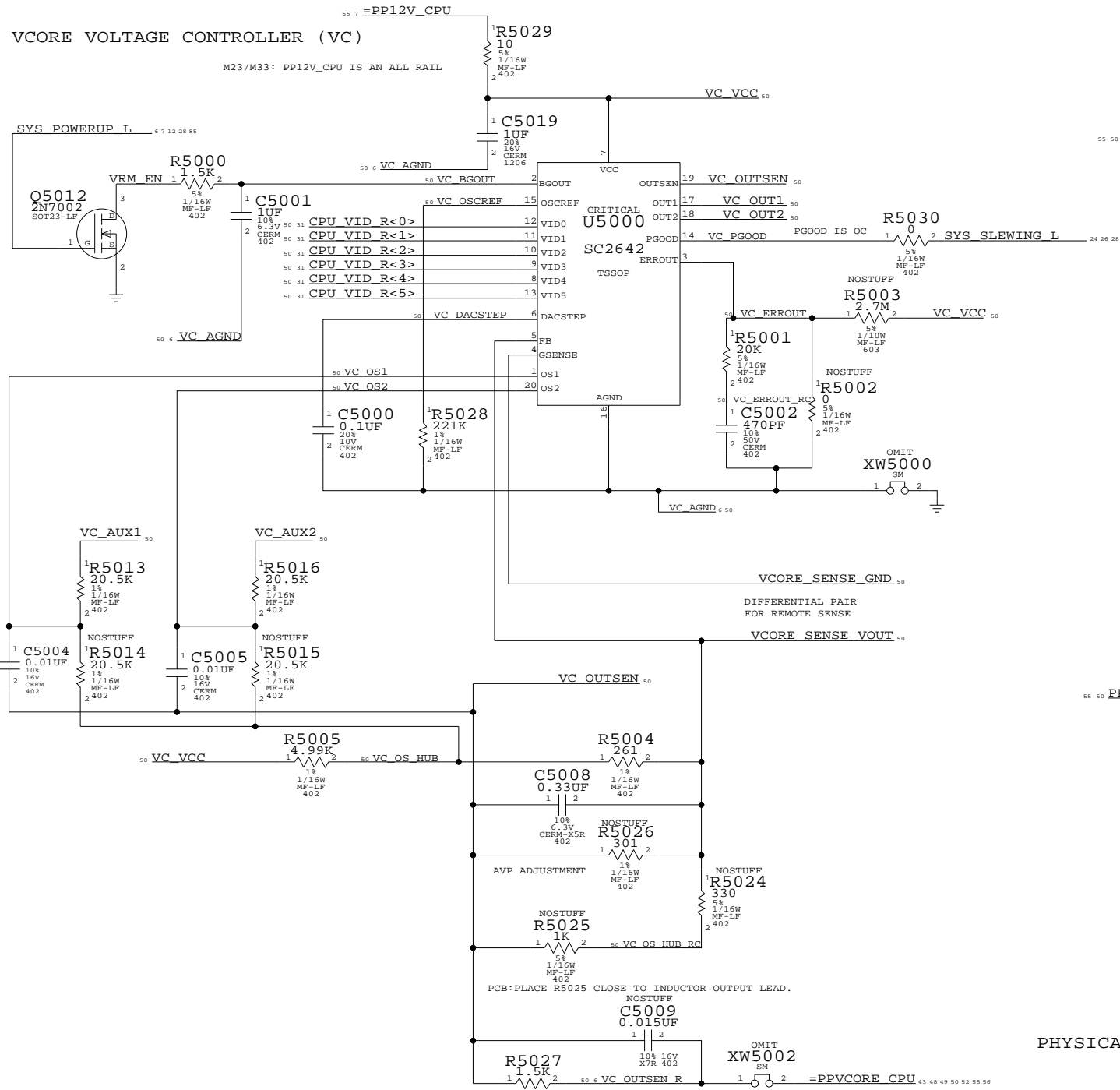
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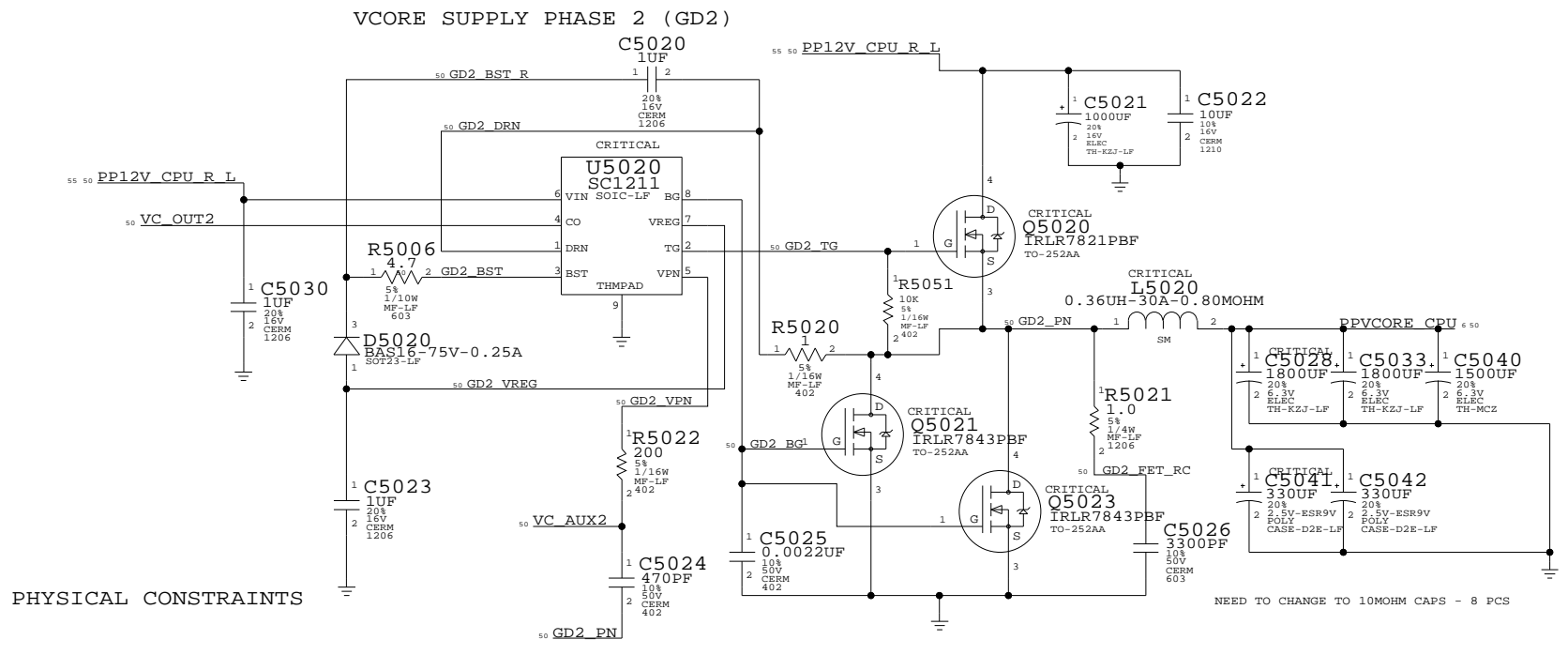
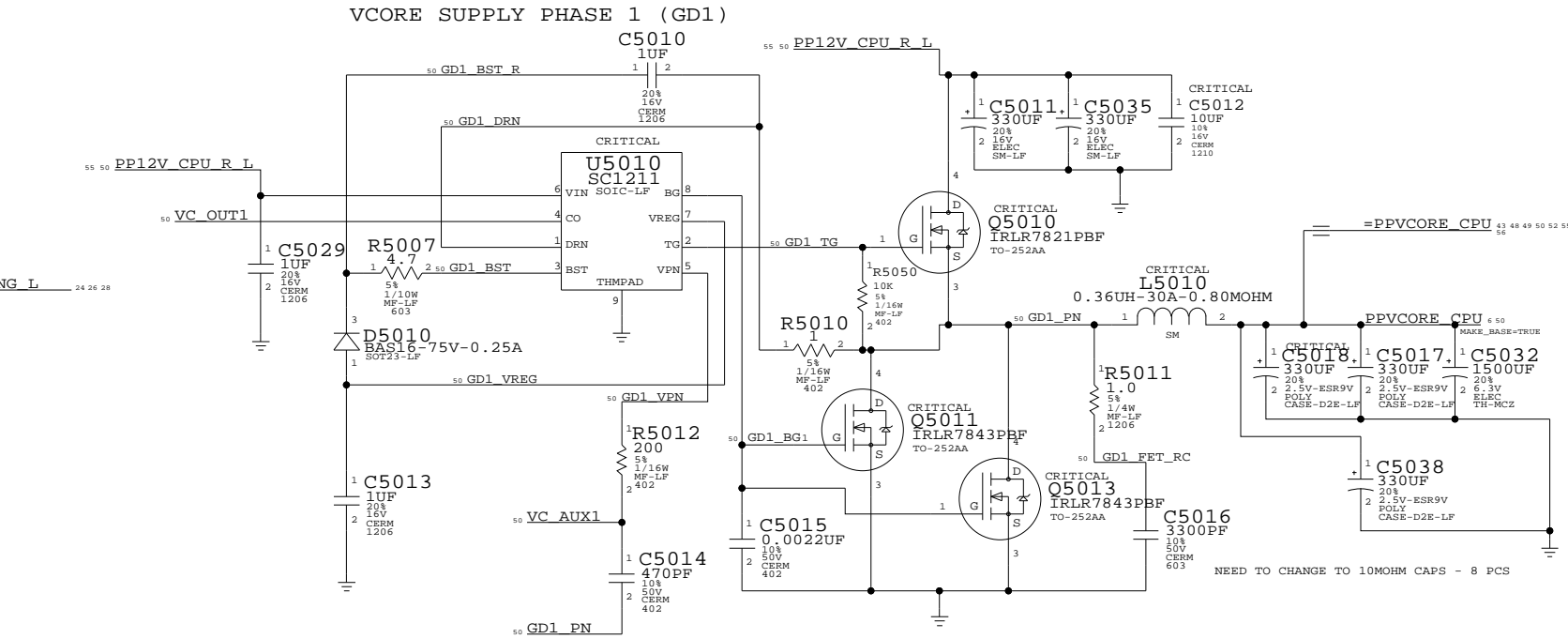
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. F
	SCALE NONE	SHT 49 OF	154



Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GD1_DRN	0.25 MM	0.25 MM	GD2_DRN	0.25 MM	0.25 MM
GD1_BST	0.25 MM	0.25 MM	GD2_BST	0.25 MM	0.25 MM
GD1_VREG	0.25 MM	0.25 MM	GD2_VREG	0.25 MM	0.25 MM
GD1_VPN	0.25 MM	0.25 MM	GD2_VPN	0.25 MM	0.25 MM
GD1_TG	0.25 MM	0.25 MM	GD2_TG	0.25 MM	0.25 MM
GD1_BG	0.25 MM	0.25 MM	GD2_BG	0.25 MM	0.25 MM
GD1_FET_RC	0.25 MM	0.25 MM	GD2_FET_RC	0.25 MM	0.25 MM
GD1_PN	0.60 MM	0.25 MM	GD2_PN	0.25 MM	0.25 MM
GD1_BST_R	0.25 MM	0.25 MM	GD2_BST_R	0.25 MM	0.25 MM



PHYSICAL CONSTRAINTS

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
VC_OSCREF	0.25 MM	0.20 MM
CPU_VID_R<0..5>	0.25 MM	0.20 MM
VC_DACSTEP	0.25 MM	0.20 MM
VC_AGND	0.50 MM	0.20 MM
VC_BGOUT	0.25 MM	0.20 MM
VC_OS1	0.25 MM	0.20 MM
VC_OS2	0.25 MM	0.20 MM
VC_VCC	0.25 MM	0.25 MM
VC_OS_HUB	0.25 MM	0.20 MM
VC_OUTSEN	0.25 MM	0.20 MM
VC_OUTSEN_R	0.25 MM	0.20 MM
VCORE_SENSE_GND	0.25 MM	0.20 MM
VCORE_SENSE_VOUT	0.25 MM	0.20 MM
VC_AUX1	0.25 MM	0.25 MM
VC_AUX2	0.25 MM	0.25 MM
VC_OUT1	0.45 MM	0.25 MM
VC_OUT2	0.45 MM	0.25 MM
VC_ERRROUT	0.25 MM	0.20 MM
VC_ERRROUT_RC	0.25 MM	0.20 MM
VC_OS_HUB_RC	0.25 MM	0.20 MM

CPU VCORE VREG

SYNC_MASTER=M33-HS SYNC_DATE=06/20/2005

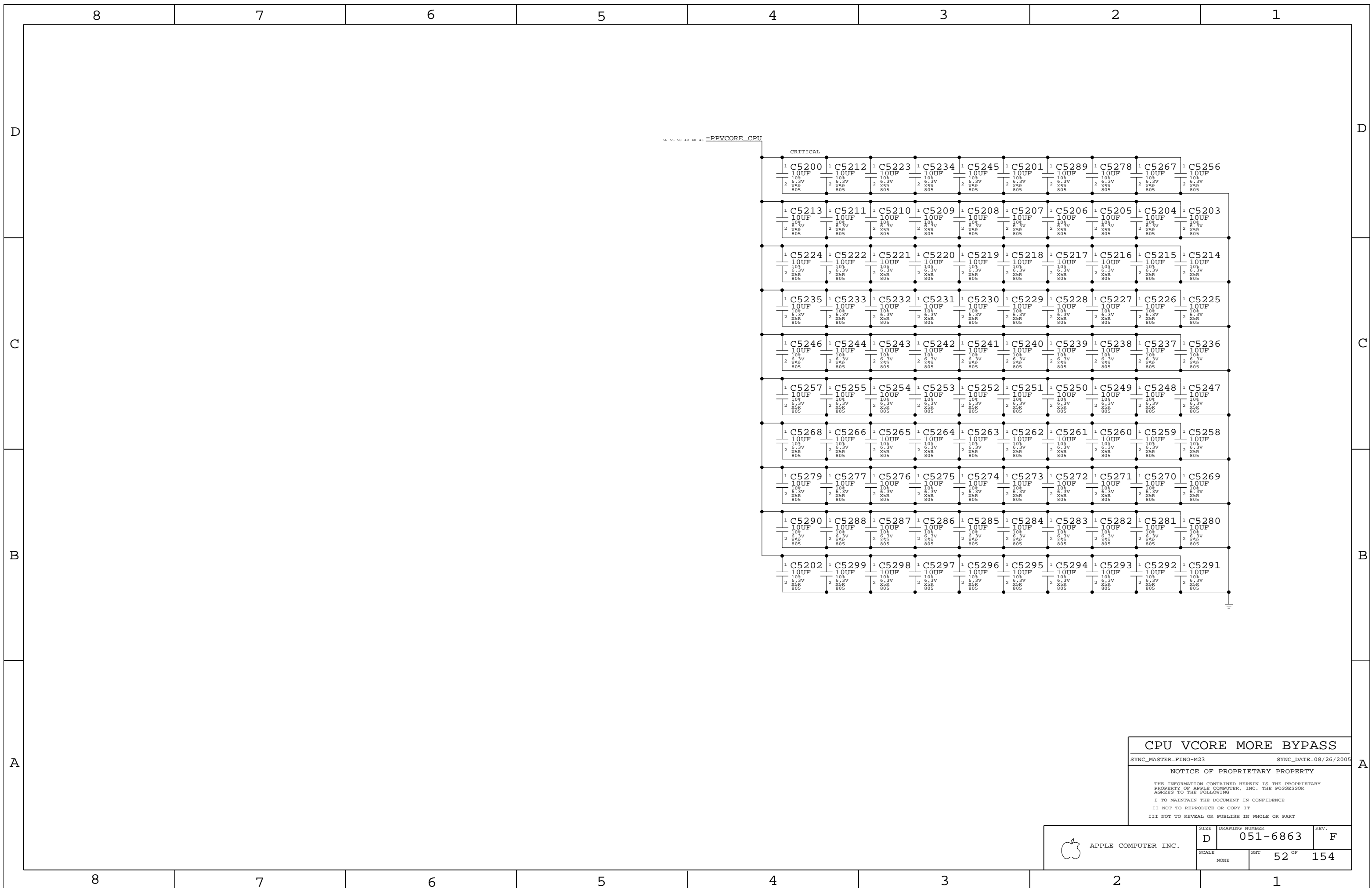
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CPU VCORE MORE BYPASS

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SCALE	SHT		
NONE	52 OF		154

8

7

6

5

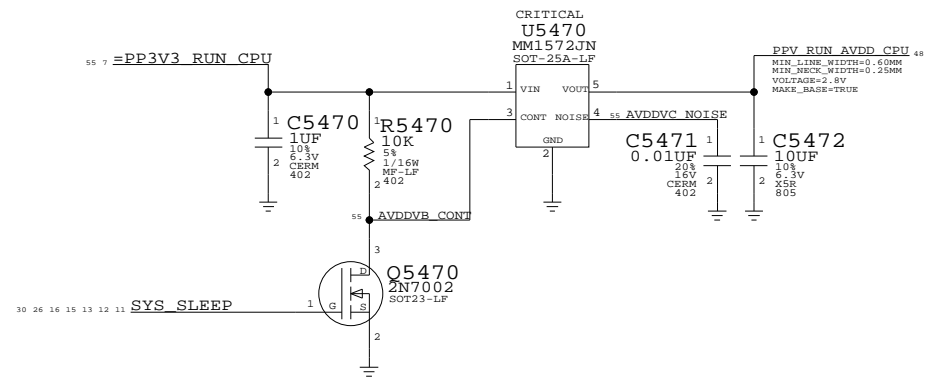
4

3

2

1

PROCESSOR AVDD VREG



CPU AVDD VREG

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

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SCALE	SHT	54 OF 154	
NONE			

8

7

6

5

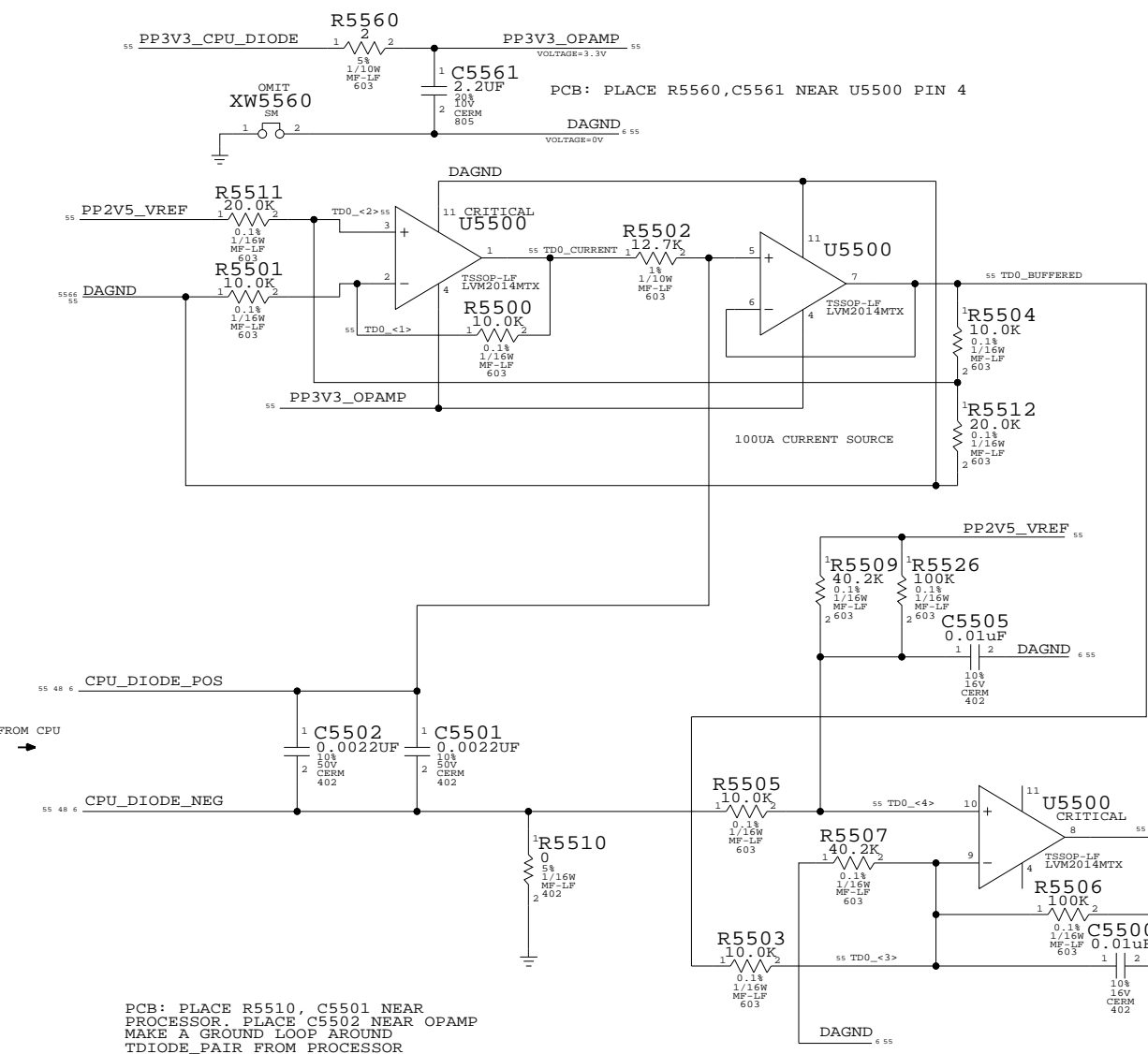
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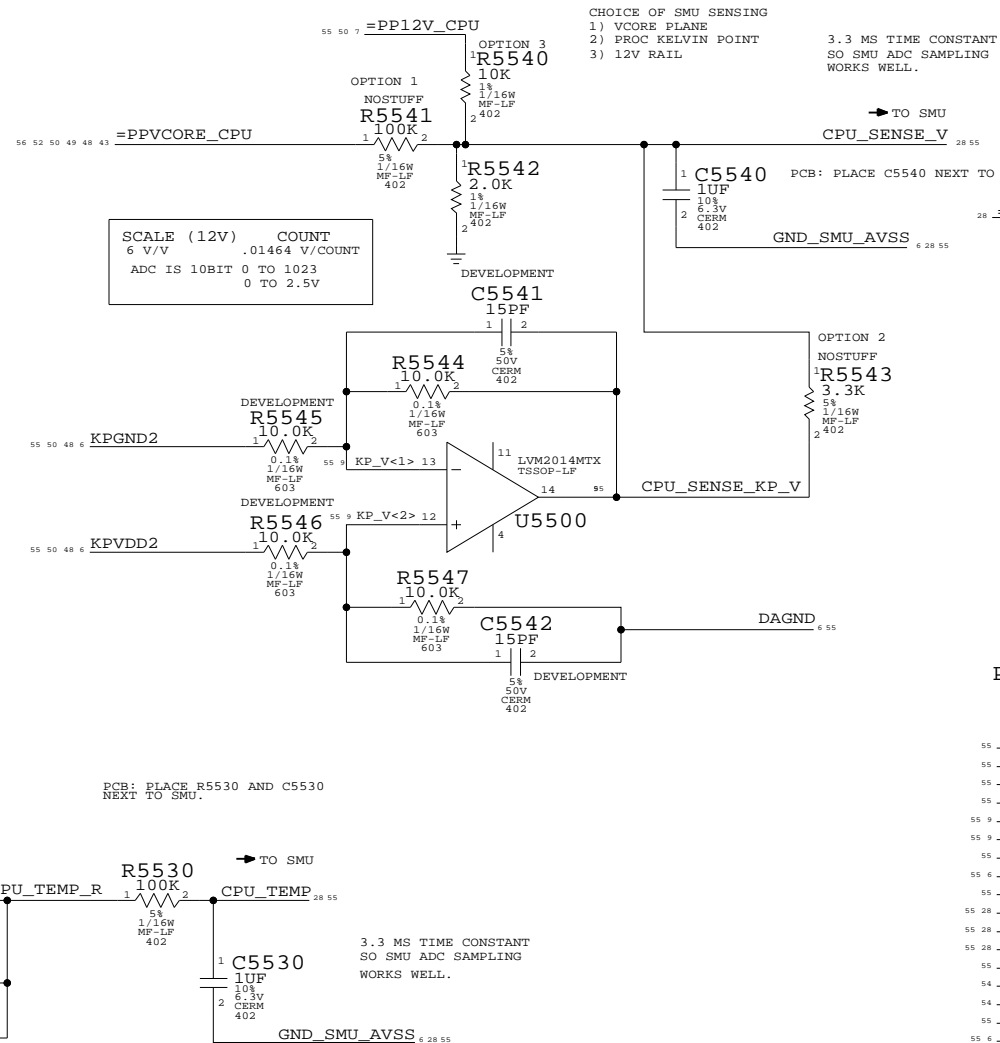
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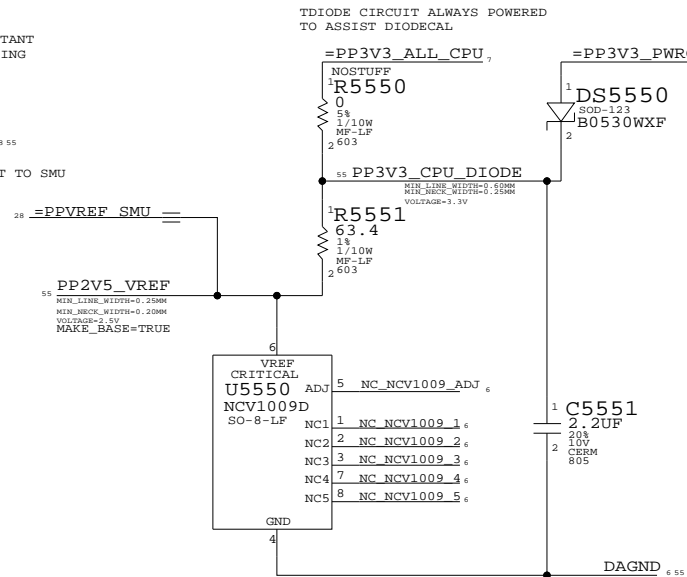
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



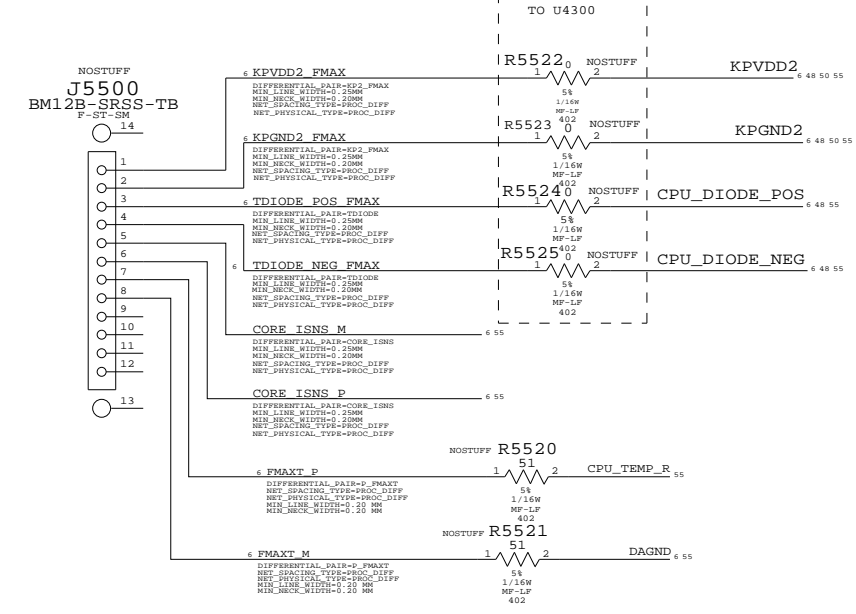
2.5V PRECISION VOLTAGE REFERENCE SOURCE



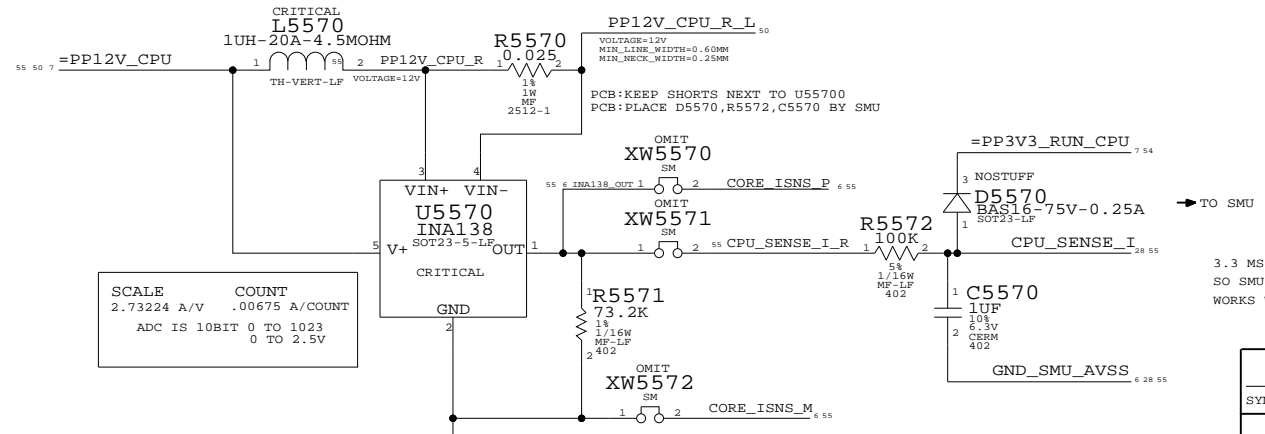
PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0 <1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V <1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.25 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE (USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T, V, I SENSORS
 SYNC_MASTER=FINO-M23 SYNC_DATE=08/29/2005
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CONNECT PULSAR CLKS TO CPU/NB

56 43 9	EI_CPU_SYSCLK_P	==	EI_CPU_A_SYSCLK_P	26
56 43 9	EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N	26
56 43 9	EI_CPU_APSYNC	==	CPU_A_APSYNC	26
56 43 9	EI_CPU_TREN_CLK	MAKE_BASE=TRUE	CPU_A_TREN_CLK_US	26
56 43 9	EI_NB_APSYNC	==	NB_APSYNC	26 42

CONNECT KODIAK EI A TO/FROM CPU

56 43 9	EI_NB_TO_CPU_CLK_P	==	EI_NB_TO_CPU_A_CLK_P	42
56 43 9	EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N	42
56 43 9	EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43>	42
56 43 9	EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1>	42
56 43 9	EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1>	42
56 43 9	EI_CPU_TO_NB_CLK_P	==	EI_CPU_A_TO_NB_CLK_P	42
56 43 9	EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N	42
56 43 9	EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43>	42
56 43 9	EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1>	42
56 43 9	EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1>	42

CONNECT CPU TO KODIAK QREQ A0

43	CPU_TO_NB_QREQ_L	==	CPU_A0_TO_NB_QREQ_L	42
----	------------------	----	---------------------	----

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

43	CPU_QACK_L	==	CPU_A0_QACK_L	42
43	NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L	42
43	NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L	44
43	NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L	44

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

43	CPU_INT_L	==	CPU_A0_INT_R_L	24 56
43	NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L	42
43	NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L	44
43	NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L	44

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

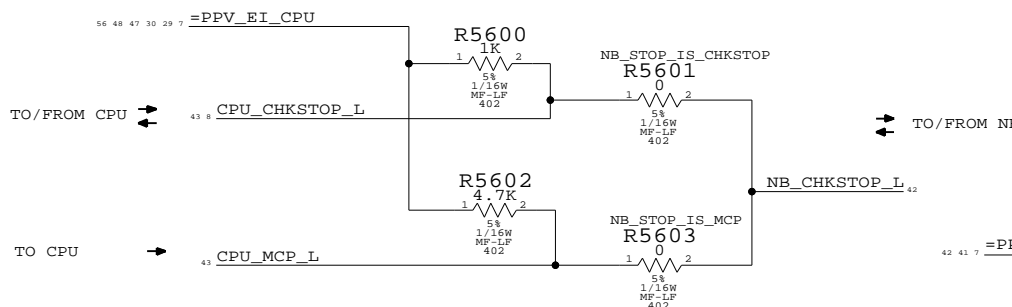
43	CPU_SRESET_L_R	==	SB_CPU_A0_SRESET_L	24 56
43	NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L	24 56
43	NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L	24 56
43	NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L	24 56

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

9	TP_NB_B_TRIGGER_OUT	==	NB_B_TRIGGER_OUT	44
9	TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT	44
9	TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT	43
9	TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN	43 47
9	TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT	43
9	NC_PSR0	MAKE_BASE=TRUE	CPU_PSR0	43
9	NC_PSR0_ENABLE	MAKE_BASE=TRUE	CPU_PSR0_ENABLE	43
9	TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION	43
9	NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN	43

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU_CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
56 43 9	EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	42 26
56 43 9	EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	42 26
56 43 9	EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD	42 26
56 43 9	EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD	42 26
56 43 9	EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD	42 26
56 43 9	EI_NB_TO_CPU_CLK_P	EINCCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	42 26
56 43 9	EI_NB_TO_CPU_CLK_N	EINCCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	42 26
56 43 9	EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD	42 26
56 43 9	EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD	42 26
56 43 9	EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD	42 26
56 43 9	EI_NB_APSYNC	EIPNAPSNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD	42 26
56 43 9	EI_CPU_APSYNC	EIPCAPSNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD	42 26
56 43 9	EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	42 26
56 43 9	EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	42 26
56 43 9	EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	42 26
56 43 9	EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	42 26
56 43 9	EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD	42 26
56 43 9	EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD	42 26

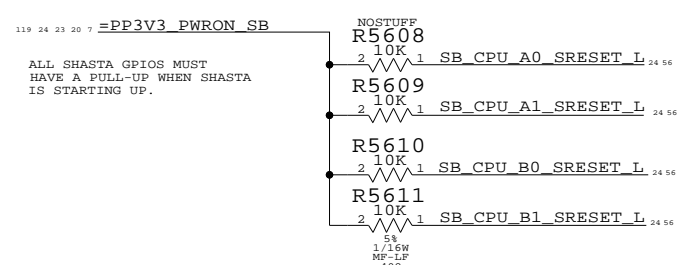
NC KODIAK EI B OUTPUT PORT

43	NC_EI_NB_TO_CPU_B_CLK_P	==	EI_NB_TO_CPU_B_CLK_P	44
43	NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N	44
43	NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43>	44
43	NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1>	44
43	NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1>	44

NC KODIAK EI B INPUT PORT

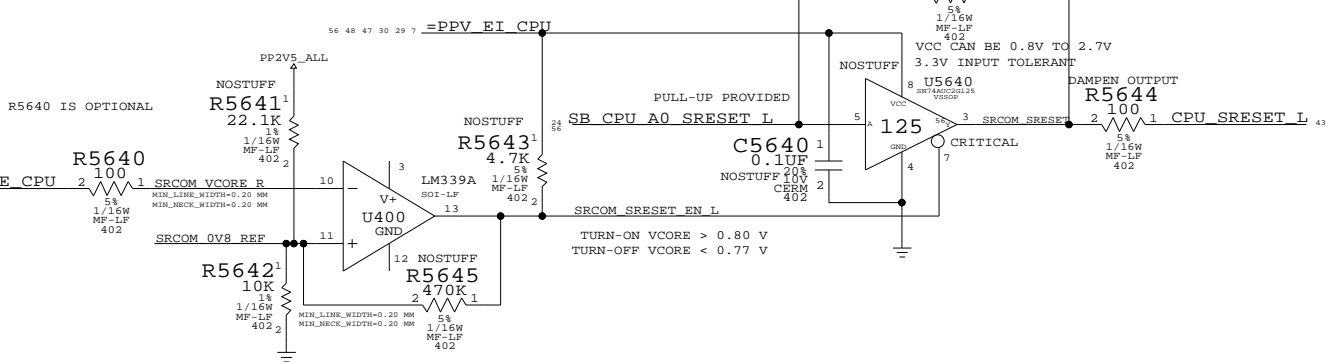
44	NC_EI_CPU_B_TO_NB_CLK_P	==	EI_CPU_B_TO_NB_CLK_P	44
44	NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N	44
44	NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43>	44
44	NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1>	44
44	NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1>	44

PULLUPS FOR SRESET'S FROM SHASTA



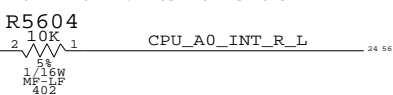
SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVOID IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.



NOTE, NB UNUSED INTS DO NOT REQUIRE PULLUPS, ONLY SHASTA (SINCE ITS OUTPUTS ARE TEMPORARILY INPUTS ON BOOTUP).

INT PULLUP IS SO INT PIN IS NOT FLOATING TO PROCESSOR BUT WEAK TO ALLOW KODIAK TO DRIVE PUSH-PULL STRONGLY



CPU ALIASES & MISC

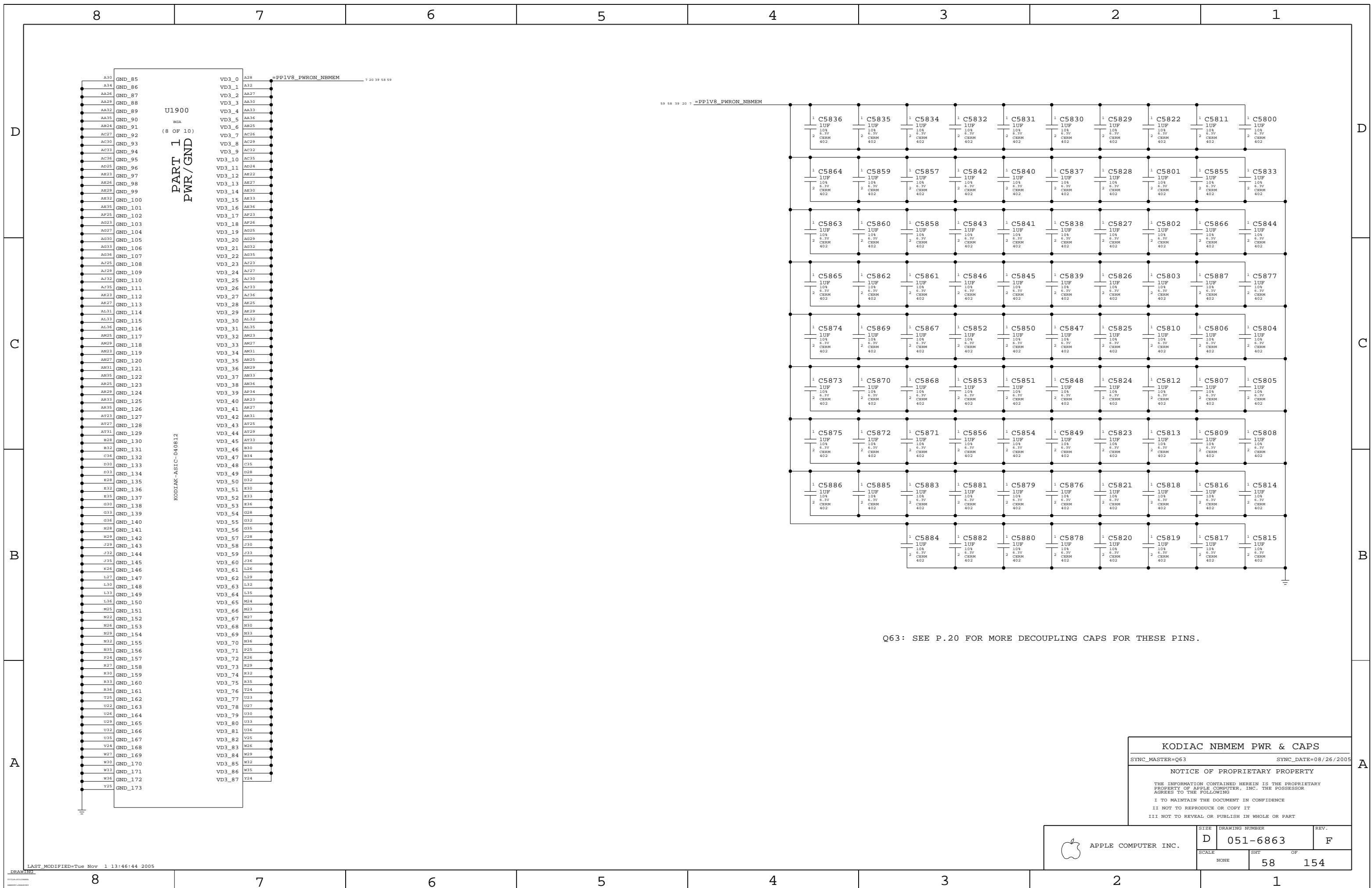
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	NONE	SHT	OF
		56	154



U1900
 (8 OF 10)
 PWR/GND

KODIAK-ASIC-040812

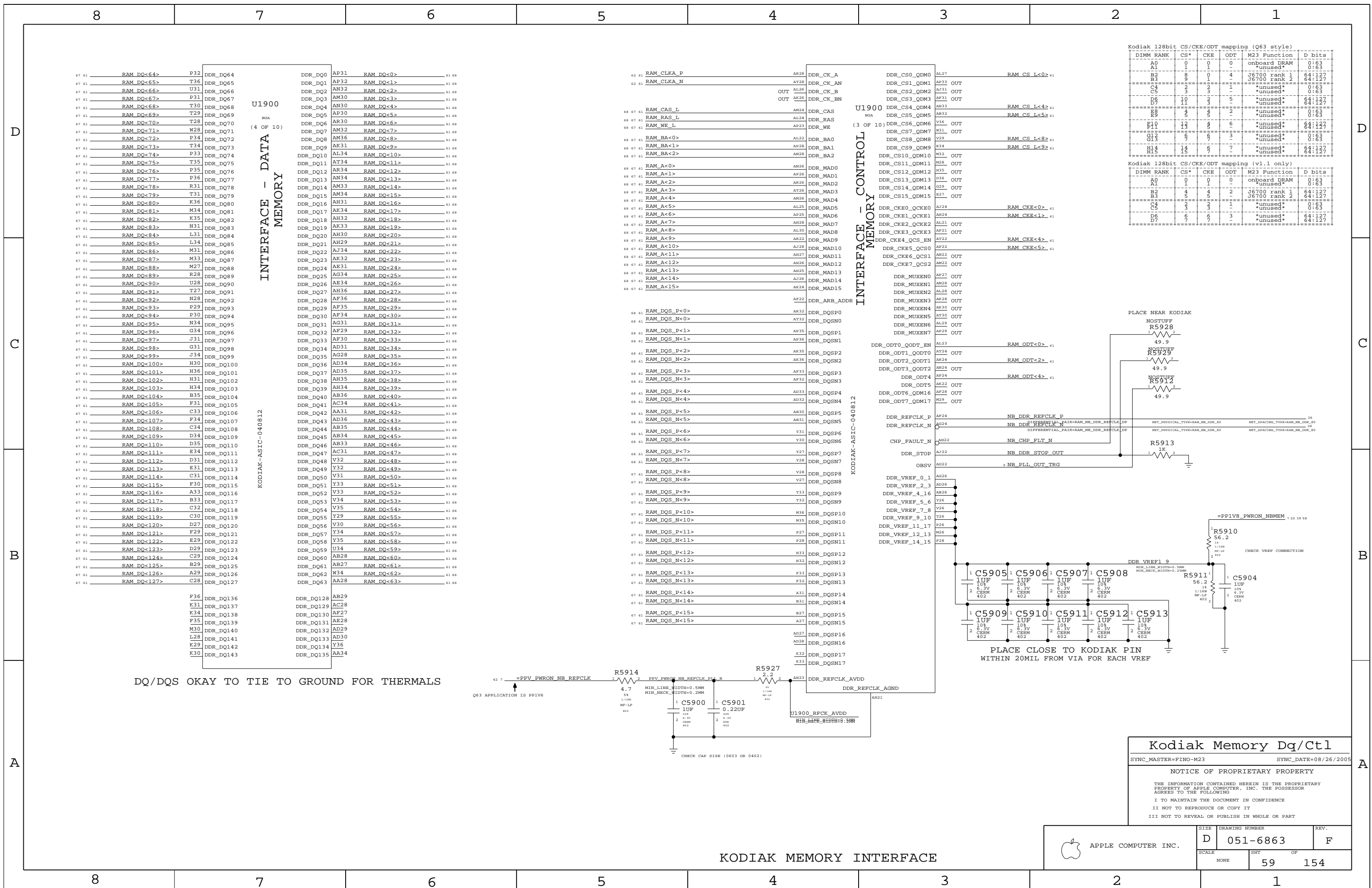
=PP1V8_PWRON_NBMEM

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

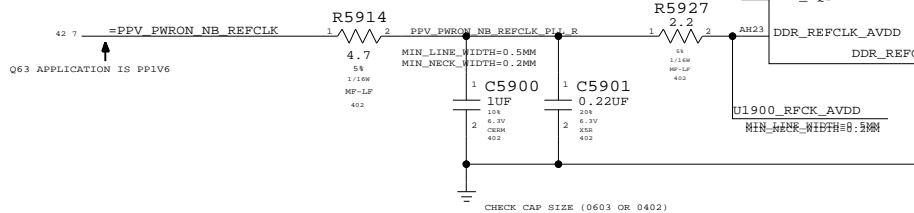
KODIAK NBMEM PWR & CAPS
 SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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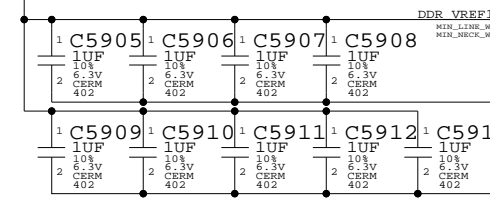
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	58		154



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS



PLACE CLOSE TO KODIAK PIN WITHIN 20MIL FROM VIA FOR EACH VREF



Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	1	onboard DRAM	0:63
B2	8	0	4	U6700 rank 1	64:127
B3	9	1	4	U6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	2	1	*unused*	0:63
D6	10	3	2	*unused*	64:127
D7	11	3	2	*unused*	64:127
E8	5	5	2	*unused*	0:63
E9	6	5	2	*unused*	0:63
F10	13	4	6	*unused*	64:127
F11	14	4	6	*unused*	64:127
G12	7	6	3	*unused*	0:63
G13	8	6	3	*unused*	0:63
H14	15	6	7	*unused*	64:127
H15	16	6	7	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

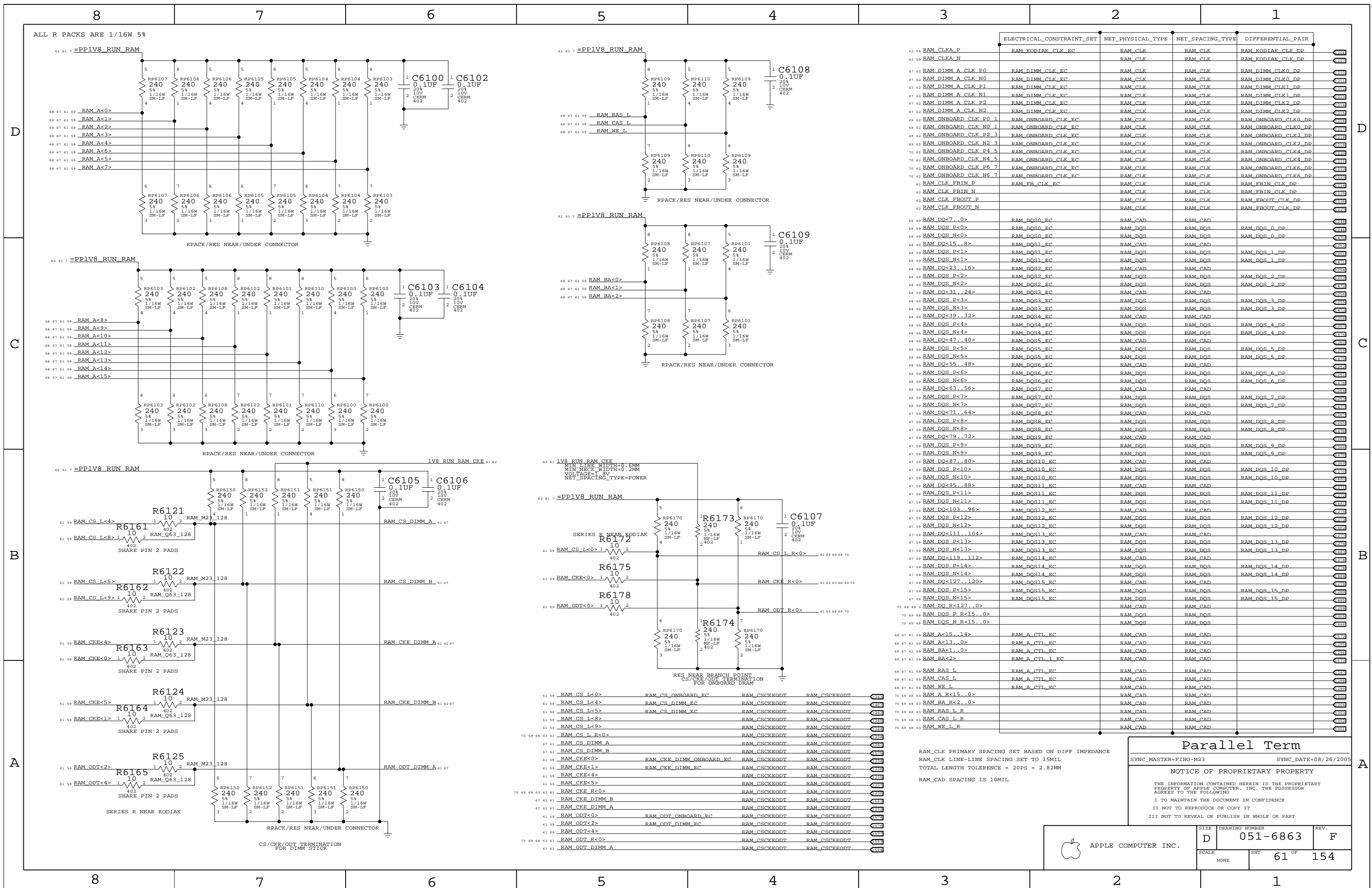
DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	1	onboard DRAM	0:63
B2	4	4	2	U6700 rank 1	64:127
B3	5	5	2	U6700 rank 2	64:127
C4	3	3	1	*unused*	0:63
C5	2	2	1	*unused*	0:63
D6	10	6	7	*unused*	64:127
D7	11	6	7	*unused*	64:127

Kodiak Memory Dq/Ctl
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D	051-6863	F
SCALE	SHEET	OF
NONE	59	154

KODIAK MEMORY INTERFACE



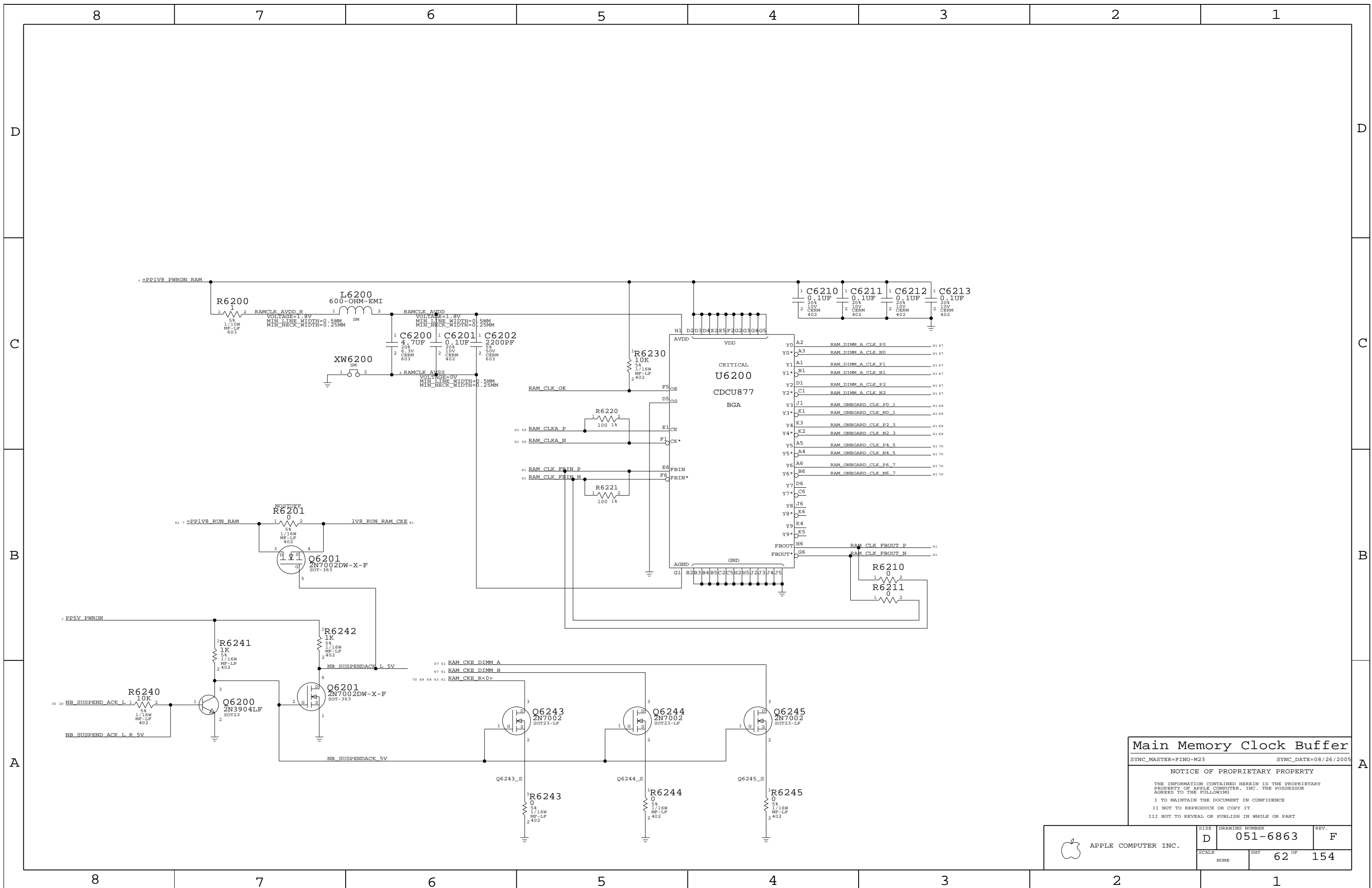
ALL R PACKS ARE 1/16W 5%

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
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62 61 7 =PP1V8_RUN_RAM	RAM_CLKA_P	RAM_CLK	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	4905
62 61 7 =PP1V8_RUN_RAM	RAM_CLKA_N	RAM_CLK	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	4906
62 61 7 =PP1V8_RUN_RAM	RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK0_DP		4907
62 61 7 =PP1V8_RUN_RAM	RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK0_DP		4908
62 61 7 =PP1V8_RUN_RAM	RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK1_DP		4909
62 61 7 =PP1V8_RUN_RAM	RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK1_DP		4910
62 61 7 =PP1V8_RUN_RAM	RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK2_DP		4911
62 61 7 =PP1V8_RUN_RAM	RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK2_DP		4912
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK0_DP		4913
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK0_DP		4914
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK2_DP		4915
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK2_DP		4916
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK4_DP		4917
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK4_DP		4918
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK6_DP		4919
62 61 7 =PP1V8_RUN_RAM	RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK6_DP		4920
62 61 7 =PP1V8_RUN_RAM	RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBIN_CLK_DP		4921
62 61 7 =PP1V8_RUN_RAM	RAM_CLK_FBIN_N	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBIN_CLK_DP		4922
62 61 7 =PP1V8_RUN_RAM	RAM_CLK_FBOUT_P	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBOUT_CLK_DP		4923
62 61 7 =PP1V8_RUN_RAM	RAM_CLK_FBOUT_N	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBOUT_CLK_DP		4924
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<7..0>	RAM_DQS0_EC	RAM_DQS0_EC	RAM_DQS_0_DP		4925
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS0_EC	RAM_DQS_0_DP		4926
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS0_EC	RAM_DQS_0_DP		4927
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<15..8>	RAM_DQS1_EC	RAM_DQS1_EC	RAM_DQS_1_DP		4928
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS1_EC	RAM_DQS_1_DP		4929
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS1_EC	RAM_DQS_1_DP		4930
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<23..16>	RAM_DQS2_EC	RAM_DQS2_EC	RAM_DQS_2_DP		4931
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS2_EC	RAM_DQS_2_DP		4932
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS2_EC	RAM_DQS_2_DP		4933
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<31..24>	RAM_DQS3_EC	RAM_DQS3_EC	RAM_DQS_3_DP		4934
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS3_EC	RAM_DQS_3_DP		4935
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS3_EC	RAM_DQS_3_DP		4936
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<39..32>	RAM_DQS4_EC	RAM_DQS4_EC	RAM_DQS_4_DP		4937
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS4_EC	RAM_DQS_4_DP		4938
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS4_EC	RAM_DQS_4_DP		4939
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<47..40>	RAM_DQS5_EC	RAM_DQS5_EC	RAM_DQS_5_DP		4940
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS5_EC	RAM_DQS_5_DP		4941
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS5_EC	RAM_DQS_5_DP		4942
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<55..48>	RAM_DQS6_EC	RAM_DQS6_EC	RAM_DQS_6_DP		4943
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS6_EC	RAM_DQS_6_DP		4944
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS6_EC	RAM_DQS_6_DP		4945
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<63..56>	RAM_DQS7_EC	RAM_DQS7_EC	RAM_DQS_7_DP		4946
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS7_EC	RAM_DQS_7_DP		4947
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS7_EC	RAM_DQS_7_DP		4948
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<71..64>	RAM_DQS8_EC	RAM_DQS8_EC	RAM_DQS_8_DP		4949
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS8_EC	RAM_DQS_8_DP		4950
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS8_EC	RAM_DQS_8_DP		4951
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<79..72>	RAM_DQS9_EC	RAM_DQS9_EC	RAM_DQS_9_DP		4952
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS9_EC	RAM_DQS_9_DP		4953
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS9_EC	RAM_DQS_9_DP		4954
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<87..80>	RAM_DQS10_EC	RAM_DQS10_EC	RAM_DQS_10_DP		4955
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS10_EC	RAM_DQS_10_DP		4956
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS10_EC	RAM_DQS_10_DP		4957
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<95..88>	RAM_DQS11_EC	RAM_DQS11_EC	RAM_DQS_11_DP		4958
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS11_EC	RAM_DQS_11_DP		4959
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS11_EC	RAM_DQS_11_DP		4960
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<103..96>	RAM_DQS12_EC	RAM_DQS12_EC	RAM_DQS_12_DP		4961
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS12_EC	RAM_DQS_12_DP		4962
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS12_EC	RAM_DQS_12_DP		4963
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<111..104>	RAM_DQS13_EC	RAM_DQS13_EC	RAM_DQS_13_DP		4964
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS13_EC	RAM_DQS_13_DP		4965
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS13_EC	RAM_DQS_13_DP		4966
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<119..112>	RAM_DQS14_EC	RAM_DQS14_EC	RAM_DQS_14_DP		4967
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS14_EC	RAM_DQS_14_DP		4968
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS14_EC	RAM_DQS_14_DP		4969
62 61 7 =PP1V8_RUN_RAM	RAM_DQ<127..120>	RAM_DQS15_EC	RAM_DQS15_EC	RAM_DQS_15_DP		4970
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS15_EC	RAM_DQS_15_DP		4971
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS15_EC	RAM_DQS_15_DP		4972
62 61 7 =PP1V8_RUN_RAM	RAM_DQ_R<127..0>					4973
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_P_R<15..0>					4974
62 61 7 =PP1V8_RUN_RAM	RAM_DQS_N_R<15..0>					4975
62 61 7 =PP1V8_RUN_RAM	RAM_A<15..14>	RAM_A_CTL_EC	RAM_A_CTL_EC			4976
62 61 7 =PP1V8_RUN_RAM	RAM_A<13..0>	RAM_A_CTL_EC	RAM_A_CTL_EC			4977
62 61 7 =PP1V8_RUN_RAM	RAM_BA<1..0>	RAM_A_CTL_EC	RAM_A_CTL_EC			4978
62 61 7 =PP1V8_RUN_RAM	RAM_BA<2>	RAM_A_CTL_1_EC	RAM_A_CTL_1_EC			4979
62 61 7 =PP1V8_RUN_RAM	RAM_BAS_L	RAM_A_CTL_EC	RAM_A_CTL_EC			4980
62 61 7 =PP1V8_RUN_RAM	RAM_CAS_L	RAM_A_CTL_EC	RAM_A_CTL_EC			4981
62 61 7 =PP1V8_RUN_RAM	RAM_WE_L	RAM_A_CTL_EC	RAM_A_CTL_EC			4982
62 61 7 =PP1V8_RUN_RAM	RAM_A_R<15..0>					4983
62 61 7 =PP1V8_RUN_RAM	RAM_BA_R<2..0>					4984
62 61 7 =PP1V8_RUN_RAM	RAM_RAS_L_R					4985
62 61 7 =PP1V8_RUN_RAM	RAM_CAS_L_R					4986
62 61 7 =PP1V8_RUN_RAM	RAM_WE_L_R					4987
62 61 7 =PP1V8_RUN_RAM	RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		4988
62 61 7 =PP1V8_RUN_RAM	RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4989
62 61 7 =PP1V8_RUN_RAM	RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4990
62 61 7 =PP1V8_RUN_RAM	RAM_CS_L<8>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4991
62 61 7 =PP1V8_RUN_RAM	RAM_CS_L<9>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4992
62 61 7 =PP1V8_RUN_RAM	RAM_CS_L_R<0>	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		4993
62 61 7 =PP1V8_RUN_RAM	RAM_CS_DIMM_A	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		4994
62 61 7 =PP1V8_RUN_RAM	RAM_CS_DIMM_B	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		4995
62 61 7 =PP1V8_RUN_RAM	RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		4996
62 61 7 =PP1V8_RUN_RAM	RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4997
62 61 7 =PP1V8_RUN_RAM	RAM_CKE<4>	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		4998
62 61 7 =PP1V8_RUN_RAM	RAM_CKE<5>	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		4999
62 61 7 =PP1V8_RUN_RAM	RAM_CKE_R<0>	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		5000
62 61 7 =PP1V8_RUN_RAM	RAM_CKE_DIMM_B	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		5001
62 61 7 =PP1V8_RUN_RAM	RAM_CKE_DIMM_A	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		5002
62 61 7 =PP1V8_RUN_RAM	RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		5003
62 61 7 =PP1V8_RUN_RAM	RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		5004
62 61 7 =PP1V8_RUN_RAM	RAM_ODT<4>	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		5005
62 61 7 =PP1V8_RUN_RAM	RAM_ODT_R<0>	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		5006
62 61 7 =PP1V8_RUN_RAM	RAM_ODT_DIMM_A	RAM_CSCKEODT	RAM_CSCKEODT	RAM_CSCKEODT		5007

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
 RAM_CLK LINE-LINE SPACING SET TO 15MIL
 TOTAL LENGTH TOLERANCE = 20PS = 2.82MM
 RAM_CAD SPACING IS 10MIL

Parallel Term
 SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005
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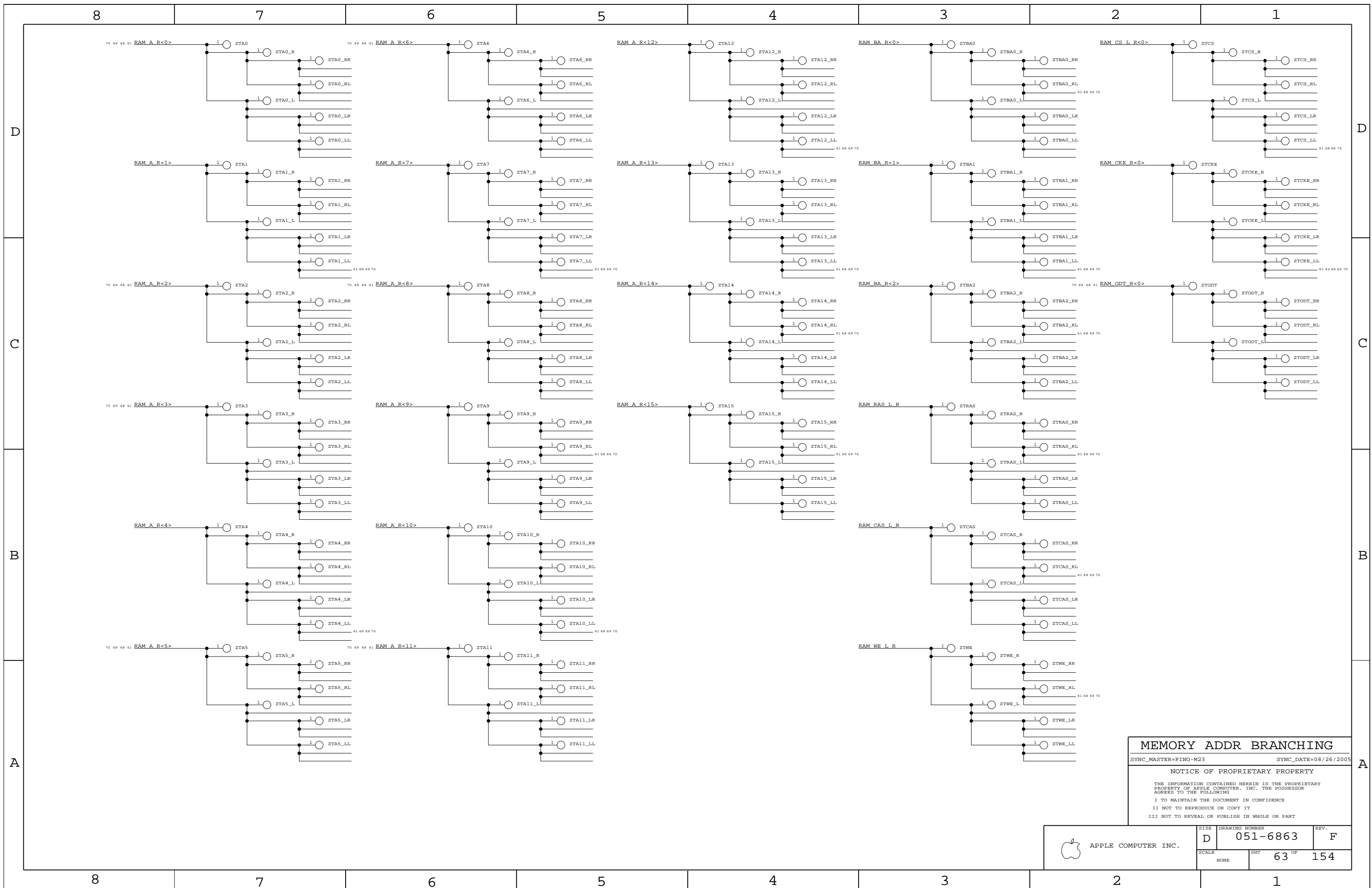
Main Memory Clock Buffer

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. F
	SCALE NONE	SHEET 62 OF 154	



MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005


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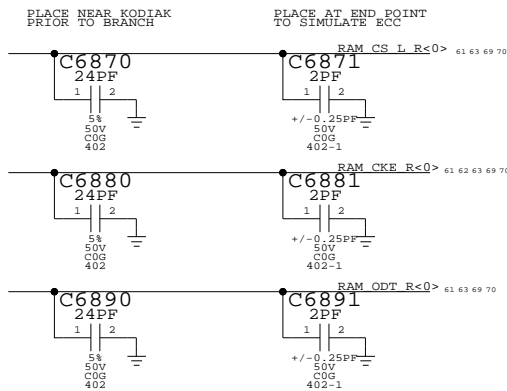
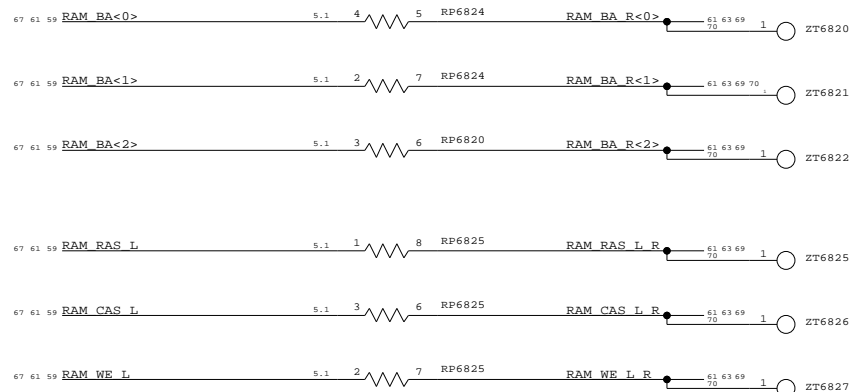
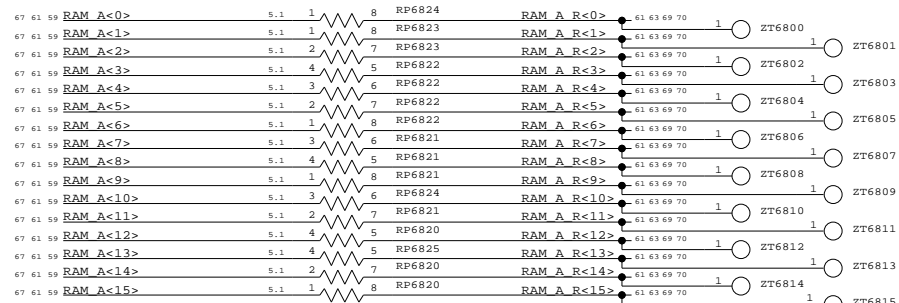
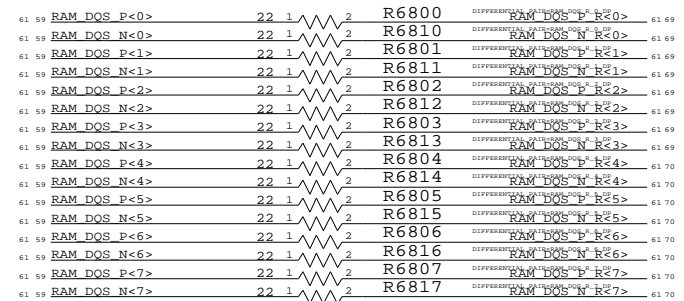
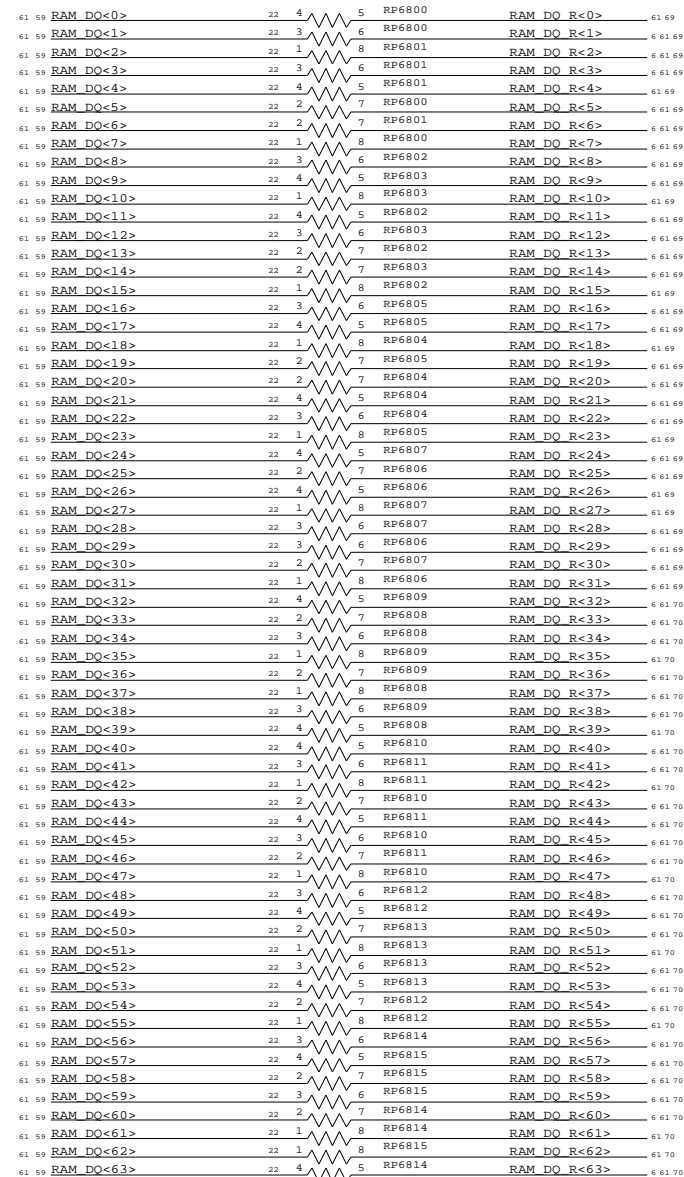
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT	63 OF 154	
NONE			

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A



VIAS FOR ECC STUB

VIAS FOR ECC STUB

MLB Mem Series Term

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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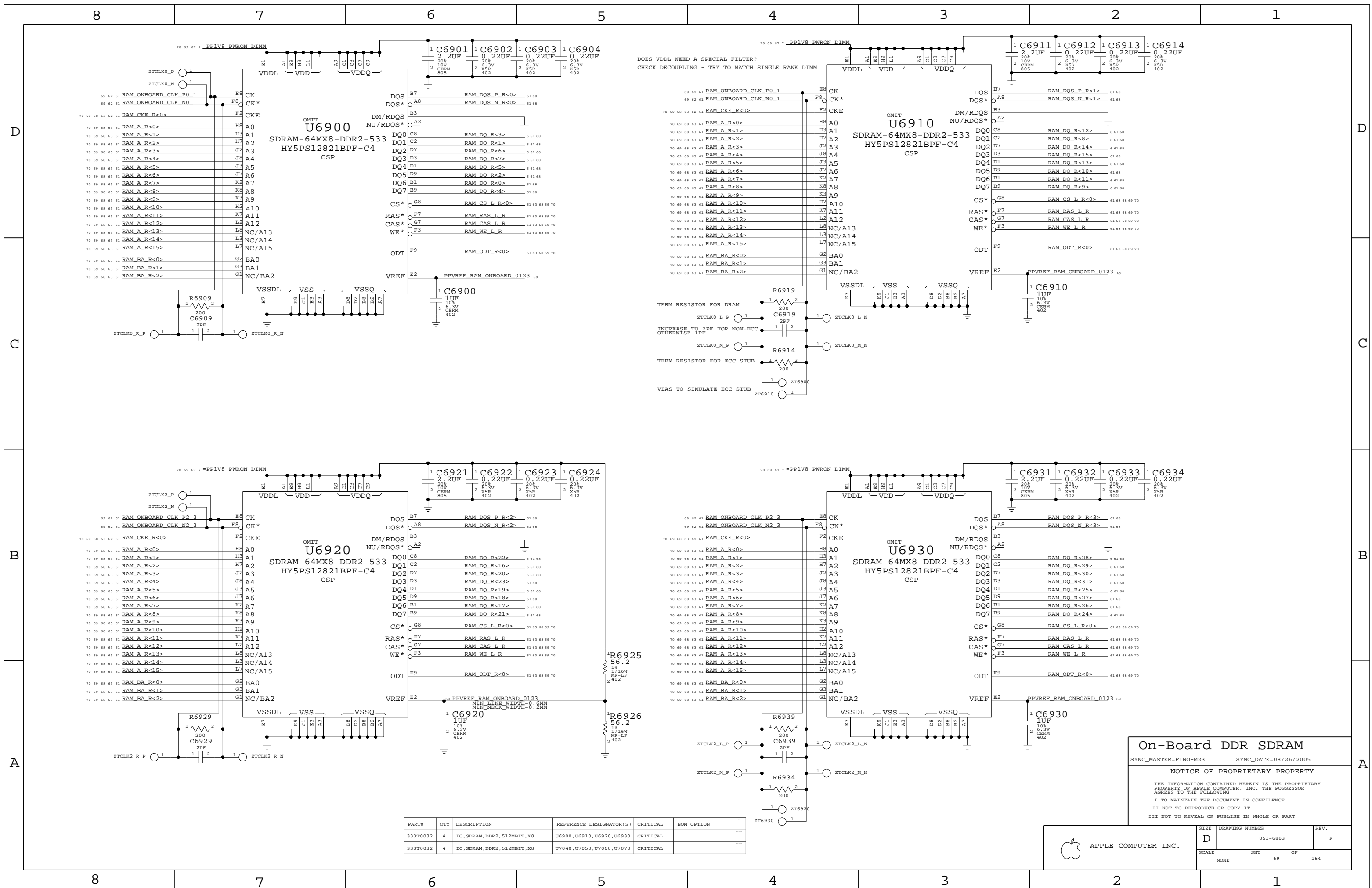


APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6863 F

SCALE NONE SHIT 68 OF 154



DOES VDDL NEED A SPECIAL FILTER?
CHECK DECOUPLING - TRY TO MATCH SINGLE RANK DIMM

On-Board DDR SDRAM

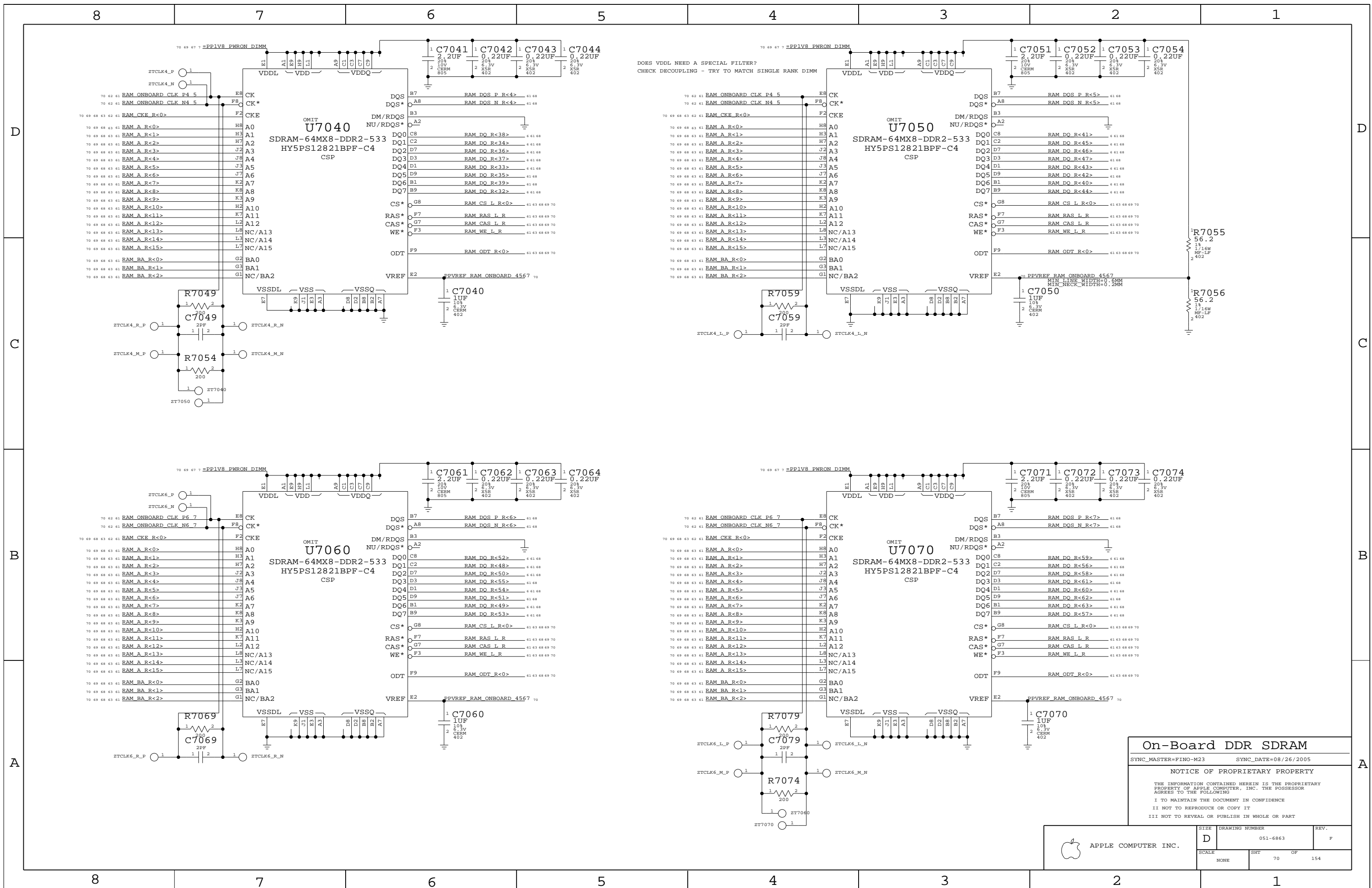
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33370032	4	IC, SDRAM, DDR2, 512MBIT, X8	U6900, U6910, U6920, U6930	CRITICAL	
33370032	4	IC, SDRAM, DDR2, 512MBIT, X8	U7040, U7050, U7060, U7070	CRITICAL	

	APPLE COMPUTER INC.	
	SCALE NONE	SHEET 69 OF 154



DOES VDDL NEED A SPECIAL FILTER?
CHECK DECOUPLING - TRY TO MATCH SINGLE RANK DIMM

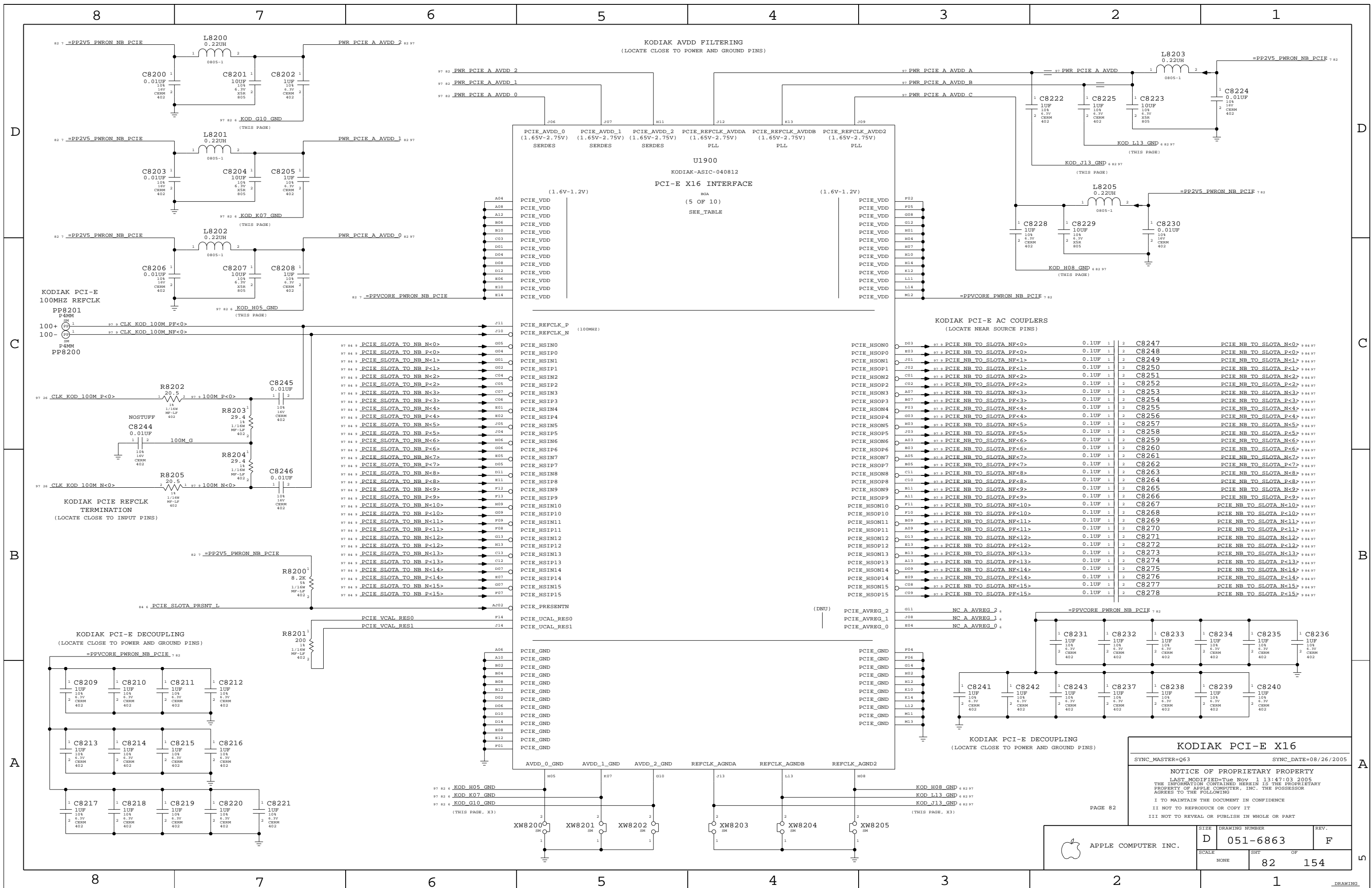
On-Board DDR SDRAM

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. F
	SCALE NONE	SHEET 70	OF 154



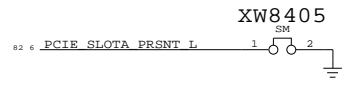
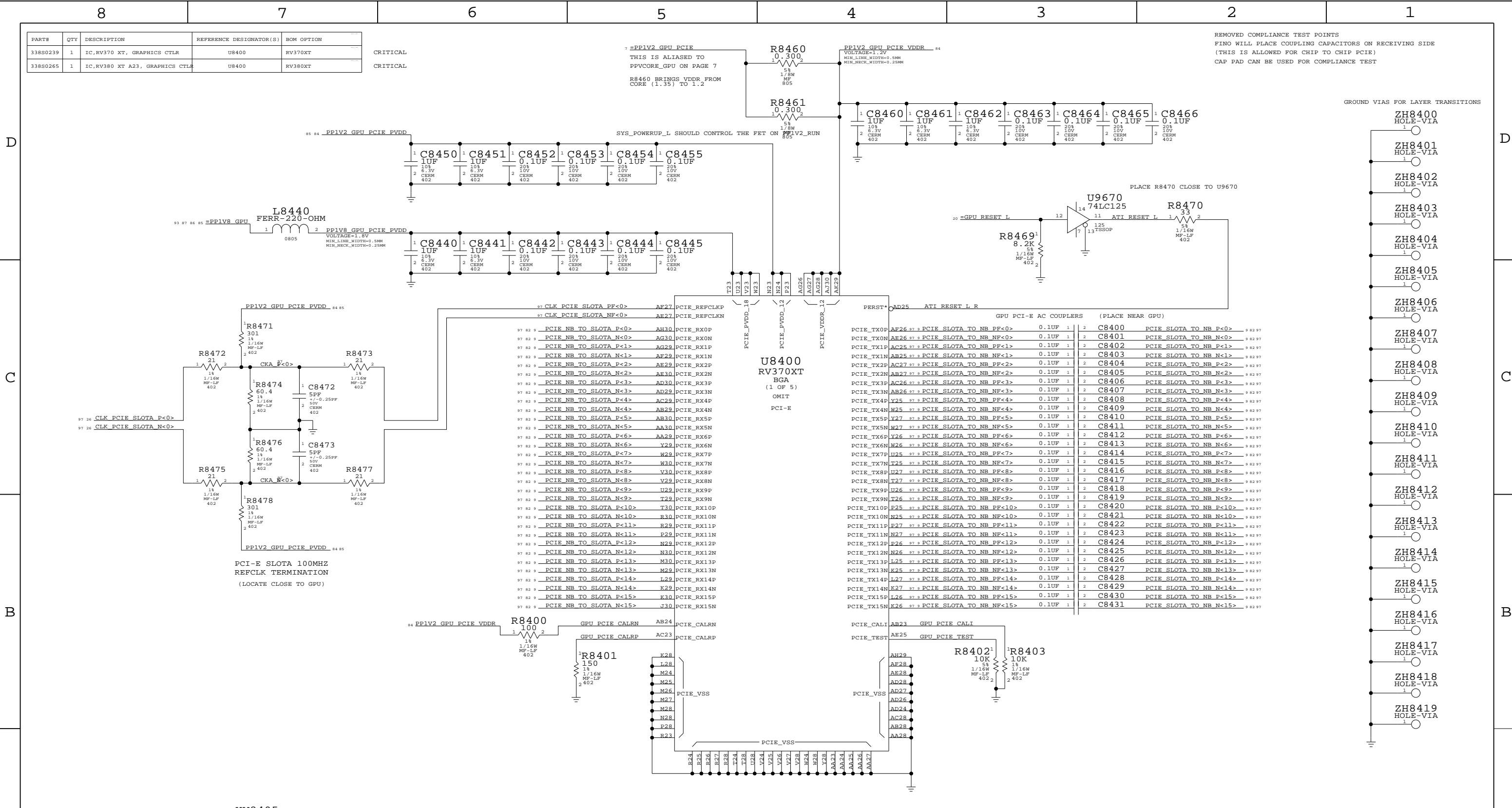
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
33880239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT
33880265	1	IC,RV380 XT A23, GRAPHICS CTLR	U8400	RV380XT

CRITICAL
CRITICAL

≡PPIV2_GPU_PCIE
THIS IS ALIASED TO
PPVCORE_GPU ON PAGE 7
R8460 BRINGS VDDR FROM
CORE (1.35) TO 1.2

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

GROUND VIAS FOR LAYER TRANSITIONS

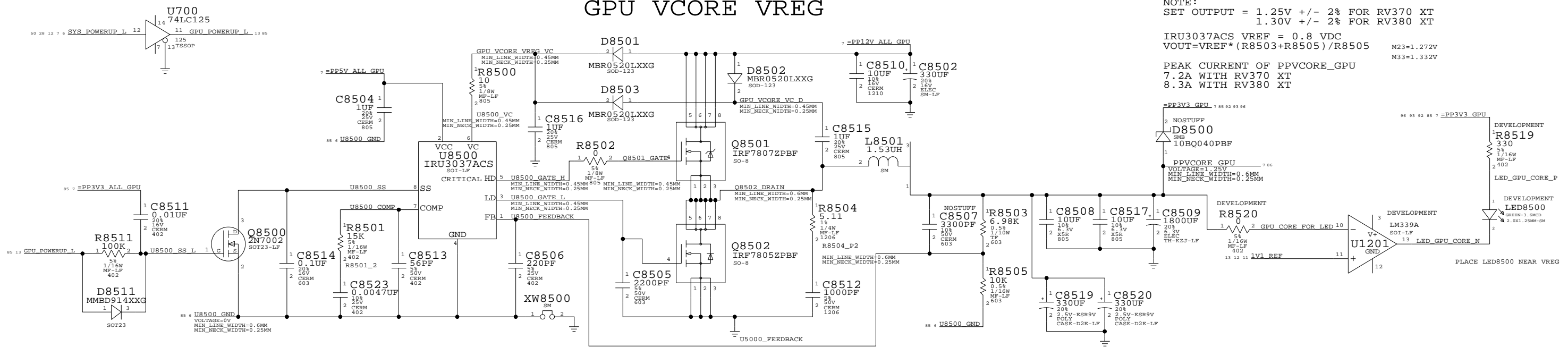


GPU PCIe		
SYNC_MASTER=FINO-M23	SYNC_DATE=08/18/2005	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	84 OF 154		

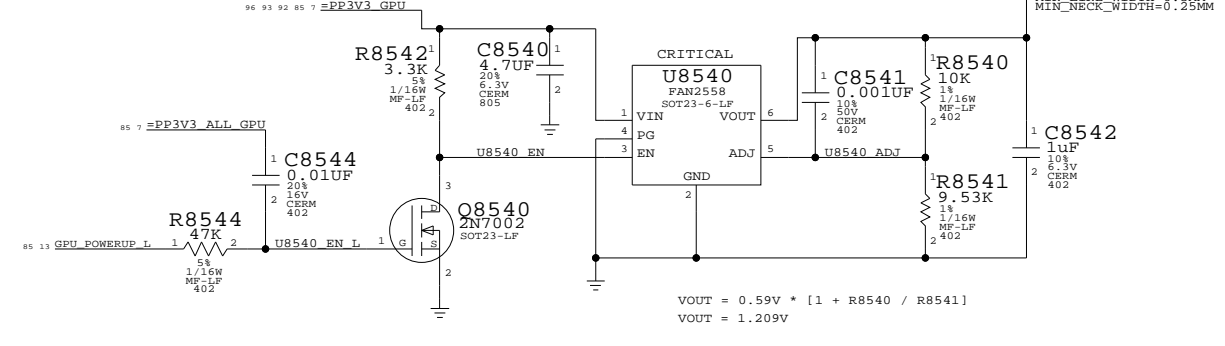
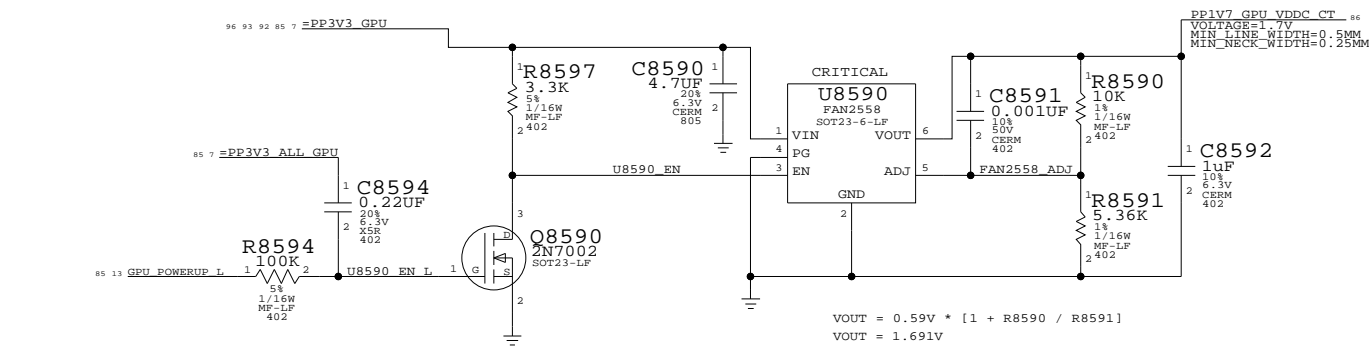
GPU VCORE VREG

NOTE:
 SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
 1.30V +/- 2% FOR RV380 XT
 IRU3037ACS VREF = 0.8 VDC
 VOUT=VREF*(R8503+R8505)/R8505 M23=1.272V
 M33=1.332V
 PEAK CURRENT OF PPVCORE_GPU
 7.2A WITH RV370 XT
 8.3A WITH RV380 XT



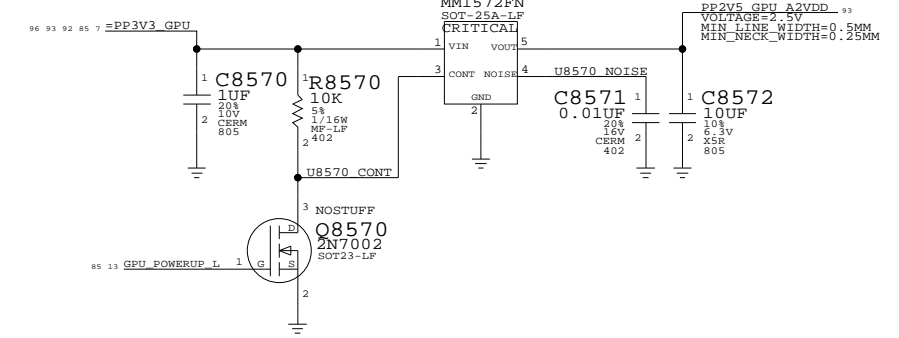
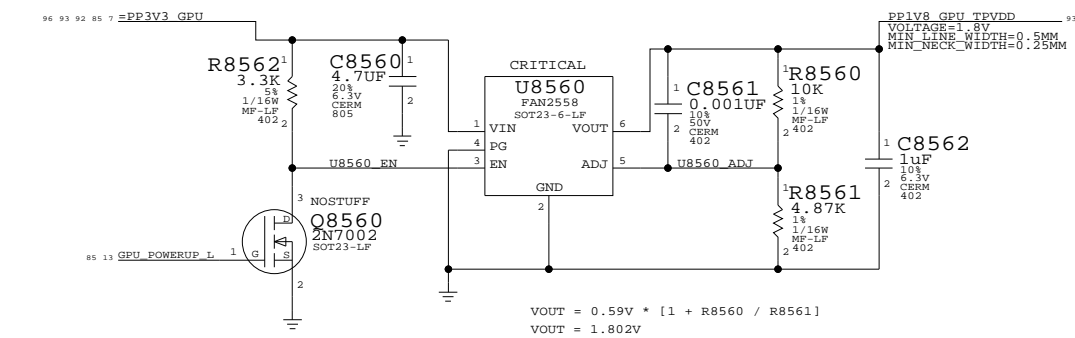
GPU 1.7V VDDC_CT

GPU 1.20V PCIE PVDD

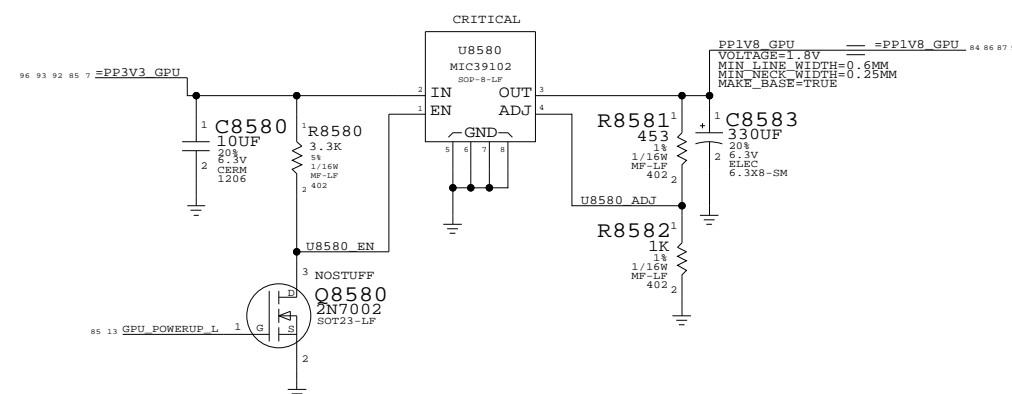


GPU 1.80V TPVDD

GPU 2.5V A2VDD



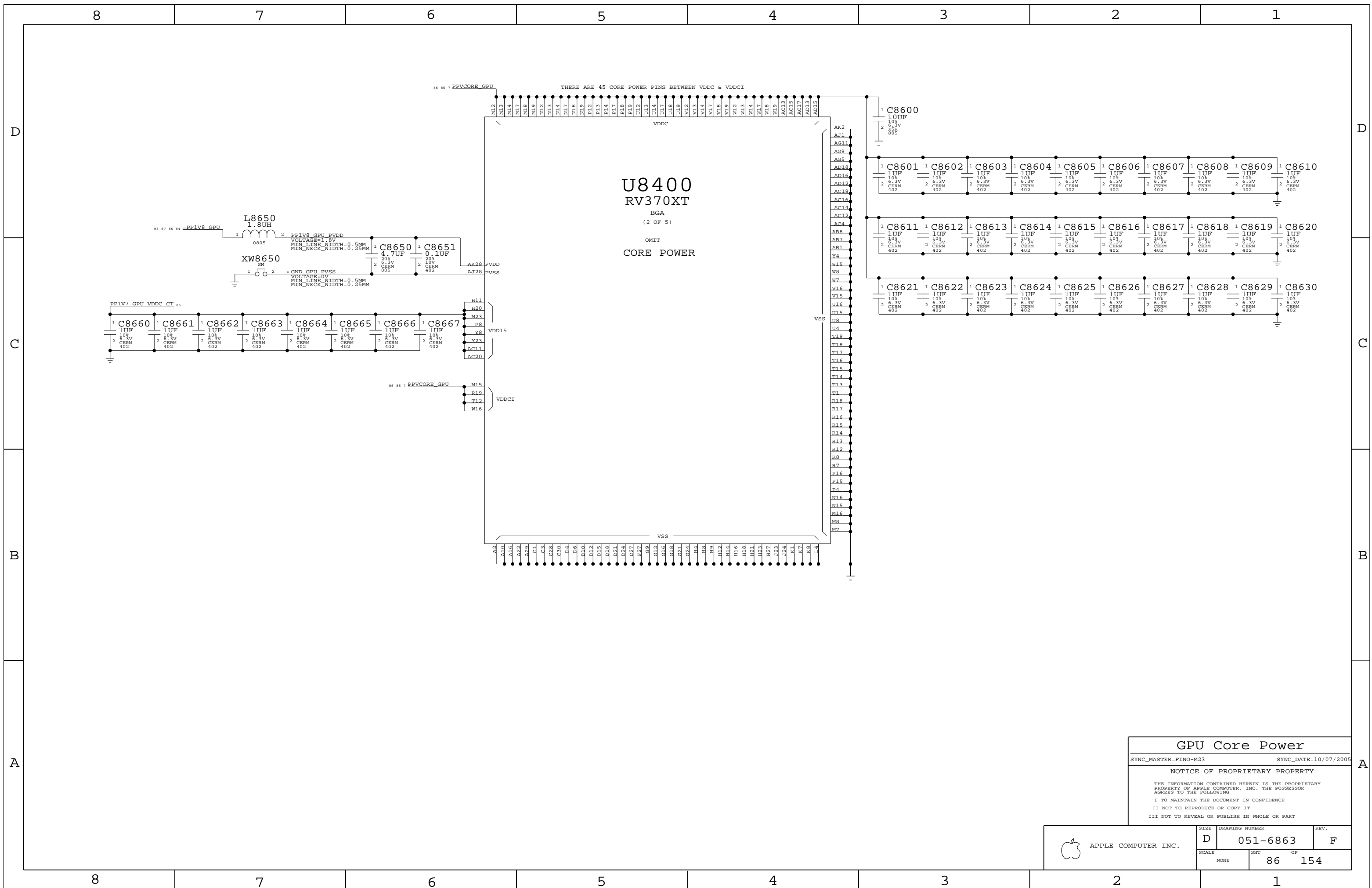
GPU 1.8V VREG



Graphics Vregs
 SYNC_MASTER=M33-DD SYNC_DATE=06/20/2005
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POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
 PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD
 THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
 HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
 POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

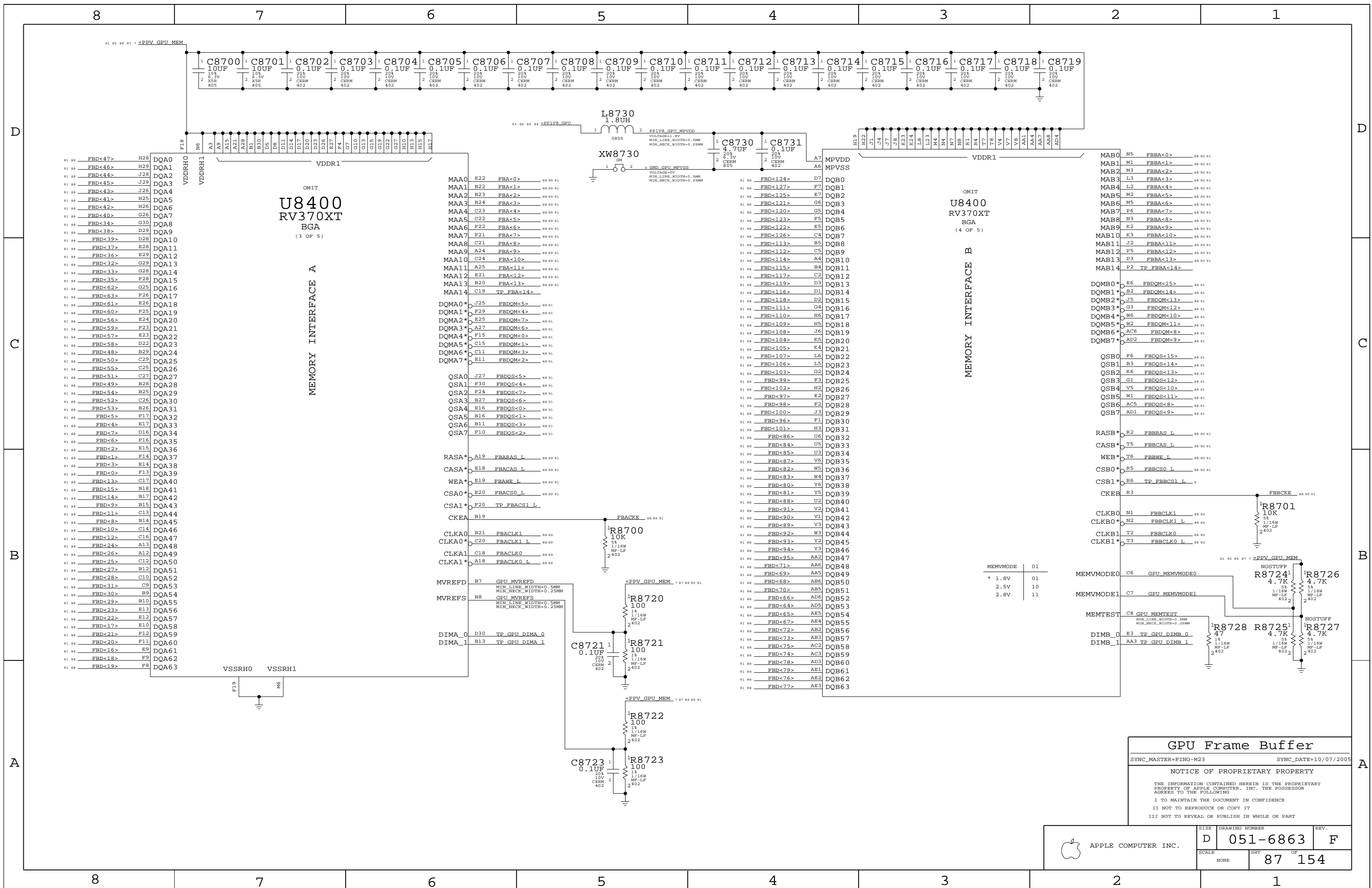
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	NONE	SHT	OF
		85	154



U8400
RV370XT
BGA
(2 OF 5)
OMIT
CORE POWER

GPU Core Power
 SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	86 OF		154



MEMVMODE	01
* 1.8V	01
2.5V	10
2.8V	11

GPU Frame Buffer

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

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	D	051-6863	F
SCALE	NONE	SHT	87 OF 154

FRAME BUFFER A TERMINATION

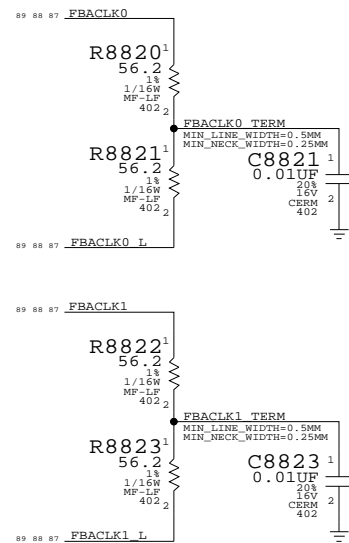
PLACE R'S CLOSE TO MEMORY

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

Table listing termination points for Frame Buffer A, including net names like FBD<31>, FBD<30>, FBD<29>, FBD<28>, FBD<27>, FBD<26>, FBD<25>, FBD<24>, FBD<0>, FBD<1>, FBD<2>, FBD<3>, FBD<17>, FBD<16>, FBD<18>, FBD<19>, FBD<15>, FBD<14>, FBD<13>, FBD<12>, FBD<10>, FBD<11>, FBD<9>, FBD<8>, FBD<5>, FBD<6>, FBD<4>, FBD<7>, FBD<20>, FBD<21>, FBD<22>, FBD<23> and their corresponding resistor values and locations.

Table listing termination points for Frame Buffer A, including net names like FBD<32>, FBD<33>, FBD<34>, FBD<35>, FBD<36>, FBD<37>, FBD<38>, FBD<39>, FBD<40>, FBD<41>, FBD<42>, FBD<43>, FBD<44>, FBD<45>, FBD<46>, FBD<47>, FBD<48>, FBD<49>, FBD<50>, FBD<51>, FBD<52>, FBD<53>, FBD<54>, FBD<55>, FBD<56>, FBD<57>, FBD<58>, FBD<59>, FBD<60>, FBD<61>, FBD<62>, FBD<63> and their corresponding resistor values and locations.

Table listing termination points for Frame Buffer A, including net names like FBDQOS<0>, FBDQOS<1>, FBDQOS<2>, FBDQOS<3>, FBDQOS<4>, FBDQOS<5>, FBDQOS<6>, FBDQOS<7>, FBDQOM<0>, FBDQOM<1>, FBDQOM<2>, FBDQOM<3>, FBDQOM<4>, FBDQOM<5>, FBDQOM<6>, FBDQOM<7> and their corresponding resistor values and locations.



FRAME BUFFER B TERMINATION

Table listing termination points for Frame Buffer B, including net names like FBD<64>, FBD<65>, FBD<66>, FBD<67>, FBD<68>, FBD<69>, FBD<70>, FBD<71>, FBD<80>, FBD<81>, FBD<82>, FBD<83>, FBD<76>, FBD<77>, FBD<78>, FBD<79>, FBD<91>, FBD<90>, FBD<89>, FBD<88>, FBD<95>, FBD<94>, FBD<93>, FBD<92> and their corresponding resistor values and locations.

Table listing termination points for Frame Buffer B, including net names like FBD<96>, FBD<97>, FBD<98>, FBD<99>, FBD<100>, FBD<101>, FBD<102>, FBD<103>, FBD<104>, FBD<105>, FBD<106>, FBD<107>, FBD<108>, FBD<109>, FBD<110>, FBD<111>, FBD<112>, FBD<113>, FBD<114>, FBD<115>, FBD<116>, FBD<117>, FBD<118>, FBD<119>, FBD<120>, FBD<121>, FBD<122>, FBD<123>, FBD<124>, FBD<125>, FBD<126>, FBD<127> and their corresponding resistor values and locations.

Table listing termination points for Frame Buffer B, including net names like FBDQOS<8>, FBDQOS<9>, FBDQOS<10>, FBDQOS<11>, FBDQOS<12>, FBDQOS<13>, FBDQOS<14>, FBDQOS<15>, FBDQOM<8>, FBDQOM<9>, FBDQOM<10>, FBDQOM<11>, FBDQOM<12>, FBDQOM<13>, FBDQOM<14>, FBDQOM<15> and their corresponding resistor values and locations.

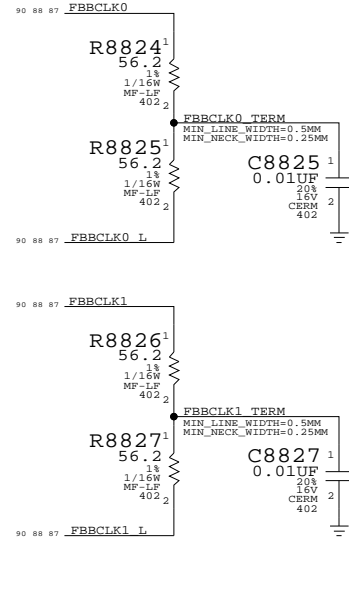
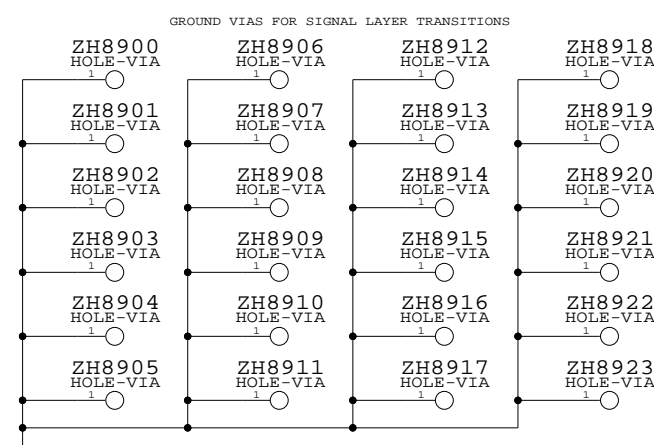
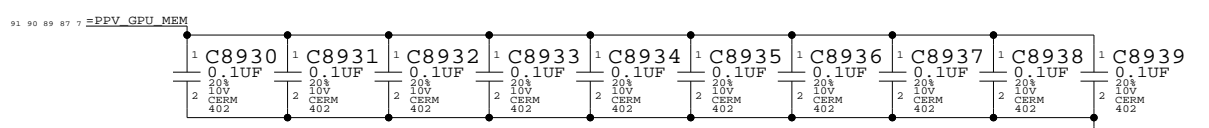
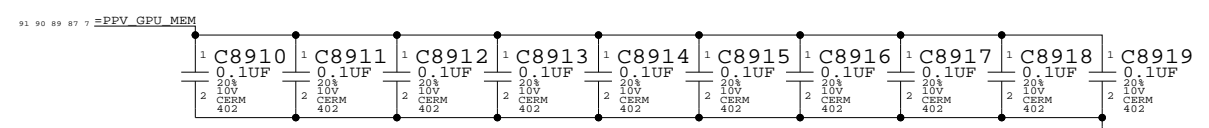
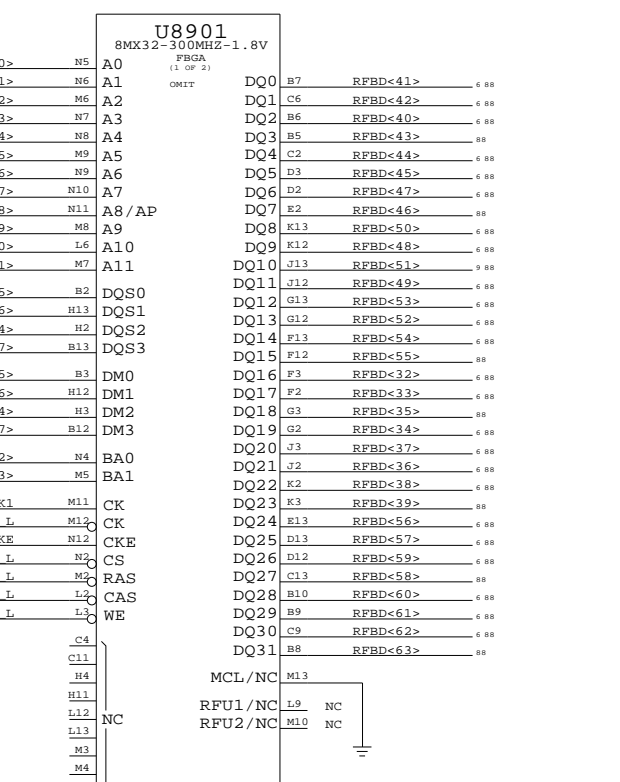
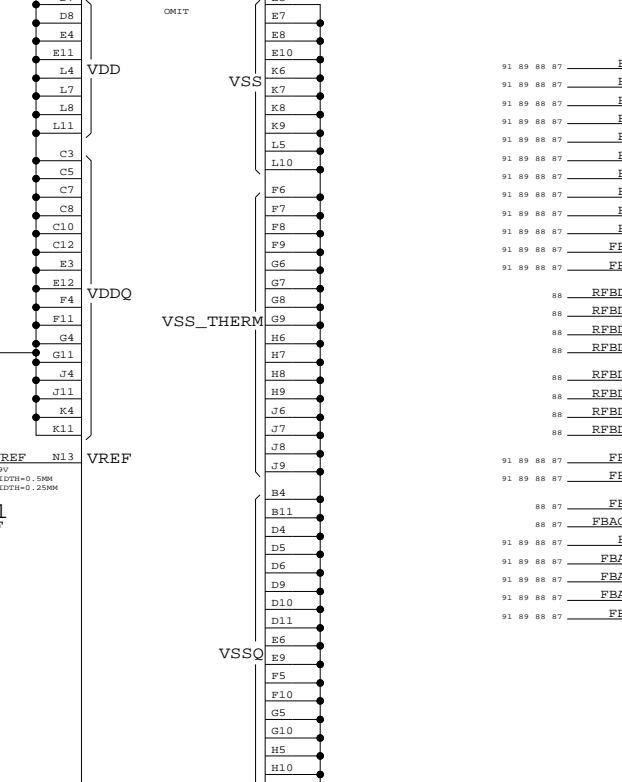
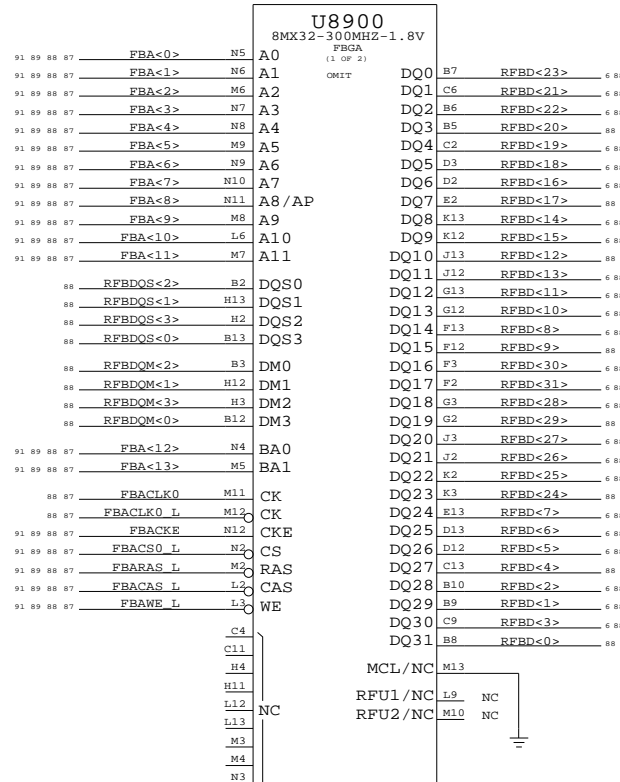
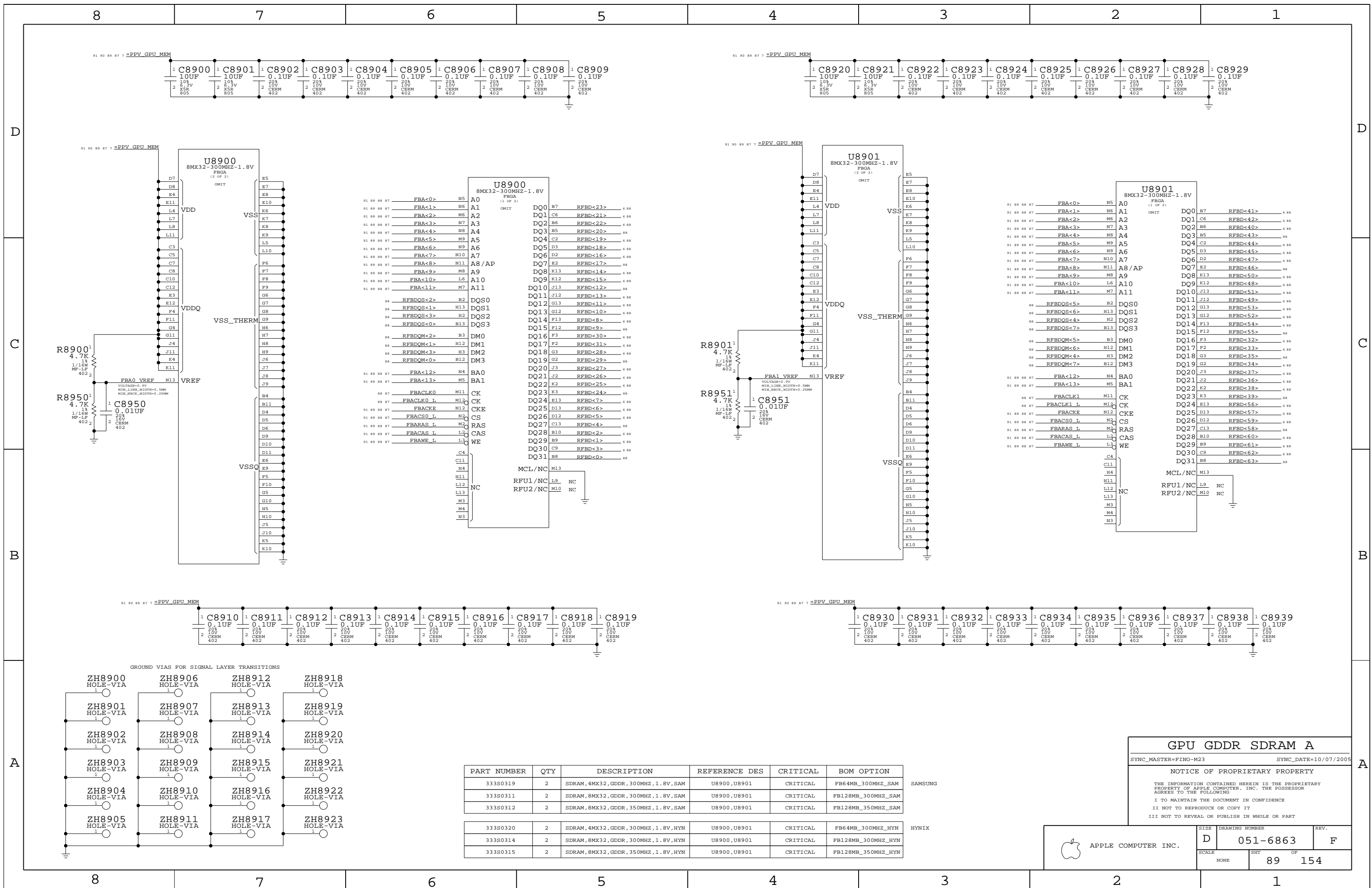


Table mapping electrical constraint sets to net physical types, net spacing types, and differential pairs for Frame Buffer A termination.

Table mapping electrical constraint sets to net physical types, net spacing types, and differential pairs for Frame Buffer B termination.

FB Series Termination
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005
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DRAWING NUMBER: D 051-6863 REV. F
SCALE: NONE SHEET: 88 OF 154

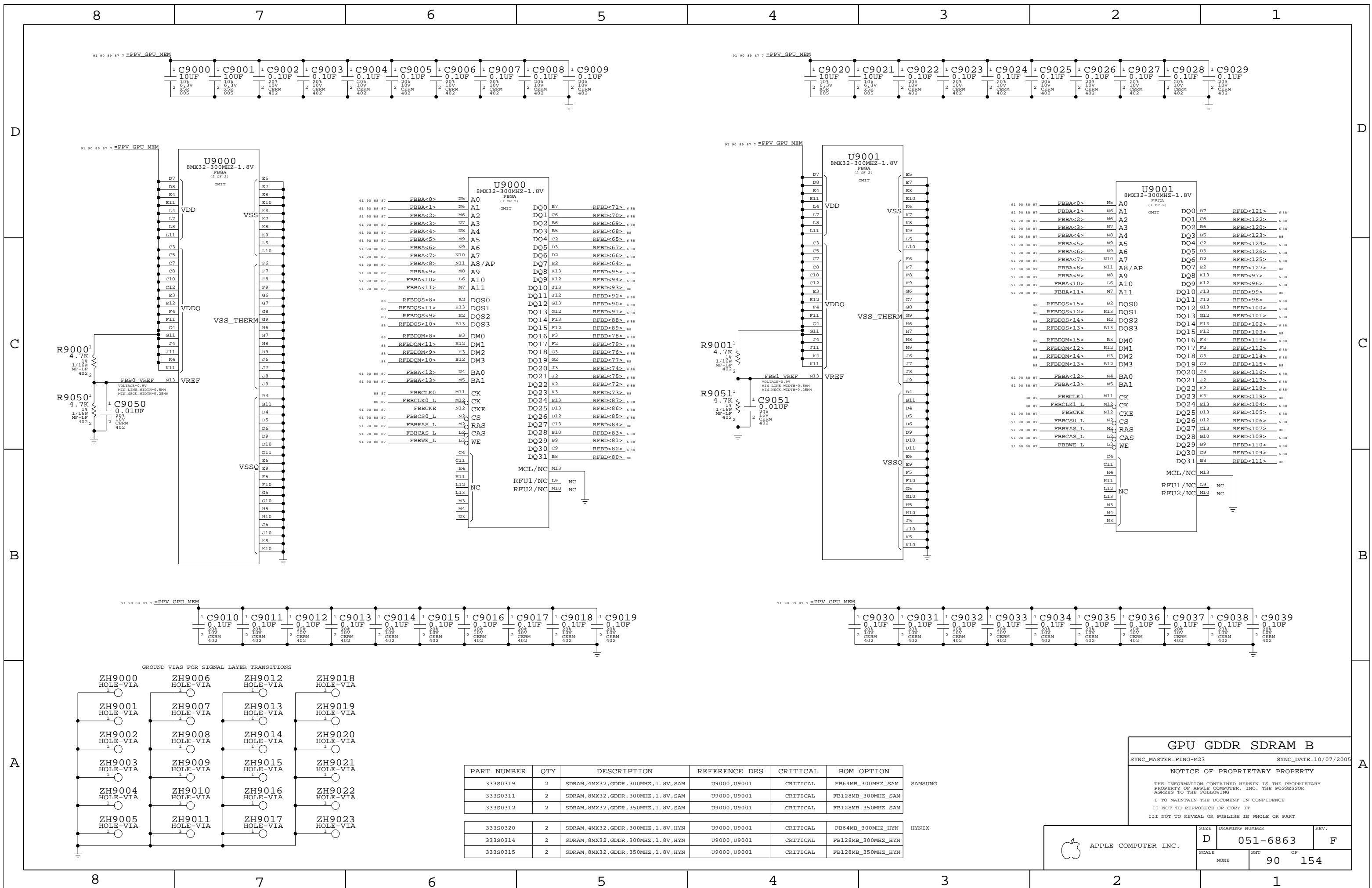


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB64MB_300MHZ_SAM
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_300MHZ_SAM
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_350MHZ_SAM
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB64MB_300MHZ_HYN
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_300MHZ_HYN
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_350MHZ_HYN

GPU GDDR SDRAM A
 SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005
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SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE	SHT	OF
NONE	89	154



GPU GDDR SDRAM B

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

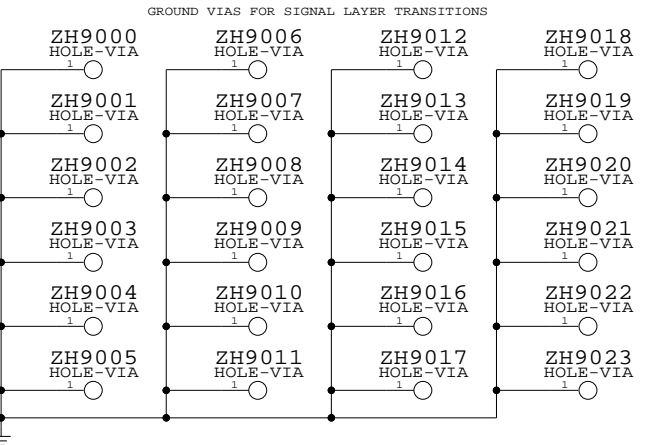
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB64MB_300MHZ_SAM SAMSUNG
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB128MB_300MHZ_SAM
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB128MB_350MHZ_SAM
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB64MB_300MHZ_HYN HYNIX
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB128MB_300MHZ_HYN
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB128MB_350MHZ_HYN

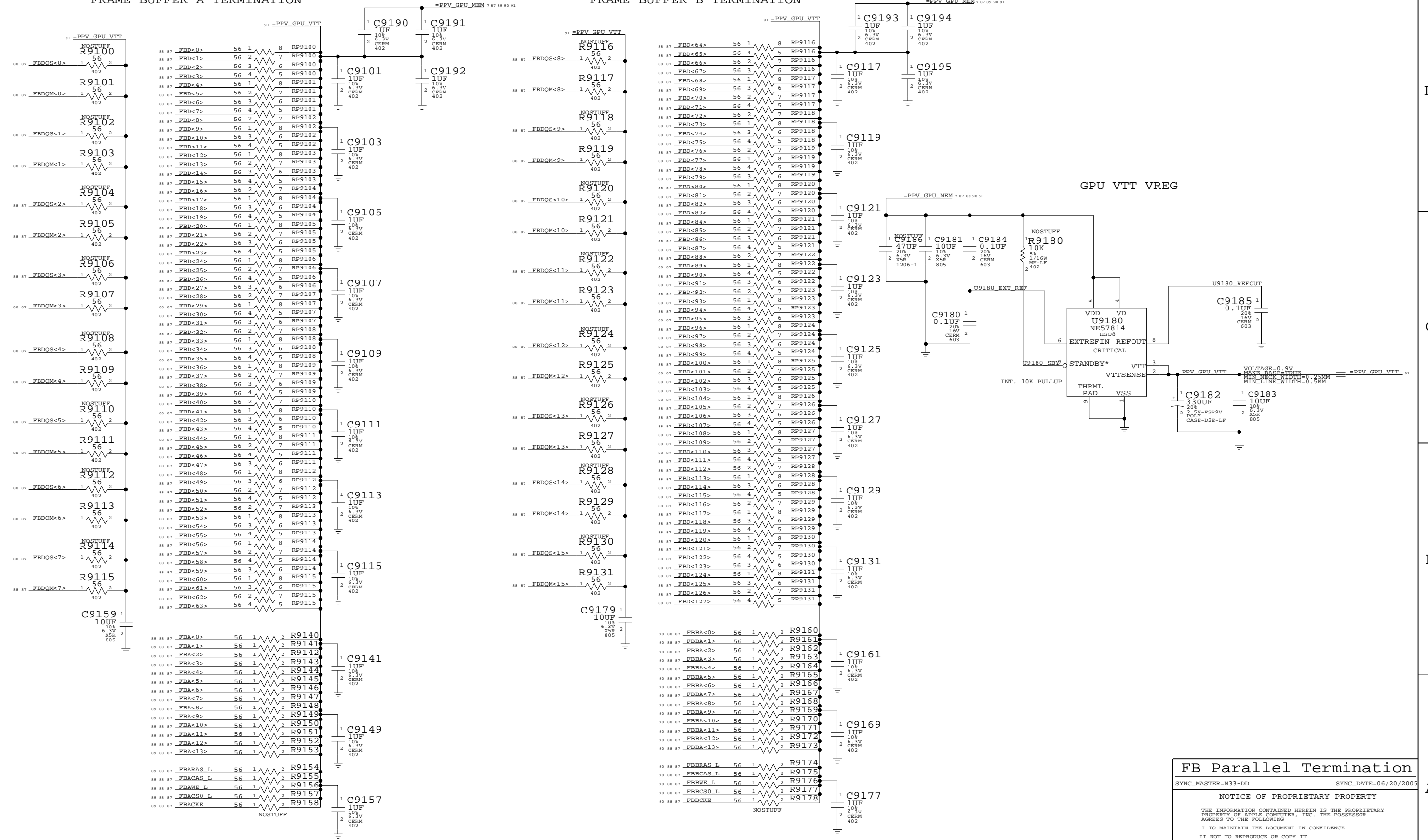
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	90	154



FRAME BUFFER A TERMINATION

FRAME BUFFER B TERMINATION



FB Parallel Termination

SYNC_MASTER=M33-DD SYNC_DATE=06/20/2005

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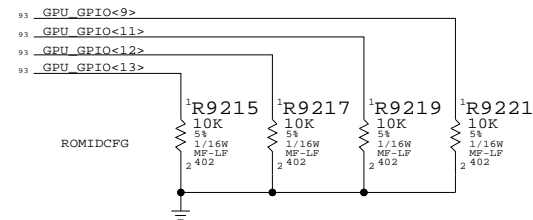
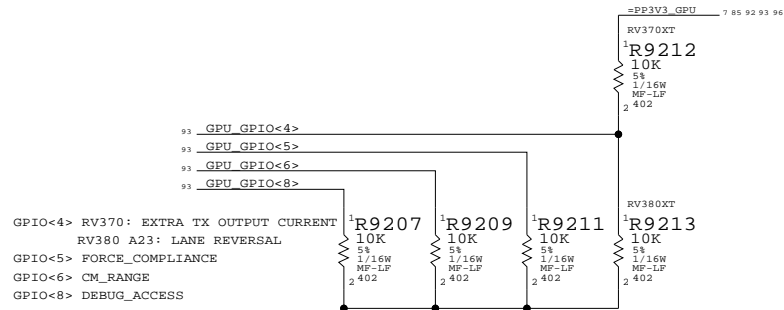
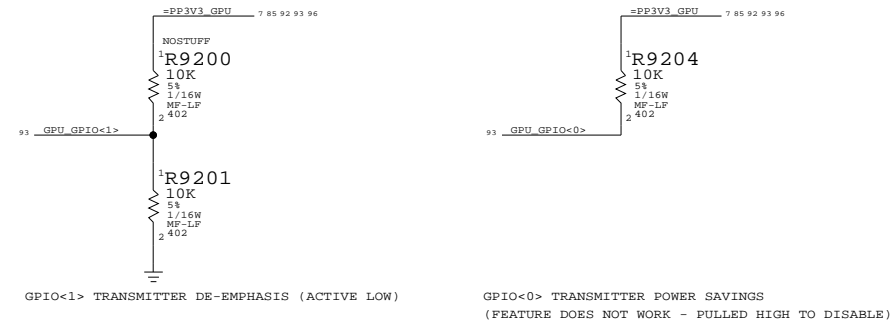
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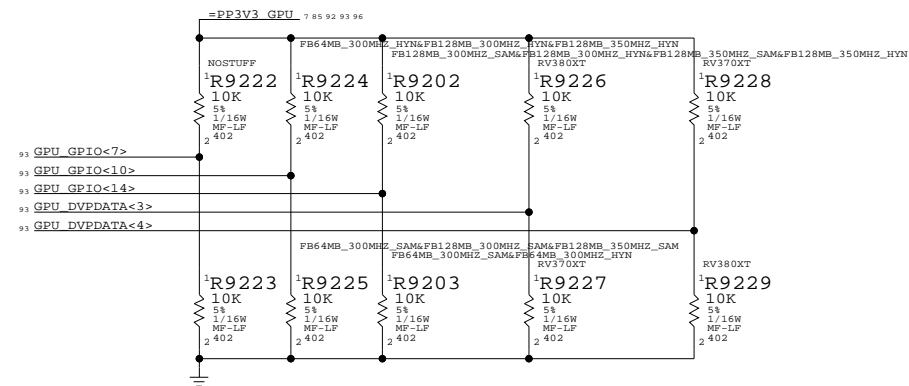
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
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ATI STRAPS

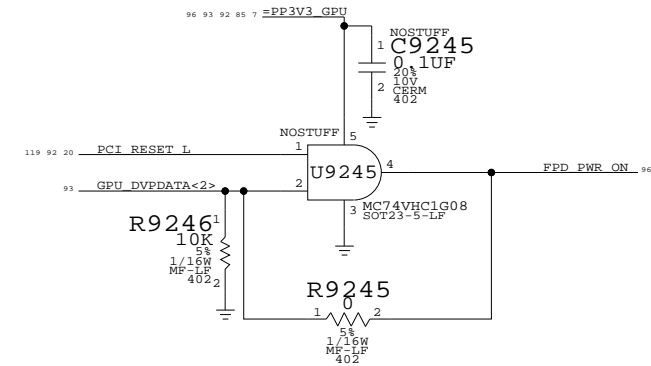
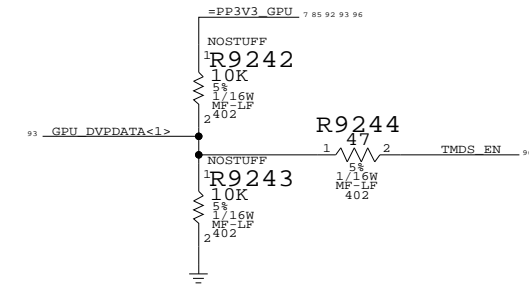
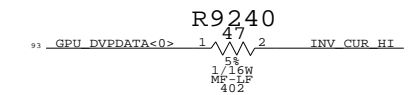
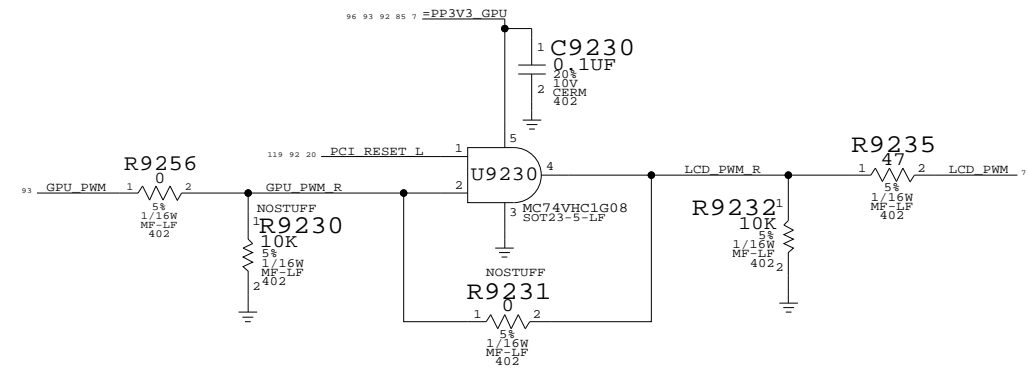


MEMORY STRAPS



GPIO<7> - MEMORY DIE REVISION
 0 - ORIGINAL DIE REVISION
 1 - NEW (FUTURE) DIE REV
 GPIO<10> - MEMORY VENDOR
 0 - SAMSUNG
 1 - HYNIX
 GPIO<14> - MEMORY DENSITY
 0 - 4MX32
 1 - 8MX32
 DVPDATA<3,4> - SPEED
 00 - 325E / 200M
 01 - 400E / 300M
 10 - 500E / 350M
 11 - RESERVED FOR FUTURE USE

APPLE GPIOs



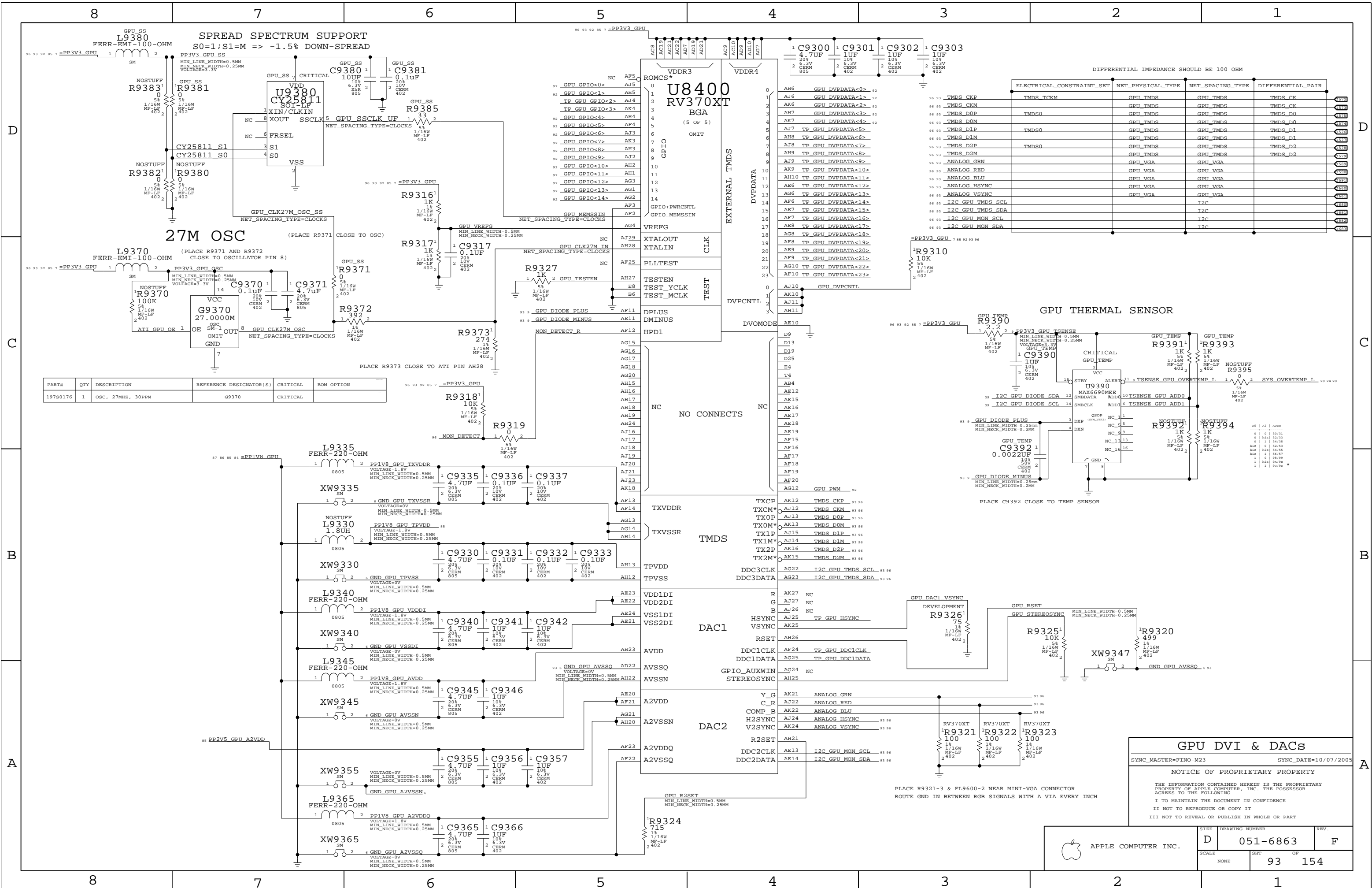
GPU Straps

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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	D	051-6863	F
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NONE	92 OF		154

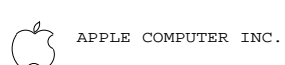


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19780176	1	OSC, 27MHZ, 30PPM	G9370	CRITICAL	

U8400 RV370XT BGA (5 OF 5)

0	ROMCS*
1	VDDR3
2	VDDR4
3	EXTERNAL TMDS
4	DVPCNTL
5	DVOMODE
6	GPIO
7	GPIO<PWRCNTL
8	GPIO<MEMSSIN
9	VREFG
10	XTALOUT
11	XTALIN
12	PLLTEST
13	TESTEN
14	TEST_YCLK
15	TEST_MCLK
16	DPLUS
17	DMINUS
18	HPD1
19	NC
20	NO CONNECTS
21	NC
22	TXCP
23	TXCM*
24	TXOP
25	TX0M*
26	TX1P
27	TX1M*
28	TX2P
29	TX2M*
30	TPVDD
31	TPVSS
32	VDD1DI
33	VDD2DI
34	VSS1DI
35	VSS2DI
36	AVDD
37	AVSSQ
38	AVSSN
39	A2VDD
40	A2VSSN
41	A2VDDQ
42	A2VSSQ
43	Y_G
44	C_R
45	COMP_B
46	H2SYNC
47	V2SYNC
48	R2SET
49	DDC2CLK
50	DDC2DATA
51	GPU DIODE PLUS
52	GPU DIODE MINUS
53	MON_DETECT_R
54	GPU VREFG
55	GPU CLK27M IN
56	GPU TESTEN
57	GPU DIODE PLUS
58	GPU DIODE MINUS
59	MON_DETECT
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496	GPU DIODE PLUS
497	GPU DIODE MINUS
498	GPU DIODE PLUS
499	GPU DIODE MINUS
500	GPU DIODE PLUS

SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE	SHEET	OF
NONE	93	154

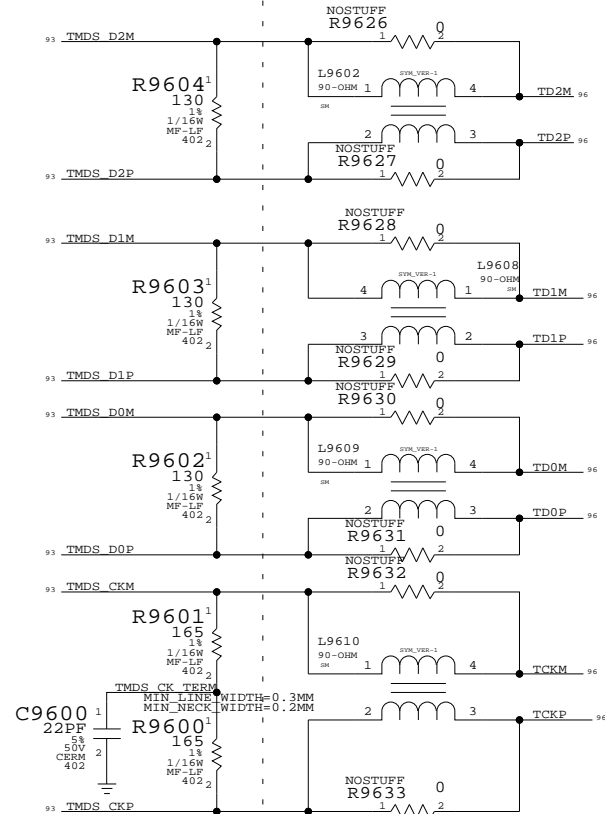


INTERNAL LCD

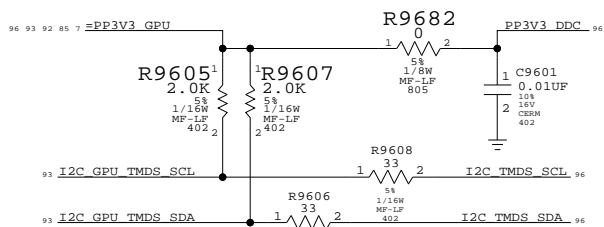
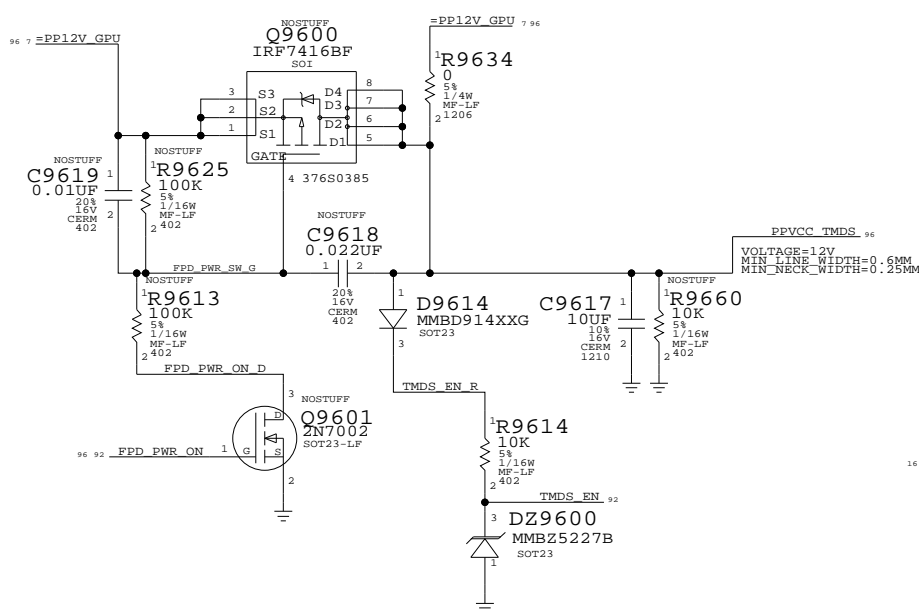
	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
96 TCKP	GPU_TMDS	GPU_TMDS	TCK
96 TCKM	GPU_TMDS	GPU_TMDS	TCK
96 TD0P	GPU_TMDS	GPU_TMDS	TD0
96 TD0M	GPU_TMDS	GPU_TMDS	TD0
96 TD1P	GPU_TMDS	GPU_TMDS	TD1
96 TD1M	GPU_TMDS	GPU_TMDS	TD1
96 TD2P	GPU_TMDS	GPU_TMDS	TD2
96 TD2M	GPU_TMDS	GPU_TMDS	TD2

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

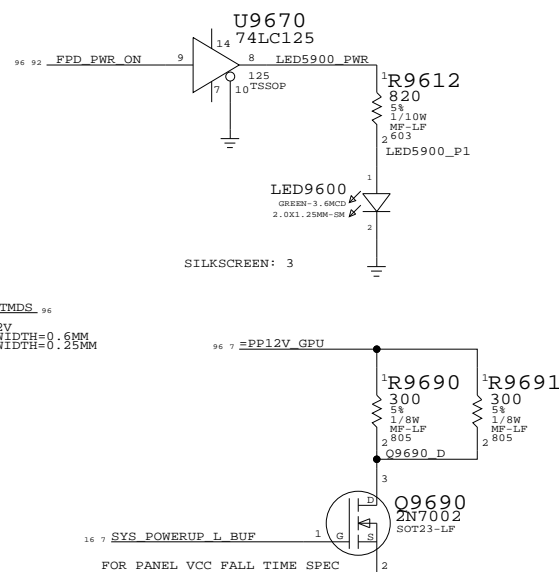
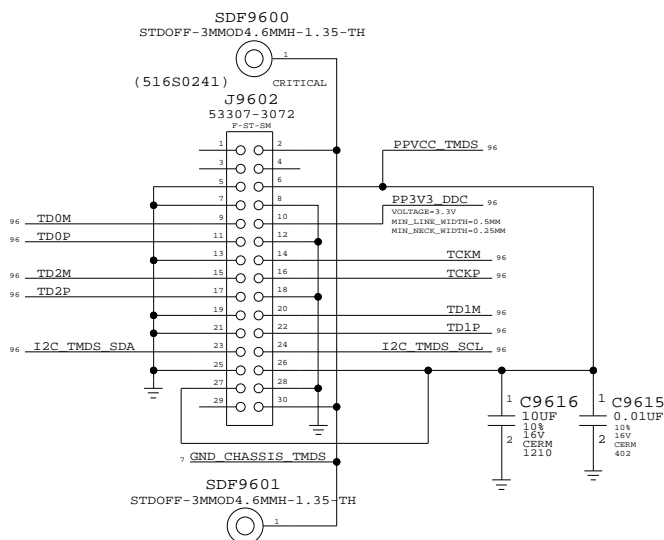
PLACE FILTER CLOSE TO TMDS CONNECTOR



PANEL POWER SEQUENCING



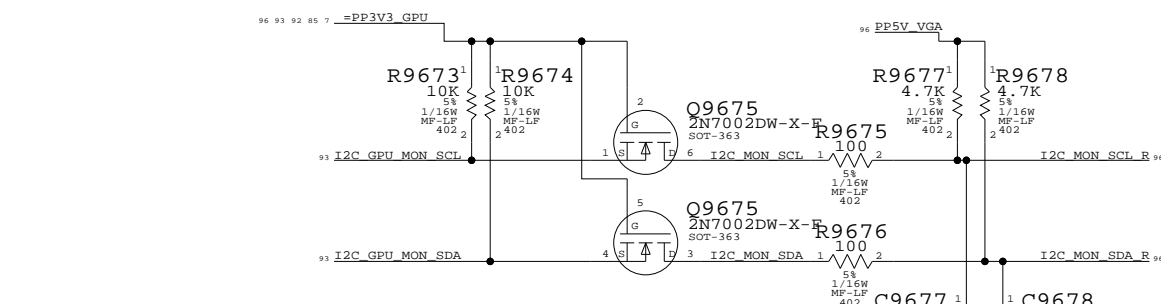
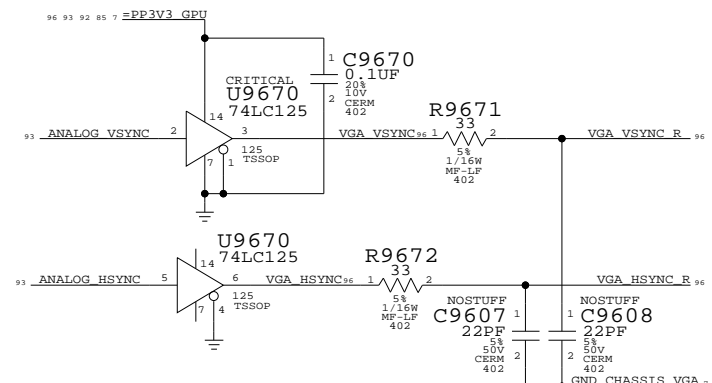
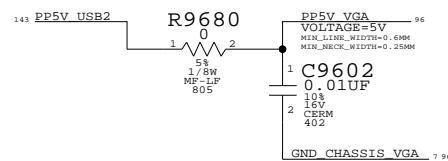
INTERNAL TMDS CONNECTOR



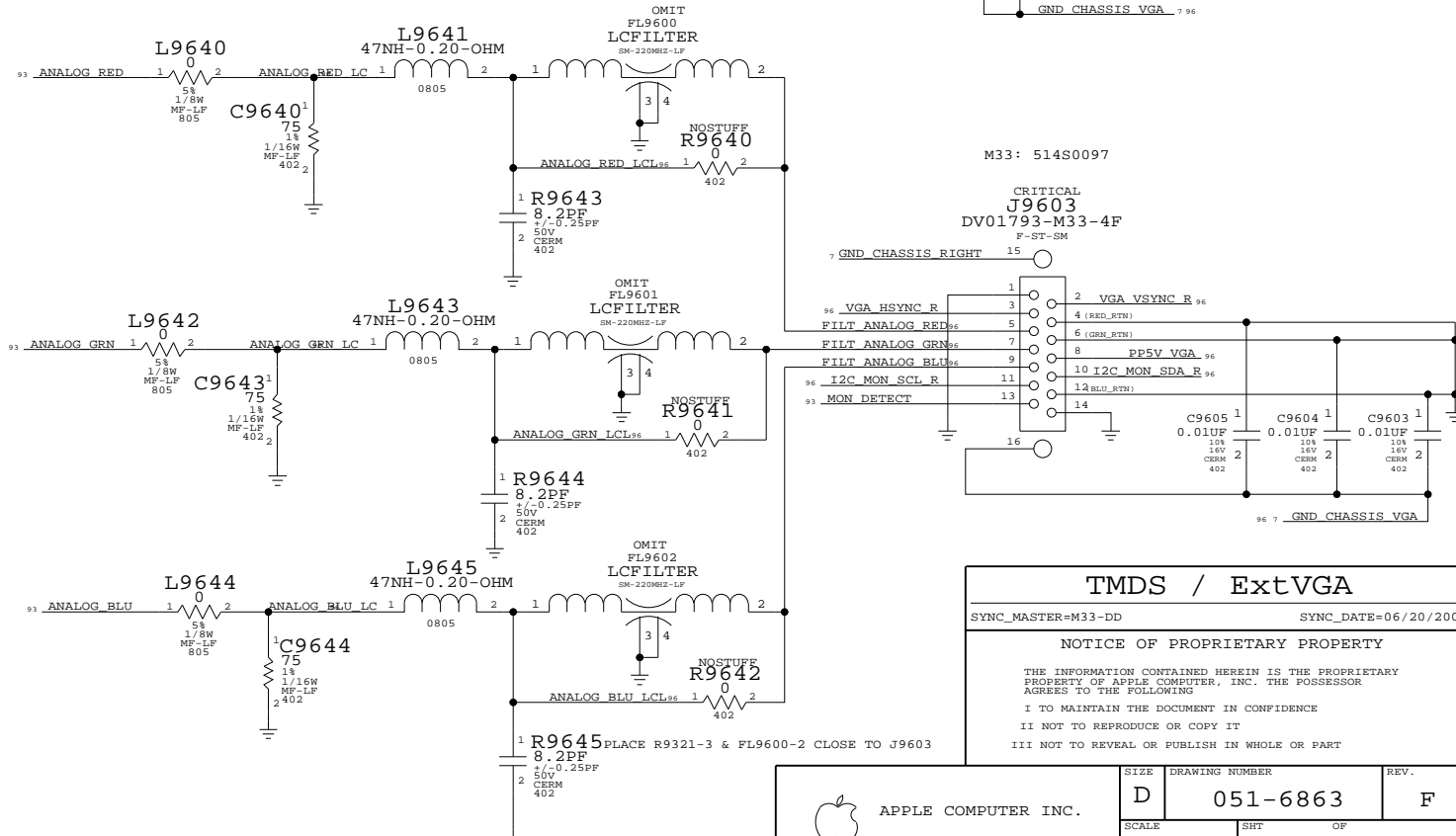
EXTERNAL VGA CONNECTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0316	3	INDUCTOR, 47NH, 0.20 OHM	FL9600, FL9601, FL9602	

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
96 FILT_ANALOG_GRN	GPU_VGA	GPU_VGA
96 ANALOG_GRN_LC	GPU_VGA	GPU_VGA
96 FILT_ANALOG_RED	GPU_VGA	GPU_VGA
96 ANALOG_RED_LC	GPU_VGA	GPU_VGA
96 FILT_ANALOG_BLU	GPU_VGA	GPU_VGA
96 ANALOG_BLU_LC	GPU_VGA	GPU_VGA
96 ANALOG_BLU_LCL	GPU_VGA	GPU_VGA
96 VGA_VSYNC	GPU_VGA	GPU_VGA
96 VGA_VSYNC_R	GPU_VGA	GPU_VGA
96 VGA_HSYNC	GPU_VGA	GPU_VGA
96 VGA_HSYNC_R	GPU_VGA	GPU_VGA

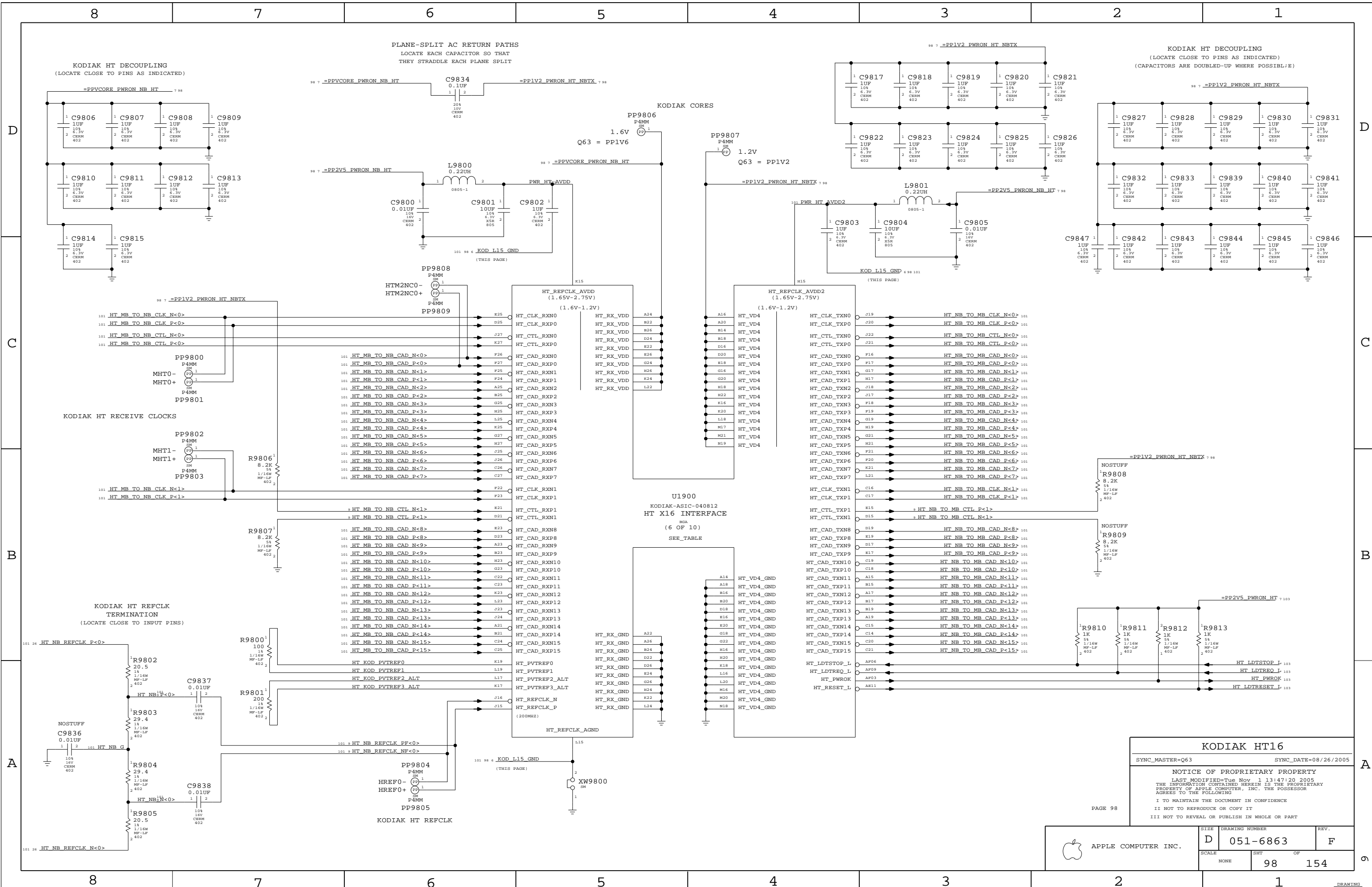


INDUCTORS SHOULD BE 47 NH ANY -8PF CAP SHOULD DO



TMDS / ExtVGA	
SYNC_MASTER=M33-DD	SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6863	REV: F
	SCALE: NONE	SHT: 96	OF: 154

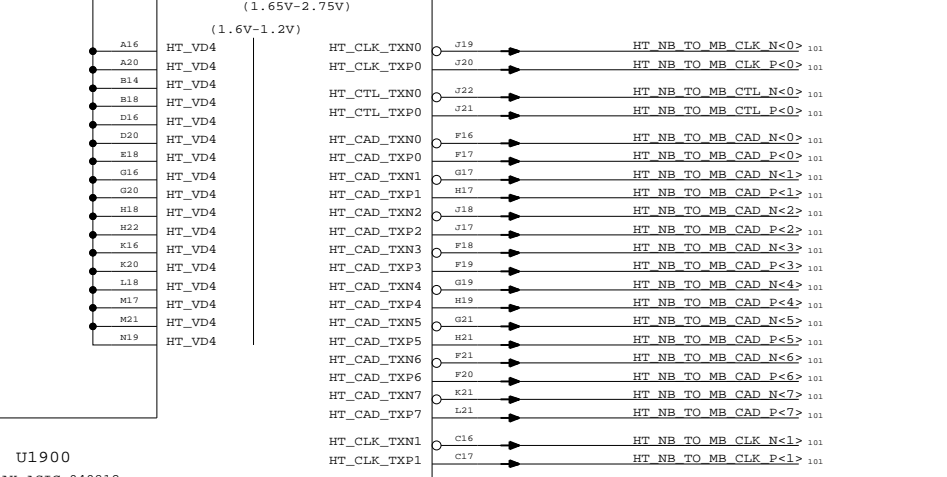
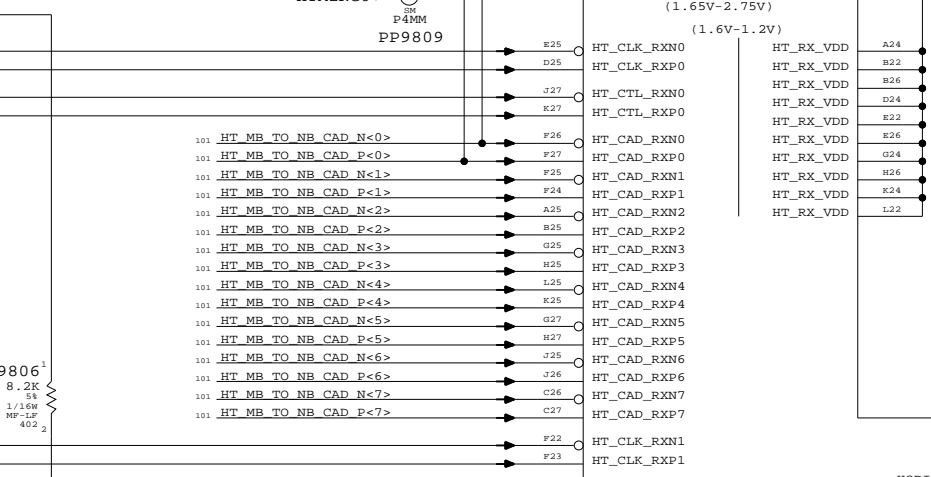
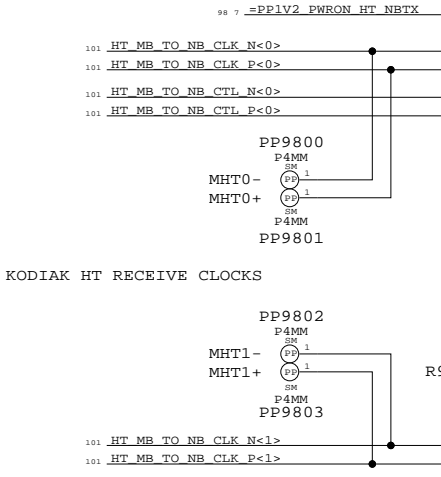
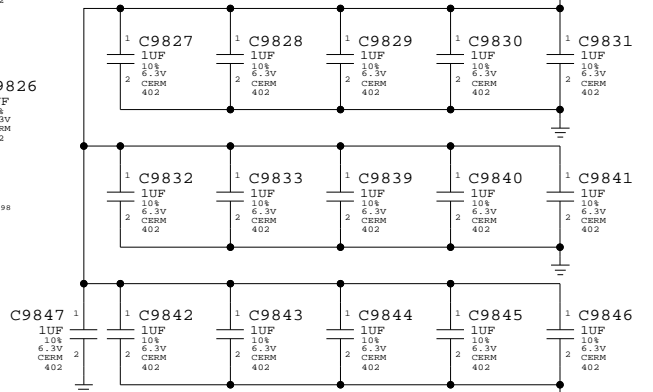
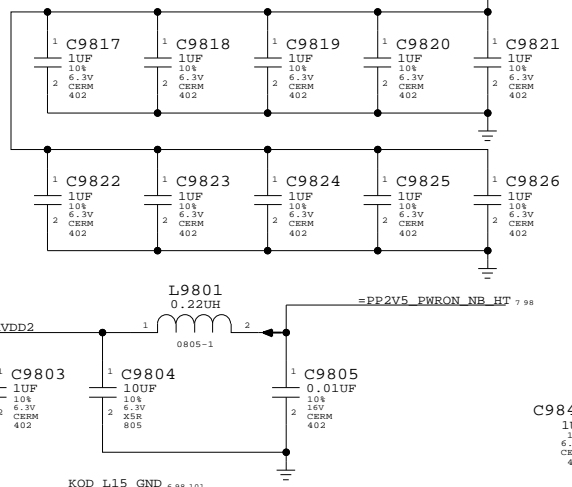
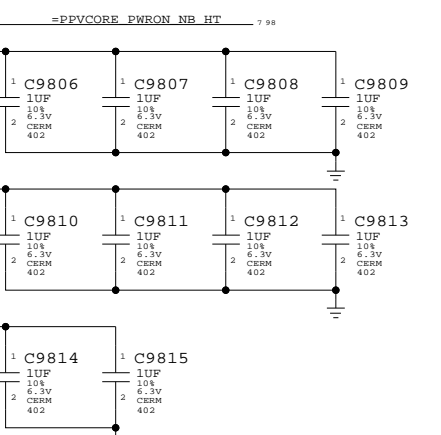


PLANE-SPLIT AC RETURN PATHS
LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT

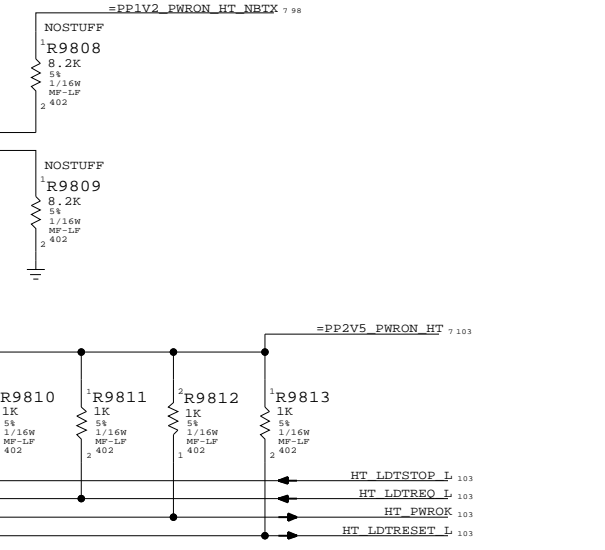
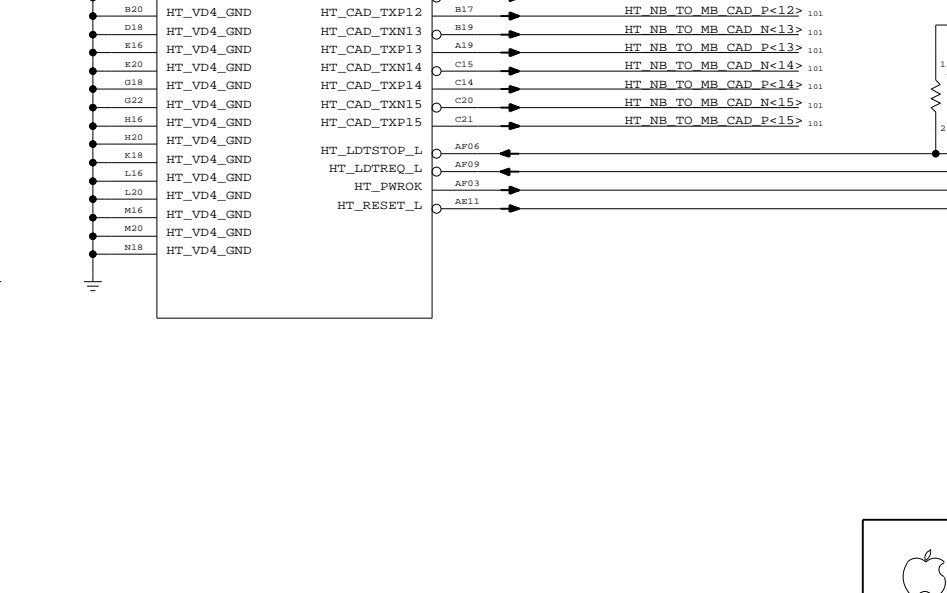
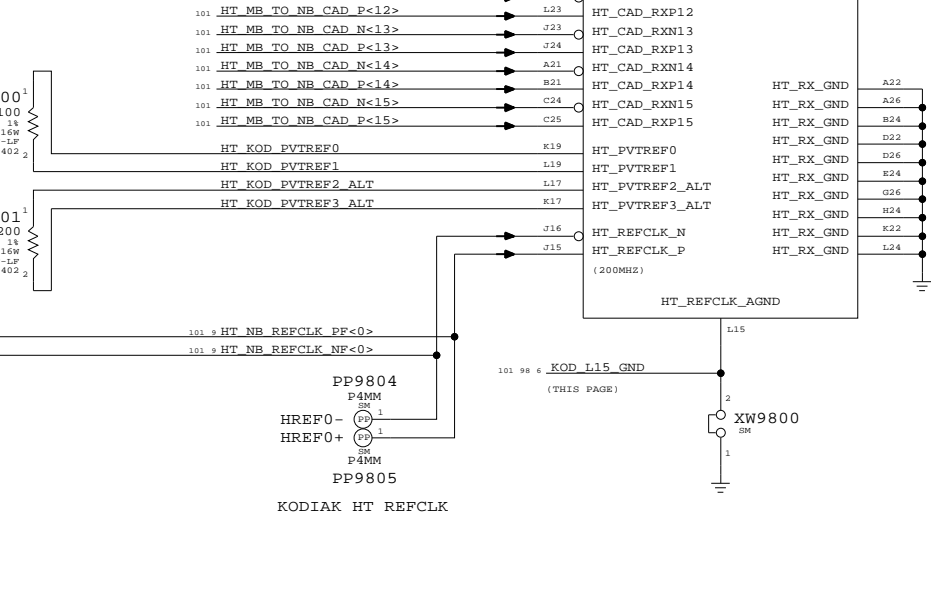
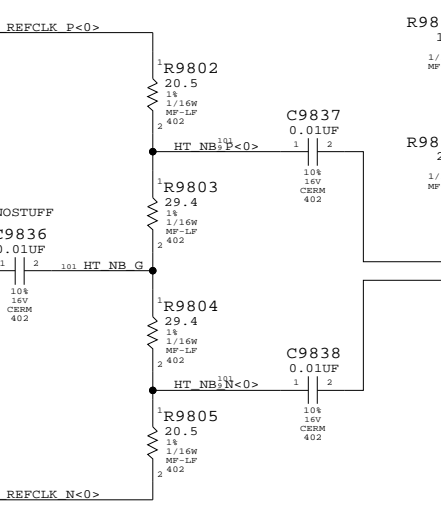
KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBLE)

KODIAK CORES



KODIAK HT REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)



KODIAK HT16
 SYNC_MASTER=Q63 SYNC_DATE=08/26/2005
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 LAST MODIFIED= Tue Nov 13 13:47:20 2005
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SCALE NONE	DRAWING NUMBER D 051-6863	REV. F
		SHEET 98
PAGE 98		OF 154



APPLE COMPUTER INC.

DRAWING

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SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
HT NB TO MB CLK N<0>	HT NB TO SB CLK N<0>	TRUE	HT NB TO SB CLK	HT NB TO SB PP	HT CAD
HT NB TO MB CAD N<0>	HT NB TO SB CAD N<0>	TRUE	HT NB TO SB CAD0	HT NB TO SB PP	HT CAD
HT NB TO MB CAD N<1>	HT NB TO SB CAD N<1>	TRUE	HT NB TO SB CAD1	HT NB TO SB	HT CAD
HT NB TO MB CAD N<2>	HT NB TO SB CAD N<2>	TRUE	HT NB TO SB CAD2	HT NB TO SB	HT CAD
HT NB TO MB CAD N<3>	HT NB TO SB CAD N<3>	TRUE	HT NB TO SB CAD3	HT NB TO SB	HT CAD
HT NB TO MB CAD N<4>	HT NB TO SB CAD N<4>	TRUE	HT NB TO SB CAD4	HT NB TO SB	HT CAD
HT NB TO MB CAD N<5>	HT NB TO SB CAD N<5>	TRUE	HT NB TO SB CAD5	HT NB TO SB	HT CAD
HT NB TO MB CAD N<6>	HT NB TO SB CAD N<6>	TRUE	HT NB TO SB CAD6	HT NB TO SB	HT CAD
HT NB TO MB CAD N<7>	HT NB TO SB CAD N<7>	TRUE	HT NB TO SB CAD7	HT NB TO SB	HT CAD
HT NB TO MB CTL N<0>	HT NB TO SB CTL N<0>	TRUE	HT NB TO SB CTL0	HT NB TO SB	HT CAD
HT MB TO NB CLK N<0>	HT SB TO NB CLK N<0>	TRUE	HT SB TO NB CLK	HT SB TO NB PP	HT CAD
HT MB TO NB CAD N<0>	HT SB TO NB CAD N<0>	TRUE	HT SB TO NB CAD0	HT SB TO NB PP	HT CAD
HT MB TO NB CAD N<1>	HT SB TO NB CAD N<1>	TRUE	HT SB TO NB CAD1	HT SB TO NB	HT CAD
HT MB TO NB CAD N<2>	HT SB TO NB CAD N<2>	TRUE	HT SB TO NB CAD2	HT SB TO NB	HT CAD
HT MB TO NB CAD N<3>	HT SB TO NB CAD N<3>	TRUE	HT SB TO NB CAD3	HT SB TO NB	HT CAD
HT MB TO NB CAD N<4>	HT SB TO NB CAD N<4>	TRUE	HT SB TO NB CAD4	HT SB TO NB	HT CAD
HT MB TO NB CAD N<5>	HT SB TO NB CAD N<5>	TRUE	HT SB TO NB CAD5	HT SB TO NB	HT CAD
HT MB TO NB CAD N<6>	HT SB TO NB CAD N<6>	TRUE	HT SB TO NB CAD6	HT SB TO NB	HT CAD
HT MB TO NB CAD N<7>	HT SB TO NB CAD N<7>	TRUE	HT SB TO NB CAD7	HT SB TO NB	HT CAD
HT MB TO NB CTL N<0>	HT SB TO NB CTL N<0>	TRUE	HT SB TO NB CTL0	HT SB TO NB	HT CAD
NC HT MB TO NB CAD P<8..15>		TRUE			
NC HT MB TO NB CAD N<8..15>		TRUE			
TP HT MB TO NB CLK N<1>		TRUE			
TP HT MB TO NB CLK P<1>		TRUE			
NC HT NB TO MB CAD P<8..15>		TRUE			
NC HT NB TO MB CAD N<8..15>		TRUE			
NC HT NB TO MB CLK N<1>		TRUE			
NC HT NB TO MB CLK P<1>		TRUE			
HT NB REFCLK P<0>			HT NB REFCLK0	HT NB REFCLK	HT CLK
HT NB REFCLK N<0>			HT NB REFCLK0	HT CLK	HT CLK
HT NB P<0>			HT NB0	HT CLK	HT CLK
HT NB N<0>			HT NB0	HT CLK	HT CLK
HT NB REFCLK PF<0>			HT NB REFCLK F0	HT CLK	HT CLK
HT NB REFCLK NF<0>			HT NB REFCLK F0	HT CLK	HT CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G	KEEP DIFF CLOCK FROM BEING A SINGLE XNET		0

HT ALIASES

FINO-M23 08/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT		
NONE	101 ^F	154	

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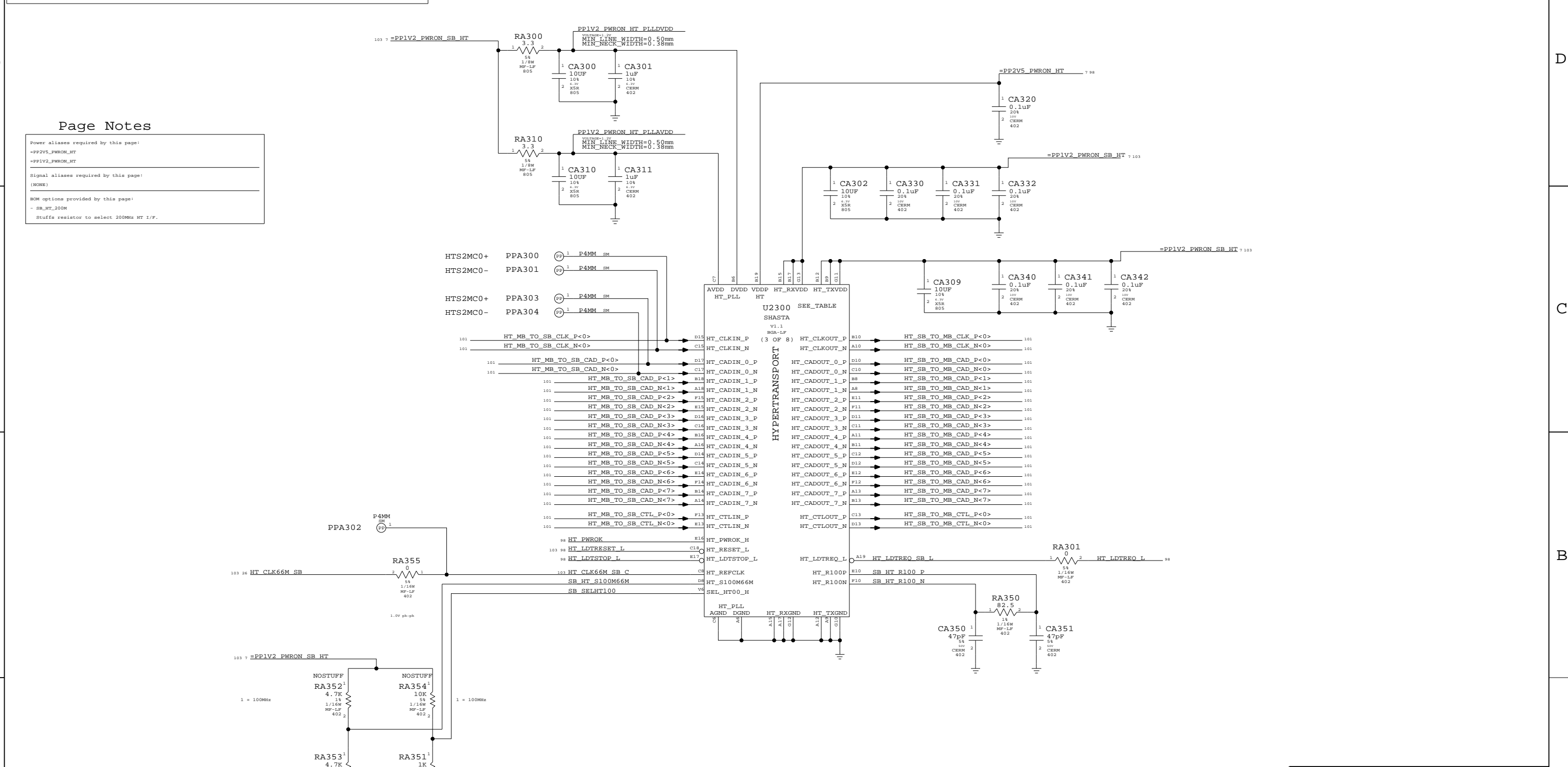
4

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1

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
HT_CLK66M_SB_C	0.38mm SPACING	
HT_CLK66M_SB	0.38mm SPACING	
HT_LDTRESET_L	2.54mm SPACING	



Page Notes

Power aliases required by this page:
 =PP2V5_PWRON_HT
 =PPIV2_PWRON_HT

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - SB_HT_200M

Stuffs resistor to select 200MHz HT 1/F.

HT RefClk HT 1/F Speed

1 = 100MHz 1 = 100MHz
 0 = 66MHz 0 = 200MHz

DETERMINES THE OPERATING FREQUENCY OF HT CORE

1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
 0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	103		154

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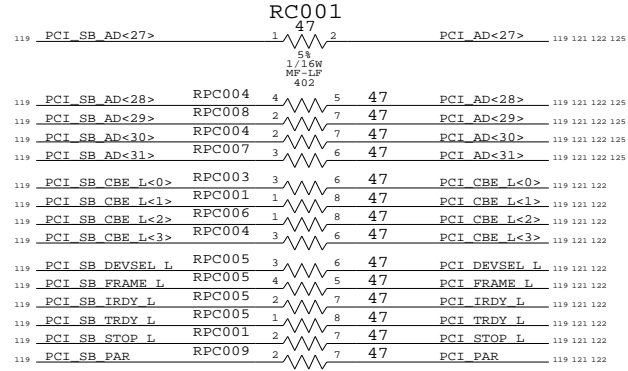
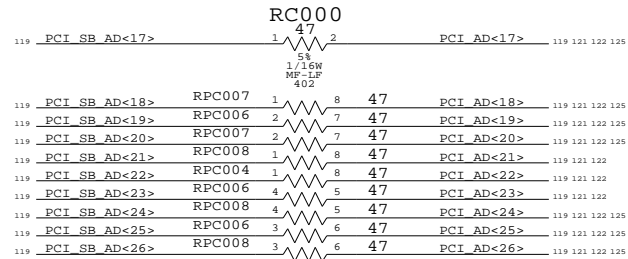
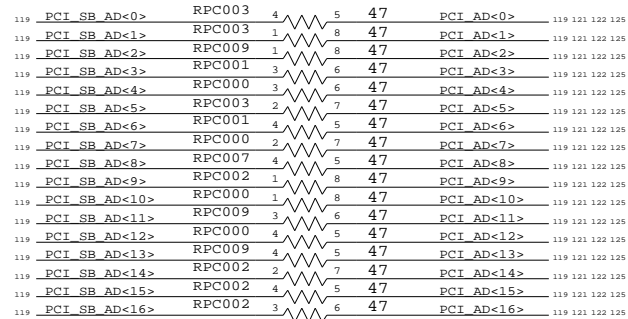
B

A

A

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)



PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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	D	051-6863	F
SCALE	SHT	OF	
NONE	120	154	

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	PCI_CLK33M_AIRPORT

Page Notes

Power aliases required by this page:
 - _PP3V3_PCI

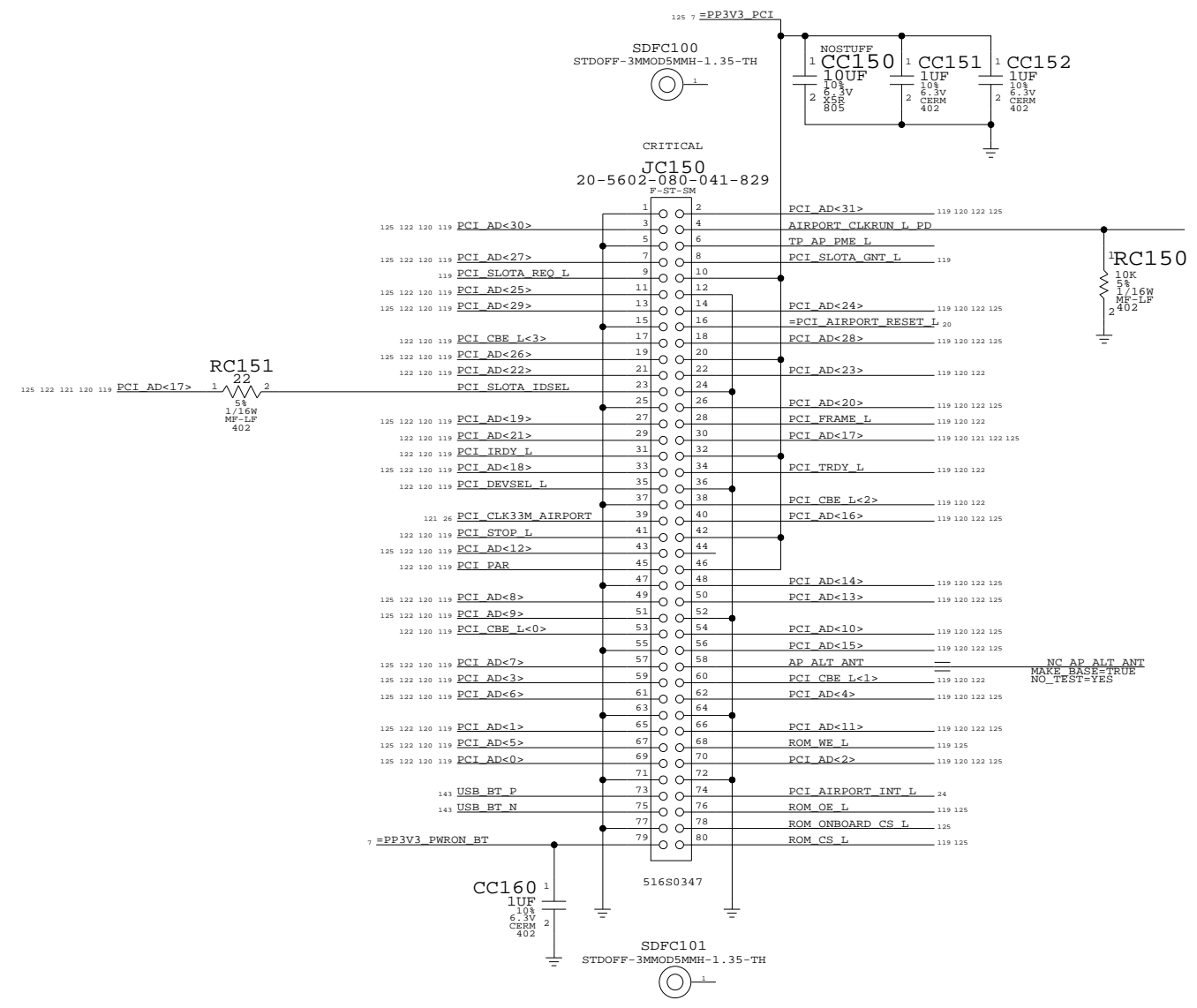
Signal aliases required by this page:
 - _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH
 SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	121	154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	=PCI_CLK33M_USB2

Page Notes

Power aliases required by this page:
 - _PPVIO_PCI (to 3.3V or 5V)

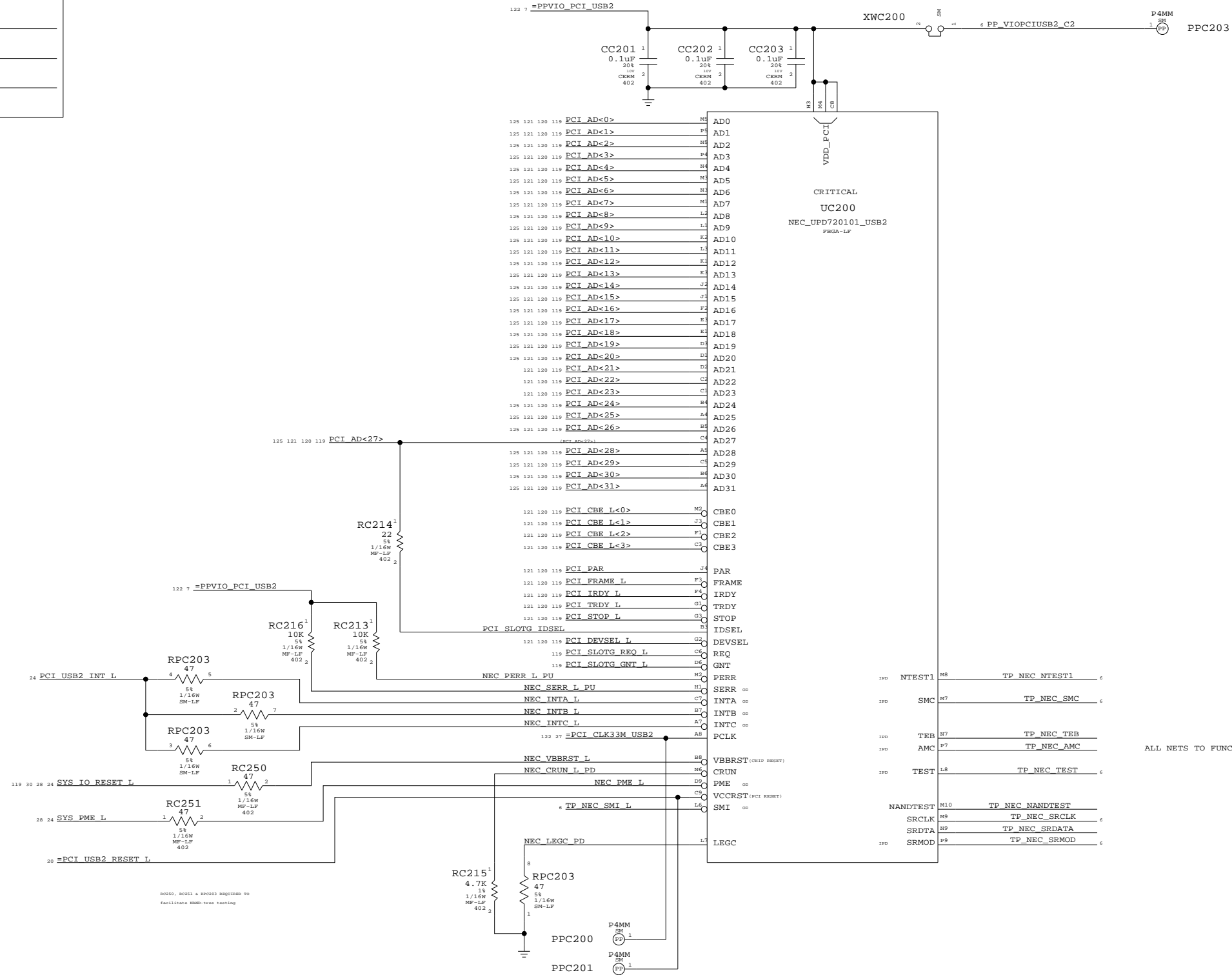
Signal aliases required by this page:
 - _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD27 (slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports Discold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN



ALL NETS TO FUNCTIONAL TEST PAGE

USB 2.0 PCI Interface
 SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	NONE	SHT OF	122 154

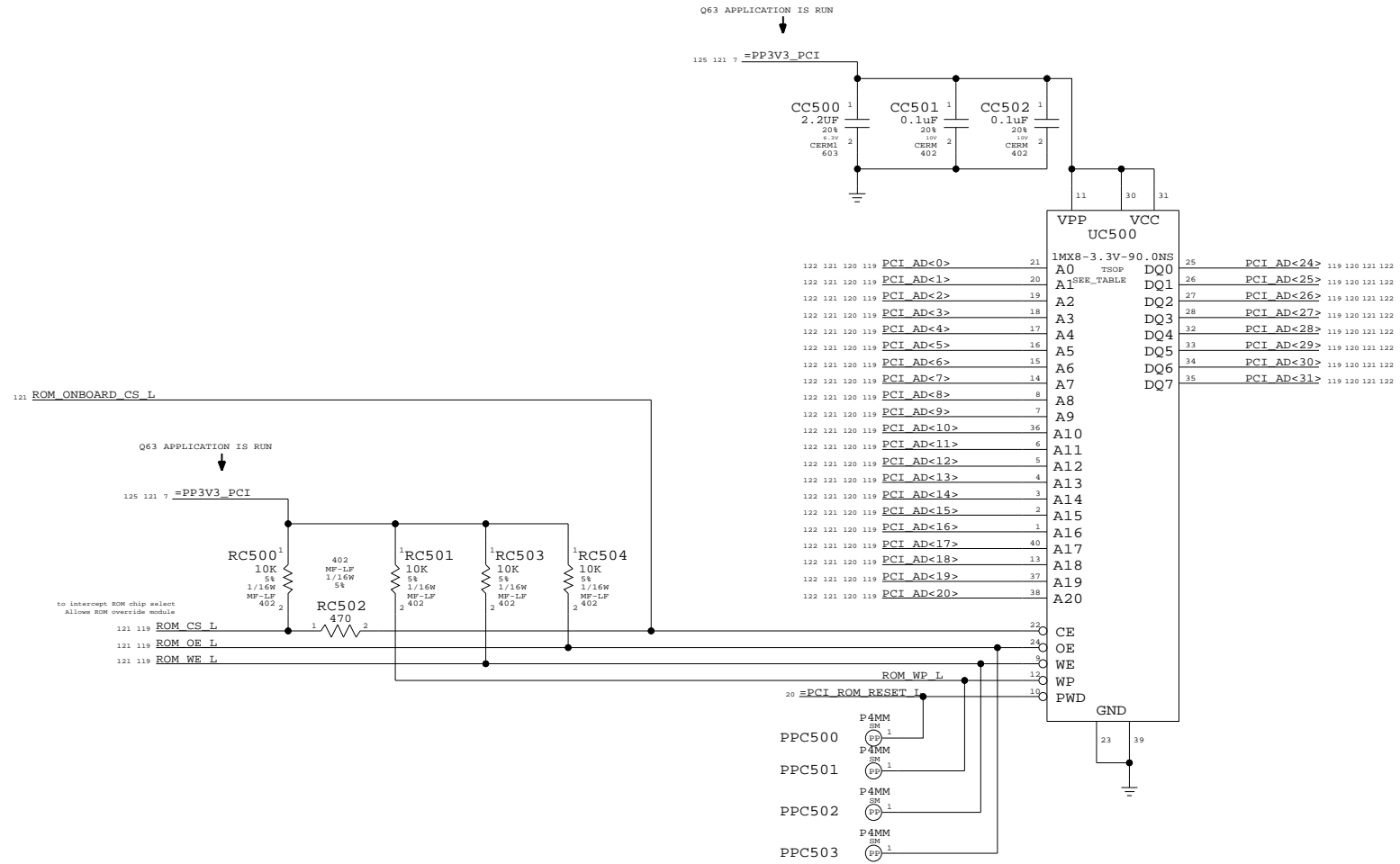
Page Notes

Power aliases required by this page:
 - =PP3V3_PCI

Signal aliases required by this page:
 (NONE)

BCM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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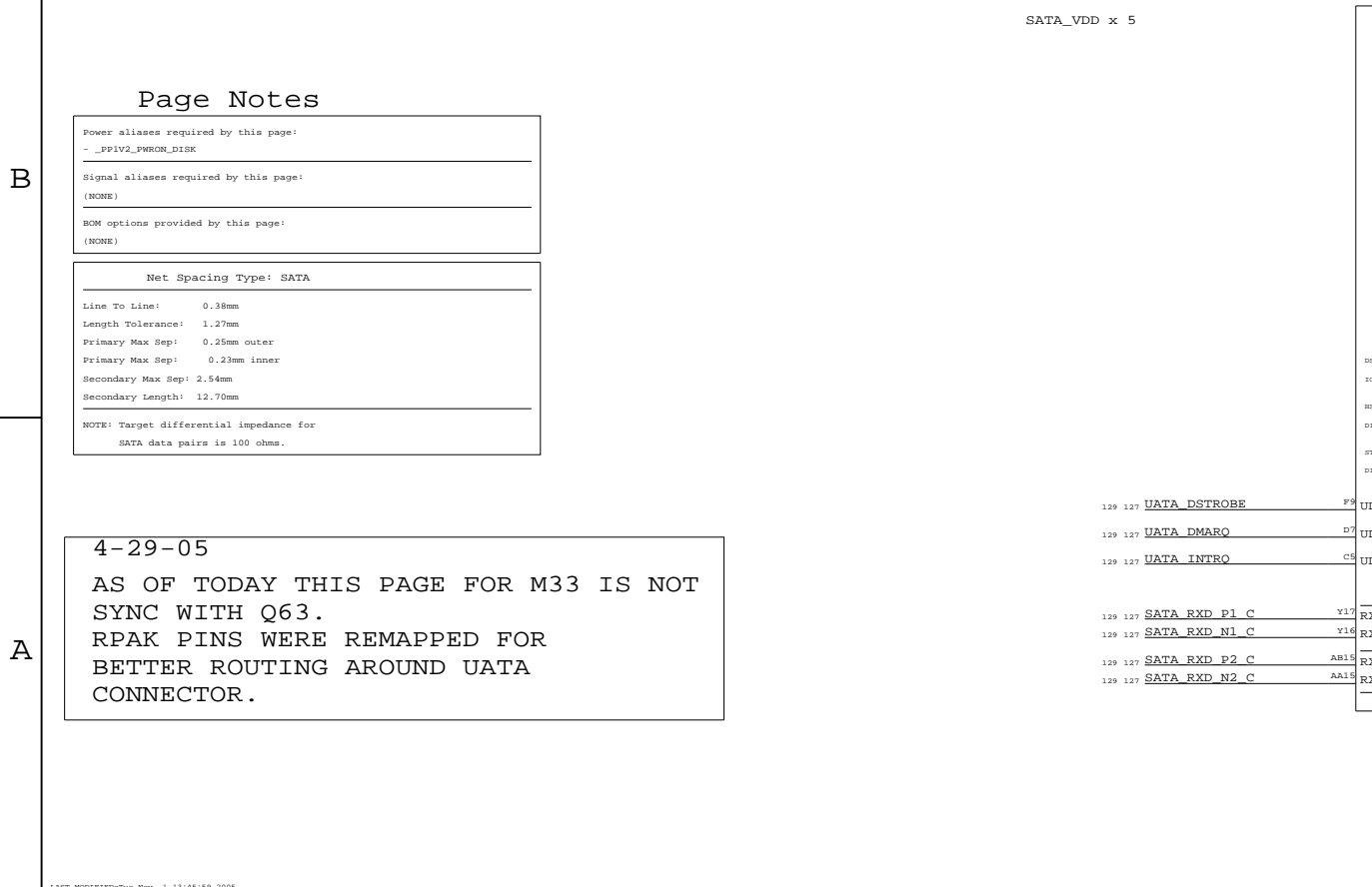
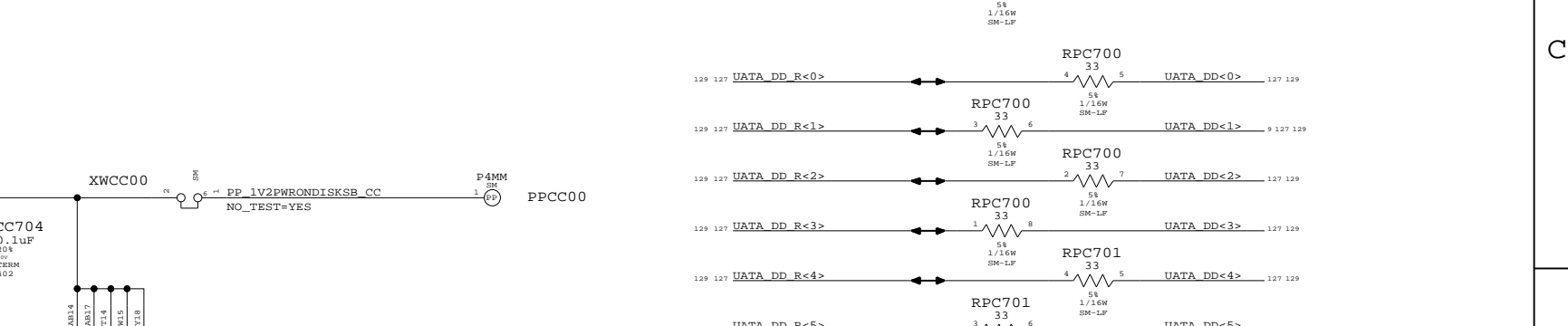
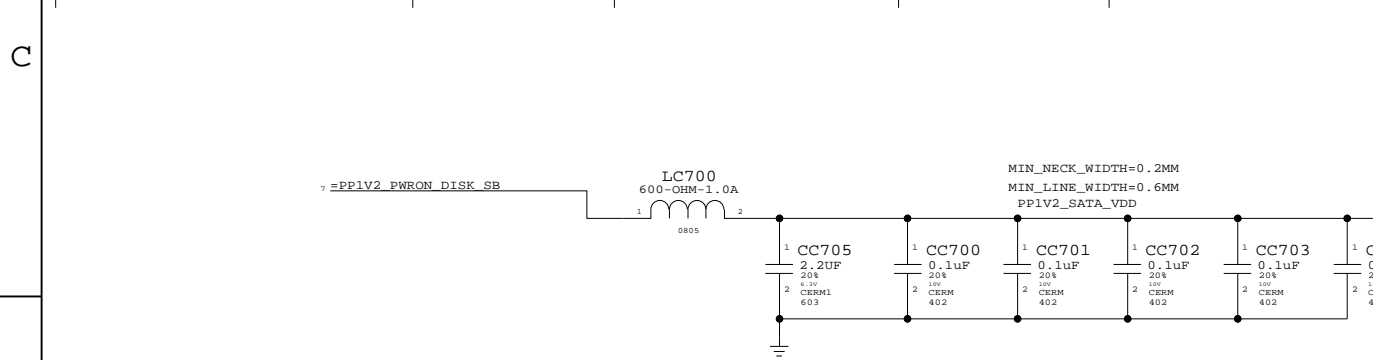
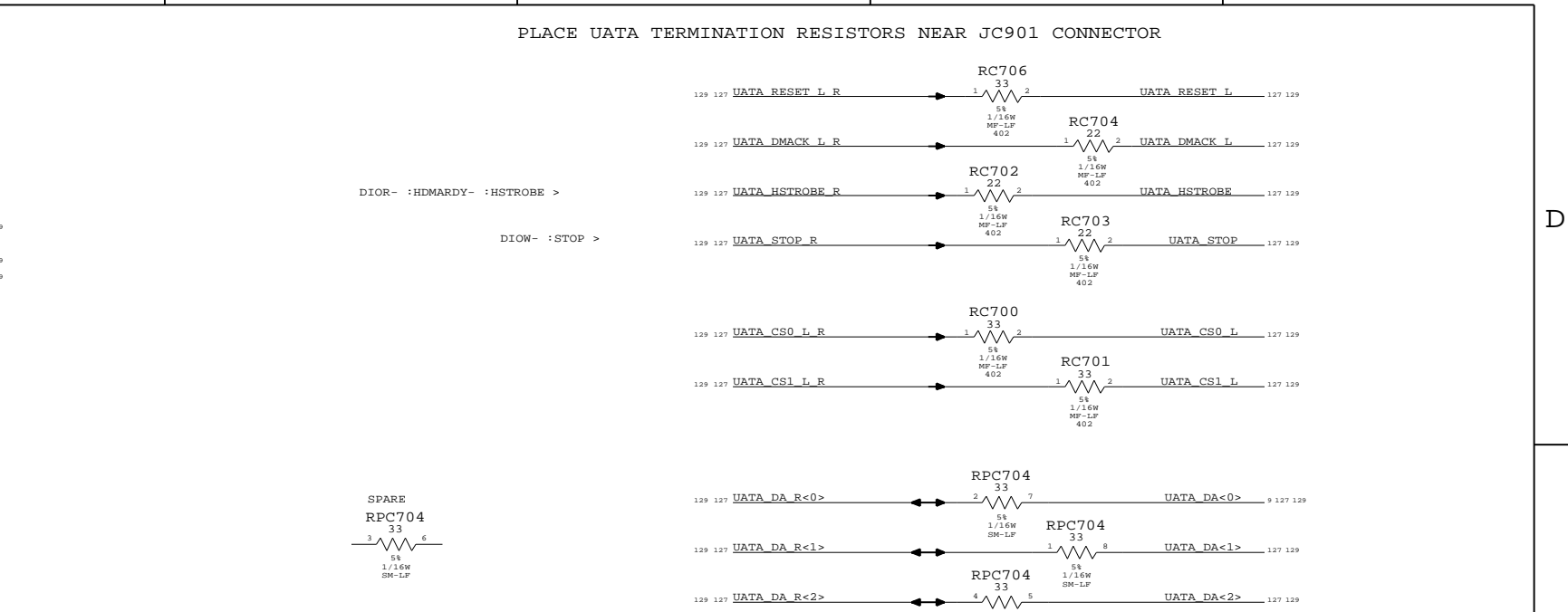
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE		SHT	OF
NONE		125	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	SATA	SATA	SATA_RXD1_C
	SATA	SATA	SATA_RXD1_C
	SATA	SATA	SATA_TXD1
	SATA	SATA	SATA_TXD1
	SATA	SATA	SATA_RXD2_C
	SATA	SATA	SATA_RXD2_C
	SATA	SATA	SATA_TXD2
	SATA	SATA	SATA_TXD2
			UATA_DD<15..8>
			UATA_DD<7>
			UATA_DD<6..0>
			UATA_DA<2..0>
			UATA_CS0_L
			UATA_CS1_L
			UATA_HSTROBE
			UATA_STOP
			UATA_DMACK_L
			UATA_RESET_L
			UATA_DSTROBE
			UATA_DMARQ
			UATA_INTRO
			UATA_DD R<15..8>
			UATA_DD R<7>
			UATA_DD R<6..0>
			UATA_DA R<2..0>
			UATA_CS0 L R
			UATA_CS1 L R
			UATA_DMACK L R
			UATA_HSTROBE R
			UATA_STOP R
			UATA_RESET L R



Page Notes

Power aliases required by this page:
 - _PP1V2_PWRON_DISK

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Net Spacing Type: SATA

Line To Line: 0.38mm
 Length Tolerance: 1.27mm
 Primary Max Sep: 0.25mm outer
 Primary Max Sep: 0.23mm inner
 Secondary Max Sep: 2.54mm
 Secondary Length: 12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

4-29-05
 AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q63.
 RPAK PINS WERE REMAPPED FOR BETTER ROUTING AROUND UATA CONNECTOR.

Shasta Disk
 SYNC_MASTER=M33-DC SYNC_DATE=06/20/2005

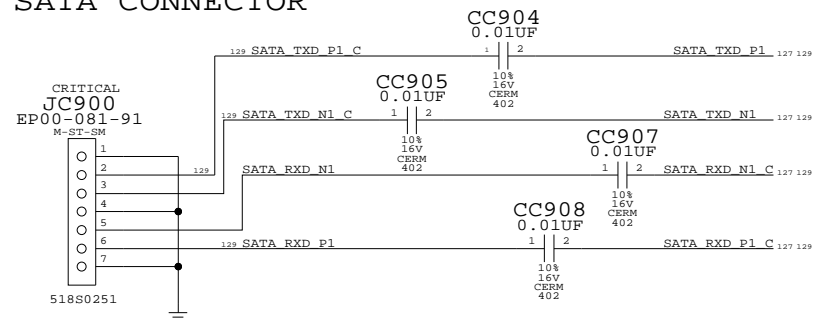
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	D	051-6863	F
SCALE	NONE	SHT	OF
		127	154

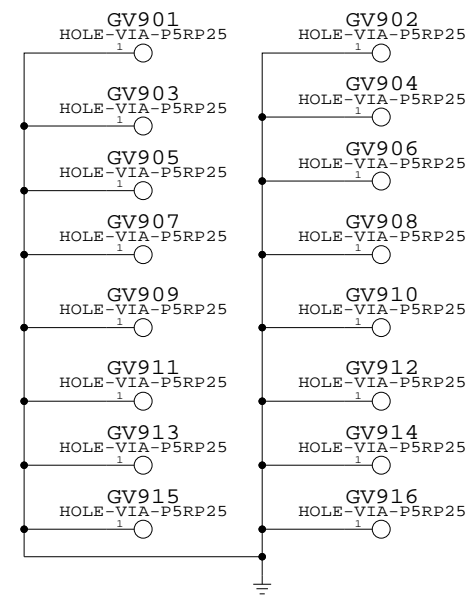
SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

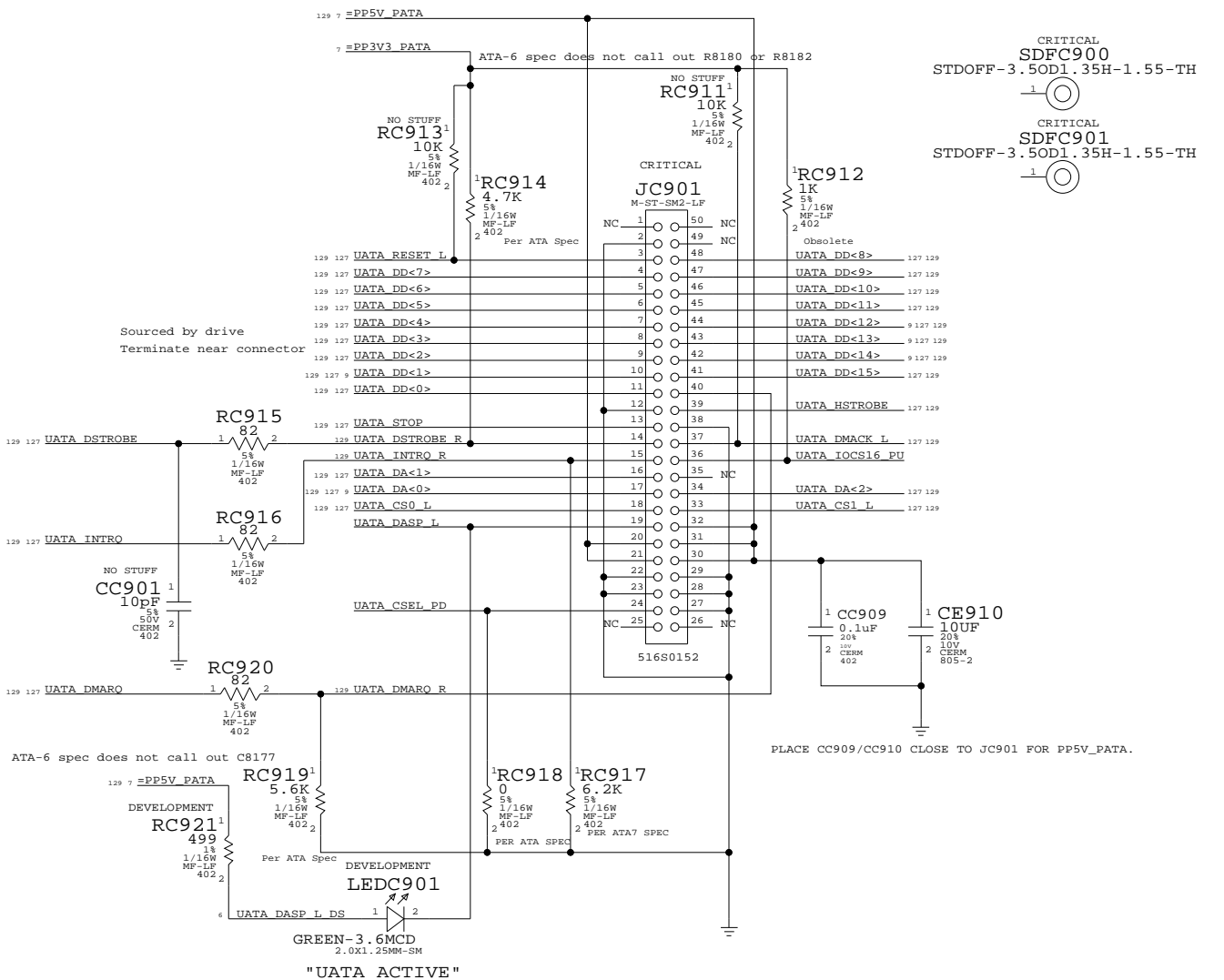
- 127 SATA_TXD_P2 == NC_SATA_TXD_P2 6 MAKE_BASE=TRUE
- 127 SATA_TXD_N2 == NC_SATA_TXD_N2 6 MAKE_BASE=TRUE
- 127 SATA_RXD_N2_C == NC_SATA_RXD_N2_C 6 MAKE_BASE=TRUE
- 127 SATA_RXD_P2_C == NC_SATA_RXD_P2_C 6 MAKE_BASE=TRUE

SATA & USB DIFF PAIR GND VIAS
ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA APPROXIMATELY 0.152MM AWAY FROM SIGNAL VIA.



M33 PATA CONNECTOR

4-12-05



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
129 127	UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA	
129 127	UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA	
129 127	UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA	
129 127	UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA	
129 127	UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA	
129 127	UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA	
129 127	UATA_HSTROBE	UATA_HOST	UATA_NETPH	UATA_NETSPA	
129 127	UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA	
129 127	UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA	
129 127	UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA	
129 127	UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA	
129 127	UATA_DMAR0	UATA_DEV_R	UATA_NETPH	UATA_NETSPA	
129 127	UATA_INTRO_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA	
129 127	UATA_DD_R<15..8>		UATA_NETPH	UATA_NETSPA	4099
127	UATA_DD_R<7>		UATA_NETPH	UATA_NETSPA	4099
127	UATA_DD_R<6..0>		UATA_NETPH	UATA_NETSPA	4099
127	UATA_DA_R<2..0>		UATA_NETPH	UATA_NETSPA	4099
127	UATA_CS0_L_R		UATA_NETPH	UATA_NETSPA	4099
127	UATA_CS1_L_R		UATA_NETPH	UATA_NETSPA	4099
127	UATA_HSTROBE_R		UATA_NETPH	UATA_NETSPA	4099
127	UATA_STOP_R		UATA_NETPH	UATA_NETSPA	4099
127	UATA_DMACK_L_R		UATA_NETPH	UATA_NETSPA	4099
127	UATA_RESET_L_R		UATA_NETPH	UATA_NETSPA	4099
129 127	UATA_DSTROBE		UATA_NETPH	UATA_NETSPA	4099
129 127	UATA_DMAR0		UATA_NETPH	UATA_NETSPA	4099
129 127	UATA_INTRO		UATA_NETPH	UATA_NETSPA	4099
129 127	SATA_TXD_P1	SATA_TXD1	SATA	SATA	TRUE
129 127	SATA_TXD_N1	SATA_TXD1	SATA	SATA	TRUE
129 127	SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C TRUE
129 127	SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C TRUE
129 127	SATA_RXD_N1_C	SATA_RXD1	SATA	SATA	TRUE
129 127	SATA_RXD_P1_C	SATA_RXD1	SATA	SATA	TRUE
129 127	SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C TRUE
129 127	SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C TRUE

UATA FROM RPAKS TO JC901

UATA FROM SHASTA U2300 TO RPAKS

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.
UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05

NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE FOR PP1V2_SATA_VDD AND THEN NECK DOWN TO THE DEFAULT VALUE WHEN NECESSARY. THE WIDTH/NECK PROPERTIES ON PAGE 127 ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL HELP MITIGATE THE LOSS ACROSS THE Q1306 FET SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M33-DC SYNC_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHEET	OF	
NONE	129	154	

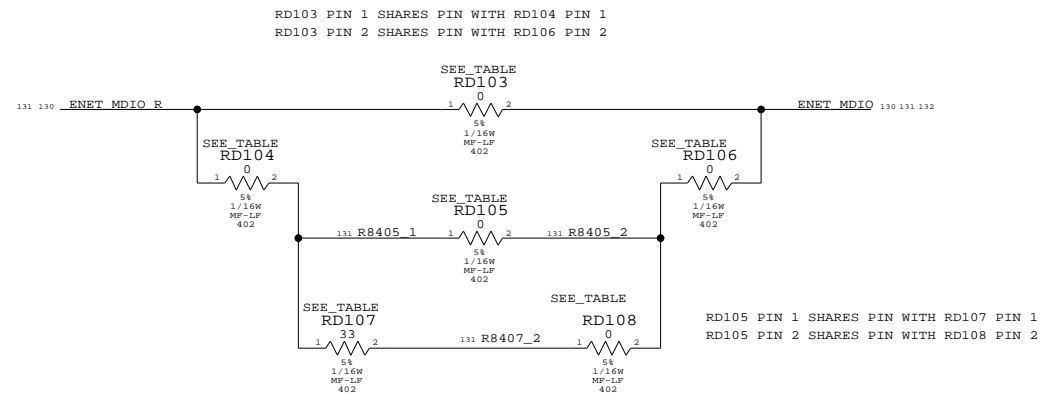
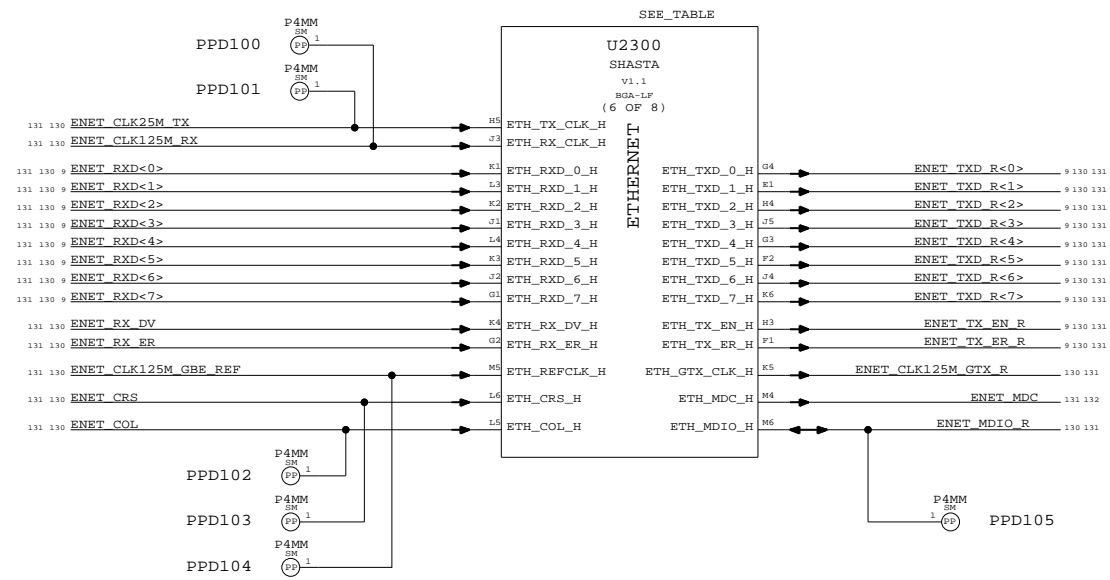
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET	0.38mm SPACING	ENET_CLK25M_TX 130 131
ENET	0.38mm SPACING	ENET_CLK125M_RX 130 131
ENET	0.38mm SPACING	ENET_CLK125M_GBR_REF 130 131
ENET	0.38mm SPACING	ENET_CLK125M_GTX 130 132
ENET	0.38mm SPACING	ENET_CLK125M_GTX_R 130 131
ENET	ENET_FW_2X	ENET_RXD_R<7..0> 9 130 132
ENET	ENET_FW_3X	ENET_RX_DV_R 130 132
ENET	ENET_FW_3X	ENET_RX_ER_R 130 132
ENET	ENET_FW_2X	ENET_RXD<7..0> 9 130 131
ENET	ENET_FW_3X	ENET_RX_DV 130 131
ENET	ENET_FW_3X	ENET_RX_ER 130 131
ENET	ENET_FW_2X	ENET_TXD_R<7..0> 9 130 131
ENET	ENET_FW_3X	ENET_TX_EN_R 9 130 131
ENET	ENET_FW_3X	ENET_TX_ER_R 9 130 131
ENET	ENET_FW_2X	ENET_TXD<7..0> 9 130 132
ENET	ENET_FW_3X	ENET_TX_EN 9 130 132
ENET	ENET_FW_3X	ENET_TX_ER 9 130 132
ENET	ENET_FW_3X	ENET_CR_S_R 130 132
ENET	ENET_FW_3X	ENET_COL_R 130 132
ENET	ENET_FW_3X	ENET_CR_S 130 131
ENET	ENET_FW_3X	ENET_COL 130 131
ENET	ENET_FW_3X	ENET_MDC 131 132
ENET	ENET_FW_3X	ENET_MDIO 130 131 132
ENET	ENET_FW_3X	ENET_MDIO_R 130 131
ENET	ENET_FW_3X	RB405_1 131
ENET	ENET_FW_3X	RB405_2 131
ENET	ENET_FW_3X	RB407_2 131

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES, 0-OHM, 402, 5%	RD103		ENET_MDIO_DELAY_0 *
116S0004	3	RES, 0-OHM, 402, 5%	RD104, RD105, RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES, 0-OHM, 402, 5%	RD104, RD108, RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES, 33-OHM, 402, 5%	RD107		ENET_MDIO_DELAY_4NS

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	131	154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET	0.38mm SPACING	ENET_CLK125M_GBE_REF_R 130 132
ENET	0.38mm SPACING	ENET_CLK125M_RX_R 130 132
ENET	0.38mm SPACING	ENET_CLK25M_TX_R 130 132
ENET	ENET	ENET_MDI0 132 136
ENET	ENET	ENET_MDI0 132 136
ENET	ENET	ENET_MDI1 132 136
ENET	ENET	ENET_MDI1 132 136
ENET	ENET	ENET_MDI2 132 136
ENET	ENET	ENET_MDI2 132 136
ENET	ENET	ENET_MDI3 132 136
ENET	ENET	ENET_MDI3 132 136
ENET	0.38mm SPACING	VESTA_CLK25M_XTALI 132
ENET	0.38mm SPACING	VESTA_CLK25M_XTALO 132
ENET	0.38mm SPACING	VESTA_CLK25M_XTALO_R 132

Page Notes

Power aliases required by this page:
 - =PP3V3_ENET
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
 Length Tolerance: 1.27mm
 Primary Max Sep: 0.13mm
 Secondary Max Sep: 2.54mm
 Secondary Length: 12.70mm

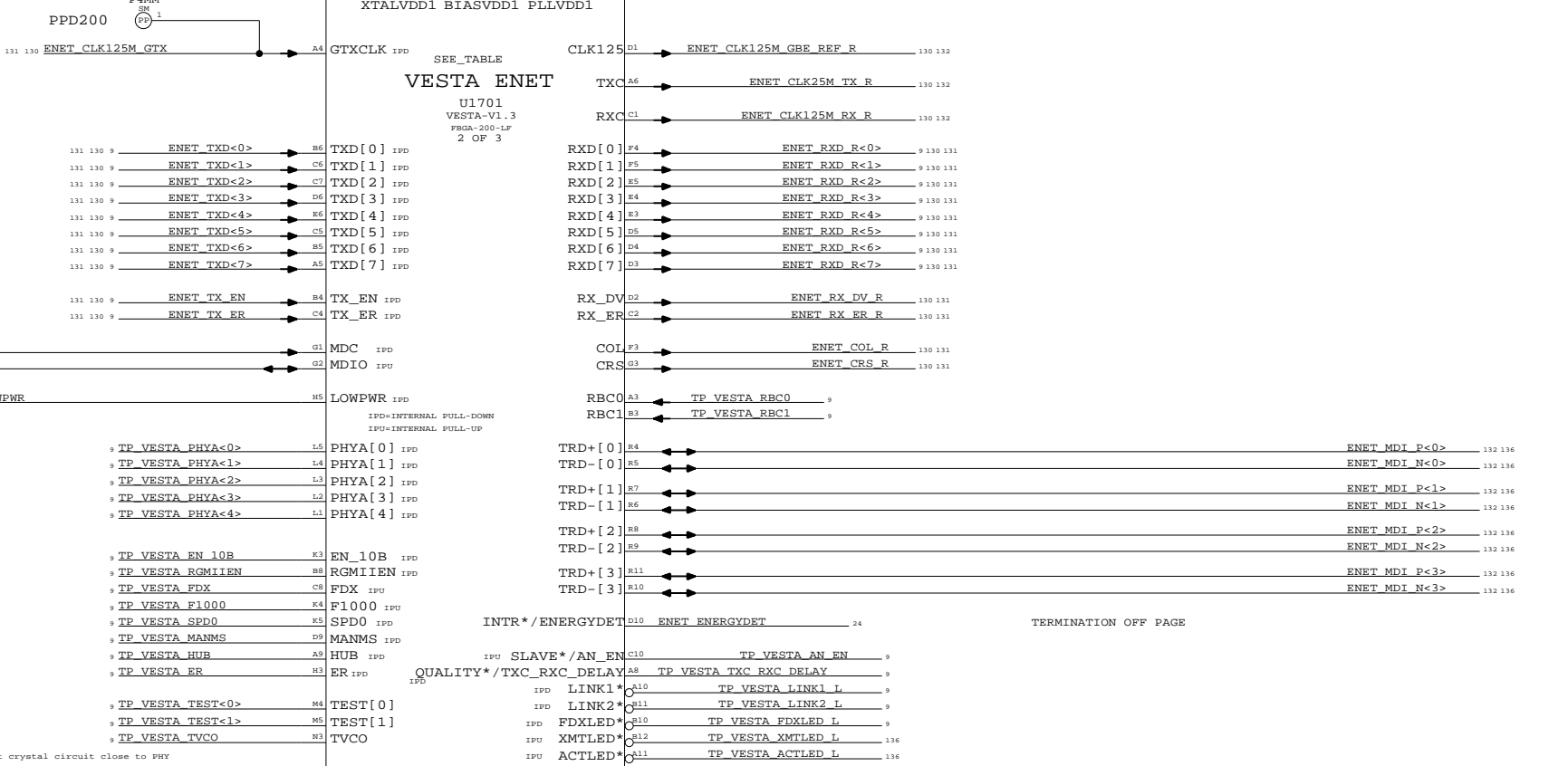
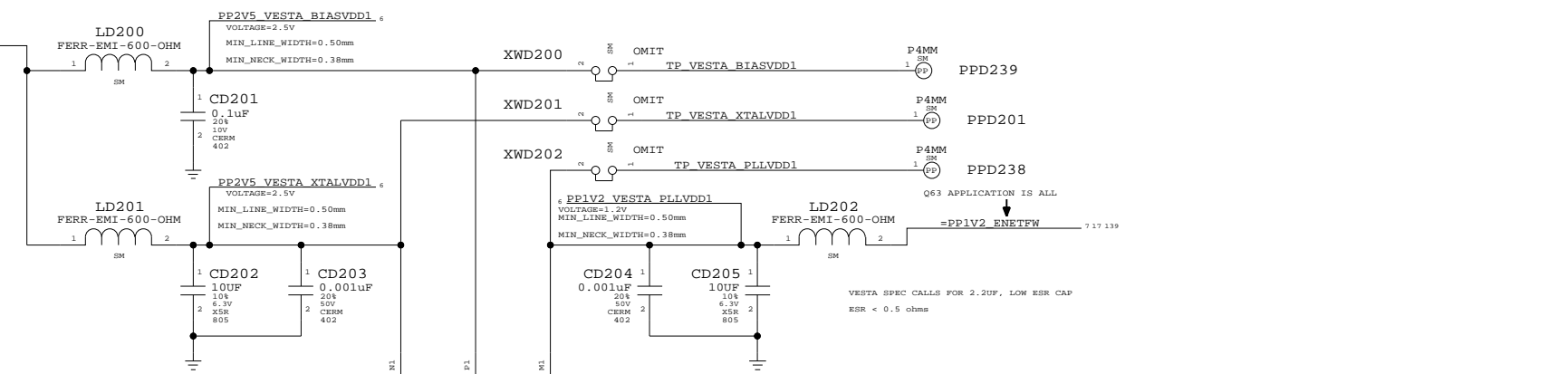
NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Q63 APPLICATION IS ALL

139 17 7 =PP2V5_ENETFW

Q63 APPLICATION IS ALL

7 17 139 =PP1V2_ENETFW

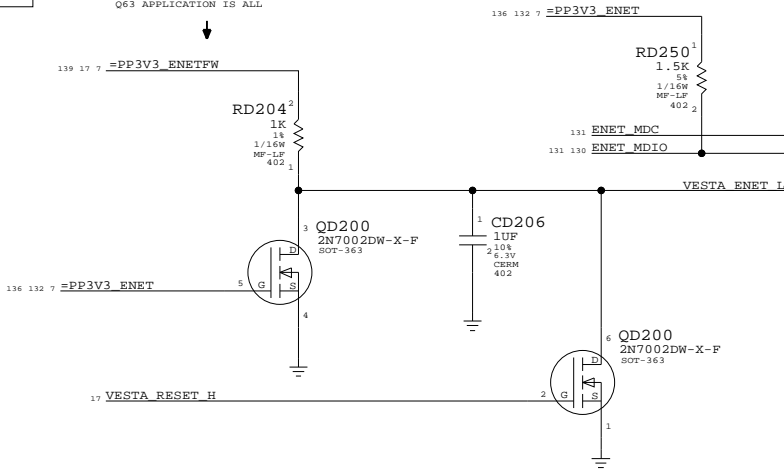


Q63 APPLICATION IS ALL

139 17 7 =PP3V3_ENETFW

Q63 APPLICATION IS ALL

136 132 7 =PP3V3_ENET



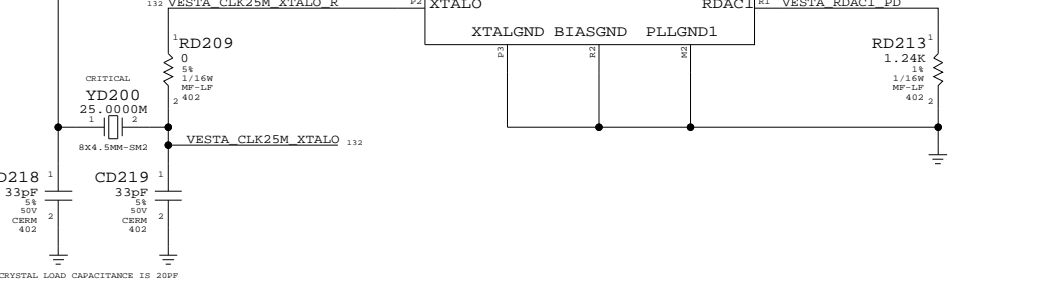
Vesta Config Straps:

PHYA<4..0>	PHY Address Select (Internal Pull-downs)	MANMS	Manual Master/Slave Configuration Select (Internal Pull-down)
EN_10B	TBI Interface Select (Internal Pull-down)	HUB	Repeater Select (Internal Pull-down)
RGMIIEN	RGMII Enable (Internal Pull-down)	ER	Edge Rate Select (Internal Pull-down)
FDX	Full-Duplex Select (Internal Pull-up)	AM_EN	Auto-Negotiation Select (Internal Pull-down)
F1000	Speed Select (Internal Pull-up)	SPD0	Speed Select (Internal Pull-down)
AN_EN	Force 10BASE-T (Internal Pull-down)		

Put crystal circuit close to PHY

CRITICAL

CRYSTAL LOAD CAPACITANCE IS 20PF



TERMINATION OFF PAGE

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. F
	SCALE NONE	SHT 132	OF 154

8

7

6

5

4

3

2

1

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET	NET PHYSICAL TYPE	VALUE	REF
ENET	ENET MDI P<0>	132 136	
ENET	ENET MDI N<0>	132 136	
ENET	ENET MDI P<1>	132 136	
ENET	ENET MDI N<1>	132 136	
ENET	ENET MDI P<2>	132 136	
ENET	ENET MDI N<2>	132 136	
ENET	ENET MDI P<3>	132 136	
ENET	ENET MDI N<3>	132 136	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDES ON TOP SIDE OF BOARD

D

D

C

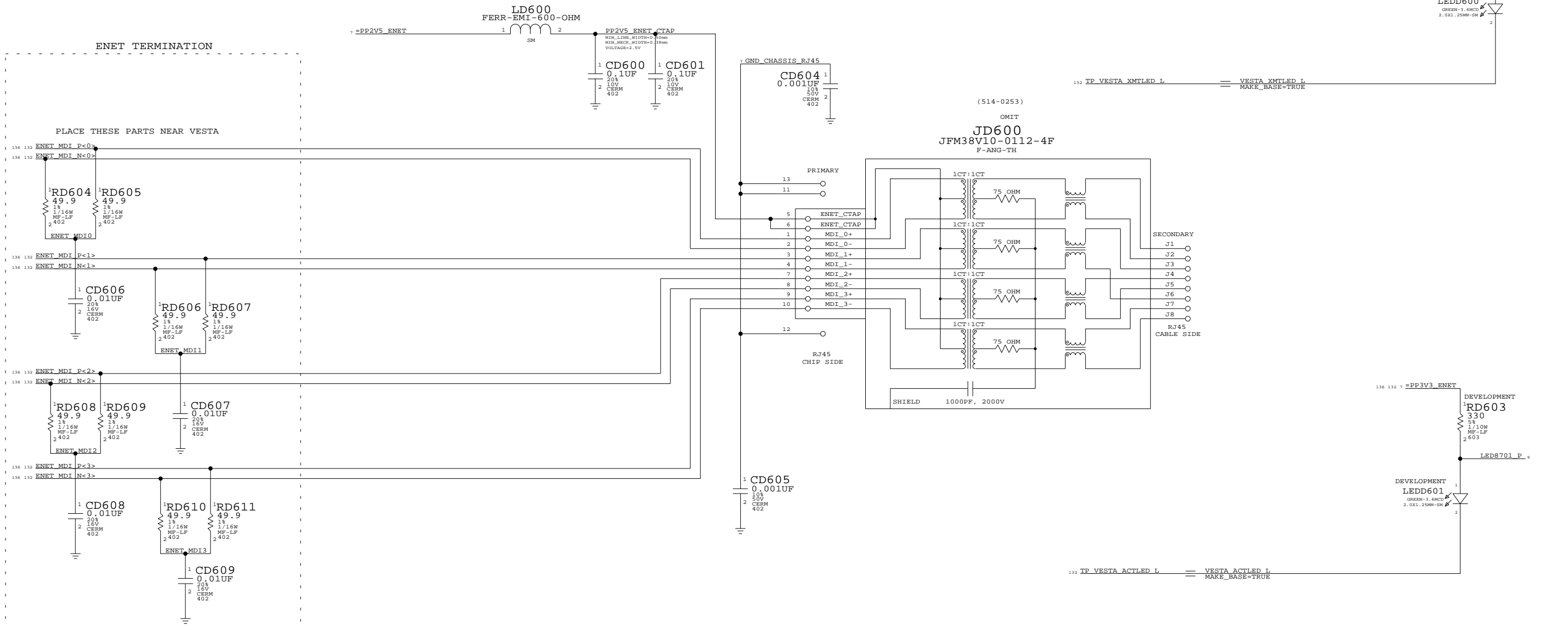
C

B

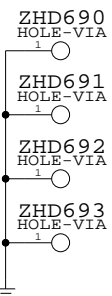
B

A

A



SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING



ETHERNET CONNECTOR
 SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	136 OF 154		

8

7

6

5

4

3

2

1

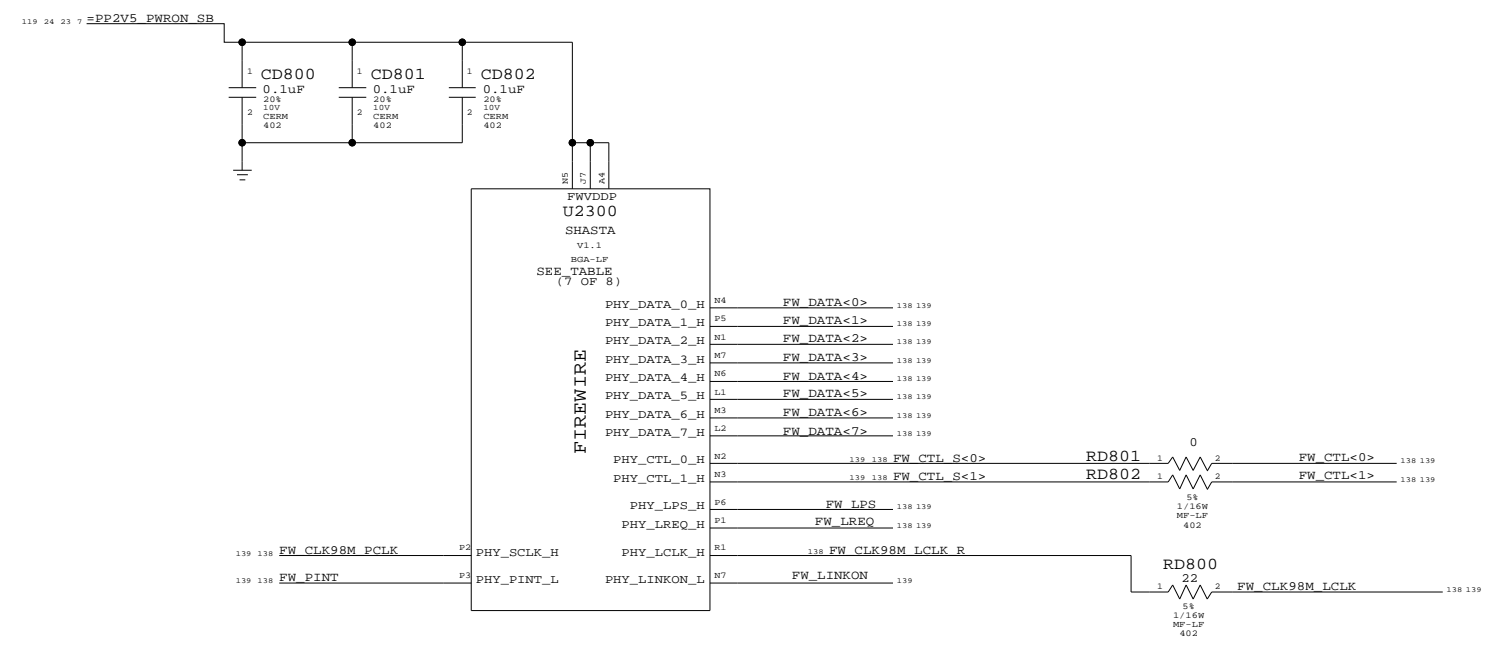
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW	ENET_FW_2X	FW_DATA<7..0>
FW	ENET_FW_3X	FW_CTL_S<1..0>
FW	ENET_FW_3X	FW_CTL<1..0>
FW	ENET_FW_2X	FW_DATA_R<7..0>
FW	ENET_FW_3X	FW_CTL_R<1..0>
FW	ENET_FW_3X	FW_LPS
FW	ENET_FW_3X	FW_LREQ
FW	ENET_FW_3X	FW_PINT
FW	0.38mm SPACING	FW_CLK98M_LCLK
FW	0.38mm SPACING	FW_CLK98M_PCLK
FW	0.38mm SPACING	FW_CLK98M_LCLK_R

Page Notes

Power aliases required by this page:
 - _PP2V5_PWRON_SB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

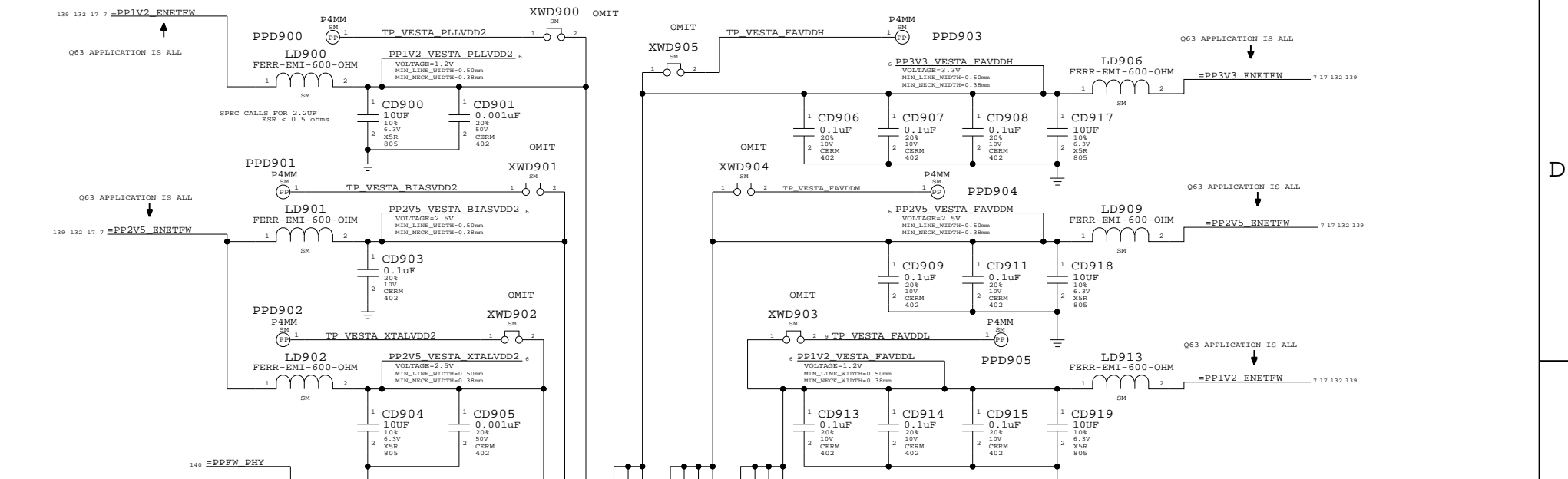
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT OF		
NONE	138	154	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
(PROVIDED BY LINK PAGE)		0.38mm SPACING	
	FW	FW	FW_TPA0
	FW	FW	FW_TPA P<0>
	FW	FW	FW_TPB0
	FW	FW	FW_TPB P<0>
	FW	FW	FW_TPA1
	FW	FW	FW_TPA P<1>
	FW	FW	FW_TPB1
	FW	FW	FW_TPB P<1>
	FW	FW	FW_TPA2
	FW	FW	FW_TPA P<2>
	FW	FW	FW_TPB2
	FW	FW	FW_TPB N<2>
		0.38mm SPACING	VESTA_CLK24M_XTALI
		0.38mm SPACING	VESTA_CLK24M_XTALO
		0.38mm SPACING	VESTA_CLK24M_XTALO_R
	FW_CTL		FW_CTL_S<1..0>
	FW_CTL		FW_CTL<1..0>
	FW_CTL		FW_CTL_R<1..0>



Page Notes

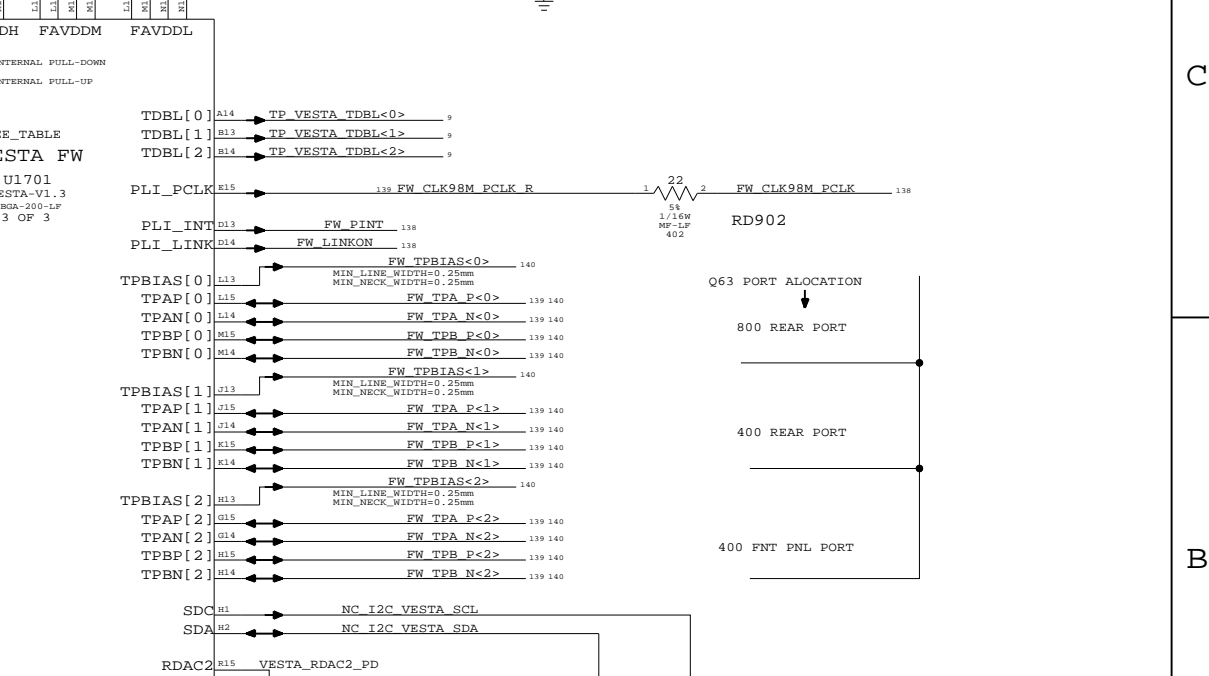
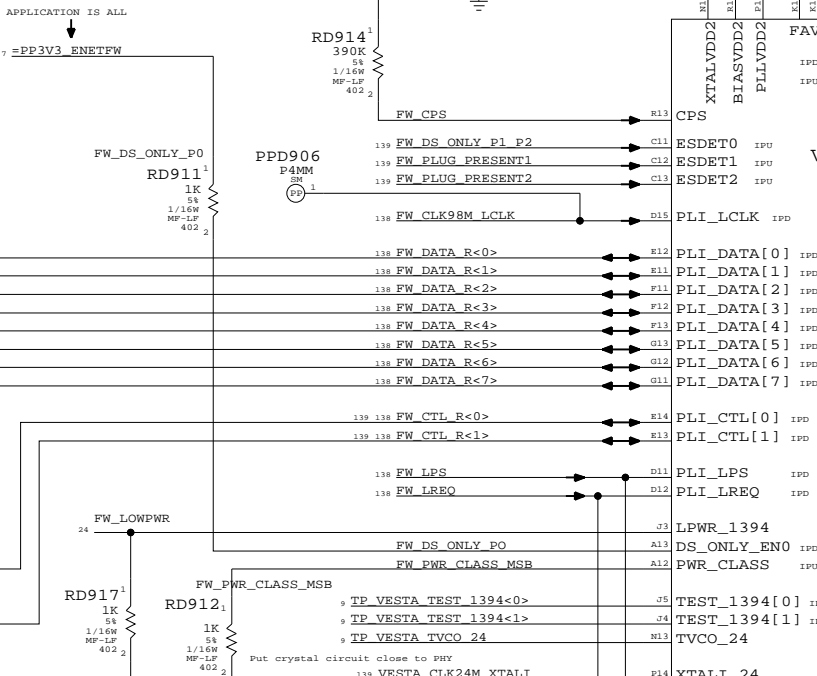
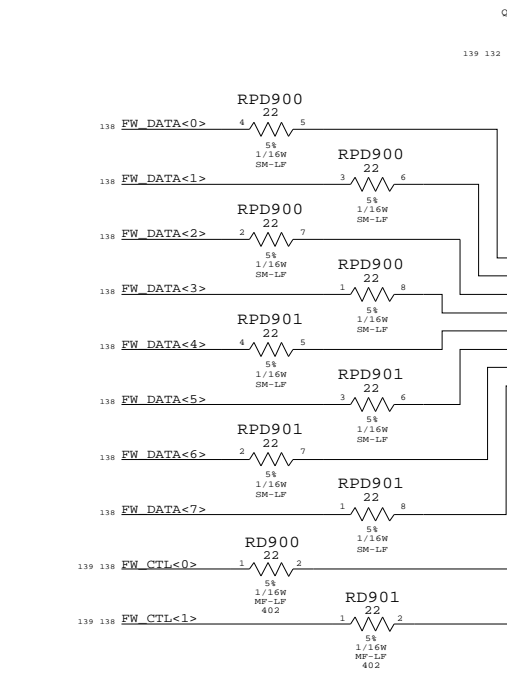
Power aliases required by this page:
 - =PPFW_PHY
 - =PP3V3_FW
 - =PP3V3_ENETFW
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - VESTA_DS_ONLY_EN0
 If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
 - VESTA_PWR_CLASS_0
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

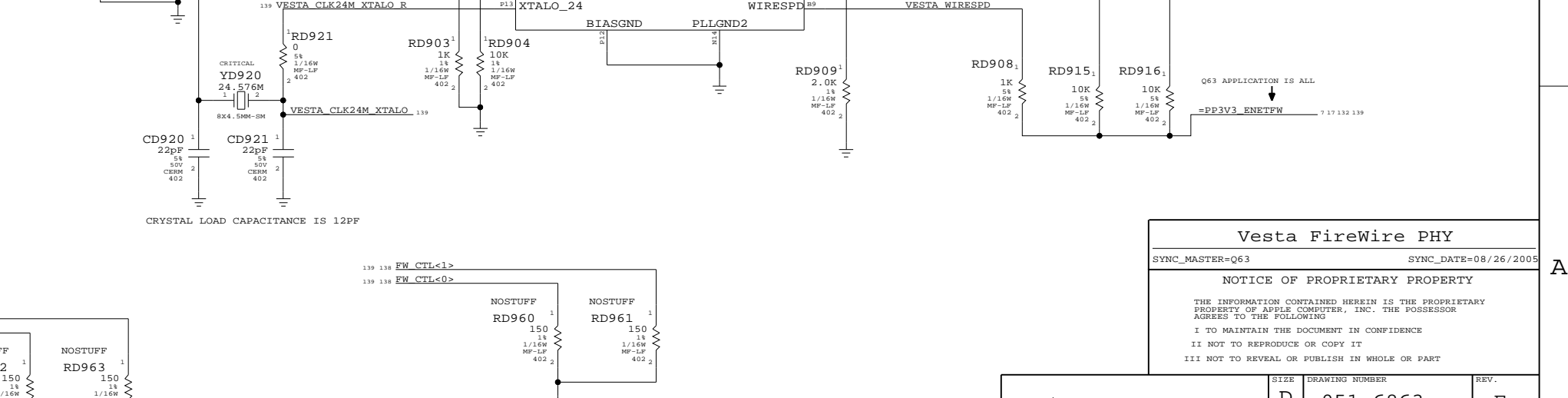
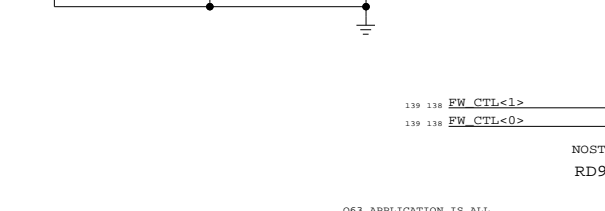
NOTE: Target differential impedance for FW data pairs is 110 ohms.



VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
 1 - Sets Power Class to 0x4
 0 - Sets Power Class to 0x0
 (Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
 1 - Port 0 Data/strobe mode only
 0 - Port 0 Billingual mode
 (Internal Pull-down)



Vesta FireWire PHY

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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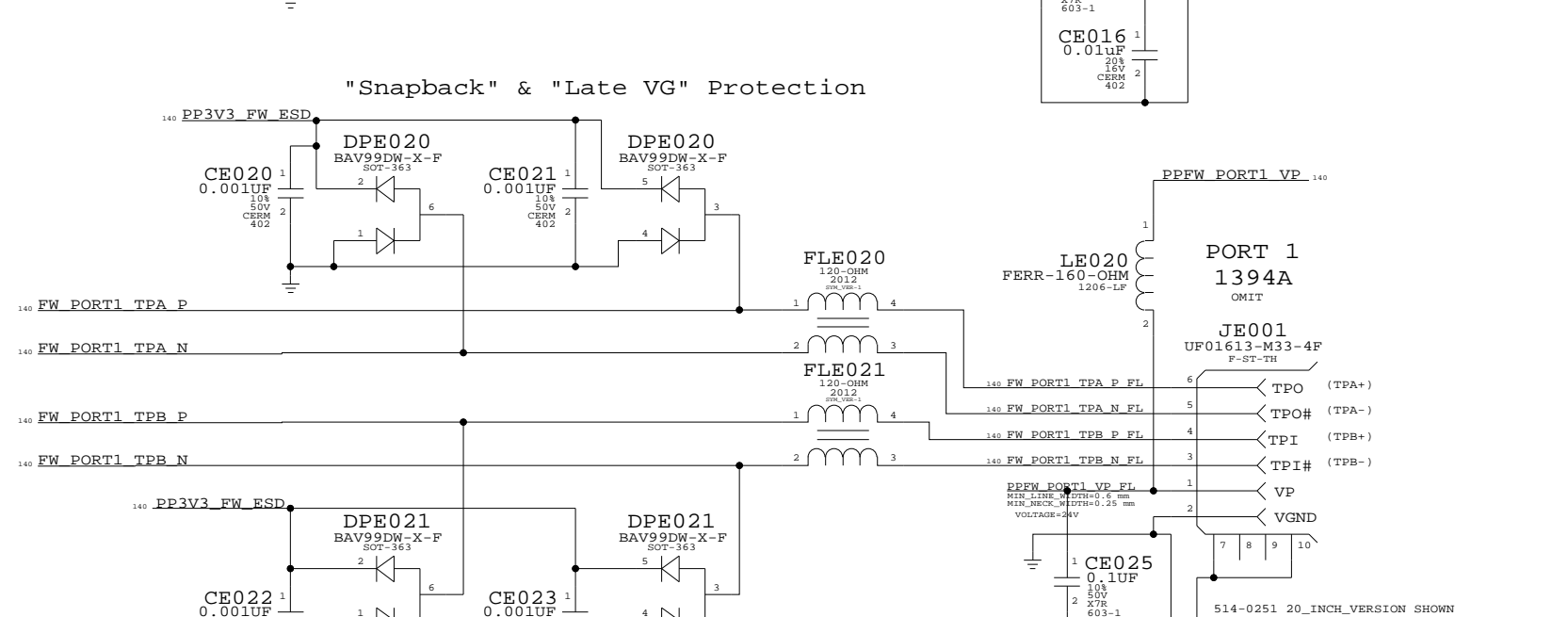
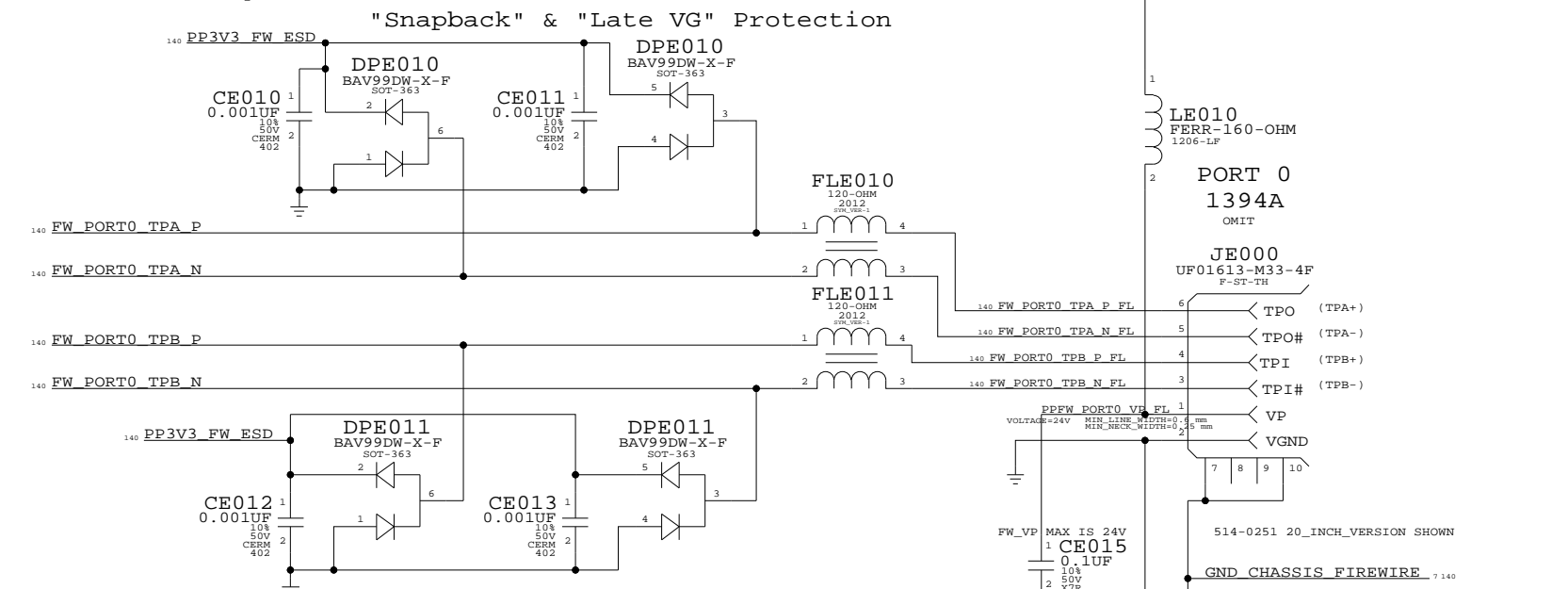
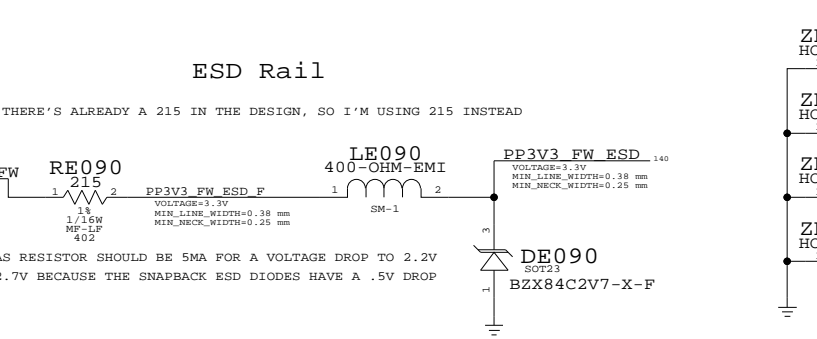
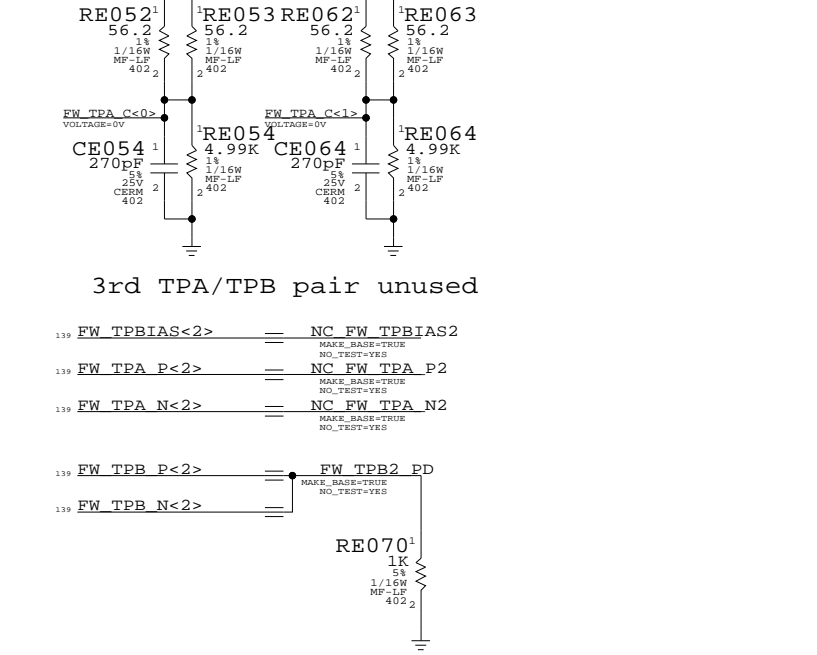
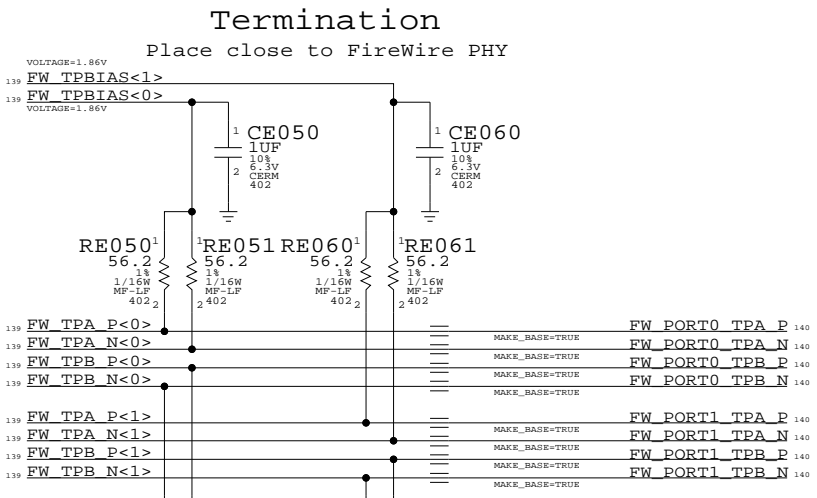
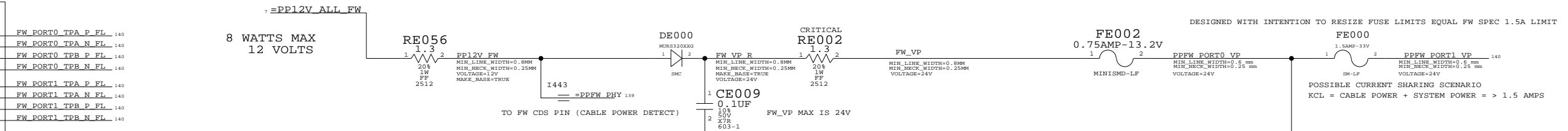
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SIZE	DRAWING NUMBER	REV.
D	051-6863	F
SCALE	SHT	OF
NONE	139	154

NET_TYPE		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FW	FW	FW_TPA0_FL	FW_TPA0_FL	FW_TPA0_FL
FW	FW	FW_TPA0_N_FL	FW_TPA0_N_FL	FW_TPA0_N_FL
FW	FW	FW_TPB0_FL	FW_TPB0_FL	FW_TPB0_FL
FW	FW	FW_TPB0_N_FL	FW_TPB0_N_FL	FW_TPB0_N_FL
FW	FW	FW_TPA1_FL	FW_TPA1_FL	FW_TPA1_FL
FW	FW	FW_TPA1_N_FL	FW_TPA1_N_FL	FW_TPA1_N_FL
FW	FW	FW_TPB1_FL	FW_TPB1_FL	FW_TPB1_FL
FW	FW	FW_TPB1_N_FL	FW_TPB1_N_FL	FW_TPB1_N_FL



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE COMPUTER INC.

SIZE: D DRAWING NUMBER: 051-6863 REV. F

SCALE: NONE SHEET: 140 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_2
	USB2	USB2_S	USB2_3
	USB2	USB2_S	USB2_4
	0.38mm SPACING		NEC_CLK30M_XT1
	0.38mm SPACING		NEC_CLK30M_XT2
	0.38mm SPACING		NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

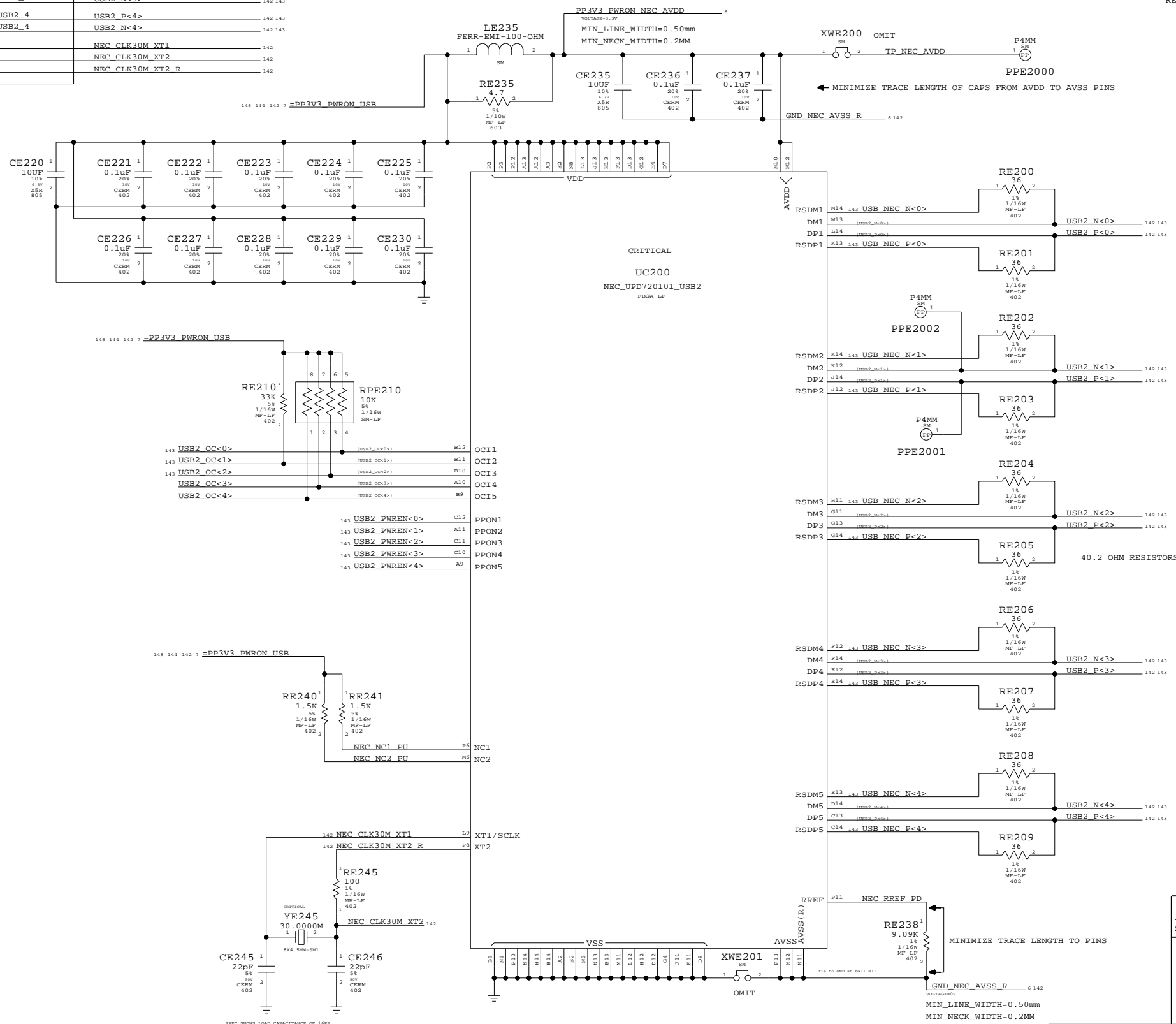
Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300 SHASTA V1.1 BGA-LP (8 OF 8)

NC0	P7	TP_SB<0>	6
NC1	P8	TP_SB<1>	6
NC2	P3	TP_SB<2>	6
NC3	P4	TP_SB<3>	6
NC4	P5	TP_SB<4>	6
NC5	P6	TP_SB<5>	6
NC6	P7	TP_SB<6>	6
NC7	P8	TP_SB<7>	6
NC8	T1	TP_SB<8>	6
NC9	T2	TP_SB<9>	6
NC10	T3	TP_SB<10>	6
NC11	T4	TP_SB<11>	6
NC12	T5	TP_SB<12>	6
NC13	T6	TP_SB<13>	6
NC14	T7	TP_SB<14>	6
NC15	T8	TP_SB<15>	6
NC16	U1	TP_SB<16>	6
NC17	U2	TP_SB<17>	6
NC18	U3	TP_SB<18>	6
NC19	U4	TP_SB<19>	6
NC20	U5	TP_SB<20>	6
NC21	U6	TP_SB<21>	6
NC22	V1	TP_SB<22>	6
NC23	V2	TP_SB<23>	6
NC24	V3	TP_SB<24>	6
NC25	V4	TP_SB<25>	6
NC26	W1	TP_SB<26>	6
NC27	W3	TP_SB<27>	6
NC28	Y1	TP_SB<28>	6
NC29	Y3	TP_SB<29>	6



Q63 USB PORT ALLOCATION

REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION

BLUETOOTH CONNECTOR, (PORT #4)

USB Host Interfaces

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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SCALE	DRAWING NUMBER	REV.
NONE	051-6863	F
	SHEET	OF
	142	154

Page Notes

Power aliases required by this page:

- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

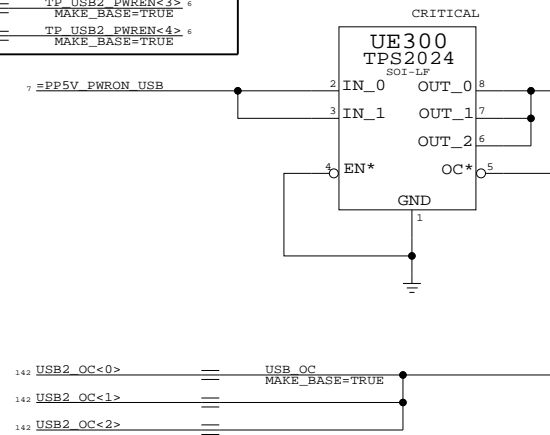
BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- 142 USB2_PWRN<0> == TP_USB2_PWRN<0> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<1> == TP_USB2_PWRN<1> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<2> == TP_USB2_PWRN<2> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<3> == TP_USB2_PWRN<3> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<4> == TP_USB2_PWRN<4> 6 MAKE_BASE=TRUE

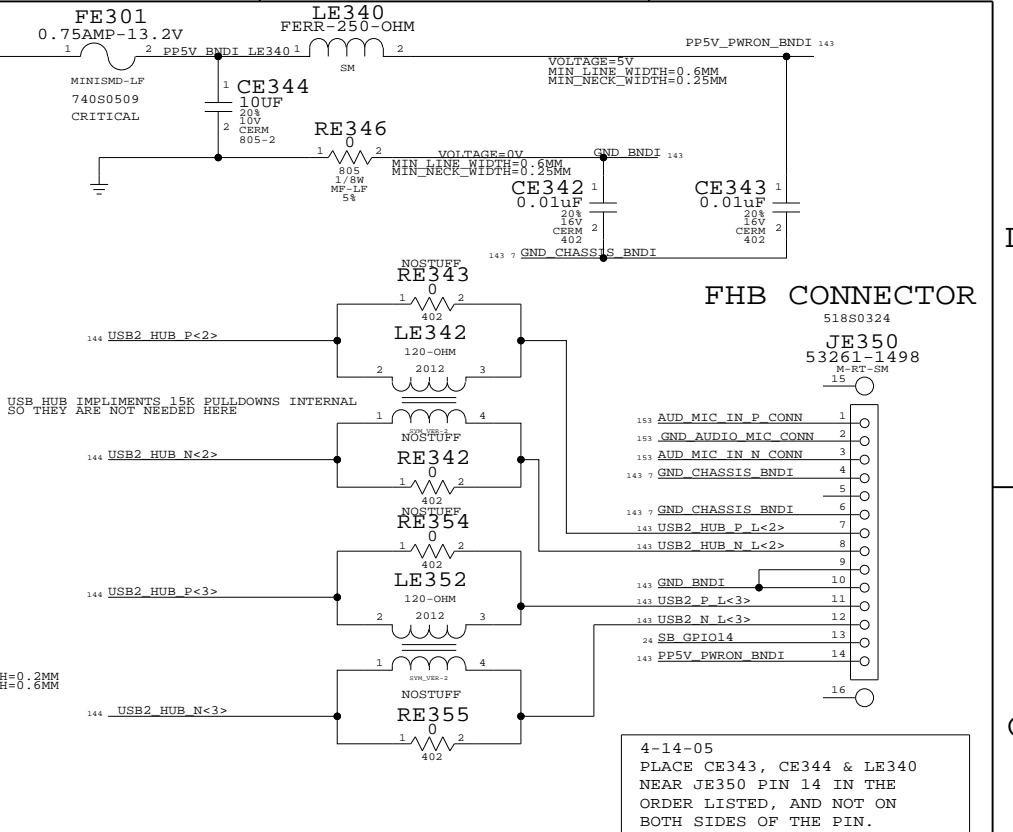
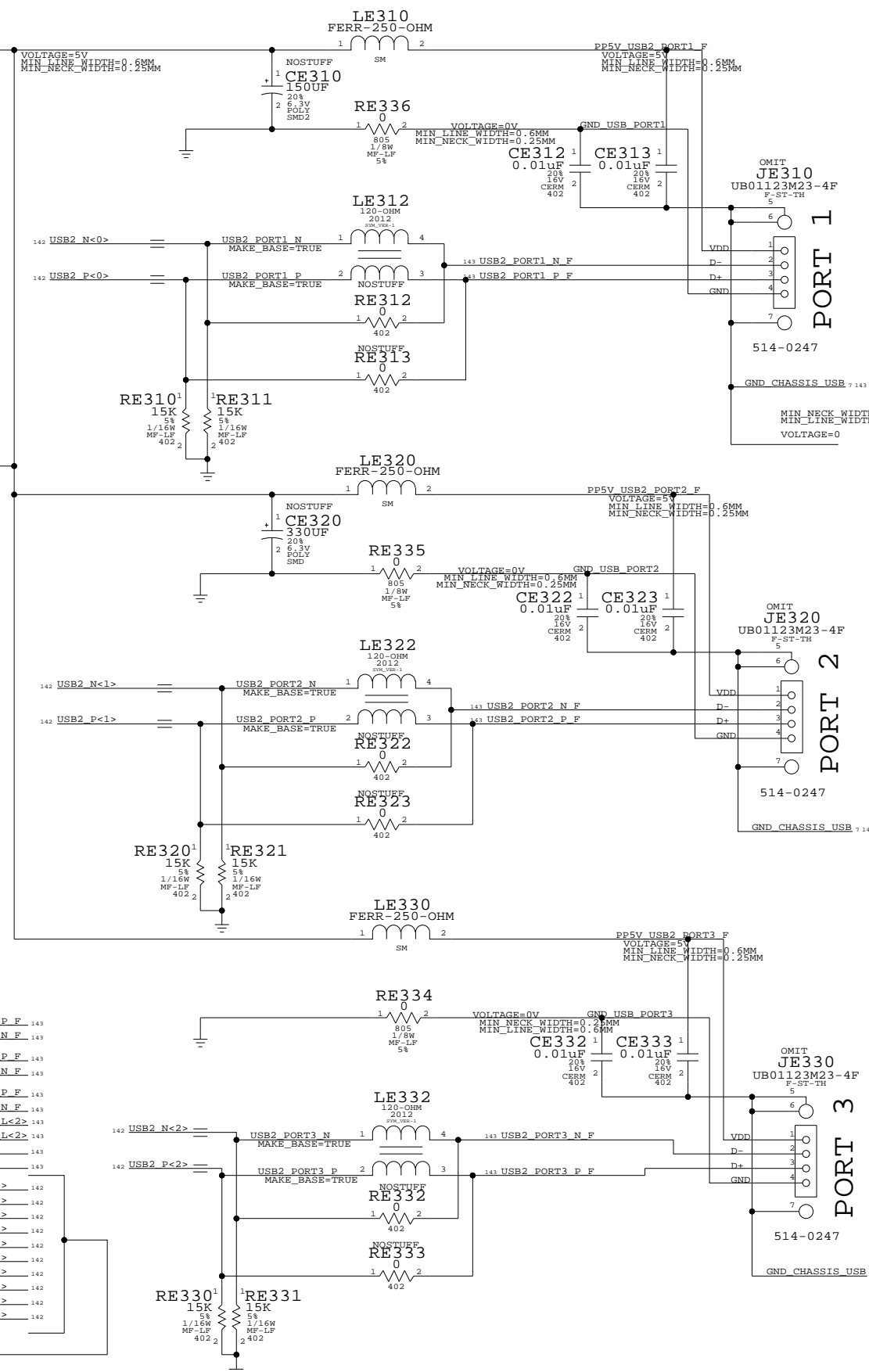


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23B-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33B-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE
PROVIDED	USB2	USB2_PORT1_P_F	USB2 USB2_PORT1_P_F 143
BY	USB2	USB2_PORT1_F	USB2 USB2_PORT1_N_F 143
USB	USB2	USB2_PORT2_F	USB2 USB2_PORT2_P_F 143
CONTROLLER	USB2	USB2_PORT2_F	USB2 USB2_PORT2_N_F 143
	USB2	USB2_PORT3_F	USB2 USB2_PORT3_P_F 143
	USB2	USB2_PORT3_F	USB2 USB2_PORT3_N_F 143
	USB2	USB2_HUB_F	USB2 USB2_HUB_P_L<2> 143
	USB2	USB2_HUB_F	USB2 USB2_HUB_N_L<2> 143
	USB2	USB2_BNDI_F	USB2 USB2_P_L<3> 143
	USB2	USB2_BNDI_F	USB2 USB2_N_L<3> 143
	USB2	USB2_0_IC	USB2 USB_NEC_P<0> 142
	USB2	USB2_0_IC	USB2 USB_NEC_N<0> 142
	USB2	USB2_1_IC	USB2 USB_NEC_P<1> 142
	USB2	USB2_1_IC	USB2 USB_NEC_N<1> 142
	USB2	USB2_2_IC	USB2 USB_NEC_P<2> 142
	USB2	USB2_2_IC	USB2 USB_NEC_N<2> 142
	USB2	USB2_3_IC	USB2 USB_NEC_P<3> 142
	USB2	USB2_3_IC	USB2 USB_NEC_N<3> 142
	USB2	USB2_4_IC	USB2 USB_NEC_P<4> 142
	USB2	USB2_4_IC	USB2 USB_NEC_N<4> 142

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

External USB Ports



4-14-05
PLACE CE343, CE344 & LE340
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

USB Device Interfaces

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

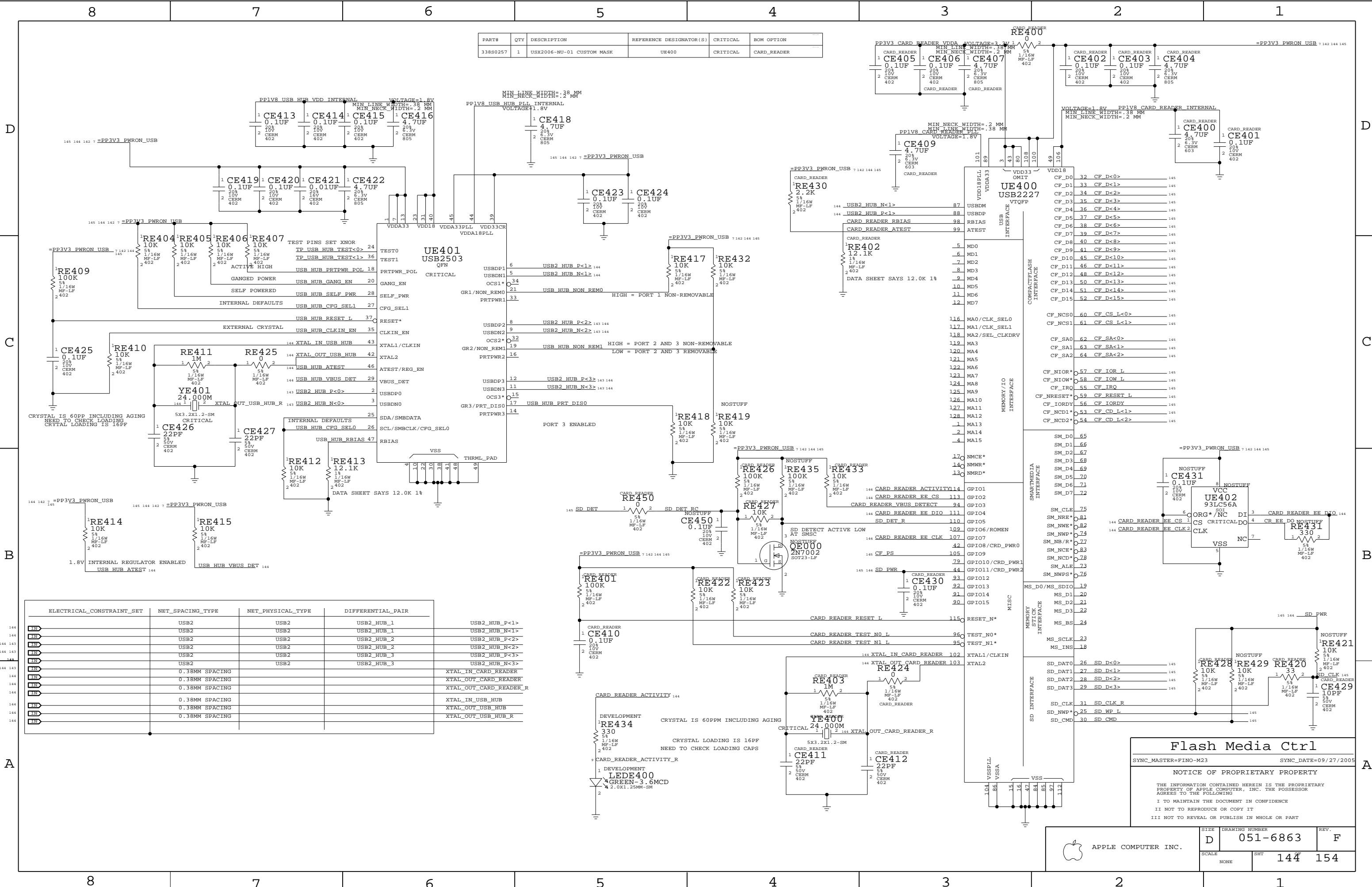
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	D	051-6863	F
SCALE	SHEET	OF	
NONE	143	154	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0257	1	USX2006-NU-01 CUSTOM MASK	UE400	CRITICAL	CARD_READER



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
MIN	USB2	USB2	USB2_HUB_1
MIN	USB2	USB2	USB2_HUB_1
MIN	USB2	USB2	USB2_HUB_2
MIN	USB2	USB2	USB2_HUB_2
MIN	USB2	USB2	USB2_HUB_3
MIN	USB2	USB2	USB2_HUB_3
MIN	0.38MM SPACING	XTAL_IN_CARD_READER	XTAL_IN_CARD_READER
MIN	0.38MM SPACING	XTAL_OUT_CARD_READER	XTAL_OUT_CARD_READER_R
MIN	0.38MM SPACING	XTAL_OUT_CARD_READER	XTAL_OUT_CARD_READER_R
MIN	0.38MM SPACING	XTAL_IN_USB_HUB	XTAL_IN_USB_HUB
MIN	0.38MM SPACING	XTAL_OUT_USB_HUB	XTAL_OUT_USB_HUB
MIN	0.38MM SPACING	XTAL_OUT_USB_HUB	XTAL_OUT_USB_HUB_R

Signal Name	Pin	Signal Name	Pin
CF_D0	32	CF_D<0>	145
CF_D1	33	CF_D<1>	145
CF_D2	34	CF_D<2>	145
CF_D3	35	CF_D<3>	145
CF_D4	36	CF_D<4>	145
CF_D5	37	CF_D<5>	145
CF_D6	38	CF_D<6>	145
CF_D7	39	CF_D<7>	145
CF_D8	40	CF_D<8>	145
CF_D9	41	CF_D<9>	145
CF_D10	45	CF_D<10>	145
CF_D11	46	CF_D<11>	145
CF_D12	48	CF_D<12>	145
CF_D13	50	CF_D<13>	145
CF_D14	51	CF_D<14>	145
CF_D15	52	CF_D<15>	145
CF_NCS0	60	CF_CS L<0>	145
CF_NCS1	61	CF_CS L<1>	145
CF_SA0	62	CF_SA<0>	145
CF_SA1	63	CF_SA<1>	145
CF_SA2	64	CF_SA<2>	145
CF_NIOR*	57	CF_IOR L	145
CF_NIOW*	58	CF_IOW L	145
CF_IRQ	55	CF_IRQ	145
CF_NRESET*	59	CF_RESET L	145
CF_IORDY	56	CF_IORDY	145
CF_NCD1*	53	CF_CD L<1>	145
CF_NCD2*	54	CF_CD L<2>	145
SM_D0	65	SM_D0	145
SM_D1	66	SM_D1	145
SM_D2	67	SM_D2	145
SM_D3	68	SM_D3	145
SM_D4	69	SM_D4	145
SM_D5	70	SM_D5	145
SM_D6	71	SM_D6	145
SM_D7	72	SM_D7	145
SM_CLE	75	SM_CLE	145
SM_NRE*	81	SM_NRE*	145
SM_NWE*	82	SM_NWE*	145
SM_NWP*	74	SM_NWP*	145
SM_NBR*	77	SM_NBR*	145
SM_NCE*	83	SM_NCE*	145
SM_NCD*	78	SM_NCD*	145
SM_ALE	73	SM_ALE	145
SM_NWPS*	76	SM_NWPS*	145
MS_D0/MS_SDIO	19	MS_D0/MS_SDIO	145
MS_D1	20	MS_D1	145
MS_D2	21	MS_D2	145
MS_D3	22	MS_D3	145
MS_BS	24	MS_BS	145
MS_SCLK	23	MS_SCLK	145
MS_INS	18	MS_INS	145
SD_DAT0	26	SD_D<0>	145
SD_DAT1	27	SD_D<1>	145
SD_DAT2	28	SD_D<2>	145
SD_DAT3	29	SD_D<3>	145
SD_CLK	31	SD_CLK R	145
SD_NWP*	25	SD_WP L	145
SD_CMD	30	SD_CMD	145

Flash Media Ctrl

SYNC_MASTER=FINO-M23 SYNC_DATE=09/27/2005

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SCALE	SHT	144	154
NONE			

8

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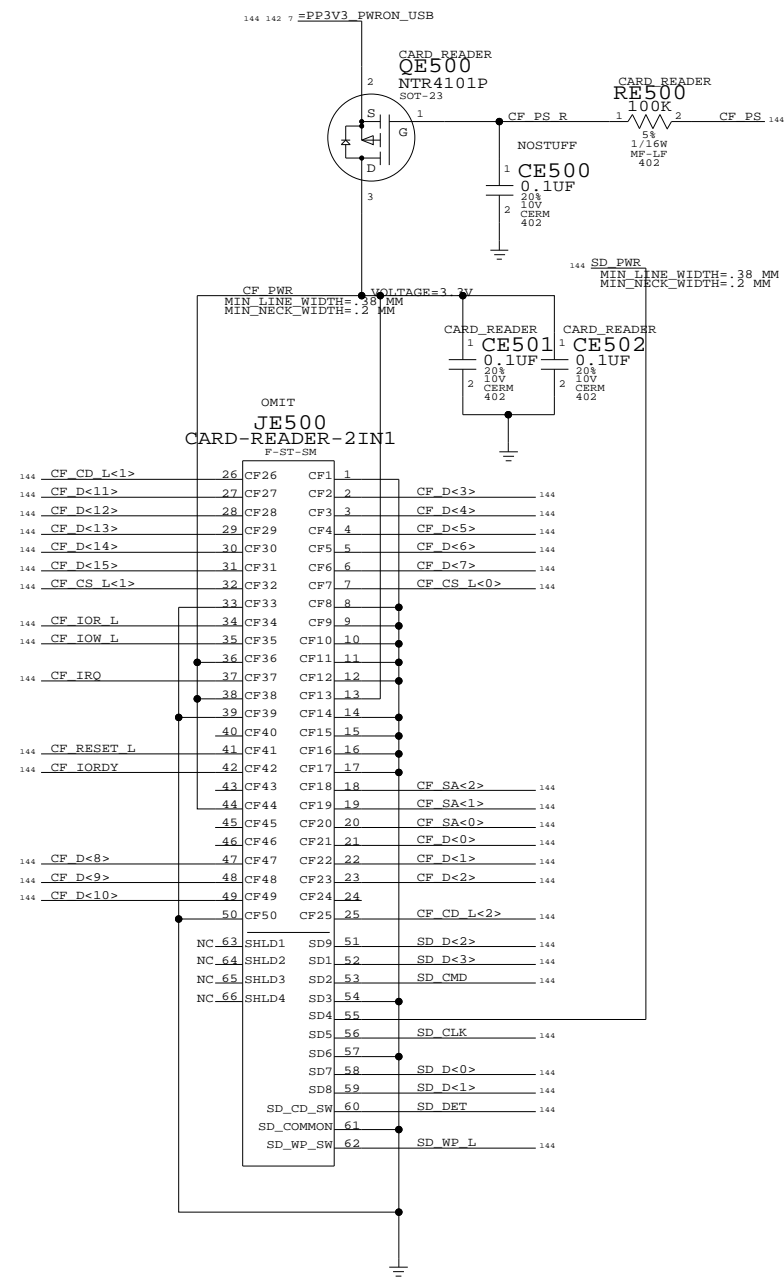
2

1

IF USING THE CARD READER, MUST CHANGE THESE BOM OPTIONS TO:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51280010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	CARD_READER
51280012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	CARD_READER

17_INCH_LCD
20_INCH_LCD



WRITE PROTECT AND CARD DETECT SWITCHES

CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	OPEN
FULLY INSERTED	OPEN	CLOSE	CLOSE

Flash Connector

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	D	051-6863	F
SCALE	SHT	145 OF 154	
NONE			

8

7

6

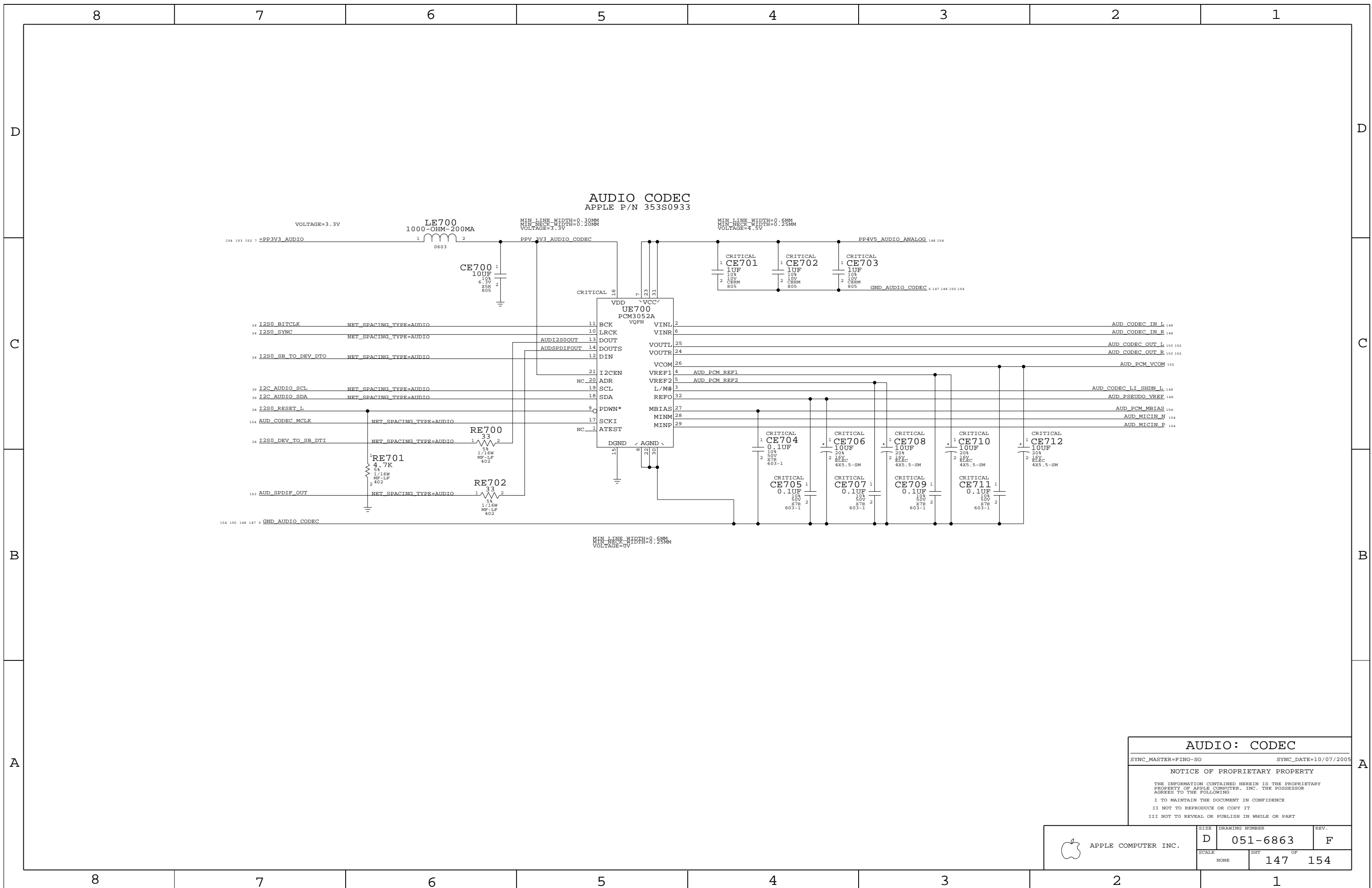
5

4

3

2

1



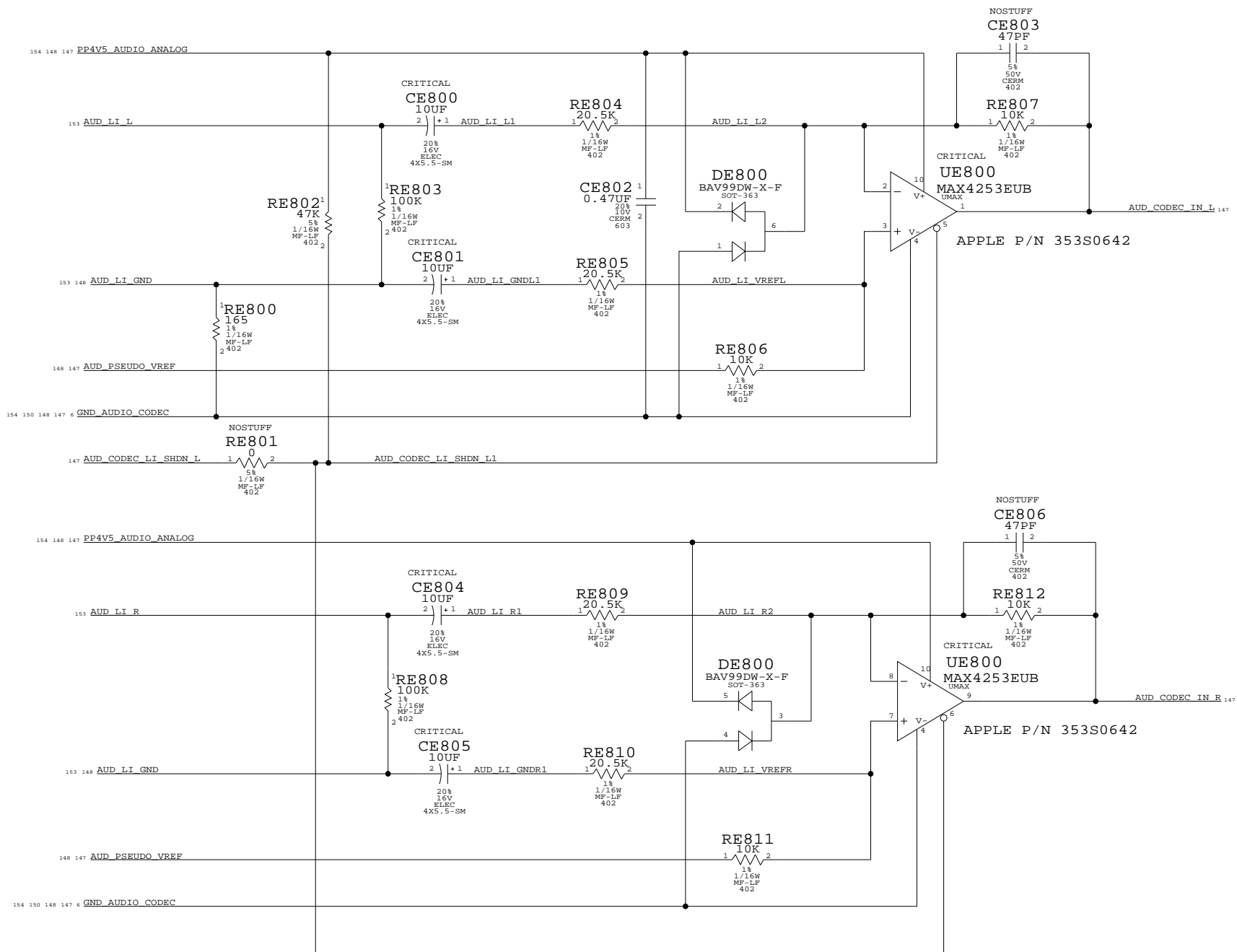
AUDIO CODEC
APPLE P/N 353S0933

AUDIO: CODEC
 SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005
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	D	051-6863	F
SCALE	SHT OF		
NONE	147 OF 154		

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

NOTICE OF PROPRIETARY PROPERTY

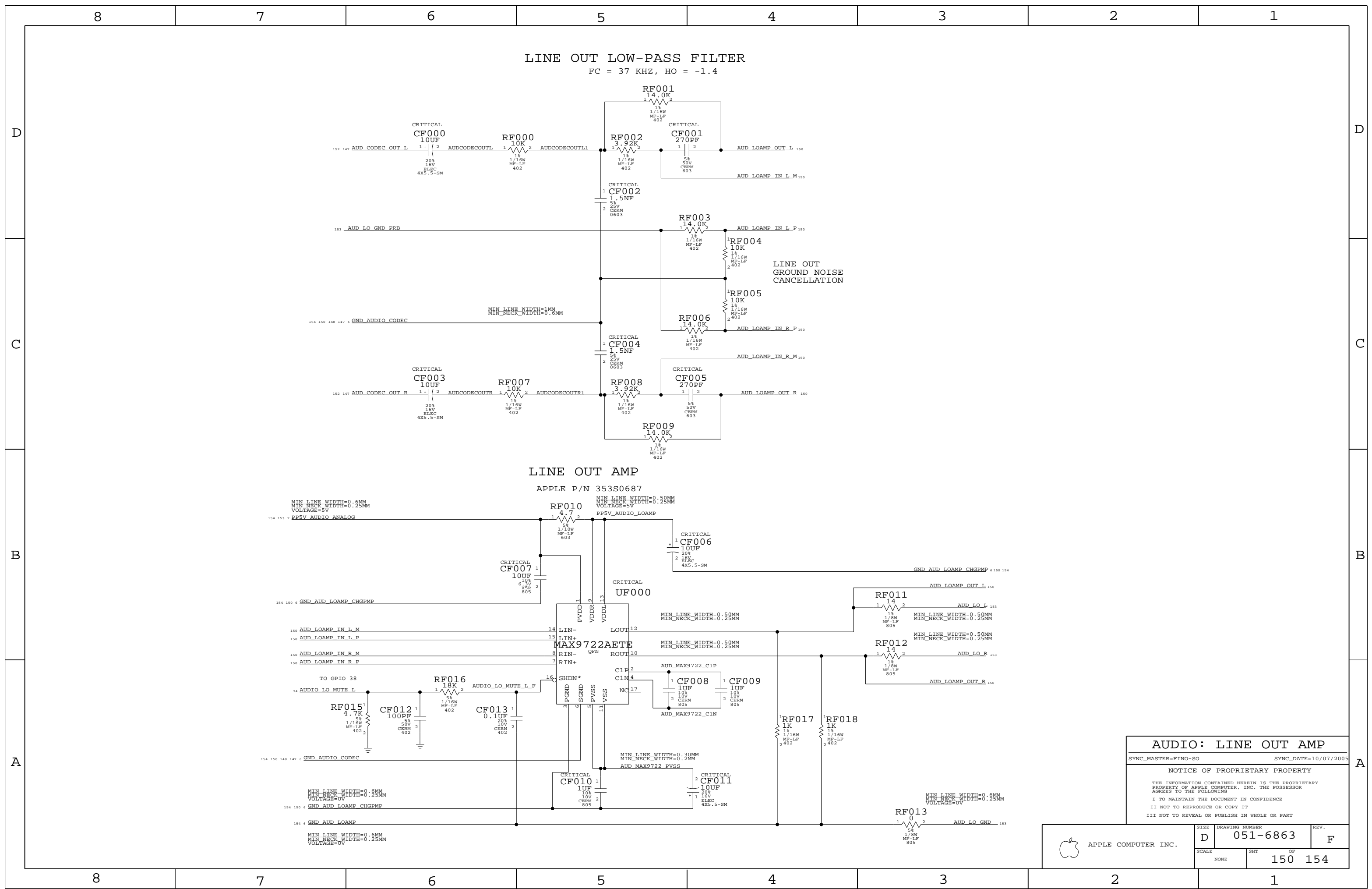
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	D	051-6863	F
SCALE	NONE	SHT OF	148 154



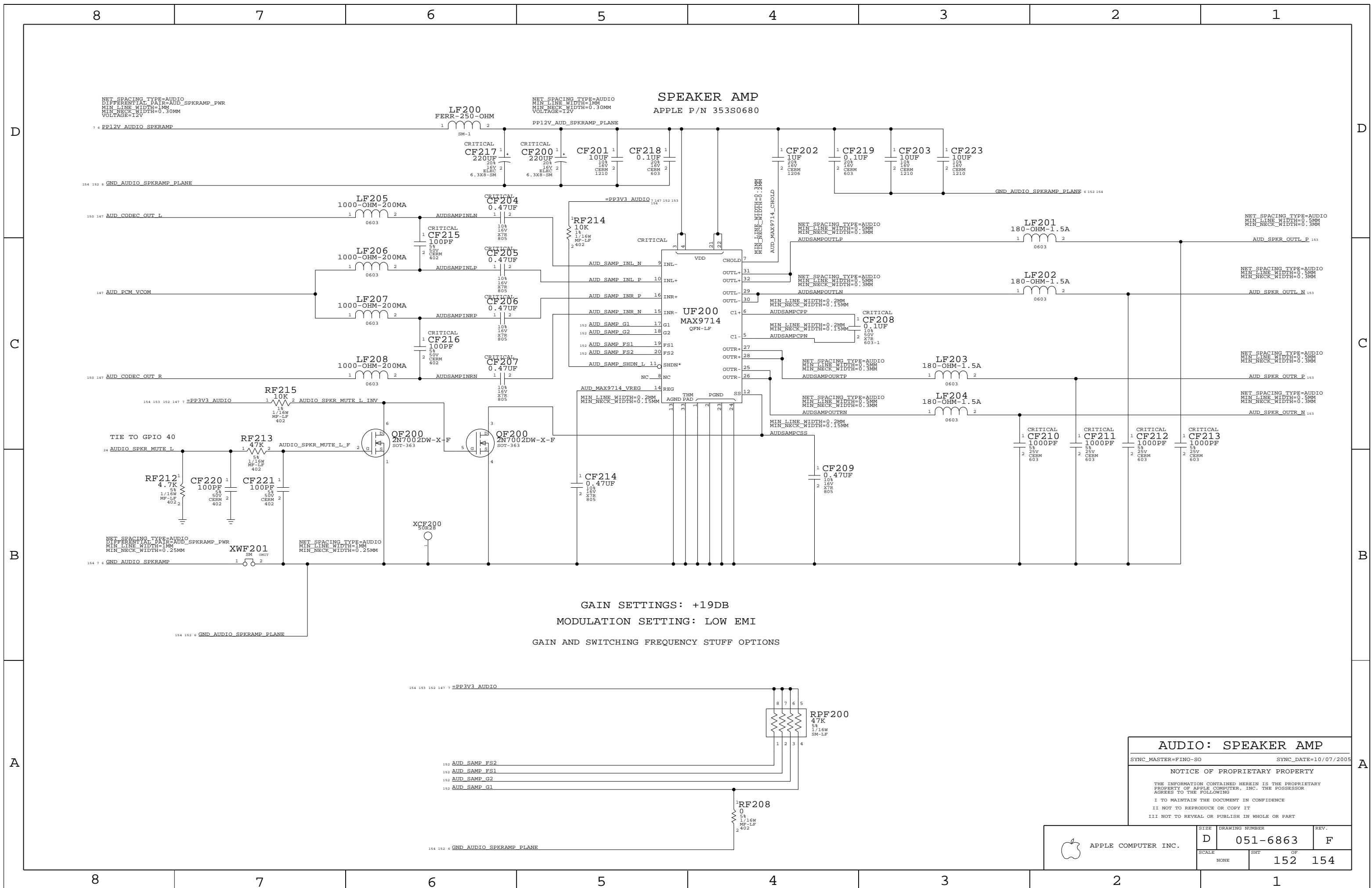
LINE OUT LOW-PASS FILTER
 FC = 37 KHZ, HO = -1.4

LINE OUT AMP
 APPLE P/N 353S0687

AUDIO: LINE OUT AMP
 SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

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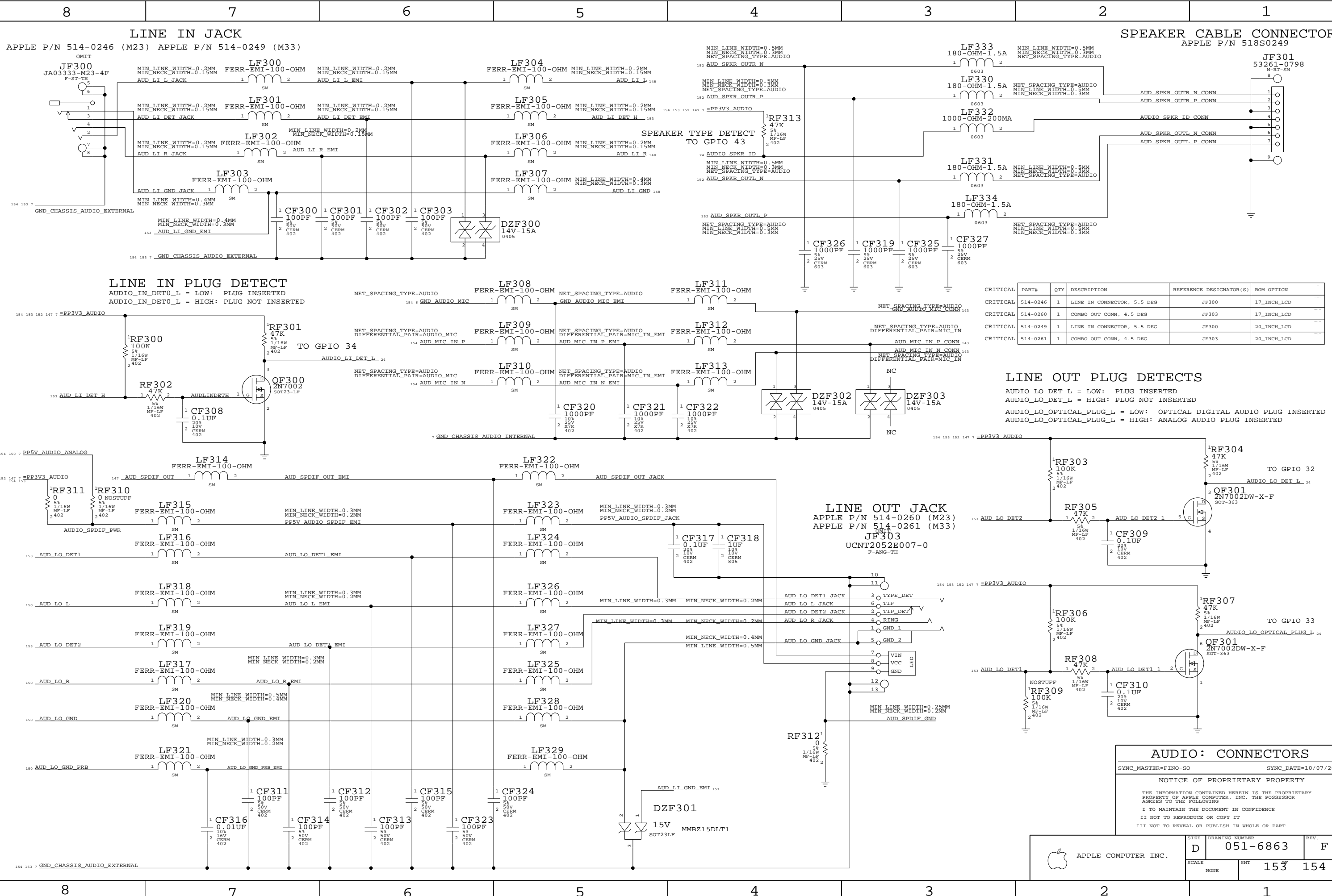
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	F
SCALE	SHT	OF	
NONE		150	154



GAIN SETTINGS: +19DB
 MODULATION SETTING: LOW EMI
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
 SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005
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	D	051-6863	F
SCALE	NONE	SHT	OF
		152	154



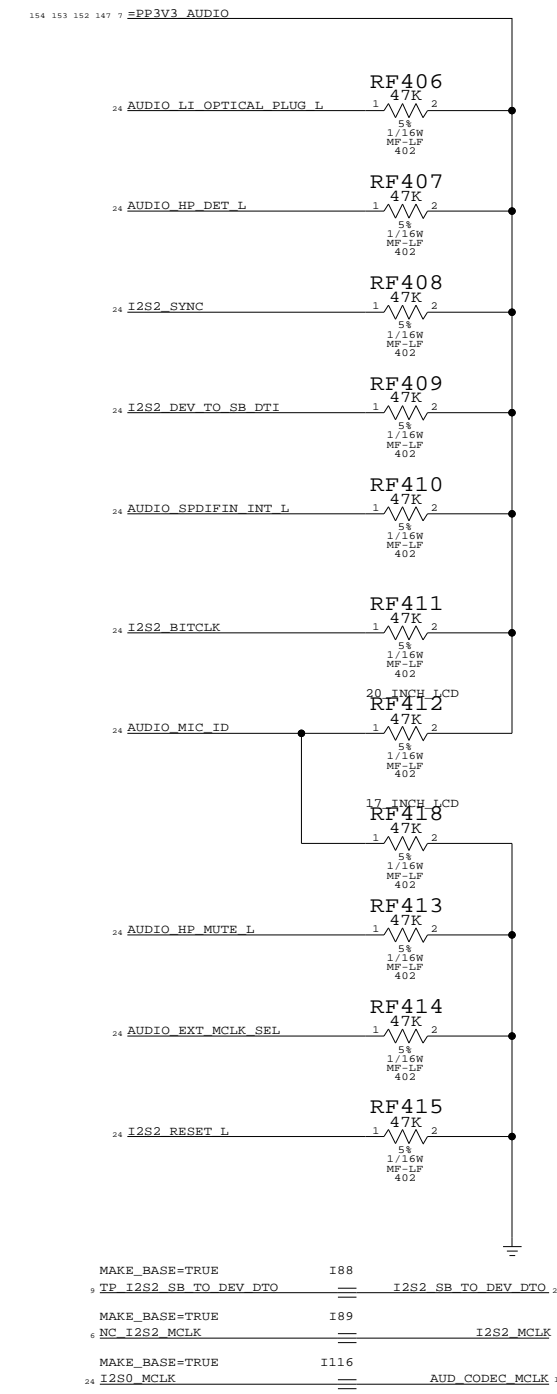
CRITICAL	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
CRITICAL	514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
CRITICAL	514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
CRITICAL	514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS
 AUDIO_LO_DET_L = LOW: PLUG INSERTED
 AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED
 AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
 AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

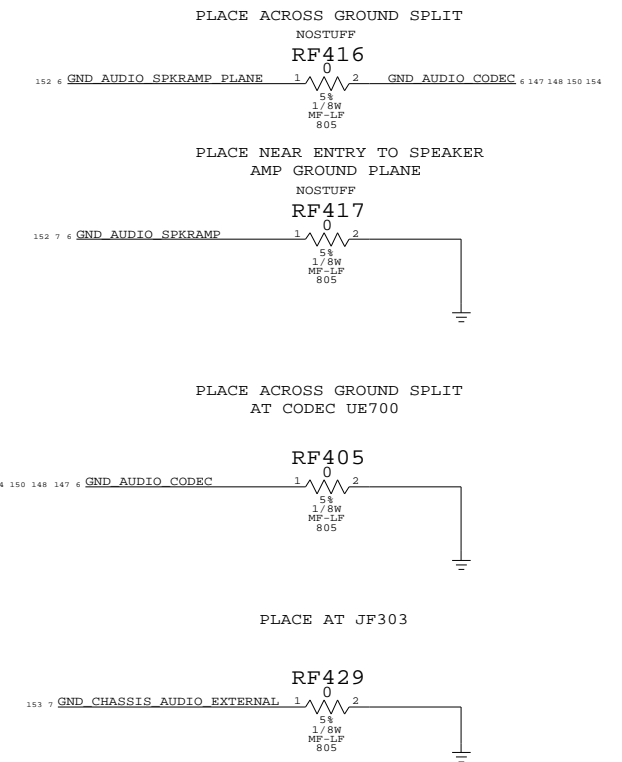
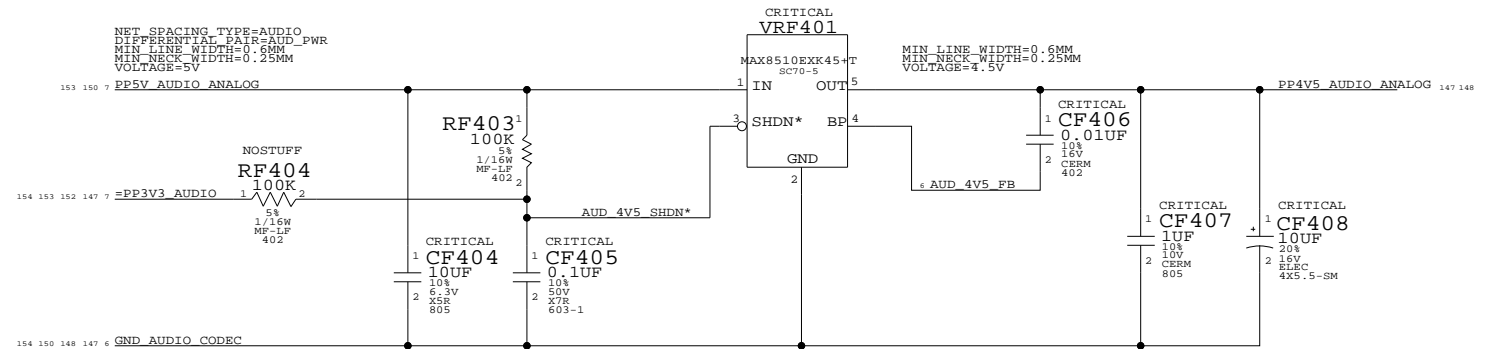
AUDIO: CONNECTORS
 SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005
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	D	051-6863	F
SCALE	SHT	153	154
NONE			

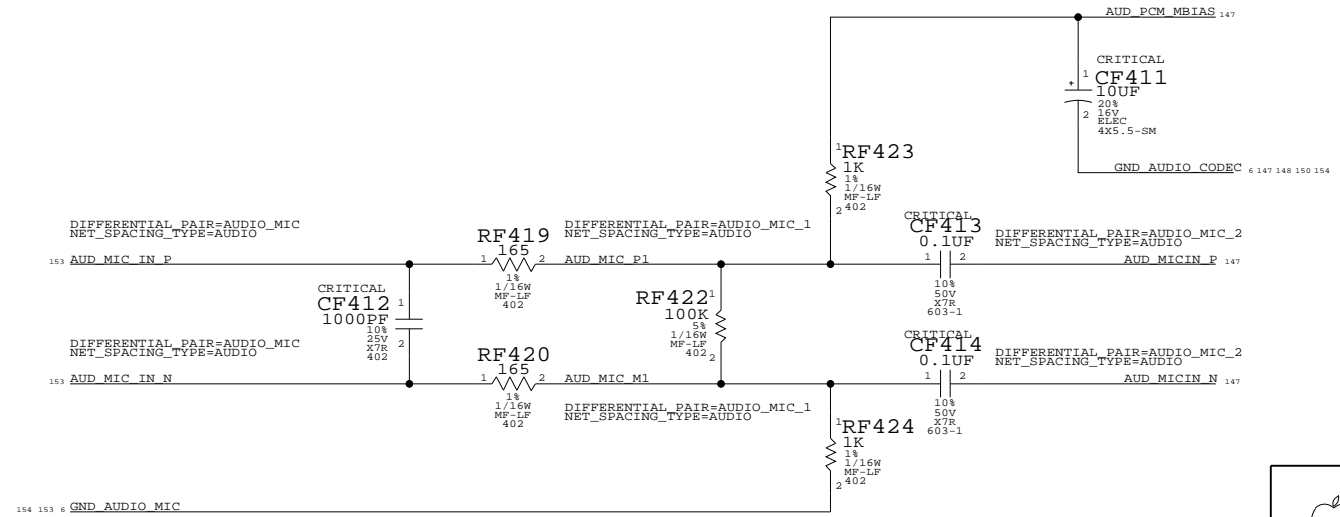
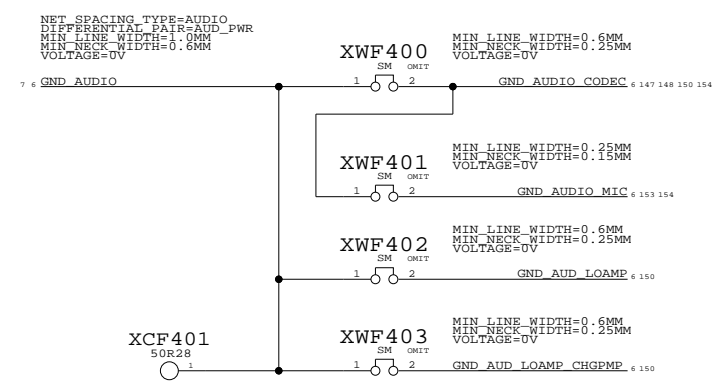
UNUSED GPIO TERMINATIONS



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APPLE P/N 353S0733



AUDIO GROUND RETURNS



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

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	D	051-6863	F
SCALE	NONE	SHT OF	154 OF 154