

MNLM158A-X-RH REV 0D1

 Original Creation Date: 01/14/99
 Last Update Date: 05/15/00
 Last Major Revision Date: 01/14/99

**LOW POWER, DUAL OPERATIONAL AMPLIFIER: ALSO AVAILABLE
 GUARANTEED TO 50K RAD (Si) TESTED TO MIL-STD-883,
 METHOD 1019.5**

General Description

The LM158A consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158A can be directly operated off of the standard +5V DC power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15V$ DC power supplies.

Industry Part Number

LM158

Prime Die

LM158

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

 LM158AH-QMLV
 LM158AH/883
 LM158AHLQML
 LM158AHLQMLV
 LM158AJ-QMLV
 LM158AJ/883
 LM158AJLQML
 LM158AJLQMLV
 LM158AWG-QMLV
 LM158AWG/883
 LM158AWGLQML
 LM158AWGLQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

| Subgrp | Description | Temp (°C) |
|--------|---------------------|------------|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100dB
- Wide bandwidth (unity gain temperature compensated) 1MHz
- Wide power supply range:
 - Single supply 3V to 32V or dual supplies $\pm 1.5V$ to $\pm 16V$
- Very low supply current drain (500uA) - essentially independent of supply voltage
- Low input offset voltage 2mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to $V+ - 1.5V$

CONTROLLING DOCUMENTS:

| | |
|---------------|-----------------|
| LM158AH-QMLV | 5962-8771002VGA |
| LM158AH/883 | 5962-8771002GA |
| LM158AHLQML | 5962L8771002QGA |
| LM158AHLQMLV | 5962L8771002VGA |
| LM158AJ-QMLV | 5962-8771002VPA |
| LM158AJ/883 | 5962-8771002PA |
| LM158AJLQML | 5962L8771002QPA |
| LM158AJLQMLV | 5962L8771002VPA |
| LM158AWG-QMLV | 5962-8771002VXA |
| LM158AWG/883 | 5962-8771002QXA |
| LM158AWGLQML | 5962L8771002QXA |
| LM158AWGLQMLV | 5962L8771002VXA |

(Absolute Maximum Ratings)

(Note 1)

| | | |
|--|--|---------------------|
| Supply Voltage, V+ | | 32Vdc |
| Differential Input Voltage | | 32Vdc |
| Input Voltage | | -0.3Vdc to +32Vdc |
| Power Dissipation (Note 2) | | 830 mW |
| Output Short-Circuit to GND (Note 3) (One Amplifier) V+ ≤ 15Vdc and TA = 25 C | | Continuous |
| Maximum Junction Temperature | | 150 C |
| Input Current (Vin < -0.3Vdc) (Note 4) | | 50mA |
| Operating Temperature Range | | -55 C ≤ Ta ≤ +125 C |
| Storage Temperature Range | | -65 C ≤ Ta ≤ +150 C |
| Lead Temperature (Soldering, 10 seconds) | | |
| METAL CAN | | 300 C |
| CERDIP | | 260 C |
| CERAMIC SOIC | | 260 C |
| Thermal Resistance | | |
| ThetaJA | | |
| METAL CAN (Still Air) | | 155 C/W |
| (500LF/Min Air Flow) | | 80 C/W |
| CERDIP (Still Air) | | 132 C/W |
| (500LF/Min Air Flow) | | 81 C/W |
| CERAMIC SOIC (Still Air) | | 195 C/W |
| (500LF/Min Air Flow) | | 131 C/W |
| ThetaJC | | |
| METAL CAN | | 42 C/W |
| CERDIP | | 23 C/W |
| CERAMIC SOIC | | 33 C/W |
| Package Weight (Typical) | | |
| METAL CAN | | 1000mg |
| CERDIP | | 1100mg |
| CERAMIC SOIC | | 220mg |
| ESD Tolerance (Note 5) | | 250V |

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
- Note 3: Short circuits from the output to V_+ , can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V_+ . At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
- Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V_+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc (at 25°C).
- Note 5: Human body model, 1.5 K ohms in series with 100 pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---------|-----------------------------|--|-------|----------|------|-----|------|------------|
| Icc | Power Supply Current | V+ = 5V, Rl = 100K, Vo = 1.4V | | | | 1.2 | mA | 1, 2, 3 |
| | | V+ = 30V, Rl = 100K, Vo = 1.4V | | | | 3 | mA | 1 |
| | | | | | | 4 | mA | 2, 3 |
| Voh | Output Voltage High | V+ = 30V, Rl = 2K Ohms | | | 26 | | V | 1, 2, 3 |
| | | V+ = 30V, Rl = 10K Ohms | | | 27 | | V | 1, 2, 3 |
| Vol | Output Voltage Low | V+ = 30V, Rl = 10K Ohms | | | | 40 | mV | 1 |
| | | | | | | 100 | mV | 2, 3 |
| | | V+ = 30V, Isink = 1uA | | | | 40 | mV | 1 |
| | | | | | | 100 | mV | 2, 3 |
| | | V+ = 5V, Rl = 10K Ohms | | | | 40 | mV | 1 |
| | | | | | 100 | mV | 2, 3 | |
| Isink | Output Sink Current | V+ = 15V, Vout = 200mV, Vin = 65 mV | | | 12 | | uA | 1 |
| | | V+ = 15V, Vout = 2V, Vin = 65mV | | | 10 | | mA | 1 |
| | | | | | 5 | | mA | 2, 3 |
| Isource | Output Source Current | V+ = 15V, Vin = 65mV, Vout = 2V | | | | -20 | mA | 1 |
| | | | | | | -10 | mA | 2, 3 |
| Ios | Short Circuit Current | V+ = 5V, Vout = 0V | | | -60 | | mA | 1 |
| Vio | Input Offset Voltage | V+ = 30V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V | | | -2 | 2 | mV | 1 |
| | | | | | -4 | 4 | mV | 2, 3 |
| | | V+ = 30V, Vcm = 28V, Rs = 50 Ohms, Vo = 1.4V | | | -4 | 4 | mV | 2, 3 |
| | | | | | -4 | 4 | mV | 2, 3 |
| | | V+ = 5V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V | | | -2 | 2 | mV | 1 |
| | | | | | -4 | 4 | mV | 2, 3 |
| | | | | | -2 | 2 | mV | 1 |
| | | | | | -2 | 2 | mV | 1 |
| CMRR | Common Mode Rejection Ratio | V+ = 30V, Vin = 0V to 28.5V, Rs = 50 Ohms | | | 70 | | dB | 1 |
| Iib+ | Input Bias Current | V+ = 5V, Vcm = 0V | | | -50 | -1 | nA | 1 |
| | | | | | -100 | -1 | nA | 2, 3 |

Electrical Characteristics

DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|--------|------------------------------|--|-------|----------|------|------|------|------------|
| Iib- | Input Bias Current | V+ = 5V, Vcm = 0V | | | -50 | -1 | nA | 1 |
| | | | | | -100 | -1 | nA | 2, 3 |
| Iio | Input Offset Current | V+ = 5V, Vcm = 0V | | | -10 | 10 | nA | 1 |
| | | | | | -30 | 30 | nA | 2, 3 |
| PSRR | Power Supply Rejection Ratio | V+ = 5V to 30V, Vcm = 0V | | | 65 | | dB | 1 |
| Vcm | Common Mode Voltage Range | V+ = 30V | 1 | | | 28.5 | V | 1 |
| | | | | | | 28.0 | V | 2, 3 |
| Vdiff | Differential Input Voltage | | 2 | | | 32 | V | 1, 2, 3 |
| Avs | Large Signal Gain | V+ = 15V, Rl = 2K Ohms, Vo = 1V to 11V | | | 50 | | V/mV | 4 |
| | | | | | 25 | | V/mV | 5, 6 |

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground. "Delta calculations performed on Jan "S" and "QLV" devices at Group B, Subgroup 5 only."

| | | | | | | | | |
|------|----------------------|--|--|--|------|-----|----|---|
| Vio | Input Offset Voltage | V+ = 30V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V | | | -0.5 | 0.5 | mV | 1 |
| | | V+ = 30V, Vcm = 28V, Rs = 50 Ohms, Vo = 1.4V | | | -0.5 | 0.5 | mV | 1 |
| | | V+ = 5V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V | | | -0.5 | 0.5 | mV | 1 |
| Iib+ | Input Bias Current | V+ = 5V, Vcm = 0V | | | -10 | 10 | nA | 1 |
| Iib- | Input Bias Current | V+ = 5V, Vcm = 0V | | | -10 | 10 | nA | 1 |

DC/AC PARAMETERS: POST RADIATION LIMITS +25 C

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

| | | | | | | | | |
|------|----------------------|--|---|--|-----|----|----|---|
| Vio | Input Offset Voltage | V+ = 30V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V | 3 | | -4 | 4 | mV | 1 |
| | | V+ = 30V, Vcm = 28V, Rs = 50 Ohms, Vo = 1.4V | 3 | | -4 | 4 | mV | 1 |
| | | V+ = 5V, Vcm = 0V, Rs = 50 Ohms, Vo = 1.4V | 3 | | -4 | 4 | mV | 1 |
| ±Iib | Input Bias Current | V+ = 5V, Vcm = 0V | 3 | | -60 | -1 | nA | 1 |

- Note 1: Parameter tested go-no-go only.
- Note 2: Guaranteed parameter not tested.
- Note 3: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5.

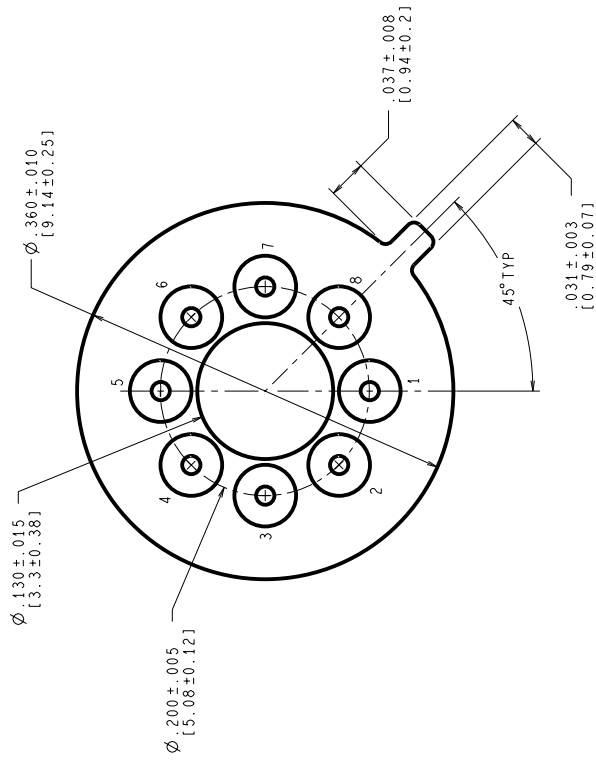
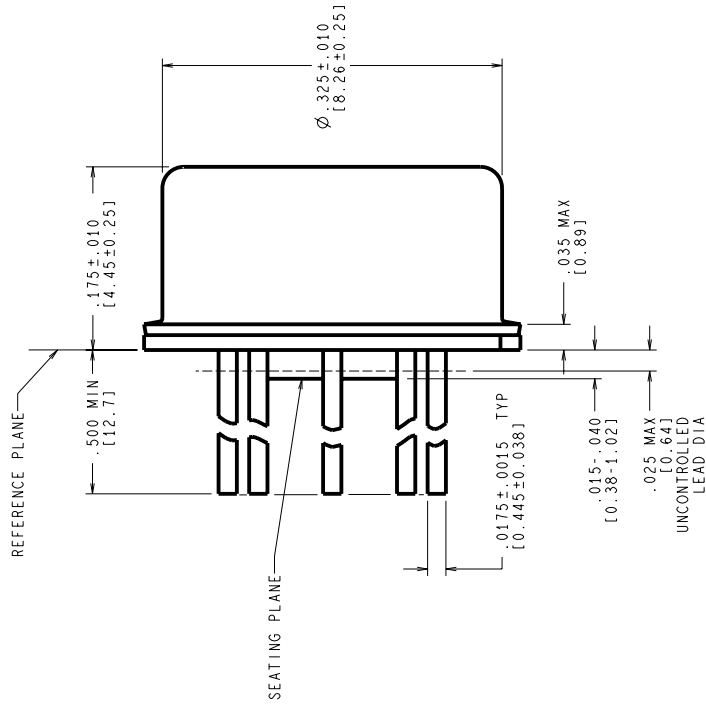
Graphics and Diagrams

| GRAPHICS# | DESCRIPTION |
|-----------|--|
| 06354HRB2 | CERAMIC SOIC (WG), 10 LEAD (B/I CKT) |
| 08571HRC2 | METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT) |
| 09294HR01 | CERDIP (J), 8 LEAD (B/I CKT) |
| H08CRF | METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG) |
| J08ARL | CERDIP (J), 8 LEAD (P/P DWG) |
| P000273A | METAL CAN (H), TO-99, 8 LD, .200 DIA P.C. (PINOUT) |
| P000274A | CERDIP (J), 8 LEAD (PINOUT) |
| P000461A | CERAMIC SOIC (WG), 10 LEAD (PINOUT) |
| WG10ARC | CERAMIC SOIC (WG), 10 LEAD (P/P DWG) |

See attached graphics following this page.

REVISIONS

| LTR | DESCRIPTION | E.C. N. | DATE | BY/APP'D |
|-----|---|---------|----------|----------|
| F | REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE. | 11002 | 06/22/95 | MS/ |



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

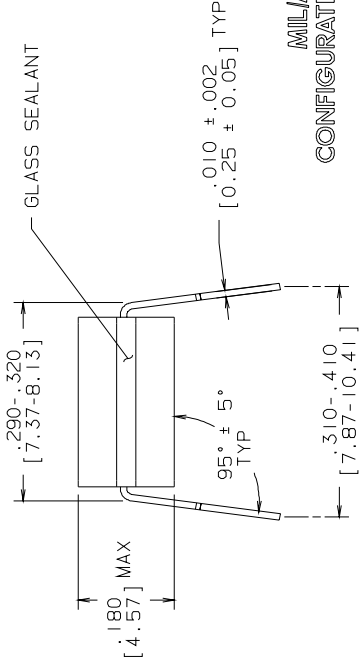
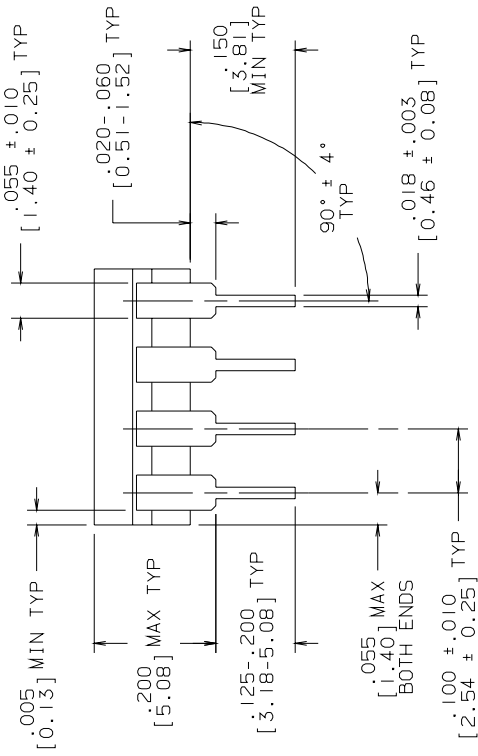
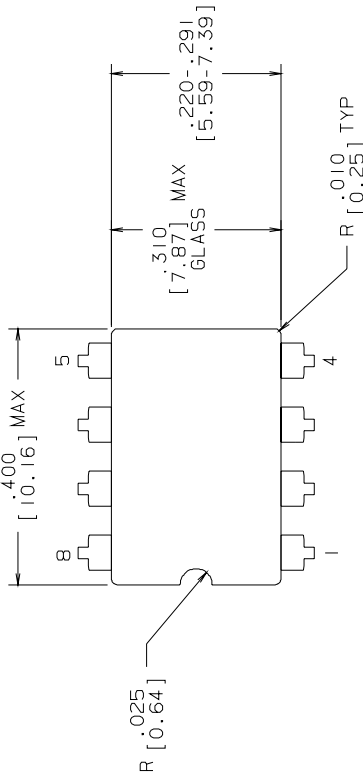
- LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
- STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
- APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
- REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No. 95.

| APPROVALS | DATE |
|------------------|----------|
| DRN: MARTA SUCHY | 06/22/95 |
| DWG. CHK. | |
| ENGR. CHK. | |

| | |
|----------------|----------|
| | |
| SCALE | N/A |
| SIZE | C |
| DRAWING NUMBER | MKT-H08C |
| REV | F |

| | |
|---|--|
| | |
| National Semiconductor | |
| 2800, Semiconductor dr., Santa Clara, CA 95052-8090 | |
| METAL CAN, 8 LEAD, .200 DIA P.C. | |

| R E V I S I O N S | | | |
|-------------------|--------------------------------|----------|-----------------|
| LTR | DESCRIPTION | E. C. N. | DATE |
| L | REVISE PER CURRENT STD; REDRAW | 10002 | 09/21/93 |
| | | | BY/APP'D TL/ |



MILAERO
 CONFIGURATION CONTROL
 MIL-M-38510
 CONFIGURATION CONTROL

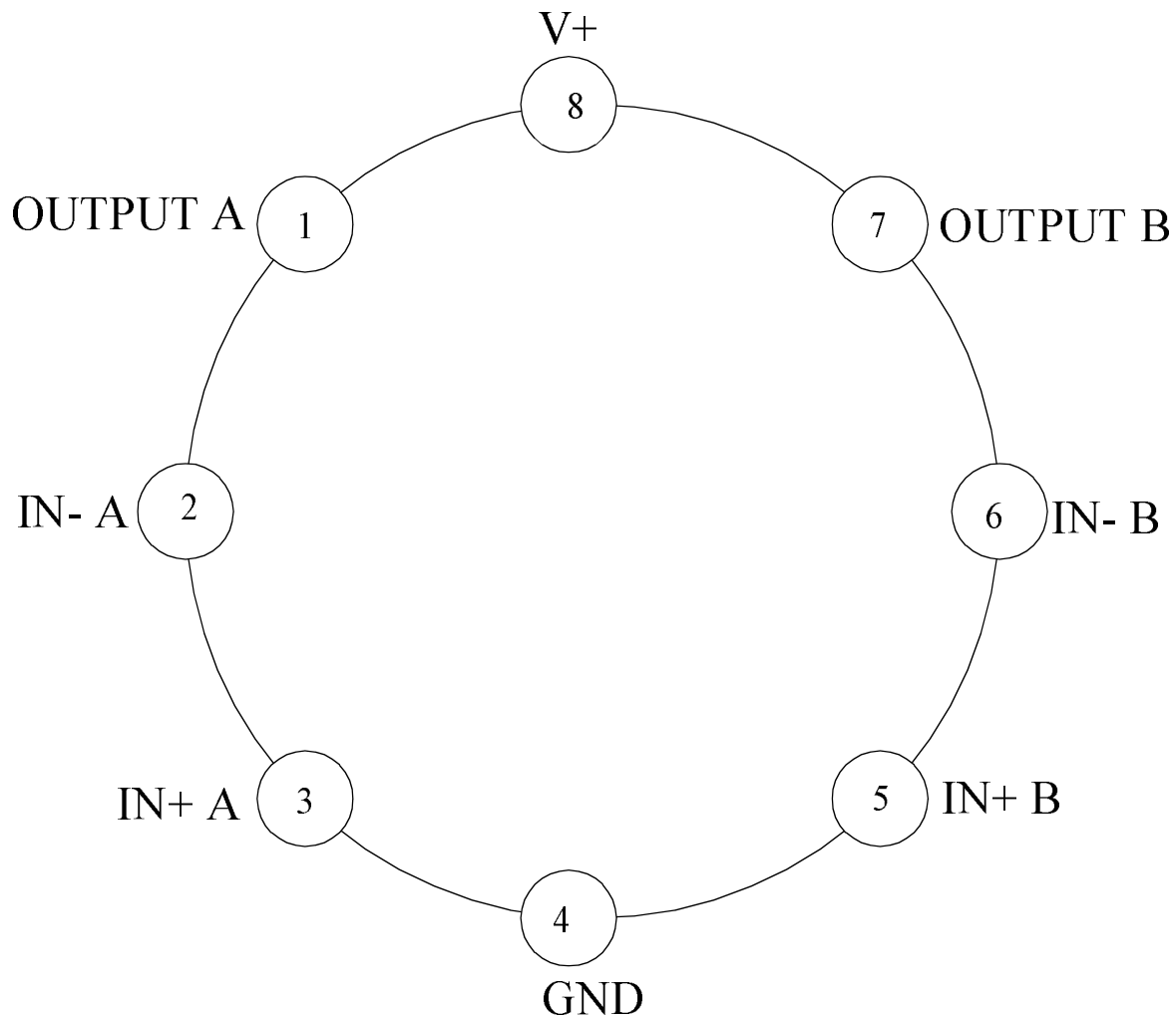
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|-----------------------------|----------------|
| APPROVALS | DATE |
| DRAWN: T. LEQUANG | 09/21/93 |
| DFTG. CHK. | |
| ENGR. CHK. | |
| APPROVAL | |
| PROJECTION | |
| | |
| SCALE | SIZE |
| N/A | B |
| DO NOT SCALE DRAWING | DRAWING NUMBER |
| | MKT-J08A |
| | SHEET |
| | OF |
| | REV |
| | L |

NATIONAL SEMICONDUCTOR CORPORATION
 2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),
 8 LEAD

NOTES: UNLESS OTHERWISE SPECIFIED

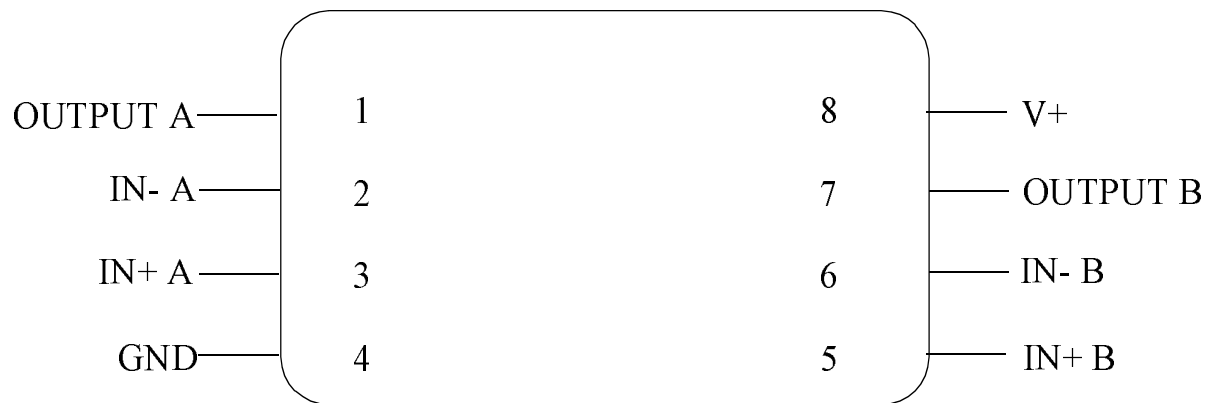
- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.



LM158AH, LM158H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000273A



National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM158AJ, LM158J

8 - LEAD DIP

CONNECTION DIAGRAM

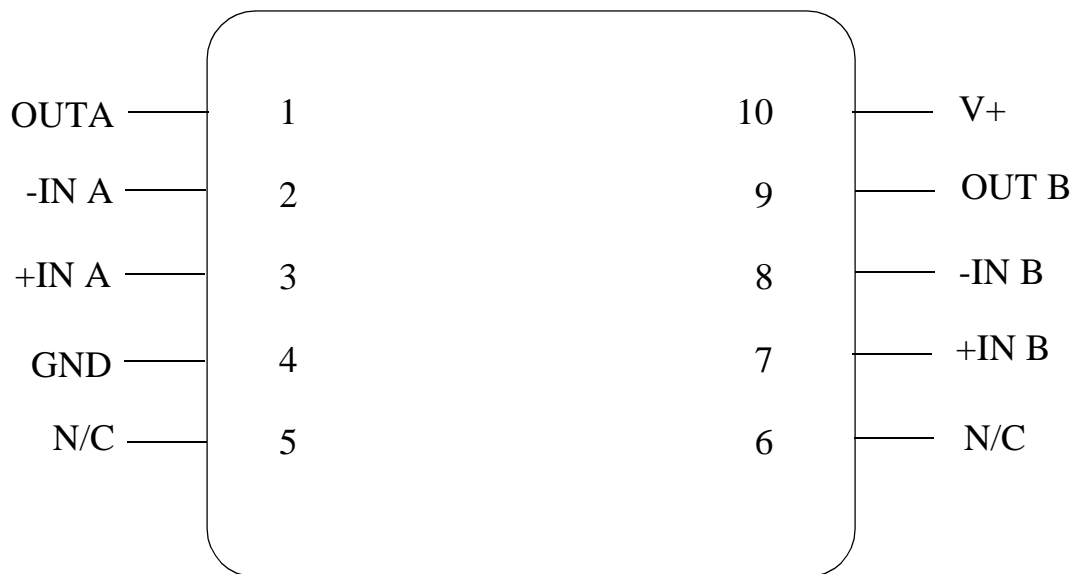
TOP VIEW

P000274A



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2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



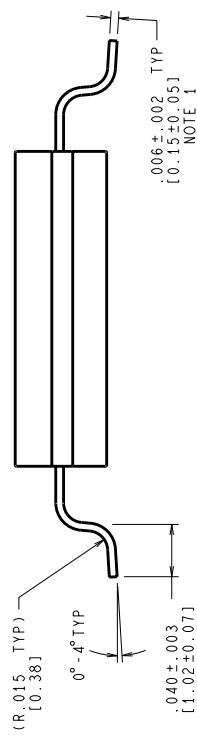
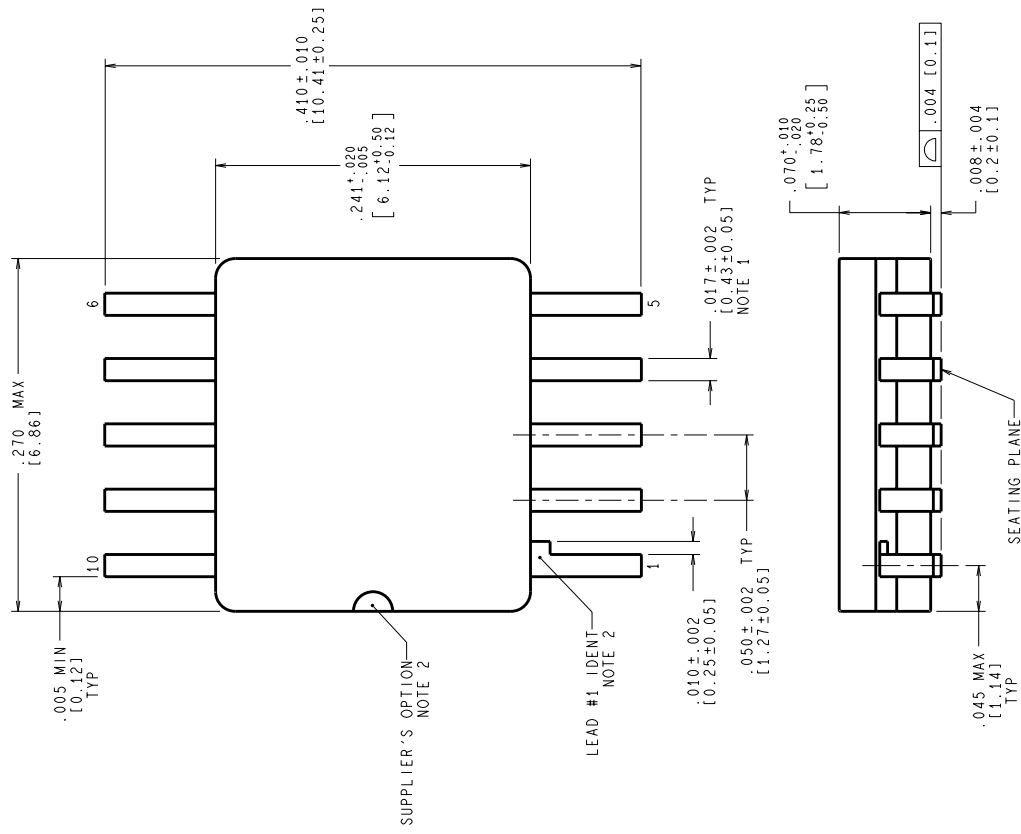
LM158AWG, LM158WG
10 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000461A



National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS

| LTR | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
|-----|---|--------|------------|----------|
| A | RELEASE TO DOCUMENT CONTROL | 11374 | 02/29/1996 | MS/KH |
| B | LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM. .040±.003 WAS .037±.003 | 11441 | 04/19/1996 | MS/KH |
| C | R .015(0.38) WAS R .006(0.15) | 11838 | 10/08/1997 | TL/ |



CONTROLLING DIMENSION IS INCH
VALUES IN | ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

| APPROVALS | DATE | SCALE | SIZE | DRAWING NUMBER | REV |
|--|----------|-------|------|----------------|-----|
| DRN: MARYA SUCHY | 02/29/96 | N/A | C | (SC)MKT-WG10A | C |
| DATE: 02/29/96 | | | | | |
| CHK: [Signature] | | | | | |
| CHK: [Signature] | | | | | |
| PROJECTION | | | | | |
| | | | | | |
| | | | | | |
| NATIONAL SEMICONDUCTOR 2800 Semiconductor Dr., Santa Clara, CA 95052-8090 | | | | | |
| CERPACK, 10 LEAD, GULL WING | | | | | |
| DO NOT SCALE DRAWING SHEET 1 of 1 | | | | | |

Revision History

| Rev | ECN # | Rel Date | Originator | Changes |
|-----|----------|----------|-------------|---|
| 0A0 | M0003236 | 03/10/00 | Rose Malone | Initial MDS Release: MNL158A-X-RH, Rev. 0A0 - Added Rad Hard Devices and Limits. Replaces MNL158A-X, Rev. 3A0. |
| 0B1 | M0003533 | 03/23/00 | Rose Malone | Update MDS: MNL158A-X-RH, Rev. 0A0 to MNL158A-X-RH, Rev. 0B1. Added reference to WG pkg - onto Main Table, Absolute Section and drawings to graphics section. |
| 0C1 | M0003643 | 05/15/00 | Rose Malone | Update MDS - MNL158A-X-RH, Rev. 0B1 to MNL158A-X-RH, Rev. 0C1. Corrected typo Package Weight for CERAMIC SOIC from 200mg to 220mg, in Absolute Maximum Section. |
| 0D1 | M0003679 | 05/15/00 | Rose Malone | Update MDS: MNL158A-X-RH, Rev. 0C1 to MNL158A-X-RH, Rev. 0D1. Corrected typo's on Main Table, Features Section and Absolute Section. |