

MDDS26LS31M-X-RH REV 2A0

 Original Creation Date: 01/24/96
 Last Update Date: 05/17/99
 Last Major Revision Date: 03/06/96

**QUAD HIGH SPEED DIFFERENTIAL LINE DRIVER, ALSO
 AVAILABLE GUARANTEED TO 300K RAD (Si) TESTED TO
 MIL-STD-883, METHOD 1019.5, CONDITION A.**

General Description

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE outputs and logically ANDED complementary outputs. The inputs are all LS compatible and are all one unit load.

The DS26LS31 features a power up/down protection circuit which keeps the output in a high impedance state (TRI-STATE) during power up or down preventing erroneous glitches on the transmission lines.

Industry Part Number

DS26LS31

Prime Die

DS26LS31

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

 DS26LS31ME-SMD
 DS26LS31MEFQML
 DS26LS31MJ-QMLV
 DS26LS31MJ-SMD
 DS26LS31MJFQML
 DS26LS31MJFQMLV
 DS26LS31MW-QMLV
 DS26LS31MW-SMD
 DS26LS31MWFQML
 DS26LS31MWFQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Operation from Single 5V Supply
- Outputs Won't Load Line When Vcc=0V
- Four Line Drivers in One Package For Maximum Package Density
- Output Short-Circuit Protection
- Complementary Outputs
- Meets the requirements of EIA Standard RS-422
- Pin Compatible with AM26LS31
- Glitch Free Power Up/Down
- Controlling Document:
 - DS26LS31MEFQML 5962F7802301Q2A
 - DS26LS31ME-SMD 5962-7802301Q2A
 - DS26LS31MJFQML 5962F7802301MEA
 - DS26LS31MJFQMLV 5962F7802301VEA
 - DS26LS31MJ-QMLV 5962-7802301VEA
 - DS26LS31MJ-SMD 5962-7802301MEA
 - DS26LS31MWFQML 5962F7802301MFA
 - DS26LS31MWFQMLV 5962F7802301VFA
 - DS26LS31MW-QMLV 5962-7802301VFA
 - DS26LS31MW-SMD 5962-7802301MFA

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5.5V
Output Voltage (Power OFF)	-0.25 to 6V
Maximum Power Dissipation @ 25 C (Note 2)	
Cavity Package	1400 mW
LCC	1600 mW
Flat Pack	850 mW

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Derate CDip 11.5mW/C, CLCC= 13mW/C, CERPACK = 7.4mW/C above 25C.

Recommended Operating Conditions

Supply Voltage, Vcc	MIN	MAX	UNITS
	4.5	5.5	V
Temperature, TA	MIN	MAX	UNITS
	-55	+125	C

Electrical Characteristics

DC PARAMETERS

See Note 3

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	Logical "1" Input Voltage	Vcc= 4.5V	1, 2		2		V	1, 2, 3
Vil	Logical "0" Input Voltage	Vcc= 5.5V	1, 2			.8	V	1, 2, 3
Voh	Logical "1" Output Voltage	Vcc= 4.5V, Ioh= -20mA	2		2.5		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc= 4.5V, Iol= 20mA	2			.5	V	1, 2, 3
Iih	Logical "1" Input Current	Vcc= 5.5V, Vin=2.7V	2		-2.0	20	uA	1, 2, 3
Iil	Logical "0" Input Current	Vcc= 5.5V, Vin= .4V	2		100	-360	uA	1, 2, 3
Ii	Input Reverse Current	Vcc=5.5V, Vin=7V	2		-.01	.1	mA	1, 2, 3
Io	TRI-STATE Output Current	Vcc=5.5V, Vo= .5V	2			-20	uA	1, 2, 3
		Vcc=5.5V, Vo=2.5V	2			20	uA	1, 2, 3
Vic	Input Clamp Voltage	Vcc=4.5V, Iin= -18mA	2			-1.5	V	1, 2, 3
Ios	Output Short Circuit Current	Vcc=5.5V	2		-30	-150	mA	1, 2, 3
Icc	Power Supply Current	Vcc=5.5V, All Outputs Disabled or Active	2			80	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: PROPAGATION DELAY TIME: See Note 3

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: $V_{cc}=5V$, $V_{in} = 1.3V$ to $V_o = 1.3V$, $V(\text{pulse}) = 0$ to $3V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Input to Output	CL = 30 pF	2			20	nS	9
			2			30	nS	10, 11
tPHL	Input to Output	CL = 30 pF	2			20	nS	9
			2			30	nS	10, 11
Skew	Output to Output	CL = 30 pF	2			6	nS	9
			2			9	nS	10, 11
tPLZ	Enable Time	S2 Open, Enable, CL = 10 pF	2			35	nS	9
			2			53	nS	10, 11
		S2 Open, $\overline{\text{Enable}}$, CL = 10 pF	2			35	nS	9
			2			53	nS	10, 11
tPHZ	Enable Time	S1 Open, Enable, CL = 10 pF	2			30	nS	9
			2			45	nS	10, 11
		S1 Open, $\overline{\text{Enable}}$, CL = 10 pF	2			30	nS	9
			2			45	nS	10, 11
tPZL	Disable Time	S2 Open, Enable, CL = 30 pF	2			45	nS	9
			2			68	nS	10, 11
		S2 Open, $\overline{\text{Enable}}$, CL = 30 pF	2			45	nS	9
			2			68	nS	10, 11
tPZH	Disable Time	S1 Open, Enable, CL = 30 pF	2			40	nS	9
			2			60	nS	10, 11
		S1 Open, $\overline{\text{Enable}}$, CL = 30 pF	2			40	nS	9
			2			60	nS	10, 11

DC PARAMETERS - DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: Delta calculations performed on QMLV only devices after burn-in and at Group B5.
 AC:

Voh	Output High Voltage	$V_{cc} = 4.5$, $I_{oh} = -20$ mA	2		-250	250	mV	1
Vol	Output Low Voltage	$V_{cc} = 4.5$, $I_{ol} = 20$ mA	2		-50	50	mV	1
Icc	Power Supply Current	$V_{cc} = 5.5$, All outputs disabled or active	2		-8	8	mA	1

Note 1: Parameter tested go-no-go only.

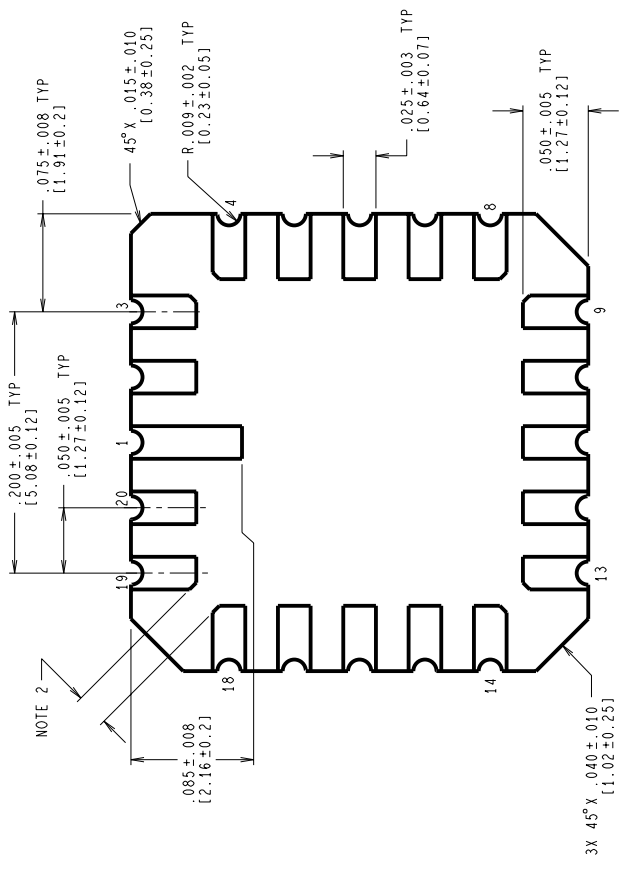
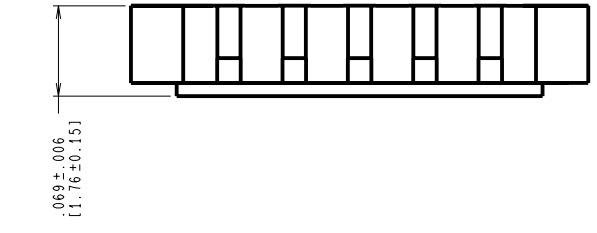
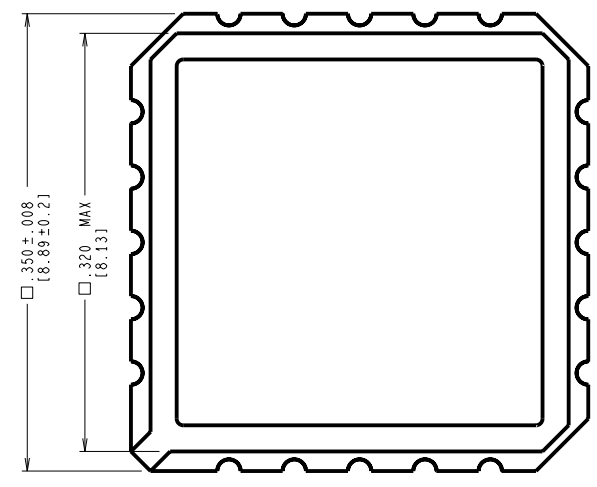
(Continued)

- Note 2: Subgroups 1,2 and 9,10: Power dissipation must be externally controlled at elevated temperatures.
- Note 3: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD 883, Method 1019.5, Condition A.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)

See attached graphics following this page.



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

- a. 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
 - b. SOLDER DIP.
SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
2. CORNER PADS MAY HAVE A 45° X .020 IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015 IN/0.38mm DIMENSION.
4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

**MIL/AERO
CONFIGURATION CONTROL**

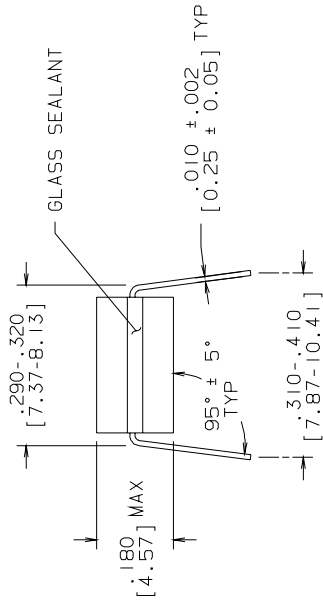
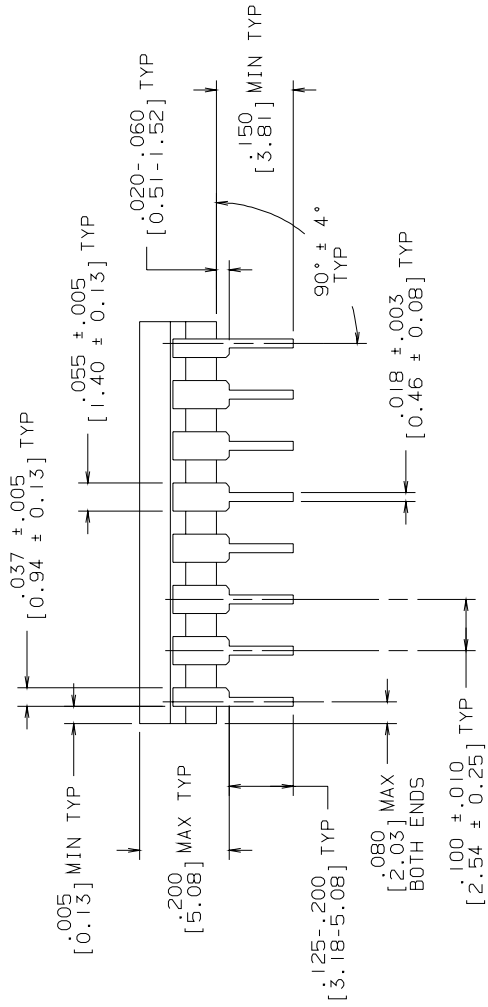
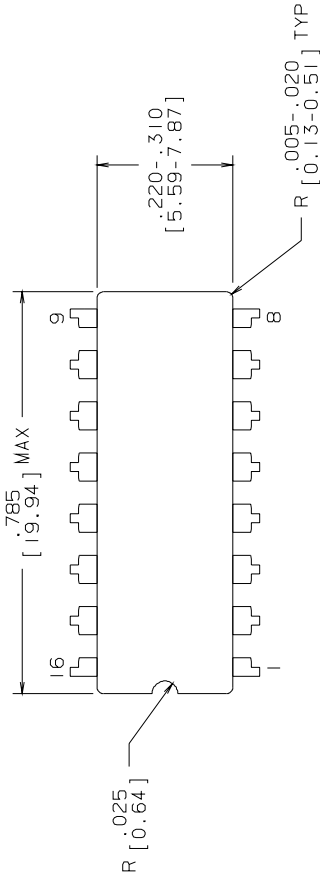
APPROVALS		DATE	BY/APP'D
DRN: <i>Debye Gedy</i>		02/10/94	
DFTG: CHK.			
ENGR: CHK.			
APPROVAL			
PROJECTION		SCALE	SIZE
		N/A	C
		DRAWING NUMBER	REV.
		MKT-E20A	E
		DO NOT SCALE DRAWING SHEET 1 of 1	

NATIONAL SEMICONDUCTOR CORPORATION
2300 Semiconductor Drive, Santa Clara, Ca. 95052-8000

**LEADLESS CHIP CARRIER,
TYPE C,
20 TERMINAL**

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW.	10005	02/10/94 DEG/

R E V I S I O N S			
LTR	DESCRIPTION	E. C. N.	DATE
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93
			TL/



MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH	
APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	
PROJECTION 	
SCALE N/A	SIZE B
DO NOT SCALE DRAWING	DRAWING NUMBER MKT-J16A
	SHEET 1 OF 1

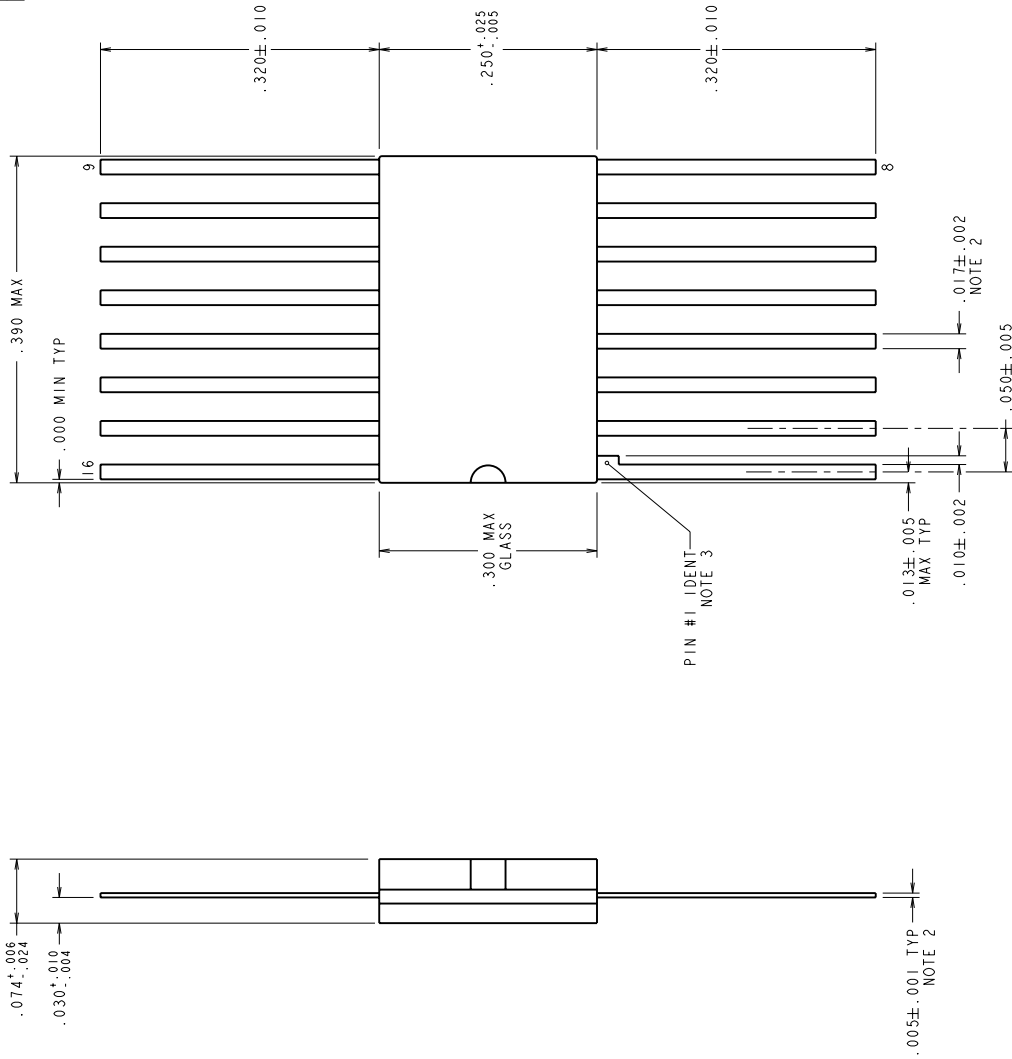
NATIONAL SEMICONDUCTOR CORPORATION 2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
CERDIP (J), 16 LEAD	

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD. .017±.002 WAS .017±.020.	10514	07/28/94	DEG/AEP
L		10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
- MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- REFERENCE JEDEC REGISTRATION M0-092, VARIATION AC, DATED 04/89.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS	DATE
DRWN: <i>D.F. Grady</i>	07/28/94
DTG. CHK.	
ENGR. CHK.	

PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
		N/A	C	MKT-W16A	L
DO NOT SCALE DRAWING					

National Semiconductor	
2800 Semiconductor dr., Santa Clara, CA 95052-8090	
CERPACK, 16 LEAD	

Revision History

Rev	ECN #	Rel Date	Originator	Changes
2A0	M0003362	05/17/99	Linda Collins	Added Rad Hard NSID's. New update: MDDS26LS31M-X-RH Rev. 2A0