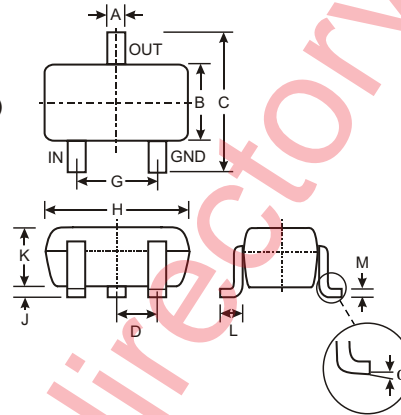


Features

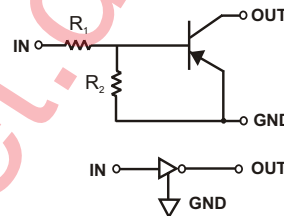
- Epitaxial Planar Die Construction
- Complementary NPN Types Available (DDTC)
- Built-In Biasing Resistors, R1 = R2
- Available in Lead Free/RoHS Compliant Version (Note 2)

Mechanical Data

- Case: SC-59
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals: Solderable per MIL-STD-202, Method 208
- Also Available in Lead Free Plating (Matte Tin Finish annealed over Copper leadframe). Please see Ordering Information, Note 4, on Page 2
- Terminal Connections: See Diagram
- Marking: Date Code and Type Code (See Table Below & Page 2)
- Ordering Information (See Page 2)
- Weight: 0.008 grams (approximate)



SC-59		
Dim	Min	Max
A	0.35	0.50
B	1.50	1.70
C	2.70	3.00
D	0.95	
G	1.90	
H	2.90	3.10
J	0.013	0.10
K	1.00	1.30
L	0.35	0.55
M	0.10	0.20
α	0°	8°
All Dimensions in mm		



SCHEMATIC DIAGRAM

P/N	R1, R2 (NOM)	Type Code
DDTA123EKA	2.2K Ω	P04
DDTA143EKA	4.7K Ω	P08
DDTA114EKA	10K Ω	P13
DDTA124EKA	22K Ω	P17
DDTA144EKA	47K Ω	P20
DDTA115EKA	100K Ω	P24

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage, (3) to (1)	V _{CC}	-50	V
Input Voltage, (2) to (1)	V _{IN}	+10 to -12 +10 to -30 +10 to -40 +10 to -40 +10 to -40 +10 to -40	V
Output Current	I _O	-100 -100 -50 -30 -100 -20	mA
Output Current	I _C (Max)	-100	mA
Power Dissipation	P _d	200	mW
Thermal Resistance, Junction to Ambient Air (Note 1)	R _{θJA}	625	°C/W
Operating and Storage and Temperature Range	T _J , T _{STG}	-55 to +150	°C

Note: 1. Mounted on FR4 PC Board with recommended pad layout at <http://www.diodes.com/datasheets/ap02001.pdf>.
2. No purposefully added lead.

Electrical Characteristics @ T_A = 25°C unless otherwise specified

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
Input Voltage		V _{I(off)}	-0.5	-1.1	—	V	V _{CC} = -5V, I _O = -100μA
		V _{I(on)}	—	-1.9	-3		V _O = -0.3V, I _O = -20mA, DDTA123EKA V _O = -0.3V, I _O = -20mA, DDTA143EKA V _O = -0.3V, I _O = -10mA, DDTA114EKA V _O = -0.3V, I _O = -5mA, DDTA124EKA V _O = -0.3V, I _O = -2mA, DDTA144EKA V _O = -0.3V, I _O = -1mA, DDTA115EKA
Output Voltage		V _{O(on)}	—	-0.1	-0.3	V	I _O /I _I = -10mA/-0.5mA, DDTA123EKA I _O /I _I = -10mA/-0.5mA, DDTA143EKA I _O /I _I = -10mA/-0.5mA, DDTA114EKA I _O /I _I = -10mA/-0.5mA, DDTA124EKA I _O /I _I = -10mA/-0.5mA, DDTA144EKA I _O /I _I = -5mA/-0.25mA, DDTA115EKA
Input Current	DDTA123EKA DDTA143EKA DDTA114EKA DDTA124EKA DDTA144EKA DDTA115EKA	I _I	—	—	-3.8 -1.8 -0.88 -0.36 -0.18 -0.15	mA	V _I = -5V
Output Current		I _{O(off)}	—	—	-0.5	μA	V _{CC} = -50V, V _I = 0V
DC Current Gain	DDTA123EKA DDTA143EKA DDTA114EKA DDTA124EKA DDTA144EKA DDTA115EKA	G _I	20 20 30 56 68 82	—	—	—	V _O = -5V, I _O = -20mA V _O = -5V, I _O = -10mA V _O = -5V, I _O = -5mA V _O = -5V, I _O = -5mA V _O = -5V, I _O = -5mA V _O = -5V, I _O = -5mA
Input Resistor (R ₁) Tolerance		ΔR ₁	-30	—	+30	%	—
Resistance Ratio		R ₂ /R ₁	0.8	1	1.2	—	—
Gain-Bandwidth Product*		f _T	—	250	—	MHz	V _{CE} = -10V, I _E = 5mA, f = 100MHz

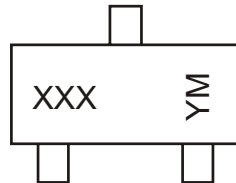
* Transistor - For Reference Only

Ordering Information (Note 3)

Device	Packaging	Shipping
DDTA123EKA-7	SC-59	3000/Tape & Reel
DDTA143EKA-7	SC-59	3000/Tape & Reel
DDTA114EKA-7	SC-59	3000/Tape & Reel
DDTA124EKA-7	SC-59	3000/Tape & Reel
DDTA144EKA-7	SC-59	3000/Tape & Reel
DDTA115EKA-7	SC-59	3000/Tape & Reel

- Notes: 3. For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.
 4. For Lead Free/RoHS Compliant version part numbers, please add "-F" suffix to the part numbers above. Example: DDTA115EKA-7-F.

Marking Information



XXX = Product Type Marking Code, See Table on Page 1
 YM = Date Code Marking
 Y = Year ex: N = 2002
 M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

TYPICAL CURVES - DDTA143EKA

NEW PRODUCT

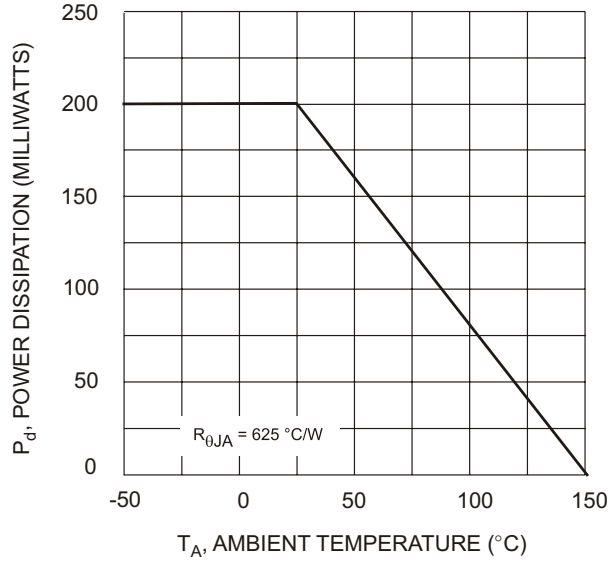


Fig. 1 Derating Curve

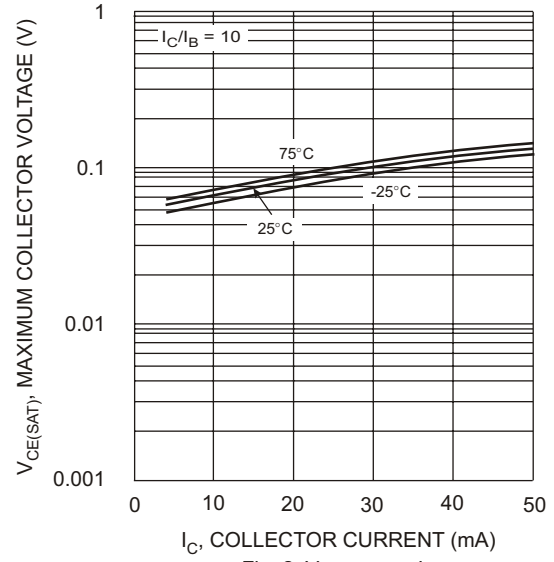


Fig. 2 $V_{CE(SAT)}$ vs. I_C

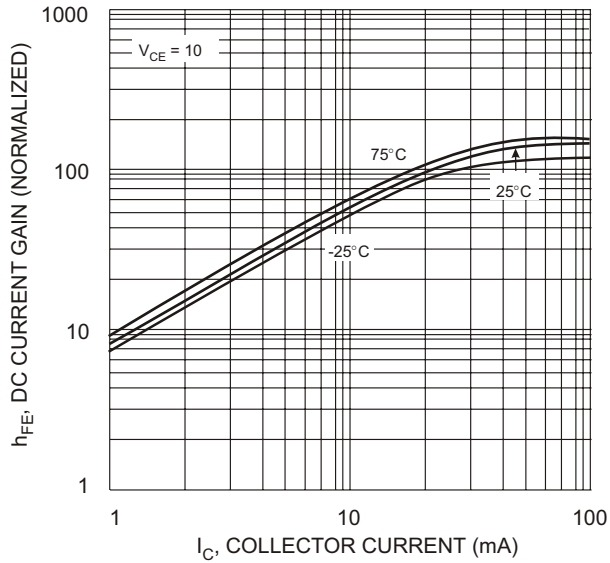


Fig. 3 DC CURRENT GAIN

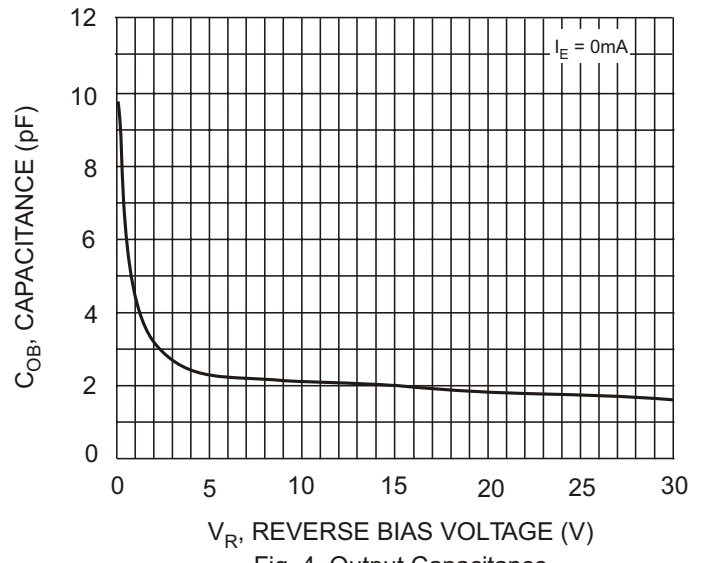


Fig. 4 Output Capacitance

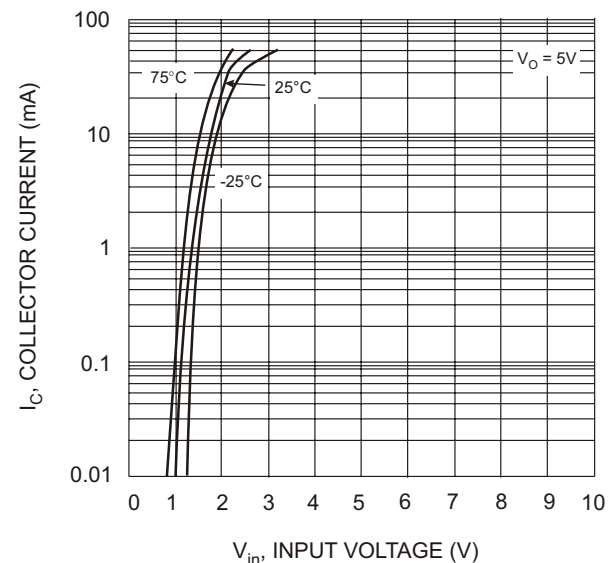


Fig. 5 Collector Current Vs. Input Voltage

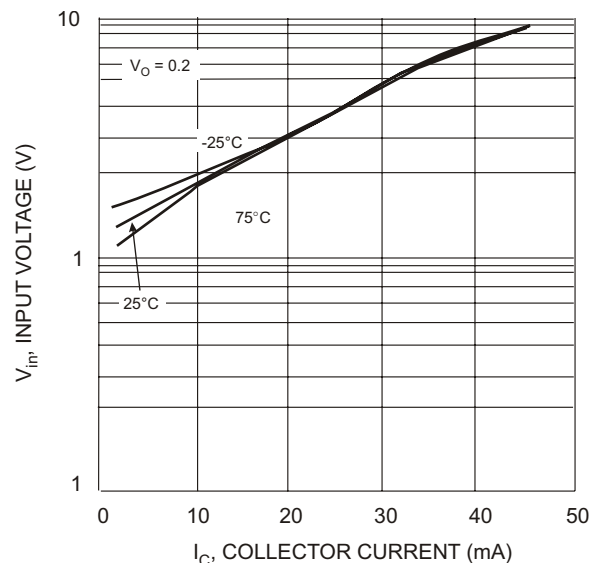


Fig. 6 Input Voltage vs. Collector Current