N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-39 envelope and designed for application as low-power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

QUICK REFERENCE DATA

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30	V
Drain current (DC)	I_D	max.	1.4	1.1	0.9	A
Total power dissipation up to T_c = 25 °C	P_{tot}	max.	6.25	6.25	6.25	W
Drain-source ON-resistance I_D = 1.0 A; V_{GS} = 10 V	R_{DSon}	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance at f = 1 kHz I_D = 0.5 A; V_{DS} = 25 V	$\|y_{fs}\|$	max.	170	170	170	mS

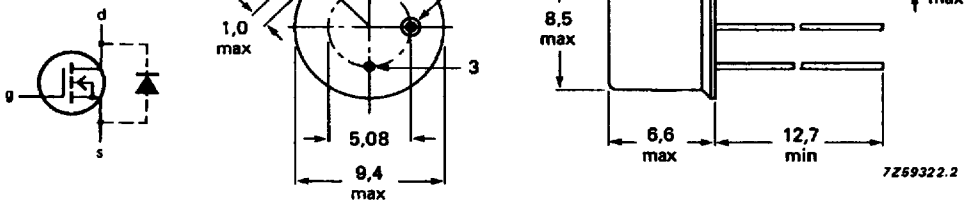
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-39.

Pinning:

1 = Source
2 = Gate
3 = Drain



Maximum lead diameter is guaranteed only for 12.7 mm

Accessories: 56245 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

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Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30	V
Drain current (DC)	I_D	max.	1.4	1.1	0.9	A
Drain current (peak) (note 1)	I_{DM}	max.		3,0		A
Total power dissipation up to $T_c = 25\ ^oC$	P_{tot}	max.		6.25		W
Storage temperature range	T_{stg}			−65 to + 150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	20	K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

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Drain-source breakdown voltage $I_D = 10\ \mu A; V_{GS} = 0$	$V_{(BR)DSS}$	min.	35	60	90	V
Drain-source leakage current at $V_{DS} = V_{DSmax}; V_{GS} = 0$	I_{DSS}	max.	10	10	10	μA
Gate-source leakage current at $V_{GS} = 15\ V; V_{DS} = 0$	I_{GSS}	max.	100	100	100	nA
Gate threshold voltage $I_D = 1\ mA; V_{DS} = V_{GS}$	$V_{GS(th)}$	min.	0.8	0.8	0.8	V
		max.	2.0	2.0	2.0	V
ON-state drain current $V_{DS} = 25\ V; V_{GS} = 10\ V$	$I_{D(on)}$	min.	1.0	1.0	1.0	A
		typ.	2.0	2.0	2.0	A
Drain-source ON-resistance $I_D = 0.3\ A; V_{GS} = 5\ V$	R_{DSon}	typ.	1.5	1.8	2.4	Ω
		max.	5.0	5.0	5.3	Ω
$I_D = 1.0\ A; V_{GS} = 10\ V$	R_{DSon}	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance at f = 1 kHz $I_D = 0.5\ A; V_{DS} = 25\ V$	$\lvert y_{fs} \rvert$	min.	170	170	170	mS
Input capacitance at f = 1 MHz $V_{DS} = 25\ V; V_{GS} = 0$	C_{iss}	max.	50	50	50	pF
Output capacitance at f = 1 MHz $V_{DS} = 25\ V; V_{GS} = 0$	C_{oss}	max.	50	40	40	pF

Note

1. Pulse conditions: $t_p \leqslant 300\ \mu s; \delta = 0.01$.

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Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	15	15	15	pF
Switching times I_D = 1.0 A; V_D = 25 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5	5	5	ns
		max.	10	10	10	ns
	t_{off}	typ.	5	5	5	ns
		max.	10	10	10	ns

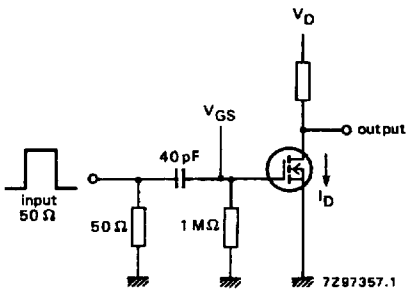

Fig. 2 Switching times test circuit.

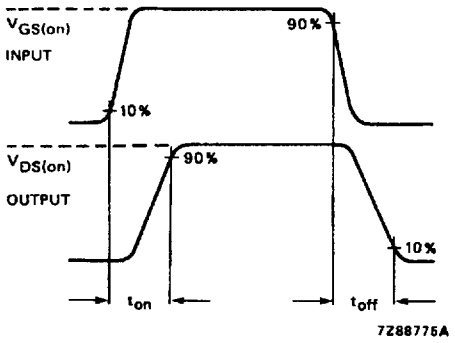

Fig. 3 Input and output waveforms.