YLCDRZA1H

HIGH RESOLUTION EMBEDDED GUI SOLUTIONS KIT

TECHNICAL REFERENCE MANUAL

Renesas Electronics America

Rev 2.20
Revision Date: Jul 21, 2015

www.renesas.com

Disclaimer

By using this Renesas YLCDRZA1H, the user accepts the following terms. The YLCDRZA1H is not guaranteed to be error free, and the entire risk as to the results and performance of the YLCDRZA1H is assumed by the User. The YLCDRZA1H is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non- infringement of intellectual property rights with regard to the YLCDRZA1H. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this YLCDRZA1H, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

This Renesas YLCDRZA1H is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- Ensure attached cables do not lie across the equipment
- Reorient the receiving antenna
- Increase the distance between the equipment and the receiver
- Connect the equipment into an outlet on a circuit different from that which the receiver is connected
- Power down the equipment when not in use
- Consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas YLCDRZA1H does not represent and ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

Table of Contents

Chapter 1 - Preface

Cautions

This document may be, wholly or partially, subject to change without notice.

Trademarks

Copyright

Website: http://www.renesas.com/

Glossary

CPU	Central Processing Unit	USB	Universal Serial Bus
GUI	Graphical User Interface		

Chapter 2 - Introduction and Purpose

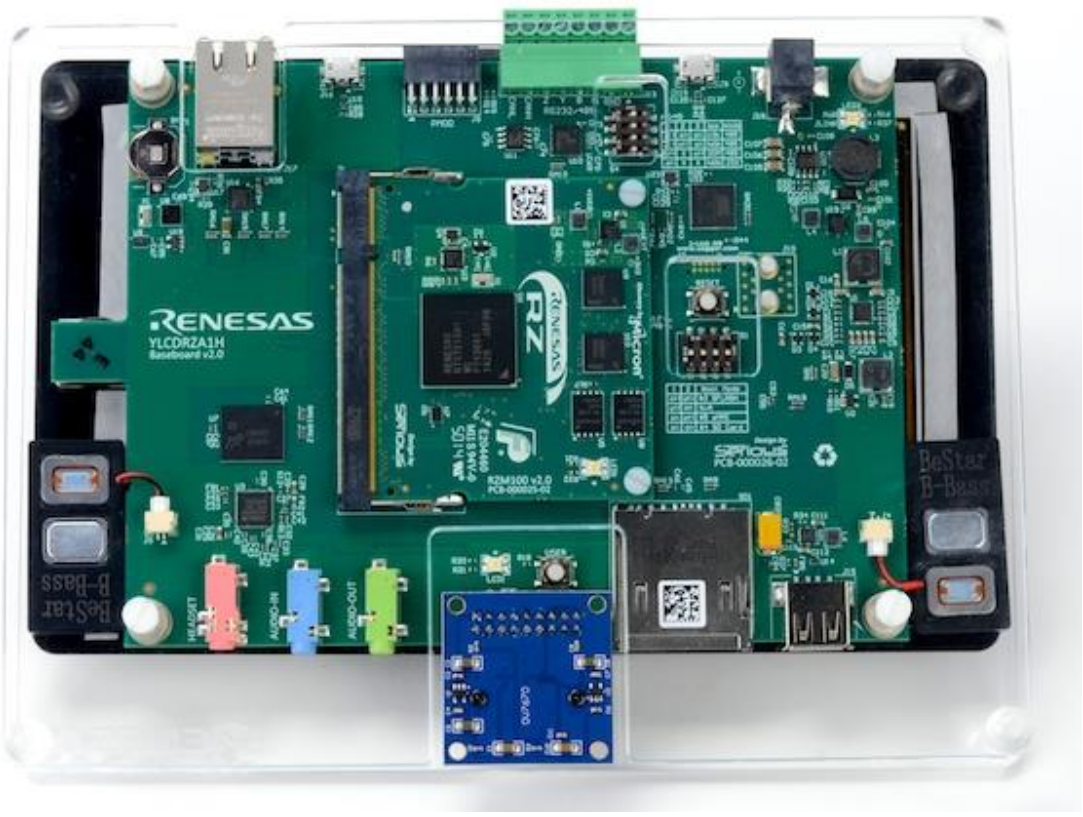
The Renesas YLCDRZA1H High Resolution Embedded GUI Solution Kit is a flexible and full-featured Human Machine Interface plus communications platform based on the Renesas RZ/A1H Microcontroller. While production worthy, the YLCDRZA1H is primarily intended for software and hardware developers to experiment and evaluate the extensive I/O features of the RZA1H on the YLCDRZA1H prior to development of their own customized and focused hardware daughter-cards and/or add-on hardware adjacent to the host module.

The YLCDRZA1H contains several communications ports, including 10/100 Ethernet, CAN, RS232, and RS485, as well as the popular PMOD™ connectors for external prototyping modules from Digilent and other vendors.

Distributor inventory of Renesas products can be found here.

For more information on the Renesas YLCDRX63N Embedded GUI Solution Kit, visit the Renesas website.

2.1 - Hardware



The YLCDRZA1H has three main elements:

- a re-usable SO-DIMM style module (the “RZ Module”) with MCU, DRAM, FLASH, local power and clocks,
- a full featured I/O baseboard, and,
- a high resolution 1280x800 IPS LCD with LVDS 24-bit color interface and capacitive touch sensing.

These elements come pre-assembled in the YLCDRZA1H kit in an acrylic enclosure along with various cables, power supplies, and accessories.

The MCU/memory module (the “RZ Module”) in the kit includes:

- Renesas RZ/A1H MCU with
  - 10Mbytes on-chip RAM, 400MHz ARM Cortex™-A9 processor
  - 32-Kbyte L1 instruction cache, a 32-Kbyte L1 data cache, and a 128-Kbyte L2 cache
  - 10-Mbyte large-capacity on-chip high-speed RAM with parallel data/address paths
  - OpenVG*-compliant Renesas graphics accelerator with JPEG encoder/decoder, capture engine unit, and pixel format converter

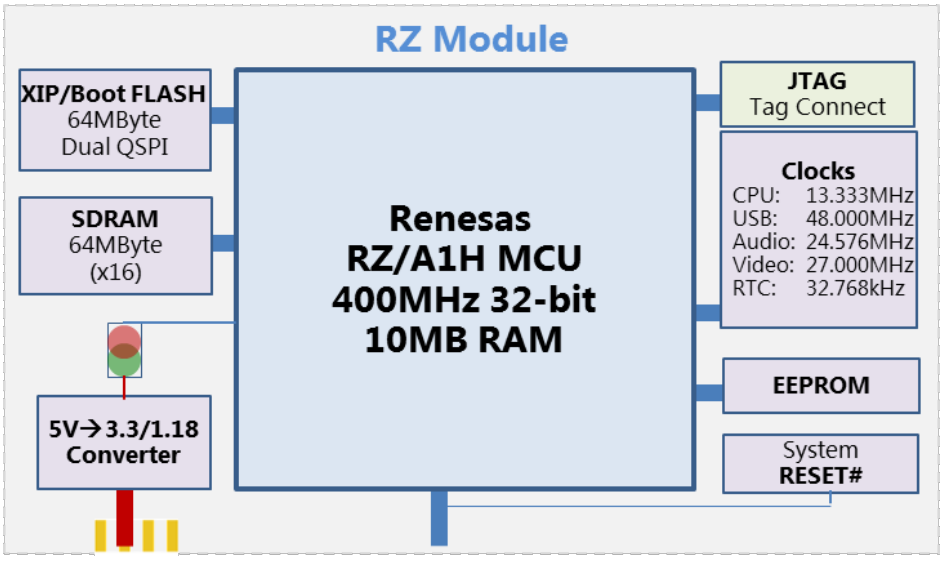
- 64Mbytes DRAM
- 64Mbytes Serial boot/XIP NOR FLASH in a dual-QSPI (x8) configuration
- On-DIMM power supplies for all on-module circuits
- 32.768kHz RTCC crystal and MCU clocks

The I/O Baseboard includes:

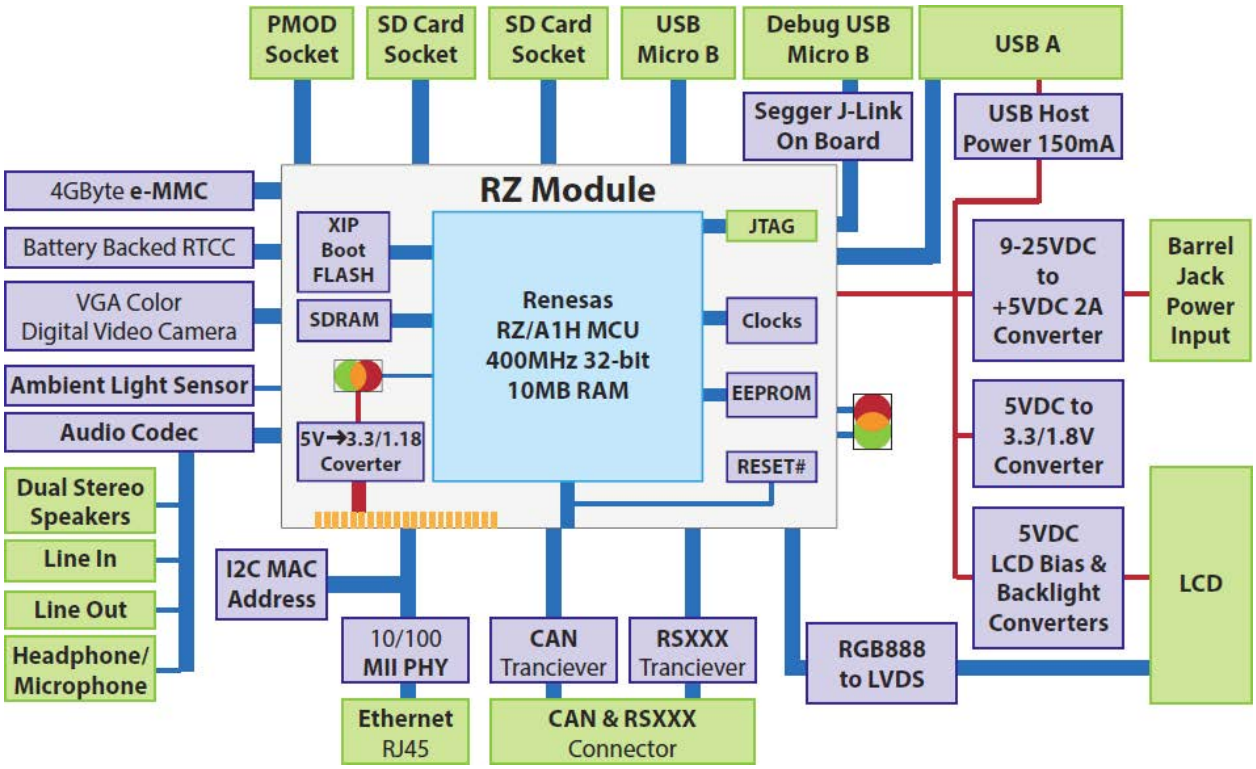
- 4GBytes e-MMC intelligent NAND flash “drive on chip”
- 9-25VDC barrel jack power input; standard 12V 10W EU/US wall adapter included in the kit
- CAN plus RS232/RS485 port on a 3.5mm screw terminal plug connector
- Digilent PMOD port with Type 2A (expanded SPI) and Type 4A (expanded UART) support
- 10/100 Ethernet Port on standard RJ45 CAT5/6 jack with dual indicator LEDs
- Stereo Audio with Dual 1W speakers, line in, line out, headset-style headphone out/microphone in
- Color VGA forward facing digital video camera
- SD Card socket (SDIO)
- High Speed USB 2.0 Host and Device ports
- Coin-cell battery-backed real time clock
- 0 to 50°C operating temperature range
- Segger J-Link On Board programmer/debugger
- Ambient light sensor, reset button, power indicator LED

2.2 - Hardware Block Diagrams

The RZ Module conceptually is structured as follows:



The baseboard incorporates the module as follows:



2.3 - Box Contents

The following items are included in the YLCDRZA1H package:

- YLCDRZA1H assembly, including I/O baseboard, LCD display, and RZ module, camera in an acrylic demo enclosure with adhesive silicone feet
- 9-25VDC US/EU Wall Power Supply
- 8 pin screw terminal plug for CAN/RS232/RS485 port
- Ethernet cable (1) and USB Micro B cables (2)

2.4 - Software & Software Development Tools

Renesas and their Platinum Partners, including Serious Integrated and Express Logic have developed numerous example projects demonstrating the various features of the YLCDRZA1H. Visit the Renesas website for more information.

Development for the YLCDRZA1H is supported under the Renesas e2Studio Eclipse-based framework, ARM® DS-5 Development Studio, as well as the IAR Embedded Workbench. No-cost fully-unlocked GNU C development tools from Renesas are available, as well as professional and fully-supported tools from IAR.

2.5 - Usage Models

The YLCDRZA1H is designed as an initial hardware reference platform as well as software development platform for OEM applications not only requiring sophisticated LCD-based GUI Human Machine Interface (HMI) capabilities but also extensive communications. The platform has little to no GPIO control on-board, and generally will be used in conjunction with an OEM's I/O subsystem, possibly communicating with the YLCDRZA1H over RS232, RS485, or UART/SPI using the PMOD connectivity.

For more extensive GPIO connectivity, more flexible port assignments and experimentation with MCU features, the complete Renesas RZ/A1H Development Kit YR0K77210S003BE is recommended.

2.6 - Versions

The production version of the MCU/Memory module is v2.0 as marked on the module silk screen. All units in circulation should have this version.

Two versions of the Baseboard have been distributed, marked v2.0 and v2.1 on the silk screen respectively. The v2.1 Baseboard has two notable changes from v2.0:

1) The USBH Power Enable, hardwired to “always on” in v2.0, is now connected through an inverter to P1.6. On power up, the USBH power delivery is disabled. When the port pin is asserted low, the inverted (active high) signal enables the USBH Power subsystem.
2) Improved USB signal routing/integrity for more reliable High Speed operation

Chapter 3 - Getting Started

The YLCDRZA1H assembly comes pre-assembled, and requires no initial assembly to operate out of the box.

Some elements, such as the LCD to the top acrylic ring, are bonded with high performance adhesive: do not attempt to detach the LCD from the acrylic or disassemble any element not fastened by simple nylon screws.

The RZ Module comes pre-inserted into the SO-DIMM socket and fastened to the Baseboard via two screws. Only remove/install this module with the power completely removed.

3.1 - Powering the YLCDRZA1H

The YLCDRZA1H can only be powered via the barrel jack, and can accept any input voltage from 9 to 25VDC (center positive) power supply with 10W or more capability; the kit comes with a standard UL/CSA/CE 12V 10W adapter with both an EU and US capability more than sufficient to power the unit.

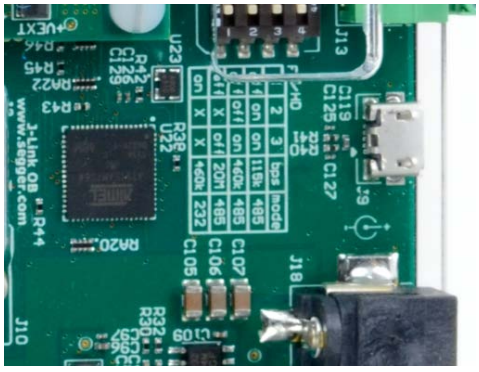
Plugging in the 12V adapter will light up the green LED near the barrel jack, confirming the board is powered. The RZ Module also has a local green power LED showing that it, too, is powered. The Baseboard LED near the barrel jack may flash orange – this is the Segger J-Link debugger activity notification.

3.2 - See the Demo

A demo, pre-installed in the RZ Module's serial FLASH, will start up when the module is first powered. If during the course of software development this demo is erased from the serial FLASH you can download this demo from the Renesas website and re-install it using your software development tools and the on-board Segger J-Link On-Board debugger.

3.3 - Connecting to the Segger J-Link On-Board Debugger

The kit comes with two (2) USB Micro B cables suitable for connecting a PC to the YLCDRZA1H. Use one of these to connect to the USB Micro connector J9 near the power jack. This is your debugger connection, and is only required when doing software development with the YLCDRZA1H.



Chapter 4 – Specifications

4.1 - DC Characteristics

The DC characteristics of the I/O elements of the platform are governed by the underlying AC timing characteristics of the individual components. Consult the bill of materials and component data sheets for more information.

Specification	Permissible			
	Minimum	Typical	Maximum	Unit
Input Voltage to Barrel Jack	9	12	25	VDC
Input Power to Barrel Jack			10	W

4.2 - AC Characteristics

The AC timing characteristics at the module level are governed by the underlying AC timing characteristics of the individual components. Consult the bill of materials and component data sheets for more information.

4.3 - Environmental Characteristics

The YLCDRZA1H, while designed with production-worthy methods and components, is not designed as a production unit to be used direction in OEM equipment. Contact Renesas for a list of hardware design partners who can develop and deliver production-ready platforms based on the ingredients used in the YLCDRZA1H kit.

Specification	Permissible			
	Minimum	Typical	Maximum	Unit
Operating Temperature	0		50	C
Storage Temperature	-20		60	C
Humidity (Non-condensing)			90%@50C	RH

4.4 - Physical Characteristics

The outer dimensions of the YLCDRZA1H, with acrylic enclosure, are approximately 207mm x 53mm x 33mm.

Chapter 5 - Power

The YLCDRZA1H has 6 different power subsystems on board:

- Baseboard Power:
  - Main power input 9-25VDC in, 5VDC out 2A buck switcher
  - 3.3V/1.8V buck switcher for Baseboard logic and I/O
  - LCD Backlight boost constant-current supply
  - LCD bias and drive voltage boost supplies
  - USB Host 150mA current-limited supply
- RZ Module Power
  - 3.3V/1.18V buck switcher for local RZ Module clocks, memory, and the MCU

Many of these may not be needed in your own derivative designs, but are included in the design so you can pick and choose depending on your specific requirements. A detailed discussion of each subsystem follows.

5.1 - Main Power Subsystem

The YLCDRZA1H can accept 9-25VDC from the Switchcraft RASM712PX barrel jack. The jack is designed to accept an industry-standard 5.5mm OD/2.5mm ID barrel plug with positive center.

The two power signals **+VIN** and **GND** are connected downstream directly to the main buck converter which delivers 5VDC at up to 2A (via signal **+5V)** to the whole assembly for use by various subsystems and further regulation. No other circuits on the YLCDRZA1H use the 9-25VDC **+VIN** power signal.

The **+5V** power signal directly powers the green portion of the Baseboard tri-color LED. The red portion of that LED is driven by the Segger J-Link On Board activity indicator.

The **+5V** power signal is the only power delivered for use by the RZ Module, which has its own subsequent regulation on-module.

5.2 - 3.3V/1.8V Main Baseboard Power Subsystem

Almost all the circuits on the Baseboard require 3.3 volts. The camera module and audio subsystem, in addition, both requires 1.8V. A dual buck switcher takes the **+5V** power signal and delivers 3.3V at up to 2A (**+3V3**) for most circuits on the board as well as 1.8V (**+1V8**) required by the audio subsystems.

5.3 - LCD Backlight Power Subsystem

The LCD on the YLCDRZA1H is backlit by an array of LEDs. This array requires a constant current supply of 100 mA at approximately 12.8VDC. The ability to pulse width modulate (PWM) this supply is important to enable well-controlled backlight dimming, and the ability to turn off the backlight is important for power management – 100mA at 12.8V is approximately 1.3W of power, and factoring in the boost conversion efficiency approximately 1.6W of power from the input supply. Unlike other power systems where typical is normally much less than maximum, this is a typical number as the LEDs are actually run at this power.

The **+5V** main power signal feeds a constant current boost controller delivering this 100mA to the LCD backlight. A PWM-capable MCU port bit is connected to this controller's ENABLE# pin:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P8.12	**PWM1E**	**P8_12/PWM1E-BLEN**	**18**	**RZM-BLEN**	LCD Backlight Enable (active high)

5.4 - LCD Logic and Bias Subsystem

As is common with most LCDs, the LCD panel in the kit requires a 3.3V supply. In this case, the 3.3V supply must be up to 300mA and is provided by the 5.2 - 3.3V/1.8V Main Baseboard Power Subsystem signal **+3V3**. This power supply is always on when the system is powered.

LCD panels also need a variety of other voltages to drive the LCD active elements, and most small LCD panels have all the voltage converters internally in the panel to make the system designer's life easy. As the panels increase in size, these voltages are often expected from the system rather than generated in the panel, especially for thin panels with minimal internal space. In addition to 3.3V, the panel on the YLCDRZA1H requires all these voltages to be supplied:

Item	Symbol	Min.	Typ.	Max.	Unit
Power voltage	AVDD	9.54	9.74	9.94	V
	VGH	22.4	22.7	23	V
	VGL	-7.7	-8	-8.3	V
Input signal voltage	VCOM	3.0	3.3	3.6	V
Current of AVDD Power supply	I_{AVDD}	-	30	80	mA
Supply Current for Gate Driver (High level)	I_{VGH}	-	0.3	1.1	mA
Supply Current for Gate Driver (Hi level)	I_{VGL}	-	0.3	1.1	mA

The Baseboard has a complete power generation subsystem for these other voltages. This subsystem is also always enabled when the system is powered.

5.5 - USB Host Power Subsystem

While the USB host A connector could have been driven directly from **+5V** (or at least via a high-side FET power switch for enable control), the design incorporates a 150mA current limited design to ensure that an inappropriate high-load device does not crash the board or overstress the main power system. At currents above 150mA, the voltage on the output to the connector drops precipitously to limit the current.

MCU		Schematic			Operation
Port	Mode	Module	#	Baseboard	
	VBUSIN1	VBUSIN1	41	RZM-USBF_VBUS	USB Device ("Function") VBUS Detect
P1.6	see below	[1]P1_6-USBH_5V_EN#	132	RZM-USBH_5V_EN#	USB Host VBUS Power Out Enable (active low)
	VBUSIN0	VBUSIN0	43	RZM-USBH_VBUS	USB Host VBUS Detect
P1.12	TINT20/GPI	P1_12/TINT20-USBH_OC	56	RZM_USBH_OC#	USB Host VBUS Overcurrent Detect (active low)

On v2.0 units, P1.6 was incorrectly used to drive the USB Host Power Enable (RZM-USBH_5V_EN on the RZ Module; DIMM pin 132). This port is open drain only on the MCU, and is incapable of driving high and enabling the power supply. All v2.0 units should include a post-production modification connecting U21 pin 7 (ENUSB) to U21 pin 8 (FAULT#) to enable the USB supply during all non-overcurrent situations. Version 2.1 units have an inverter with input pull-up added to this path. In this configuration, the RESET# condition disables the USB Host Power Enable, and asserting P1_6 low enables the USB Host Power.

Software intending on using the USB Host Power Subsystem needs to accommodate both the v2.0 with post-production modification as well as the v2.1 units, since in the former case the USBH_5V_EN# pin should not be driven low and in the latter, driving it low is required to enable USB Host power. During driver initialization, perform the following sequence to determine a v2.0 vs. v2.1 baseboard:

Set USBH_5V_EN# to low
USBH_EnableValue = inverse of read value of USBH_OC#

On v2.1, setting USBH_5V_EN# low will drive the enable high (via the inverter); assuming a non-overcurrent situation immediately after the enable the read value of OC# will be high, indicating a 2.1 board. On v2.0, setting USBH_5V_EN# low drive the enable low (no inverter), which since pin 7 & 8 are tied together, we'll see an overcurrent active (low) as well, indicating a 2.0 board. Use the inverted value of the OC# test read from now on in the driver to enable or disable the USB Host Power subsystem.

5.6 - 3.3V/1.18V Module Power Subsystem

The RZ Module is powered by the **+5V** power signal from the Baseboard. The MCU, memory, and clocks on the module require 3.3V and the MCU requires 1.18V for its core voltage. The RZ Module contains a dual 5V in dual output 3.3/1.18V buck switcher that delivers the voltages exclusively for the module's usage as module schematic signals **+3V3** and **+1V18** respectively. These are not joined with any power signals on the Baseboard except by sharing a common system ground.

Chapter 6 – Graphics Capacitive Touch LCD

One of the most important features of the YLCDRZA1H is the high resolution LCD graphic color display with the following characteristics:

- 1280x800 pixel resolution
- In Plane Switching (IPS) technology for excellent visibility at nearly any viewing angle
- Integrated capacitive touch controller
- 24-bit color Low Voltage Differential Signaling (LVDS) interface

6.1 - LCD Interface

Lower resolution displays, typically at and below 800x480 (WVGA), use parallel RGB (red green blue) interfaces, for example 8 bits for red, 8 for blue, and 8 for green over a 24-bit wide cable to the LCD along with other control signals such as clock, data enable, vertical, and horizontal sync. The RZ/A1H has a built-in RGB LCD interface capable of driving such displays at 16, 18, or 24 bits wide for RGB565 (65,536 color), RGB666 (262,144 color), or RGB888 (16M color) support respectively.

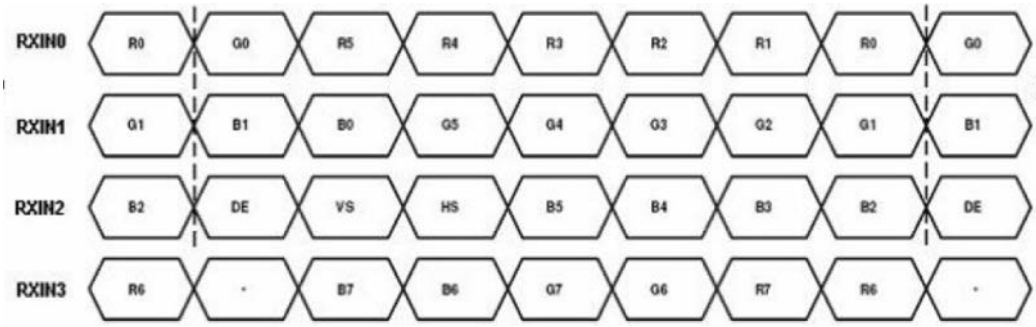
As pixel resolutions increase, the electrical noise generated and routing challenges due to wide high speed parallel buses over the 3-10" cable to the LCD become problematic and a few Low Voltage Differential Signal (LVDS) channels are used where each color (red, green, blue) along with and the control signals are encoded and serialized, often resulting in an 8 signal cable (4 differential pairs). The Renesas RZ/A1H MCU, in addition to its 24-bit RGB interface, also has an 18-bit color LVDS interface.

The MCU's LVDS interface is very well suited to many high-resolution OEM applications. It is very cost effective, requiring smaller cables and connectors than parallel RGB and is natively supported by the MCU with minimal external components beyond a few impedance matching resistors.

For lower resolution applications, typically 800x480 and below, the RGB interface is an excellent solution.

In order to fully highlight the capabilities of the MCU's graphics controller, the YLCDRZAH1 uses the full 24-bit color RGB888 interface. However the LCD panel is an LVDS panel. The YLCDRZA1H Baseboard includes a low cost RGB888 to LVDS serializer to convert the signal format from the MCU to the LCD's required timing/orientation:

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	fclk	(67.55)	(71.11)	(78.22)	MHz	Frame rate =60Hz
Horizontal display area	thd		1280			
HS period time	th	(1410)	(1440)	(1470)	DCLK	
HS Blanking	thb	130	160	190	DCLK	
Vertical display area	tvd		800			
VS period time	tv	(813)	(823)	(833)	H	
VS Blanking	thb	13	23	33	H	



Both the MCU's RGB and LVDS interfaces are fully exposed to the RZ Module's edge fingers, however the LVDS signals are not connected or used on the YLCDRZA1H Baseboard. The RZ Module chapter describes the edge finger assignment. A baseboard could be designed that uses the RZ Module and employs the LVDS rather than RGB interface.

The LCD RGB data, control and power signals are wired on the YLCDRZA1H assembly as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P8.12	PWM1E	P8_12/PWM1E-BLEN	18	RZM-BLEN	LCD Backlight Enable (active high)
P3.0	LCD0_CLK	P3_0/LCD_CLK	23	RZM-LCD_CLK	Dot Clock
P11.8	LCD0_TCON6	P11_8/LCD_DEN	3	RZM-LCD_DEN	Data Enable
P11.9	LCD0_TCON5	P11_9/LCD_VSYNC	5	RZM-LCD_VSYNC	Vertical Sync
P11.10	LCD0_TCON4	P11_10/LCD_HSYNC	8	RZM-LCD_HSYNC	Horizontal Sync
P11.7	LCD_DATA0	P11_7/LCD_DATA0	4	RZM-LCD_DATA0	Blue 0 (LSB)
P11.6	LCD_DATA1	P11_6/LCD_DATA1	6	RZM-LCD_DATA1	Blue 1
P11.5	LCD_DATA2	P11_5/LCD_DATA2	199	RZM-LCD_DATA2	Blue 2
P11.4	LCD_DATA3	P11_4/LCD_DATA3	197	RZM-LCD_DATA3	Blue 3
P11.3	LCD_DATA4	P11_3/LCD_DATA4	177	RZM-LCD_DATA4	Blue 4
P11.2	LCD_DATA5	P11_2/LCD_DATA5	183	RZM-LCD_DATA5	Blue 5
P11.1	LCD_DATA6	P11_1/LCD_DATA6	175	RZM-LCD_DATA6	Blue 6
P11.7	LCD_DATA0	P11_7/LCD_DATA0	181	RZM-LCD_DATA7	Blue 7 (MSB)
P4.0	LCD_DATA8	P4_0/LCD_DATA8	103	RZM-LCD_DATA8	Green 0 (LSB)
P4.1	LCD_DATA9	P4_1/LCD_DATA9	66	RZM-LCD_DATA9	Green 1
P4.2	LCD_DATA10	P4_2/LCD_DATA10	68	RZM-LCD_DATA10	Green 2
P4.3	LCD_DATA11	P4_3/LCD_DATA11	70	RZM-LCD_DATA11	Green 3
P4.4	LCD_DATA12	P4_4/LCD_DATA12	105	RZM-LCD_DATA12	Green 4
P4.5	LCD_DATA13	P4_5/LCD_DATA13	78	RZM-LCD_DATA13	Green 5
P4.6	LCD_DATA14	P4_6/LCD_DATA14	82	RZM-LCD_DATA14	Green 6
P4.7	LCD_DATA15	P4_7/LCD_DATA15	111	RZM-LCD_DATA15	Green 7 (MSB)
P5.0	LCD_DATA16	P5_0/LCD_DATA16	142	RZM-LCD_DATA16	Red 0 (LSB)
P5.1	LCD_DATA17	P5_1/LCD_DATA17	144	RZM-LCD_DATA17	Red 1
P5.2	LCD_DATA18	P5_2/LCD_DATA18	154	RZM-LCD_DATA18	Red 2
P5.3	LCD_DATA19	P5_3/LCD_DATA19	156	RZM-LCD_DATA19	Red 3
P5.4	LCD_DATA20	P5_4/LCD_DATA20	148	RZM-LCD_DATA20	Red 4
P5.5	LCD_DATA21	P5_5/LCD_DATA21	150	RZM-LCD_DATA21	Red 5
P5.6	LCD_DATA22	P5_6/LCD_DATA22	160	RZM-LCD_DATA22	Red 6
P5.7	LCD_DATA23	P5_7/LCD_DATA23	162	RZM-LCD_DATA23	Red 7 (MSB)

6.2 - Capacitive Touch Controller

The LCD on the YLCDRZA1H includes a capacitive touch sensor system and built-in Pixcir Tango C48 controller. The C48 has the following features:

- 400kHz I2C interface with activity interrupt out
- 5 finger simultaneous multi-touch detection
- Palm detection for lock function, and
- <100 idle-to-active touch response time.

The 7-bit I2C address of the C48 controller is `0x5C`:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x5C	0xB9	0xB8	1	400	Baseboard	Pixcir C48 Capacitive Touch Controller

Chapter 10 – I2C Device Summary lists all the I2C devices on the YLCRZA1H.

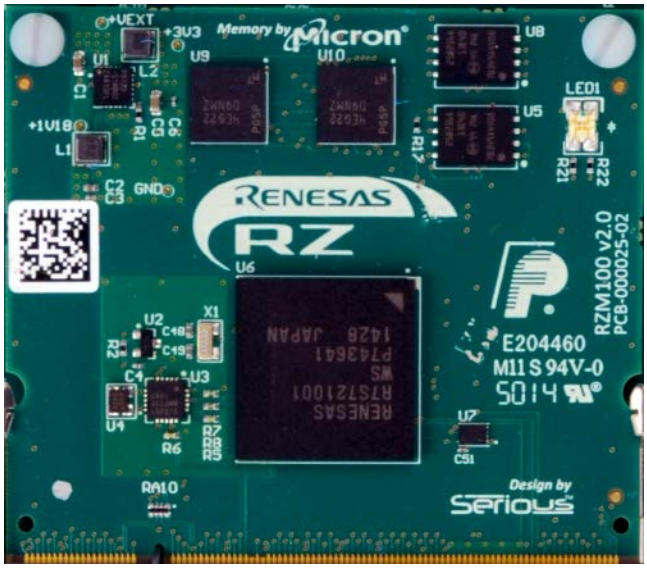
On system boot the controller is held in reset with a weak pull-up on the `P8_13-TOUCH_RST` signal and the driver should drive this signal low to enable the C48 to accept commands. The controller is connected as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P8.13	GPIO	P8_13-TOUCH_RST	7	RZM-TOUCH_RST	LCD Touch controller reset (active high)
P1.10	IRQ4	P1_10/IRQ4-TOUCH_IRQ	52	RZM-TOUCH_IRQ	LCD Touch controller interrupt
P1.2	SCL1	P1_2/SCL1	165	RZM-SCL1	Touch dedicated I2C1 Clock
P1.3	SDA1	P1_3/SDA1	169	RZM-SDA1	Touch dedicated I2C1 Data

The Pixcir Tango C48 instruction set and data sheet are available only under non-disclosure agreement from Pixcir.

Chapter 7 – The MCU/Memory Module

As discussed, the YLCDRZA1H is comprised of two circuit boards, the Baseboard and the MCU/Memory module, or "RZ Module" that plugs into the Baseboard via a commodity 200 pin SO-DIMM socket. For a complete pin-out of the SO-DIMM socket, see Chapter 12.1 - SO-DIMM Detail.



The MCU/memory module (the "RZ Module") in the kit includes:

- Renesas RZ/A1H MCU
- 64Mbytes DRAM
- 64Mbytes Serial boot/XIP NOR FLASH in a dual-QSPI (x8) configuration
- On-DIMM power supplies for all on-module circuits
- 32.768kHz RTCC crystal and 12MHz MCU clock
- 2kbit configuration/user EEPROM
- On-module system reset

The local power supplies are fully described in Section 5.6 - 3.3V/1.18V Module Power Subsystem.

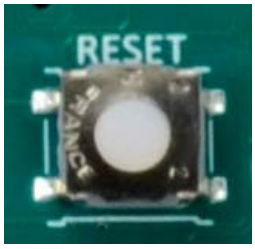
7.1 - Renesas RZ/A1 MCU

The Renesas RZ/A1 MCU family has several members; the YLCDRZA1H uses the R7S721001VCBG with the following key features:

- 10Mbytes on-chip RAM, 400MHz ARM Cortex™-A9 processor
- 32-Kbyte L1 instruction cache, a 32-Kbyte L1 data cache, and a 128-Kbyte L2 cache
- 10-Mbyte large-capacity on-chip high-speed RAM with parallel data/address paths
- OpenVG™-compliant Renesas graphics accelerator with JPEG encoder/decoder, capture engine unit, and pixel format converter
- SDRAM controller
- 324 pin BGA

The MCU is fully described in the Renesas RZ/A1H Group User's Manual: Hardware along with other documentation on the Renesas RZ/A1 Family Documentation Website.

7.2 - System Reset

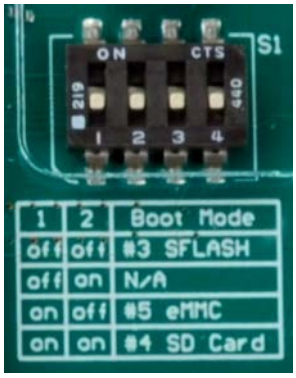


The RZ Module includes a small system reset chip, designed to not only reset the MCU but any attached baseboard if desired. On power-up, the system reset is asserted low for approximately 100-250mS and then is released to rise high with a simple pull-up resistor. Pushbutton S3 on the baseboard is connected directly to this reset signal – the reset chip automatically senses the pushbutton and, when pressed (RESET# grounded) debounces the switch and initiates a reset cycle as if power were being applied for the first time.

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
RES	RES	RESET#	27	RZM-RESET#	System Reset (open drain, active low) Also RESET Pushbutton S3 on Baseboard

7.3 - MCU Boot Mode Selection

The RZ/A1H MCU can boot from a variety of memory devices, selectable by the levels present on the MD_BOOT2/1/0 pins on the MCU when RES is de-asserted. The Baseboard includes a 4 element DIP Switch where switch 1 and 2 control MD_BOOT1/2 respectively.



Option			Boot Mode		YLCDRZA1H
MD_BOOT2	MD_BOOT1	MD_BOOT0	#	Description	Support
-	0	0	0	CS0# RAM/ROM	No
-	1	0	1	CS1# RAM/ROM	No
1	0	1	3	Serial FLASH	Default
0	1	1	4	SD Card	via Baseboard
1	1	1	5	e-MMC	via Baseboard

On the YLDRZA1H, the BOOTMD2/1/0 pins have a default weakly strapped selection to the serial FLASH on the RZ Module (since the module has the serial FLASH populated), but the boot mode can be changed on the Baseboard through DIP switch S1. The boot pins are controlled/connected as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P7.0	MD_BOOT2	P7_0/MD_BOOT2	179	RZM-BOOT2	Weakly high (47kΩ) on RZ Module S1.2 pulls this low (GND) when ON
P0.1	MD_BOOT1	P0_1/MD_BOOT1	61	RZM-BOOT1	Weakly low (47kΩ) on RZ Module S1.1 pulls this high (4.7kΩ) when ON
P0.0	MD_BOOT0	P0_0/MD_BOOT0	-	-	Permanently high on RZ Module

7.4 - 64Mbytes SDRAM

The Renesas RZ/A1H MCU has a full on-chip 16-bit SDRAM controller. The YLCDRZA1H RZ Module has this SDRAM connection (address, data, control) isolated on the module connected to two (2) Micron 32MByte SDRAM devices for a total of 64MBytes of system DRAM.

7.5 - 64Mbytes Dual QSPI Serial NOR FLASH

The Renesas RZ/A1H MCU supports two (2) parallel Quad SPI (QSPI) interfaces designed for direct-attach to Serial NOR FLASH devices. In this configuration, the MCU can boot from the primary device in single-SPI traditional 4-wire (MISO, MOSI, SCLK, SSL#) mode and software can switch access modes such that both devices are accessed simultaneously in QSPI mode for an equivalent 8-bit wide interface at very high speed.

Not only can the MCU access these devices as data storage areas, but it can also execute in place (XIP) from the devices at surprisingly high speeds – the MCU's SPI Multi I/O Bus Controller handles all the SPI traffic and FLASH commands to make the devices completely memory mapped and accessible as if it were on a traditional address/data bus.

The YLCDRZA1H features two Micron N25Q256A13EF840E NOR Serial FLASH devices with 32Mbytes each, totaling 64Mbytes connected in the Dual QSPI configuration.

7.6 - On-Module Clocking

On the RZ Module there are two local clocks for use by the MCU. A simple 32.768 kHz tuning fork crystal is attached to the MCU to drive the on-chip Real Time Clock Calendar (RTCC). There is no VBAT battery backup capability on the chip, so this oscillator must be re-enabled at each MCU reset. The YLCDRZA1H has an I2C Battery Backed RTCC chip with coin cell for this purpose, and on system reset software can retrieve the battery-backed date/time from the external RTCC and load the internal RTCC for quick software access at runtime.

While the MCU can operate with as little as a single 12MHz oscillator for the core, USB, and peripherals, to fully exploit the capabilities of the MCU a variety of input clocks are desirable:

- 13.3333MHz to enable the core at 400MHz
- 27.0MHz for video

- 24.576MHz to deliver industry standard audio frequencies
- 48.000MHz for USB

The RZ Module includes a complete clock oscillator/synthesizer subsystem generating and delivering all four of these frequencies to the MCU. These are not crystals but rather external clock sources to the MCU therefore software should not turn on the crystal oscillator drivers for these clock inputs.

The clock synthesizer/generator is a Silicon Labs Si5351C. At power-up, the device is factory programmed for the frequencies listed above, but the Si5351C is an I2C device and the generated frequencies can be modified at runtime if desired. Whether for EMI tuning, power management, or, for example, to change the input frequencies for different audio sampling/generation time bases beyond the capabilities of the MCU's programmable prescaler, this feature can be valuable in many system designs.

The Si5351C is available on the I2C bus 0 as device number 0x60:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x60	0xC1	0xC0	0	400	Module	Si5351C Clock Synthesizer

Chapter 10 – I2C Device Summary lists all the I2C devices on the YLCRZA1H.

The interrupt output (INTR) of the Si5351C is not connected to the MCU.

7.7 - Spread Spectrum Clock Generator (SSCG)

The Renesas RZ/A1H MCU has the ability to slightly and randomly modulate the internal PLLs to dampen potential and undesirable RF emissions. This feature is controlled by the MCU's MD_CLKS pin, which is weakly (47kΩ) pulled low (disabled) on the RZ Module. The Baseboard DIP Switch S1 position 3 (when ON) strongly (4.7kΩ) pulls this high and enables this feature on the MCU.

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P0.3	MD_CLKS/GPIO	P0_3/MD_CLKS	176	RZM-SSCG	Enables Spread Spectrum Clocking in MCU by Baseboard S1.2 (ON/active GND,OFF pulled high (4.7kΩ) on RZ Baseboard)

Note this pin is sampled on the release of system reset, after which a different Baseboard design could optionally use this signal for a GPIO or other function at runtime.

7.8 - EEPROM

On the MCU/Memory module is a small I2C EEPROM, an On Semiconductor CAT34C02, located on I2C bus 0 at 7-bit address 0x57:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x57	0xAD	0xAC	0	400	Module	CAT34C02 EEPROM

Chapter 10 – I2C Device Summary lists all the I2C devices on the YLCRZA1H.

7.9 - Switches and LEDs

The MCU/Memory module has a single dual-color red and green LED that can be turned on independently and when both are on simultaneously the LED appears orange. The green LED is powered automatically when the local 3.3V power is present. The red LED is controlled by a processor GPIO for software use:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P11.11	GPO	P11_11-LED1R			Module LED Red (active high)

There are no other switches, jumpers or other user I/O on the module.

Chapter 8 – Baseboard

The I/O Baseboard included with the YLCDRZA1H includes:

- 9-25VDC barrel jack power input with 5V 2A DC-DC converter for Baseboard and RZ Module
- All local power supplies and clocks
- RGB888 to LVDS translator and connection to LVDS LCD
- Connection to the 4GBytes e-MMC intelligent NAND flash “drive on chip”
- CAN plus RS232/RS485 port on a 3.5mm screw terminal plug connector
- 10/100 Ethernet Port on standard RJ45 CAT5/6 jack with dual indicator LEDs
- Stereo Audio with Dual 1W speakers, line in, line out, headset-style headphone out/microphone in
- Color VGA forward facing digital video camera
- SD Card socket (SDIO)
- High Speed USB 2.0 Host and Device ports
- Coin-cell battery-backed real time clock
- Digilent PMOD* port with Type 2A (expanded SPI) and Type 4A (expanded UART) support
- Segger J-Link On Board programmer/debugger
- User I/O including ambient light sensor, user and reset pushbuttons, user and power LEDs

8.1 - Power

The YLCDRZA1H’s Baseboard has 5 different power subsystems:

- Main power input 9-25VDC in, 5VDC out 2A buck switcher
- 3.3V/1.8V buck switcher for Baseboard logic and I/O
- LCD Backlight boost constant-current supply
- LCD bias and drive voltage boost supplies
- USB Host 150mA current-limited supply

These are all described in Chapter 5 - Power.

8.2 - Clocking

There are several clock sources generated and used on the Baseboard for various peripherals.

- 32,768 kHz crystal for the Battery Backed Real Time Clock Calendar (RTCC)
- 25.000 MHz oscillator for the 10/100 Ethernet Port
- 24.000 MHz oscillator for the Digital Video Camera
- Audio clock generated in the RZ MCU on the RZ Module for the Audio Subsystem

8.3 - LCD Connection and RGB888 to LVDS Translation

As mentioned above, even though the RZ/A1H has an 18-bit color LVDS port native on the MCU (and brought to the connector for optional use by a baseboard), the YLCDRZA1H elects to feature the full 24-bit color capabilities of the RZ/A1H and use the RGB888 port instead.

The LCD display, however, is LVDS. Therefore the baseboard includes a straightforward and inexpensive RBG888 to LVDS translator.

This interface, including MCU signals and connector pins, are described in detail in Chapter 6.1 - LCD Interface

8.4 - e-MMC Memory

In addition to the memory on the RZ Module, the Baseboard adds a 4 Gigabyte “embedded MultiMedia Card” or e-MMC. This is a complete FLASH drive-on-a-chip, with built in wear levelling, bad block management, and more. Software drivers are greatly simplified compared with using NAND FLASH directly. The Micron MTFC4GMDEA-4M

is an e-MMC v4.41 compatible device; for more information about the e-MMC specification see the JEDEC MMC Specification.

Normally, the e-MMC will be used by a software application to run a file system, such as a FAT file system, storing GUI data and other files, possibly including applications and demos.

The RZ/A1H MCU has a built-in MMC controller, and the e-MMC chip is connected as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P0.4	GPO	P0_4-MMC_RST#	31	RZM-MMC_RST	MMC Reset (active low with pull-up)
P3.13	MMC_CMD	P3_13/MMC_CMD	97	RZM-MMC_CMD	MMC Command/response
P3.12	MMC_CLK	P3_12/MMC_CLK	91	RZM-MMC_CLK	MMC clock
P3.11	MMC_D0	P3_11/MMC_D0	93	RZM-MMC_D0	e-MMC Data Bus D0 (LSB)
P3.10	MMC_D1	P3_10/MMC_D1	89	RZM-MMC_D1	e-MMC Data Bus D1
P3.15	MMC_D2	P3_15/MMC_D2	99	RZM-MMC_D2	e-MMC Data Bus D2
P3.14	MMC_D3	P3_14/MMC_D3	64	RZM-MMC_D3	e-MMC Data Bus D3
P11.12	MMC_D4	P11_12/MMC_D4	187	RZM-MMC_D4	e-MMC Data Bus D4
P11.13	MMC_D5	P11_13/MMC_D5	191	RZM-MMC_D5	e-MMC Data Bus D5
P11.14	MMC_D6	P11_14/MMC_D6	185	RZM-MMC_D6	e-MMC Data Bus D6
P11.15	MMC_D7	P11_15/MMC_D7	193	RZM-MMC_D7	e-MMC Data Bus D7 (MSB)

With 8.16 - DIP Switch S1 set in the correct position and the e-MMC carefully partitioned and programmed, the YLCDRZA1H is capable of booting directly from this device.

8.5 - 10/100 Ethernet Port

The RZ/A1H has a full 10/100 Ethernet MAC with MII interface. The RZ Module brings these signals to the edge connector, and the YLCDRZA1H Baseboard delivers these signals interface through a Micrel KSZ8081MNX MII PHY to a standard RJ45 jack.

The MII interface is as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P0.5	GPO	P0_5-ET_RESET#	29	RZM-ET_RESET#	Holds PHY in reset (active low)
P1.5	IRQ5	P1_5/IRQ5-ET_IRQ	171	RZM-ET_IRQ	PHY Interrupt (active low)
P3.3	MDIO	P3_3/ET_MDIO	21	RZM-ET_MDIO	Management data I/O
P5.9	MDC	P5_9/ET_MDC	168	RZM-ET_MDC	Management data clock
P1.14	COL	P1_14/ET_COL	58	RZM-ET_COL	Collision detection
P2.3	CRS	P2_3/ET_CRS	121	RZM-ET_CRS	Carrier detection
P3.6	RXDV	P3_6/ET_RXDV	28	RZM-ET_RXDV	Receive data valid
P3.5	RXER	P3_5/ET_RXER	36	RZM-ET_RXER	Receive error
P3.4	RXCLK	P3_4/ET_RXCLK	40	RZM-ET_RXCLK	Receive clock
P2.8	RXD[0]	P2_8/ET_RXD0	137	RZM-ET_RXD0	Receive data 0 (LSB)
P2.9	RXD[1]	P2_9/ET_RXD1	118	RZM-ET_RXD1	Receive data 1
P2.10	RXD[2]	P2_10/ET_RXD2	122	RZM-ET_RXD2	Receive data 2
P2.11	RXD[3]	P2_11/ET_RXD3	131	RZM-ET_RXD3	Receive data 3 (MSB)
P2.0	TXCLK	P2_0/ET_TXCLK	80	RZM-ET_TXCLK	Transmit clock
P2.1	P2.1/ET_TXER	P2_1/ET_TXER	86	RZM-ET_TXER	Transmit Error or GPIO (unused on Baseboard)
P2.2	TXEN	P2_2/ET_TXEN	104	RZM-ET_TXEN	Transmit enable
P2.4	TXD[0]	P2_4/ET_TXD0	129	RZM-ET_TXD0	Transmit data 0 (LSB)
P2.5	TXD[1]	P2_5/ET_TXD1	110	RZM-ET_TXD1	Transmit data 1

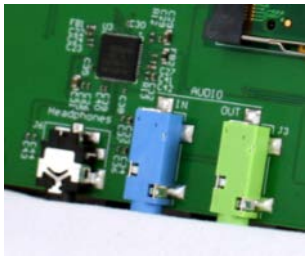
P2.6	TXD[2]	P2_6/ET_TXD2	135	RZM-ET_TXD2	Transmit data 2
P2.7	TXD[3]	P2_7/ET_TXD3	120	RZM-ET_TXD3	Transmit data 3 (MSB)

In order to use the Ethernet interface, a globally unique 48-bit MAC address is required. Most companies purchase batches of thousands of these to assign to their devices. To simplify the demonstration of the YLCDRZA1H, the Baseboard includes a tiny I2C chip, the Microchip 24AA02E48T, which contains a single unique MAC address that software can retrieve and use for the board:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x50	0xA1	0xA0	0	400	Baseboard	24AA02E48T EEPROM/MAC Address

8.6 - Audio Subsystem

One of the features of the Renesas RZ/A1 family is extensive support for external audio codecs for audio input/output. The YLCDRZA1H highlights this capability using the Maxim MAX98089ETN+ Audio Codec/Amplifier, exposing:



- stereo line in jack (blue)
- stereo line out jack (green)
- stereo headphone and microphone mobile phone headset-style jack (black)
- stereo amplified bass-enhanced “B-Bass” speakers from BeStar

The codec is connected to the high performance full-duplex Serial Sound Interface (SSI) on the RZ MCU as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
		CLKAUDIO_24MHZ	67	RZM-AUDIO_CLK	24MHz Base Codec Clock from RZ Module
P1.9	IRQ3	P1_9/IRQ3-AUDIO_IRQ	63	RZM-AUDIO_IRQ	Audio Codec Interrupt
P10.12	SSICLK1	P10_12/SSISCK	108	RZM_SSISCK	Serial Sound Interface Clock
P10.13	SSIWS1	P10_13/SSIWS	133	RZM_SSIWS	Serial Sound Word Select
P10.15	SSITxD1	P10_15/SSITxD	112	RZM_SSITxD	Serial Sound Transmit Data (output)
P10.14	SSIRxD1	P10_14/SSIRxD	116	RZM_SSIRxD	Serial Sound Receive Data (input)

The Maxim codec is an I2C controlled device, appearing on I2C Bus 0 at 7-bit I2C address 0x20:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x10	0x21	0x20	0	400	Baseboard	MAX98089ETN+ Audio Codec/Amplifier

8.7 - Industrial Networking: CAN, RS232, RS485

The large green 3.5mm connector J13 delivers RS232, RS422, or RS485 as well as high performance CAN to external industrial networks. A screw terminal plug is supplied, enabling easy wiring of termination or daisy chained cabling. The connector’s signals are clearly marked on the Baseboard PCB as follows:

Pin	Name	Description
1		No connection
2	GND	Ground
3	RS485_A	Receive non-inverting input
4	RS485_B	Receive inverting input
5	RS485_X	Transmit non-inverting output
6	RS485_Y	Transmit inverting output
7	CANH	CAN Transmit/Receive H
8	CANL	CAN Transmit/Receive L

There is no termination facility on the YLCDRZA1H; if cable termination is required insert a 75 ohm resistor across the appropriate signals at the screw-in connector.

Note that two additional UARTs and an additional CAN port are available on the PMOD Port; only one of those UARTs is in a standard Digilent PMOD configuration however it is possible to create custom non-standard PMODs for that port and access these extra serial interfaces.

8.7.1 - RS232, RS433, and RS485

The YLCDRZA1H employs an Intersil ISL41387IRZ-T multi-protocol transceiver has the following key features:

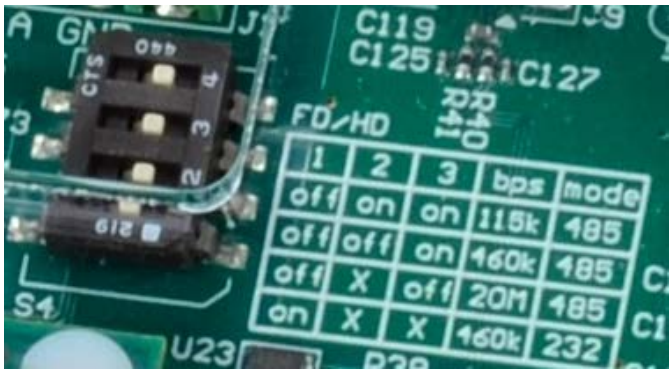
- Selectable RS232 or RS485/RS422
- ±15kV (HBM) ESD protected
- Single ended or differential
- Half or full duplex
- Large (2.7V) differential V_{OUT} for improved noise immunity in RS485/RS422 networks
- Full failsafe (open/short) RX in RS485/RS422 mode
- RS232 transmit rates up to 650kbps, receive rates to 2mbps
- RS485/RS422 data rates up to 20Mbps
- RS485/RS422 slew rate limit options for 460kbps and 115kbps

It is an excellent choice for many RS485 point-to-point and multi-drop networks and works particularly well in many industrial PLC configurations. The dual mode support enables, via the S4 DIP switch, RS232 instead of RS485 levels. Only one mode (RS232 or RS422/485) can be supported at any given time, and the mode is not software selectable – it is assumed that the installation process and environment determines which transmission standard is being connected.

The transceiver is connected to the MCU's UART as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P8.10	GPO	P8_10/RS_DEN	11	RZM-RS_DEN	Transmit Drive Enable (active high)
P8.11	GPO	P8_11/RS_ON	9	RZM-RS_ON	Transceiver Enable (active high)
P3.1	TxD2	P3_1/UART_TX	25	RZM_UART_TX	Transmit Data
P3.2	RxD2	P3_2/UART_RX	15	RZM-UART_RX	Receive Data

The DIP Switch S4 enables a variety of features on this port. The legend on the Baseboard PCB can help with these settings.



RS232 or RS422/RS485 Mode

DIP switch **S4.3** controls which standard the transceiver conforms to; setting this switch ON puts the transceiver in RS232 level mode; the switch OFF puts the transceiver in RS422/RS485 mode.

Slew Rate and Speed Limiting (RS422/RS485 only)

In RS422/485 mode, DIP switch **S4.1** and **S4.2** control the slew rate and speed limits respectively. Set these switches as slow as possible but adequate for the target network rate according to the table.

RSXXX Half/Full Duplex Selection

The RSXXX port can operate in full duplex mode where data can be independently and simultaneously flowing *in* the receive and *out* the transmit pins. It can also be configured to operate in half duplex mode where input/output data is often carried on the same wire(s) and the directionality takes turns.

The main difference between the modes lies in how the transmit and receive enable of the transceiver are configured and used. In full duplex mode, the transceiver receive data is always enabled and being processed by the RZ MCU. In half duplex mode, the receive data is only valid when not transmitting – this avoids receive MCU algorithms from "seeing" the same data that they send if the network shares the same wires for transmit and receive. Full duplex mode always implies separate network wires for transmit and receive. Even then, you may not want to always have your transmitter enabled – there are many custom networks where the "master" in a network owns one network wire (or pair in differential mode) and can broadcast at any time to the "slaves" whereas the slaves must share the return line according to some convention to avoid collisions.

Given the many possible combinations on custom networks, there are two key elements that need to be addressed:

1. Is the receiver always on, delivering data to the MCU's UART all the time, or is the network wiring half duplex and the receiver disabled during transmission to avoid "seeing your own packets"?
2. Is the transmitter always on, or must it be only turned on when the UART transmits on the network?

Receive Enable: Full and Half Duplex Selection

DIP switch **S4.4** controls how the RSXXX transceiver's *receiver* is enabled. When S4.4 is OFF (full duplex mode), a weak pull-up on the RSXXX transceiver's **RXEN** pin ensures that by default the RSXXX transceiver's receiver is always enabled and delivering data to the MCU.

When **S4.4** is **ON** (half duplex mode), the RSXXX transceiver's **RXEN** pin is connected to GND. In this mode, the RSXXX transceiver's receive enable is controlled by its **RXEN#** which is connected to the opposite polarity DEN (drive enable) pin. In this configuration, whenever the transmitter is enabled, the receiver is disabled and the receive data "marks idle" with a weak pull-up.

Transmit Enable

The transceiver's transmit drive enable (**DEN**) pin (when asserted/high) turns on the output drivers on the transceiver and presents UART transmit data onto the network. To avoid any network glitches on power-up, this is always held low (inactive) until the MCU explicitly asserts this signal active/high.

8.7.2 - CAN

The CAN transceiver on the YLCDRZA1H Baseboard is implemented with an Infineon IFX1050GVIO or similar device with the following specifications:

- CAN data transmission rate up to 1 Mbaud
- Suitable for 12V and 24V network applications
- Excellent EMC performance (very high immunity and very low emission)
- ISO/DIS 11898 compatible

The transceiver is connected to the MCU's CAN1 port as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P5.10	CAN1TX	P5_10/CAN1TX	170	RZM-CANTX	CAN Transmit Data
P1.4	CAN1RX	P1_4/CAN1RX	134	RZM_CANRX	CAN Receive Data

8.8 - SD Card Socket

The full sized SD Card socket on the Baseboard is connected directly to the MCU via the Renesas RZ/A1H's built-in SD Card controller, channel 0:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P4.13	SD_CMD_0	P4_13/SD_CMD	98	RZM-SD_CMD	SD Command/Response
P4.12	SD_CLK_0	P4_12/SD_CLK	96	RZM-SD_CLK	SD Clock
P4.8	SD_CD_0	P4_8/SD_CD	115	RZM-SD_CD	SD Card Detect (active low, pulled high)
P4.9	SD_WP_0	P4_9/SD_WP	84	RZM-SD_WP	SD Write Protect (active low, pulled high)
P4.11	SD_D0_0	P4_11/SD_D0	119	RZM-SD_D0	SD Data Bus D0 (LSB)
P4.10	SD_D1_0	P4_10/SD_D1	92	RZM-SD_D1	SD Data Bus D1
P4.15	SD_D2_0	P4_15/SD_D2	106	RZM-SD_D2	SD Data Bus D2
P4.14	SD_D3_0	P4_14/SD_D3	123	RZM-SD_D3	SD Data Bus D3 (MSB)

With 8.16 - DIP Switch S1 set in the correct position, and an SD Card correctly formatted inserted in the SD Card socket, the YLCDRZA1H is capable of booting directly from this device.

8.9 - USB Host and Device

The Renesas RZ/A1H MCU features independent USB 2.0 host and USB 2.0 device (or "function") ports, both capable of 480mbps data rates.

The USB Device port is exposed via a standard USB Micro B connector on the YLCDRZA1H Baseboard and is connected to the MCU as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
VBUSIN1		VBUSIN1	41	RZM-USBF_VBUS	USB Device ("Function") VBUS Detect
DP_0		USBF_P	37	RZM-USBF_P	USB Device ("Function") D+
DP_1		USBF_N	35	RZM-USBF_N	USB Device ("Function") D-

The USB host port is exposed via a standard USB A connector on the YLCDRZA1H Baseboard, and is current limited to 150mA to prevent inappropriately large current devices from affecting the operation of the YLCDRZA1H system. See Chapter 5.5 - USB Host Power Subsystem for more information. The port is connected to the MCU as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P1.6	[1]see note	[1]P1_6-USBH_5V_EN#	132	RZM-USBH_5V_EN#	USB Host VBUS Power Out Enable (active low)
				USBH_5V	USB Host VBUS Power Out
VBUSIN0		VBUSIN0	43	RZM-USBH_VBUS	USB Host VBUS Detect
P1.12	TINT20/GPI	P1_12/TINT20-USBH_OC	56	RZM_USBH_OC#	USB Host VBUS Overcurrent Detect (active low)
DP_1		USBH_P	47	RZM-USBH_P	USB Host D+
DM_1		USBH_N	49	RZM-USBH_N	USB Host D-

[1]on v2.0 units, P1.6 was incorrectly used to drive the USB Host Power Enable (RZM-USBH_5V_EN on the RZ Module; DIMM pin 132). This port is open drain only on the MCU, and is incapable of driving high and enabling the power supply. All v2.0 units should include a post-production modification connecting U21 pin 7 (ENUSB) to U21 pin 8 (FAULT#) to enable the USB supply during all non-overcurrent situations. Version 2.1 units have an inverter with input pull-up added to this path. In this configuration, the RESET# condition disables the USB Host Power Enable, and asserting P1_6 low enables the USB Host Power.

8.10 - Battery Backed Real Time Clock Calendar (RTCC)

The Renesas RZ/A1H MCU has a built-in Real Time Clock Calendar (RTCC), and the RZ Module provides a 32.768 kHz dedicated crystal to enable precise timekeeping while power is connected. Often network connected , systems can fetch the current time from the network on boot and program the MCU's RTCC to the correct time, which will be maintained for the duration of the powered session.

The Baseboard adds an extra feature: a separate lithium coin-cell backed I2C RTCC subsystem. The NXP PCF8523 RTCC requires less than a few hundred nano Amperes to operate and the small CR1025 3V 30mAH coin cell can keep the RTCC running for several years without replacement.

When replacing the battery, ensure correct orientation: the flat side (+) should be up and away from the PCB surface, and the rounded side (-) should be contacting the PCB surface.

The NXP RTCC is an I2C controlled device, appearing on I2C Bus 0 at 7-bit I2C address 0x68:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x68	0xD1	0xD0	0	1000	Baseboard	PCF8523 Real Time Clock Calendar

Chapter 10 – I2C Device Summary lists all the I2C devices on the YLCRZA1H.

YLCDRZA1H v2.1 Baseboards have an additional R/C circuit on the main power input as recommended by NXP to improve battery to main power switchover.

8.11 - PMOD Port

The YLCDRZA1H has one Digilent PMOD™ compatible 2x6 host port. It supports, depending on MCU configuration and software, one of these standard PMOD configurations:

- Type 1 - GPIO
- Type 2 - SPI
- Type 2A - Expanded SPI
- Type 4 - UART without CTS/RTS flow control
- Type 4A - Expanded UART without CTS/RTS flow control

For information on the PMOD convention, see the Digilent website, or read the PMOD standard.

The PMOD port on the YLCDRZA1H also has some non-standard and unique features you can exploit with custom cards. Normally with PMOD mode 2/2A/4/4A support, you choose SPI or UART mode. The YLCDRZA1H's PMOD offers the following choices:

- SPI (standard pin-out mode 2/2A)
- UART (standard pin-out mode 4/4A)
- UART + CAN (both non-standard pin-out)
- UART + UART (one UART standard pin-out, one non-standard)

These ports do not have transceivers, are in addition and separate from the Industrial Networking: CAN, RS232, RS485 ports which have full transceivers on the Baseboard.

With custom PMOD-like cards, or a simple wire harness from the YLCDRZA1H's PMOD connector, you can access this additional functionality. Contact Renesas for information about any example cards available.

Pay special attention to the pin order of the PMOD connectors: it is not the zigzag numbering convention normally used for headers. Incorrectly wiring to the PMOD connectors may damage your YLCDRZA1H or even other connected equipment.

The PMOD signals are 3.3V only. Do not connect 5V or higher signals, for example full-level RS232 signals, to this port directly. If, for example, a full-level RS232 port is desired the Digilent PMOD RS232X plugs into the connector and translates these voltages.

The PMOD connector signals are connected throughout the YLCDRZA1H as follows; the PMOD pin numbers are per the PMOD (non-zigzag) specification:

MCU		Schematic			PMOD	Operation
Port	Function	Module	#	Baseboard	Pin	
				+3V3	12	+3.3V to PMOD
				GND	11	System GND
					10	NC
					9	NC
P3.7	GPIO	P3_7-PMOD_RST#	30	RZM-PMOD_RST#	8	PMOD Reset Out (active low)
P1.11	TINT19/GPIO	P1_11/TINT19-PMOD_IRQ	57	RZM-PMOD_IRQ	7	PMOD connector IRQ or GPIO
P8.14	GPIO/RXPCK2/TxD4	P8_14/RSPCK2	22	RZM_RSPCK2	4	PMOD SPI Clock or UART Tx
P9.1 P8.9	GPIO/MISO2/CAN0RX GPIO/RXD3/SPDIF_OUT	P9_1/MISO2-P8_9/RXD3	26	RZM_PMOD_RX	3	PMOD SPI Master In/Slave Out or CAN RX PMOD UART RxD or SPDIF OUT
P9.0 P8.8	GPIO/MOSI2/CAN0TX GPIO/TXD3/SPDIF_IN	P9_0/MOSI2-P8_8/TXD3	24	RZM_PMOD_TX	2	PMOD SPI Master Out/Slave In or CAN Tx PMOD UART TxD or SPDIF IN
P8.15	GPIO/SSL20/RxD4	P8_15/SSL20	20	RZM_SSL20	1	PMOD SPI Slave Select or UART Rx

Note how two pairs of MCU pins are joined and overlaid on the PMOD connector. This enables both the standard UART and SPI modes as well as other possibilities, including CAN, SPDIF, and a second UART.

Only enable one function per joined signal (e.g. P9.1 & P8.9) on the MCU to be an output to avoid damaging the MCU.

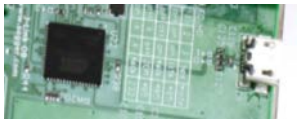
This table summarizes the configuration of the MCU pins for the various standard PMOD modes:

MCU Port	PMOD Pin	Standard PMOD Configuration for Mode				
		1A GPIO	4A UART	4B XUART	2A SPI	2B XSPI
P3.7	8	GPIO		GPO		GPO
P1.11	7	GPIO/TINT19		TINT19		TINT19
P8.14	4	GPIO	GPO/RTS#	GPO/RTS#	RXPCK2	RXPCK2
P9.1	3	GPIO			MISO2	MISO2
P8.9		GPIO	RxD3	RxD3		
P9.0	2	GPIO			MOSI2	MOSI2
P8.8		GPIO	TxD3	TxD3		
P8.15	1	GPIO	GPI/CTS#	GPI/CTS#	SSL20/GPO	SSL20/GPIO

This table summarizes the configuration of the MCU pins for the various non-standard PMOD modes:

MCU Port	PMOD Pin	Non-Standard PMOD Configuration for Mode					
		CAN GPIO	CAN UART	UART GPIO	UART UART	SPDIF GPIO	UART SPDIF
P3.7	8	GPIO/TINT47	GPIO/TINT47	GPIO/TINT47	GPIO/TINT47	GPIO/TINT47	GPIO/TINT47
P1.11	7	GPIO/TINT19	GPIO/TINT19	GPIO/TINT19	GPIO/TINT19	GPIO/TINT19	GPIO/TINT19
P8.14	4	TxD4	TxD4	TxD4	TxD4		TxD4
P9.1	3	CAN0RX	CAN0RX	GPIO/TINT132			
P8.9					RxD3	SPDIF_OUT	SPDIF_OUT
P9.0	2	CAN0TX	CAN0TX	GPIO/TINT131			
P8.8					TxD3	SPDIF_IN	SPDIF_IN
P8.15	1	RxD4	RxD4	TxD4	TxD4		TxD4

8.12 - Segger J-Link On-Board Debugger/Programmer



The YLCDRZA1H Baseboard includes a Segger J-Link On-Board debugger/programmer to enable easy and effective software development without the need for an external programmer/debugger. The USB Micro connector near the barrel power jack is the PC's connection point for this debugger – see Chapter 3 – Getting Started, Section 3.3 - Connecting to the Segger J-Link On-Board Debugger. The debugger is connected directly to the MCU:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
JP0_1	TDO	TDO	81	RZM-TDO	JTAG test data out
TCK	TCK	TCK	85	RZM-TCK	JTAG test clock
JP0_0	TDI	TDI	79	RZM-TDI	JTAG test data In
TMS	TMS	TMS	83	RZM-TMS	JTAG test mode select
TRST	TRST	TRST#	77	RZM-TRST#	JTAG test reset (active low)
RES	RES	RESET#	27	RZM-RESET#	System Reset (open drain, active low) Also RESET Pushbutton S3 on Baseboard

Details of this circuit are the proprietary and confidential property of SEGGER Microcontroller GmbH & Co. KG, and can only be implemented under license from Segger; contact Segger for details.

The Baseboard's LED2 green element is controlled directly by the Segger J-Link On-Board and flashes to indicate activity on the debugger.

8.13 - Ambient Light Sensor

In low-light conditions, the LCD can be so bright it can visually "bloom" and difficult to read. As in mobile phones and tablets, the YLCDRZA1H includes a forward-facing through-glass ambient light sensor, enabling software to monitor the ambient light conditions and dynamically adjust the LCD backlight intensity.

The Avago APDS-9002-021 Ambient Light Sensor (ALS) is a simple device that outputs a current proportional to the ambient light conditions. Through a resistor, this appears as a voltage between 0 and 3.3V on an Analog to Digital Converter (ADC) input on the MCU. Software can poll this ADC periodically. The ALS is connected as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P1.8	AN0	P1_8/AN0_ALS	53	RZM-AN0_ALS	Ambient light sensor analog input

8.14 - Digital Video Camera

A forward-facing VGA (640x480) color digital video camera module based on the popular OmniVision OV7670 smart sensor is included in the YLCDRZA1H.

The video data is moved over a dedicated high speed parallel video data channel. Operation and features of the camera are controlled over I2C.

The camera module is connected as follows:

MCU		Schematic			Operation
Port	Function	Module	DIMM	Baseboard	
P10.0	VIO_CLK	P10_0/VIO_CLK	32	RZM-VIO_CLK	Camera CLK
P10.1	VIO_VD	P10_1/VIO_VSYNC	19	RZM-VIO_VSYNC	Camera Vertical Sync
P10.2	VIO_HD	P10_2/VIO_HSYNC	17	RZM-VIO_HSYNC	Camera Horizontal Sync
P10.3	VIO_FLD	P10_3/VIO_FLD	38	RZM-VIO_FLD	Camera FLD
P10.4	VIO_D0	P10_4/VIO_D0	109	RZM-VIO_D0	Camera D0 (LSB)
P10.5	VIO_D1	P10_5/VIO_D1	107	RZM-VIO_D1	Camera D1
P10.6	VIO_D2	P10_6/VIO_D2	72	RZM-VIO_D2	Camera D2
P10.7	VIO_D3	P10_7/VIO_D3	76	RZM-VIO_D3	Camera D3
P10.8	VIO_D4	P10_8/VIO_D4	90	RZM-VIO_D4	Camera D4
P10.9	VIO_D5	P10_9/VIO_D5	127	RZM-VIO_D5	Camera D5
P10.10	VIO_D6	P10_10/VIO_D6	94	RZM-VIO_D6	Camera D6
P10.11	VIO_D7	P10_11/VIO_D7	117	RZM-VIO_D7	Camera D7 (MSB)
P1.0	P1.0/SCL0	P1_0/SCL0	126	RZM-SCL0	I2C0 Clock
P1.0	P1.1/SDA0	P1_1/SDA0	128	RZM-SDA0	I2C0 Data

The OV7670 I2C communication protocol is described in detail in the OmniVision Serial Camera Control Bus (SCCB) Functional Specification, and is present on I2C bus 0 at 7-bit address 0x21:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x21	0x43	0x42	0	400	Baseboard	OV7670 Camera Module

See Chapter 10 – I2C Device Summary for a complete list of I2C Devices on the YLCDRZA1H.

8.15 - Switches

The baseboard has two pushbuttons and two 4-position DIP switches for selecting YLCDRZA1H features:

Switch	Type	Purpose
S1	4 Switch DIP Slide	MCU Boot Mode and Spread Spectrum Clocking
S2	NOMC SPST Pushbutton	User Input
S3	NOMC SPST Pushbutton	System Reset when pressed
S4	4 Switch DIP Slide	RS232/485 Transceiver Options

DIP Switch S1 controls the MCU boot modes and spread spectrum clocking. See Chapter 7.3 - MCU Boot Mode Selection and Chapter 7.6 - On-Module Clocking.

DIP Switch S4 controls various RS232/485 transceiver capabilities: See Chapter 8.7 - Industrial Networking: CAN, RS232, RS485.

S2 is a simple GPIO/Interrupt input into the MCU, and can be used by software for any user-input purpose. S3 is connected to the system RESET# line, debounced and managed on the RZ Module as described in 7.2 - System Reset. They are connected as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P7.8	GPI/IRQ1	P7_8/IRQ1	195	RZM-P7_8/IRQ1	Baseboard Pushbutton S2 (active low w/ IRQ)
RES	RES	RESET#	27	RZM-RESET#	System Reset (open drain, active low) Also RESET Pushbutton S3 on Baseboard

8.16 - LEDs

The Baseboard has two tri-color LEDs (red, green, orange=red+green):

LED	Green	Red
LED1	Software P3.9 (active high)	Software P3.8 (active high)
LED2	Segger J-Link Activity	Baseboard Power Present

LED1 is connected as follows:

MCU		Schematic			Operation
Port	Function	Module	DIMM	Baseboard	
P3.8	P3.8	P3_8-RZM_LED_RED	71	RZM-LED_RED	Baseboard LED1 Red element (active high)
P3.9	P3.9	P3_9-RZM_LED_GRN	65	RZM-LED_GRN	Baseboard LED1 Green element (active high)

8.17 - CryptoAuthentication

The YLCDRZA1H Baseboard includes an Atmel ATSHA204A CryptoAuthentication Chip, which includes 4.5kbit EEPROM and a Random Number Generator (RNG).

The encryption key OTP area within the 4.5kbit EEPROM is pre-programmed by Serious Integrated Inc. for support of the Serious Human Interface™ Platform (SHIP) and is unavailable for other uses. Modifying or writing to this area will permanently remove your ability to use SHIP on the YLCDRZA1H.

The chip appears on I2C bus 0 at 7-bit address 0x64:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x64	0xC9	0xC8	0	1000	Baseboard	ATSHA204A Crypto + RNG + EEPROM

Consult the Atmel ATSHA204 Data Sheet for programming and hardware information of the ATSHA204 device.

Chapter 9 – External Interrupt Summary

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
	IRQ0				
P7.8	IRQ1/GPIO	P7_8/IRQ1	195	RZM-P7_8/IRQ1	Baseboard Pushbutton S2 (active low w/IRQ)
	IRQ2				
P1.9	IRQ3	P1_9_IRQ-AUDIO_IRQ	63	RZM-AUDIO_IRQ	Audio System
P1.10	IRQ4	P1_10/IRQ4-TOUCH_IRQ	52	RZM-TOUCH_IRQ	LCD Touch controller
P1.5	IRQ5	P1_5/IRQ5-ET_IRQ	171	RZM-ET_IRQ	Ethernet PHY (WOL)
	IRQ6				
	IRQ7				
P1.11	TINT19/GPIO	P1_11/TINT19-PMOD_IRQ	57	RZM-PMOD_IRQ	PMOD connector IRQ or GPIO
P1.12	TINT20/GPI	P1_12/TINT20-USBH_OC	56	RZM-USBH_OC#	USB host overcurrent

Chapter 10 – I2C Device Summary

The two I2C interfaces on the YLCDRZA1H are as follows:

MCU		Schematic			Operation
Port	Function	Module	DIMM	Baseboard	
P1.0	SCL0	P1_0/SCL0	126	RZM-SCL0	I2C0 Clock
P1.1	SDA0	P1_1/SDA0	128	RZM-SDA0	I2C0 Data
P1.2	P1.2/SCL1	P1_2/SCL1	165	RZM-SCL1	I2C1 Clock (Touch dedicated)
P1.3	P1.3/SDA1	P1_3/SDA1	169	RZM-SDA1	I2C1 Data (Touch dedicated)

The devices on these channels are as follows:

Address			I2C	Max	Location	Device
7-bit	Read	Write	Bus	kHz		
0x10	0x21	0x20	0	400	Baseboard	MAX98089ETN+ Audio Codec/Amplifier
0x21	0x43	0x42	0	400	Baseboard	OV7670 Camera Module
0x50	0xA1	0xA0	0	400	Baseboard	24AA02E48T EEPROM/MAC Address
0x57	0xAD	0xAC	0	400	Module	CAT34C02 EEPROM
0x60	0xC1	0xC0	0	400	Module	Si5351C Clock Synthesizer
0x64	0xC9	0xC8	0	1000	Baseboard	ATSHA204A Crypto + RNG + EEPROM
0x68	0xD1	0xD0	0	1000	Baseboard	PCF8523 Real Time Clock Calendar
0x5C	0xB9	0xB8	1	400	LCD	Pixcir C48 Capacitive Touch Controller

Chapter 11 – SPI Device Summary

The SPI interfaces on the YLCDRZA1H are as follows:

MCU		Schematic			Operation
Port	Function	Module	#	Baseboard	
P9.2	SPBCLK0	P9_2/SPBCLK0	166	RZM-SPBCLK0	XIP/Boot Serial FLASH Clock
P9.3	SPBSSL0	P9_3/SPBSSL0	174	RZM-SPBSSL0	XIP/Boot Serial FLASH SSL#
P9.4	SPBIO00	P9_4/SPBIO00	178	RZM-SPBIO00	XIP Lo/Boot Serial FLASH Data 0/MOSI
P9.5	SPBIO10	P9_5/SPBIO10	173	RZM-SPBIO10	XIP Lo/Boot Serial FLASH Data 1/MISO
P9.6	SPBIO20	P9_6/SPBIO20			XIP Lo/Boot Serial FLASH Data 2
P9.7	SPBIO30	P9_7/SPBIO30			XIP Lo/Boot Serial FLASH Data 3
P2.12	SPBIO01	P2_12/SPBIO01	178	RZM-SPBIO01	XIP Hi Serial FLASH Data 0
P2.13	SPBIO11	P2_13/SPBIO11	173	RZM-SPBIO11	XIP Hi XIP Serial FLASH Data 1
P2.14	SPBIO21	P2_14/SPBIO21			XIP Hi XIP Serial FLASH Data 2
P2.15	SPBIO31	P2_15/SPBIO31			XIP Hi XIP Serial FLASH Data 3

The devices on these interfaces are:

Slave Select	SPI Bus	Max MHz	Location	Device
P9_3/SPBSSL0	0		Module	Both Serial FLASH Devices

Chapter 12 - Schematics & Bills of Materials

12.1 - SO-DIMM Detail

The SO-DIMM socket on the YLCDRZA1H Baseboard is an inexpensive and readily-available TE 1473005-4 200Pos 0.6mm pitch socket. Designers can make their own baseboards and reuse the RZ Module as a time-to-prototype vehicle. The DIMM socket has the following pin-out:

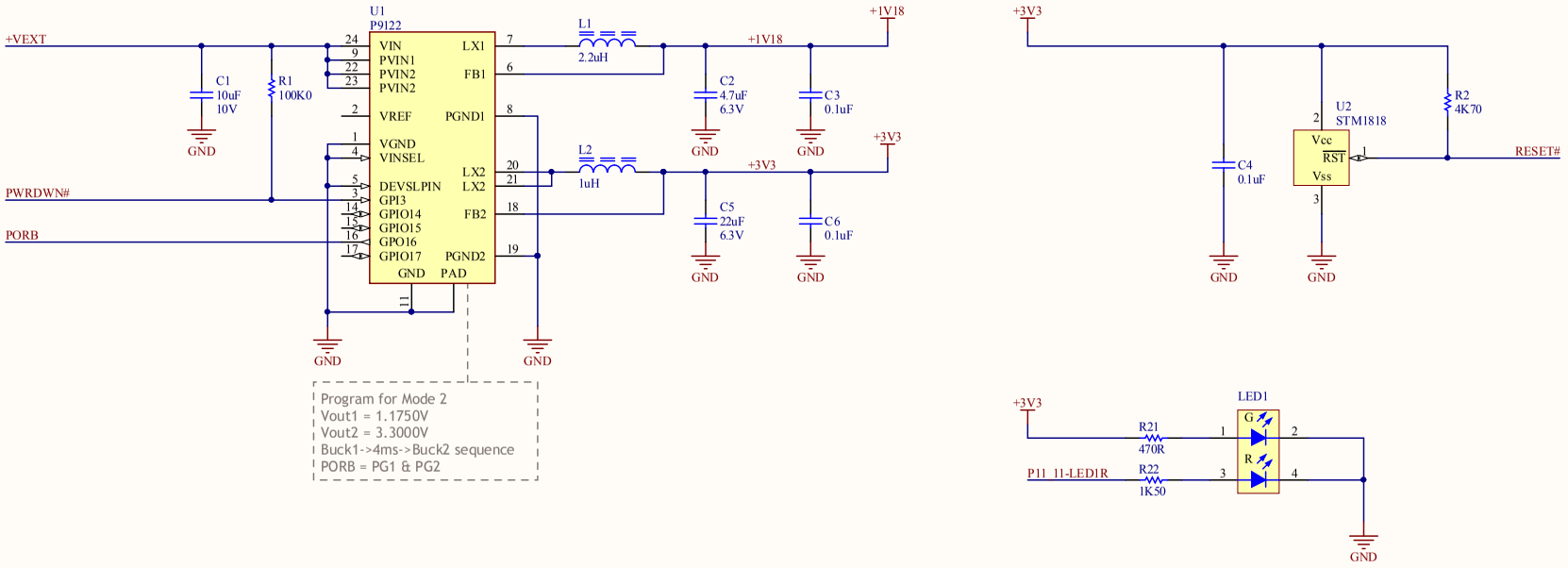
	MCU	Schematic			Operation
Port	Function	Module	#	Baseboard	
		GND	1	GND	System Ground
		+5V	2	+5V	System +5V Main Supply
P11.8	LCD0_TCON6	P11_8/LCD_DEN	3	RZM-LCD_DEN	LCD Data Enable
P11.7	LCD_DATA0	P11_7/LCD_DATA0	4	RZM-LCD_DATA0	LCD Blue 0 (LSB)
P11.9	LCD0_TCON5	P11_9/LCD_VSYNC	5	RZM-LCD_VSYNC	LCD Vertical Sync
P11.6	LCD_DATA1	P11_6/LCD_DATA1	6	RZM-LCD_DATA1	LCD Blue 1
P8.13	GPIO	P8_13-TOUCH_RST#	7	RZM-TOUCH_RST#	LCD Touch controller reset (active low)
P11.10	LCD0_TCON4	P11_10/LCD_HSYNC	8	RZM-LCD_HSYNC	LCD Horizontal Sync
P8.11	GPO	P8_11/RS_ON	9	RZM-RS_ON	RSXXX Transceiver Enable (active high)
	CKIO	CKIO	10	RZM-CKIO	MCU System Clock Out (unused on Baseboard)
P8.10	GPO	P8_10/RS_DEN	11	RZM-RS_DEN	RSXXX Transmit Drive Enable (active high)
P8.8	GPIO/TXD3/SPDIF_IN	P9_0/MOSI2-P8_8/TXD3	12	RZM_PMOD_TX	PMOD UART TxD or SPDIF IN
		GND	13	GND	System Ground
		+5V	14	+5V	System +5V Main Supply
P3.2	RxD2	P3_2/UART_RX	15	RZM-UART_RX	RSXXX Receive Data
P8.9	GPIO/RXD3/SPDIF_OUT	P9_1/MISO2-P8_9/RXD3	16	RZM_PMOD_RX	PMOD UART RxD or SPDIF OUT
P10.2	VIO_HD	P10_2/VIO_HSYNC	17	RZM-VIO_HSYNC	Camera Horizontal Sync
P8.12	PWM1E	P8_12/PWM1E-BLEN	18	RZM-BLEN	LCD Backlight Enable (active high)
P10.1	VIO_VD	P10_1/VIO_VSYNC	19	RZM-VIO_VSYNC	Camera Vertical Sync
P8.15	GPIO/SSL20/RxD4	P8_15/SSL20	20	RZM_SSL20	PMOD SPI Slave Select or UART Rx
P3.3	MDIO	P3_3/ET_MDIO	21	RZM-ET_MDIO	MII Management data I/O
P8.14	GPIO/RXPCK2/TxD4	P8_14/RSPCK2	22	RZM_RSPCK2	PMOD SPI Clock or UART Tx
P3.0	LCD0_CLK	P3_0/LCD_CLK	23	RZM-LCD_CLK	Dot Clock
P9.0	GPIO/MOSI2/CAN0TX	P9_0/MOSI2-P8_8/TXD3	24	RZM_PMOD_TX	PMOD SPI Master Out/Slave In or CAN Tx
P3.1	TxD2	P3_1/UART_TX	25	RZM_UART_TX	RSXXX Transmit Data
P9.1	GPIO/MISO2/CAN0RX	P9_1/MISO2-P8_9/RXD3	26	RZM_PMOD_RX	PMOD SPI Master In/Slave Out or CAN RX
	RES	RESET#	27	RZM-RESET#	System Reset (open drain, active low) Also RESET Pushbutton S3 on Baseboard
P3.6	RXDV	P3_6/ET_RXDV	28	RZM-ET_RXDV	MII Receive data valid
P0.5	GPO	P0_5-ET_RESET#	29	RZM-ET_RESET#	MII PHY Reset (active low)
P3.7	GPIO	P3_7-PMOD_RST#	30	RZM-PMOD_RST#	PMOD Reset Out (active low)
P0.4	GPO	P0_4-MMC_RST#	31	RZM-MMC_RST	MMC Reset (active low with pull-up)
P10.0	VIO_CLK	P10_0/VIO_CLK	32	RZM-VIO_CLK	Camera CLK
		GND	33	GND	System Ground
		+5V	34	+5V	System +5V Main Supply
	DP_1	USBF_N	35	RZM-USBF_N	USB Device (“Function”) D-
P3.5	RXER	P3_5/ET_RXER	36	RZM-ET_RXER	MII Receive error
	DP_0	USBF_P	37	RZM-USBF_P	USB Device (“Function”) D+
P10.3	VIO_FLD	P10_3/VIO_FLD	38	RZM-VIO_FLD	Camera FLD
		GND	39	GND	System Ground
P3.4	RXCLK	P3_4/ET_RXCLK	40	RZM-ET_RXCLK	MII Receive Clock
	VBUSIN1	VBUSIN1	41	RZM-USBF_VBUS	USB Device (“Function”) VBUS Detect
		+3V3	42	RZM_3V3	+3.3V Module Supply Out (unconnected on Baseboard)
	VBUSIN0	VBUSIN0	43	RZM-USBH_VBUS	USBH Power Detection (active high)
			44		unconnected/reserved

MCU		Schematic			Operation
		GND	45	GND	System Ground
			46		unconnected/reserved
	DP_1	USBH_P	47	RZM-USBH_P	USB Host D+
		+5V	48	+5V	System +5V Main Supply
	DM_1	USBH_N	49	RZM-USBH_N	USB Host D-
			50		unconnected/reserved
		GND	51	GND	System Ground
P1.10	IRQ4	P1_10/IRQ4-TOUCH_IRQ	52	RZM-TOUCH_IRQ	LCD Touch controller interrupt
P1.8	AN0	P1_8/AN0_ALS	53	RZM-AN0_ALS	Ambient light sensor analog input
P1.15	GPIO	P1_15-LCD_ON	54	RZM-P1_15	(unused on Baseboard, input only signal)
P1.13	GPIO	P1_13-USBH_5V_EN	55	RZM-P1_13	(unused on Baseboard, input only signal)
P1.12	TINT20/GPIO	P1_12/TINT20-USBH_OC	56	RZM_USBH_OC#	USB Host VBUS Overcurrent Detect (active low)
P1.11	TINT19/GPIO	P1_11/TINT19-PMOD_IRQ	57	RZM-PMOD_IRQ	PMOD connector IRQ or GPIO
P1.14	COL	P1_14/ET_COL	58	RZM-ET_COL	MII Collision detection
		GND	59	GND	System Ground
		+5V	60	+5V	System +5V Main Supply
P0.1	MD_BOOT1	P0_1/MD_BOOT1	61	RZM-BOOT1	MCU Boot Mode
P1.9	IRQ3	P1_9/IRQ3-AUDIO_IRQ	63	RZM-AUDIO_IRQ	Audio Codec Interrupt
			62		unconnected/reserved
P1.9	IRQ3	P1_9_IRQ-AUDIO_IRQ	63	RZM-AUDIO_IRQ	Audio System
P3.14	MMC_D3	P3_14/MMC_D3	64	RZM-MMC_D3	e-MMC Data Bus D3
P3.9	P3.9	P3_9-RZM_LED_GRN	65	RZM-LED_GRN	Baseboard LED1 Green element (active high)
P4.1	LCD_DATA9	P4_1/LCD_DATA9	66	RZM-LCD_DATA9	LCD Green 1
		CLKAUDIO_24MHZ	67	RZM-AUDIO_CLK	24MHz Base Codec Clock from RZ Module
P4.2	LCD_DATA10	P4_2/LCD_DATA10	68	RZM-LCD_DATA10	LCD Green 2
			69		unconnected/reserved
P4.3	LCD_DATA11	P4_3/LCD_DATA11	70	RZM-LCD_DATA11	LCD Green 3
P3.8	P3.8	P3_8-RZM_LED_RED	71	RZM-LED_RED	Baseboard LED1 Red element (active high)
P3.8	P3.8	P3_8-RZM_LED_RED	71	RZM-LED_RED	Baseboard LED1 Red element (active high)
P10.6	VIO_D2	P10_6/VIO_D2	72	RZM-VIO_D2	Camera D2
			73		unconnected/reserved
		+5V	74	+5V	System +5V Main Supply
		GND	75	GND	System Ground
P10.7	VIO_D3	P10_7/VIO_D3	76	RZM-VIO_D3	Camera D3
	TRST	TRST#	77	RZM-TRST#	JTAG test reset (active low)
P4.5	LCD_DATA13	P4_5/LCD_DATA13	78	RZM-LCD_DATA13	LCD Green 5
JP0.0	TDI	TDI	79	RZM-TDI	JTAG test data In
P2.0	TXCLK	P2_0/ET_TXCLK	80	RZM-ET_TXCLK	Transmit Clock
JP0.1	TDO	TDO	81	RZM-TDO	JTAG test data out
P4.6	LCD_DATA14	P4_6/LCD_DATA14	82	RZM-LCD_DATA14	LCD Green 6
	TMS	TMS	83	RZM-TMS	JTAG test mode select
P4.9	SD_WP_0	P4_9/SD_WP	84	RZM-SD_WP	SD Write Protect (active low, pulled high)
	TCK	TCK	85	RZM-TCK	JTAG test clock
P2.1	P2.1/ET_TXER	P2_1/ET_TXER	86	RZM-ET_TXER	MII Transmit Error or GPIO (unused on Baseboard)
		GND	87	GND	System Ground
		+5V	88	+5V	System +5V Main Supply
P3.10	MMC_D1	P3_10/MMC_D1	89	RZM-MMC_D1	e-MMC Data Bus D1
P10.8	VIO_D4	P10_8/VIO_D4	90	RZM-VIO_D4	Camera D4
P3.12	MMC_CLK	P3_12/MMC_CLK	91	RZM-MMC_CLK	MMC clock
P4.10	SD_D1_0	P4_10/SD_D1	92	RZM-SD_D1	SD Data Bus D1
P3.11	MMC_D0	P3_11/MMC_D0	93	RZM-MMC_D0	e-MMC Data Bus D0 (LSB)
P10.10	VIO_D6	P10_10/VIO_D6	94	RZM-VIO_D6	Camera D6
		GND	95	GND	System Ground
P4.12	SD_CLK_0	P4_12/SD_CLK	96	RZM-SD_CLK	SD Clock
P3.13	MMC_CMD	P3_13/MMC_CMD	97	RZM-MMC_CMD	MMC Command/response

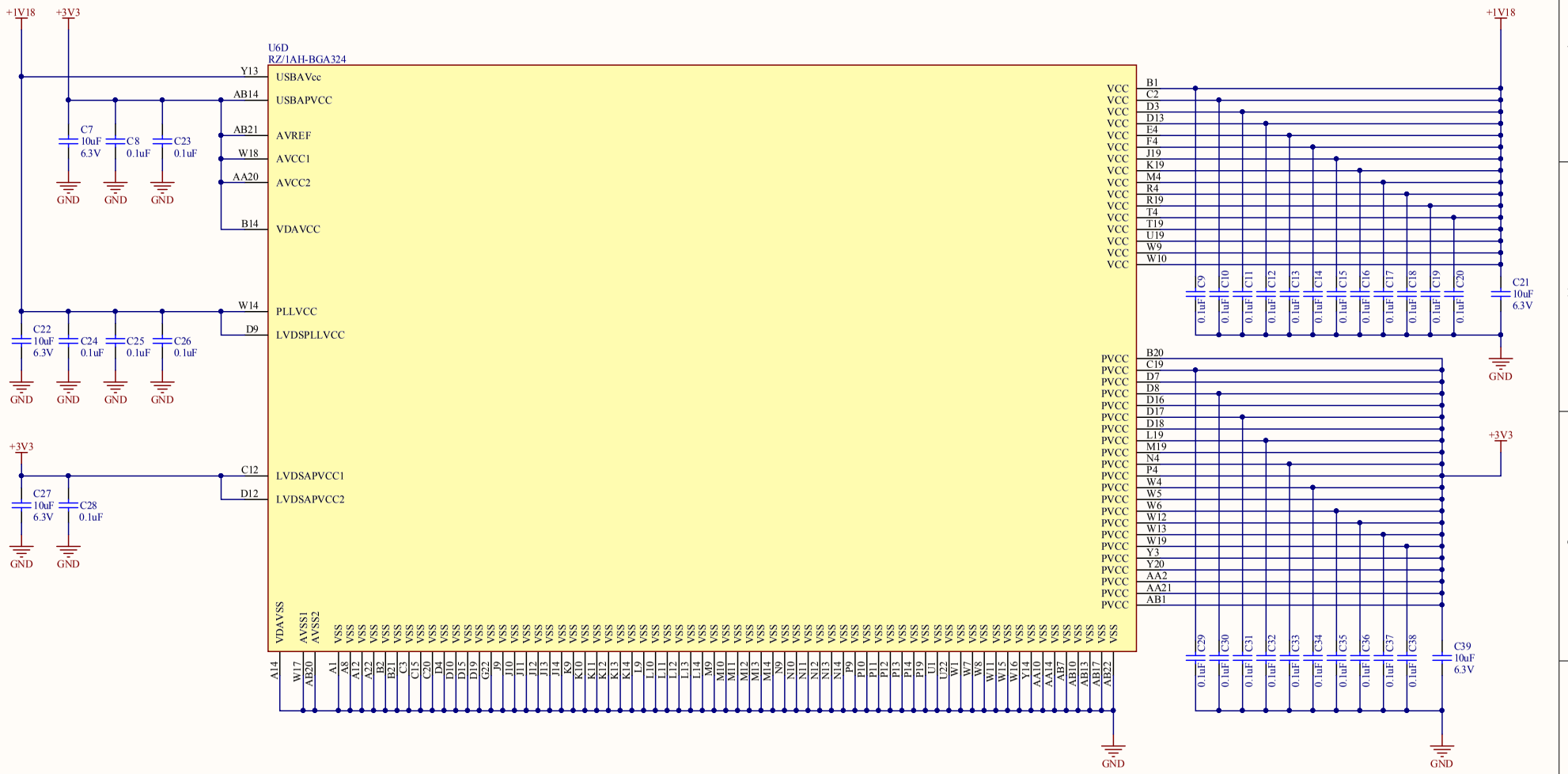
MCU		Schematic			Operation
P4.13	SD_CMD_0	P4_13/SD_CMD	98	RZM-SD_CMD	SD Command/Response
P3.15	MMC_D2	P3_15/MMC_D2	99	RZM-MMC_D2	e-MMC Data Bus D2
		+5V	100	+5V	System +5V Main Supply
		GND	101	GND	System Ground
		+5V	102	+5V	System +5V Main Supply
P4.0	LCD_DATA8	P4_0/LCD_DATA8	103	RZM-LCD_DATA8	LCD Green 0 (LSB)
P2.2	TXEN	P2_2/ET_TXEN	104	RZM-ET_TXEN	MII Transmit Enable
P4.4	LCD_DATA12	P4_4/LCD_DATA12	105	RZM-LCD_DATA12	LCD Green 4
P4.15	SD_D2_0	P4_15/SD_D2	106	RZM-SD_D2	SD Data Bus D2
P10.5	VIO_D1	P10_5/VIO_D1	107	RZM-VIO_D1	Camera D1
P10.12	SSICLK1	P10_12/SSISCK	108	RZM_SSISCK	Serial Sound Interface Clock
P10.4	VIO_D0	P10_4/VIO_D0	109	RZM-VIO_D0	Camera D0 (LSB)
P2.5	TXD[1]	P2_5/ET_TXD1	110	RZM-ET_TXD1	MII Transmit Data 1
P4.7	LCD_DATA15	P4_7/LCD_DATA15	111	RZM-LCD_DATA15	LCD Green 7 (MSB)
P10.15	SSITxD1	P10_15/SSITxD	112	RZM_SSITxD	Serial Sound Transmit Data (output)
		GND	113	GND	System Ground
		+5V	114	+5V	System +5V Main Supply
P4.8	SD_CD_0	P4_8/SD_CD	115	RZM-SD_CD	SD Card Detect (active low, pulled high)
P10.14	SSIRxD1	P10_14/SSIRxD	116	RZM_SSIRxD	Serial Sound Receive Data (input)
P10.11	VIO_D7	P10_11/VIO_D7	117	RZM-VIO_D7	Camera D7 (MSB)
P2.9	RXD[1]	P2_9/ET_RXD1	118	RZM-ET_RXD1	MII Receive Data 1
P4.11	SD_D0_0	P4_11/SD_D0	119	RZM-SD_D0	SD Data Bus D0 (LSB)
P2.7	TXD[3]	P2_7/ET_TXD3	120	RZM-ET_TXD3	MII Transmit Data 3 (MSB)
P2.3	CRS	P2_3/ET_CRS	121	RZM-ET_CRS	Carrier detection
P2.10	RXD[2]	P2_10/ET_RXD2	122	RZM-ET_RXD2	MII Receive Data 2
P4.14	SD_D3_0	P4_14/SD_D3	123	RZM-SD_D3	SD Data Bus D3 (MSB)
			124		unconnected/reserved
		GND	125	GND	System Ground
P1.0	SCL0	P1_0/SCL0	126	RZM-SCL0	I2C0 Clock
P10.9	VIO_D5	P10_9/VIO_D5	127	RZM-VIO_D5	Camera D5
P1.1	SDA0	P1_1/SDA0	128	RZM-SDA0	I2C0 Data
P2.4	TXD[0]	P2_4/ET_TXD0	129	RZM-ET_TXD0	MII Transmit Data 0 (LSB)
		+5V	130	+5V	System +5V Main Supply
P2.11	RXD[3]	P2_11/ET_RXD3	131	RZM-ET_RXD3	MII Receive Data 3 (MSB)
P1.6	P1.6/SCL3	P1_6/SCL3	132	RZM-USBH_5V_EN#	See 5.5 - USB Host Power Subsystem
P10.13	SSIWS1	P10_13/SSIWS	133	RZM_SSIWS	Serial Sound Word Select
P1.4	CAN1RX	P1_4/CAN1RX	134	RZM_CANRX	CAN Receive Data
P2.6	TXD[2]	P2_6/ET_TXD2	135	RZM-ET_TXD2	MII Transmit Data 2
P1.7	P1.7/SDA3	P1_7/SDA3	136	RZM-P1_7	(unused on Baseboard)
P2.8	RXD[0]	P2_8/ET_RXD0	137	RZM-ET_RXD0	MII Receive Data 0 (LSB)
		+5V	138	+5V	System +5V Main Supply
		GND	139	GND	System Ground
		GND	140	GND	System Ground
		GND	141	GND	System Ground
P5.0	LCD_DATA16	P5_0/LCD_DATA16	142	RZM-LCD_DATA16	LCD Red 0 (LSB)
		GND	143		System Ground
P5.1	LCD_DATA17	P5_1/LCD_DATA17	144	RZM-LCD_DATA17	LCD Red 1
		GND	145	GND	System Ground
		GND	146	GND	System Ground
		GND	147	GND	System Ground
P5.4	LCD_DATA20	P5_4/LCD_DATA20	148	RZM-LCD_DATA20	LCD Red 4
		GND	149	GND	System Ground
P5.5	LCD_DATA21	P5_5/LCD_DATA21	150	RZM-LCD_DATA21	LCD Red 5
		GND	151	GND	System Ground
		GND	152	GND	System Ground
		GND	153	GND	System Ground

MCU		Schematic			Operation
P5.2	LCD_DATA18	P5_2/LCD_DATA18	154	RZM-LCD_DATA18	LCD Red 2
		GND	155	GND	System Ground
P5.3	LCD_DATA19	P5_3/LCD_DATA19	156	RZM-LCD_DATA19	LCD Red 3
		GND	157	GND	System Ground
		GND	158	GND	System Ground
		GND	159	GND	System Ground
P5.6	LCD_DATA22	P5_6/LCD_DATA22	160	RZM-LCD_DATA22	LCD Red 6
		GND	161	GND	System Ground
P5.7	LCD_DATA23	P5_7/LCD_DATA23	162	RZM-LCD_DATA23	LCD Red 7 (MSB)
		GND	163	GND	System Ground
		GND	164	GND	System Ground
		P1_2/SCL1	165	RZM-SCL1	Touch dedicated I2C1 Clock
P9.2	SPBCLK0	P9_2/SPBCLK0	166	RZM-SPBCLK0	Serial FLASH Clock
		GND	167	GND	System Ground
P5.9	MDC	P5_9/ET_MDC	168	RZM-ET_MDC	Management data clock
		P1_3/SDA1	169	RZM-SDA1	Touch dedicated I2C1 Data
P5.10	CAN1TX	P5_10/CAN1TX	170	RZM-CANTX	CAN Transmit Data
P1.5	IRQ5	P1_5/IRQ5-ET_IRQ	171	RZM-ET_IRQ	PHY Interrupt (active low)
		GND	172	GND	System Ground
P9.5	SPBIO10	P9_5/SPBIO10	173	RZM-SPBIO10	Serial FLASH MISO
P9.3	SPBSSL0	P9_3/SPBSSL0	174	RZM-SPBSSL0	Serial FLASH SSL#
P11.1	LCD_DATA6	P11_1/LCD_DATA6	175	RZM-LCD_DATA6	LCD Blue 6
P0.3	MD_CLKS/GPIO	P0_3/MD_CLKS	176	RZM-SSCG	Enables Spread Spectrum Clocking in MCU by Baseboard S1.2 (ON/active GND,OFF pulled high (4.7kΩ) on RZ Baseboard)
P11.3	LCD_DATA4	P11_3/LCD_DATA4	177	RZM-LCD_DATA4	LCD Blue 4
P9.4	SPBIO00	P9_4/SPBIO00	178	RZM-SPBIO00	Serial FLASH MOSI
P7.0	MD_BOOT2	P7_0/MD_BOOT2	179	RZM-BOOT2	MCU Boot Mode
			180		unconnected/reserved
P11.7	LCD_DATA0	P11_7/LCD_DATA0	181	RZM-LCD_DATA7	LCD Blue 7 (MSB)
			182		unconnected/reserved
P11.2	LCD_DATA5	P11_2/LCD_DATA5	183	RZM-LCD_DATA5	LCD Blue 5
			184		unconnected/reserved
P11.14	MMC_D6	P11_14/MMC_D6	185	RZM-MMC_D6	e-MMC Data Bus D6
			186		unconnected/reserved
P11.12	MMC_D4	P11_12/MMC_D4	187	RZM-MMC_D4	e-MMC Data Bus D4
			188		unconnected/reserved
		GND	189	GND	System Ground
			190		unconnected/reserved
P11.13	MMC_D5	P11_13/MMC_D5	191	RZM-MMC_D5	e-MMC Data Bus D5
			192		unconnected/reserved
P11.15	MMC_D7	P11_15/MMC_D7	193	RZM-MMC_D7	e-MMC Data Bus D7 (MSB)
			194		unconnected/reserved
P7.8	P7.8/IRQ1	P7_8/IRQ1	195	RZM-P7_8/IRQ1	Baseboard Pushbutton S2 (active low w/IRQ)
			196		unconnected/reserved
P11.4	LCD_DATA3	P11_4/LCD_DATA3	197	RZM-LCD_DATA3	LCD Blue 3
			198		unconnected/reserved
P11.5	LCD_DATA2	P11_5/LCD_DATA2	199	RZM-LCD_DATA2	LCD Blue 2
		PWRDWN#	200	PWRDWN#	Power Down RZ Module (unconnected on Baseboard, active low)

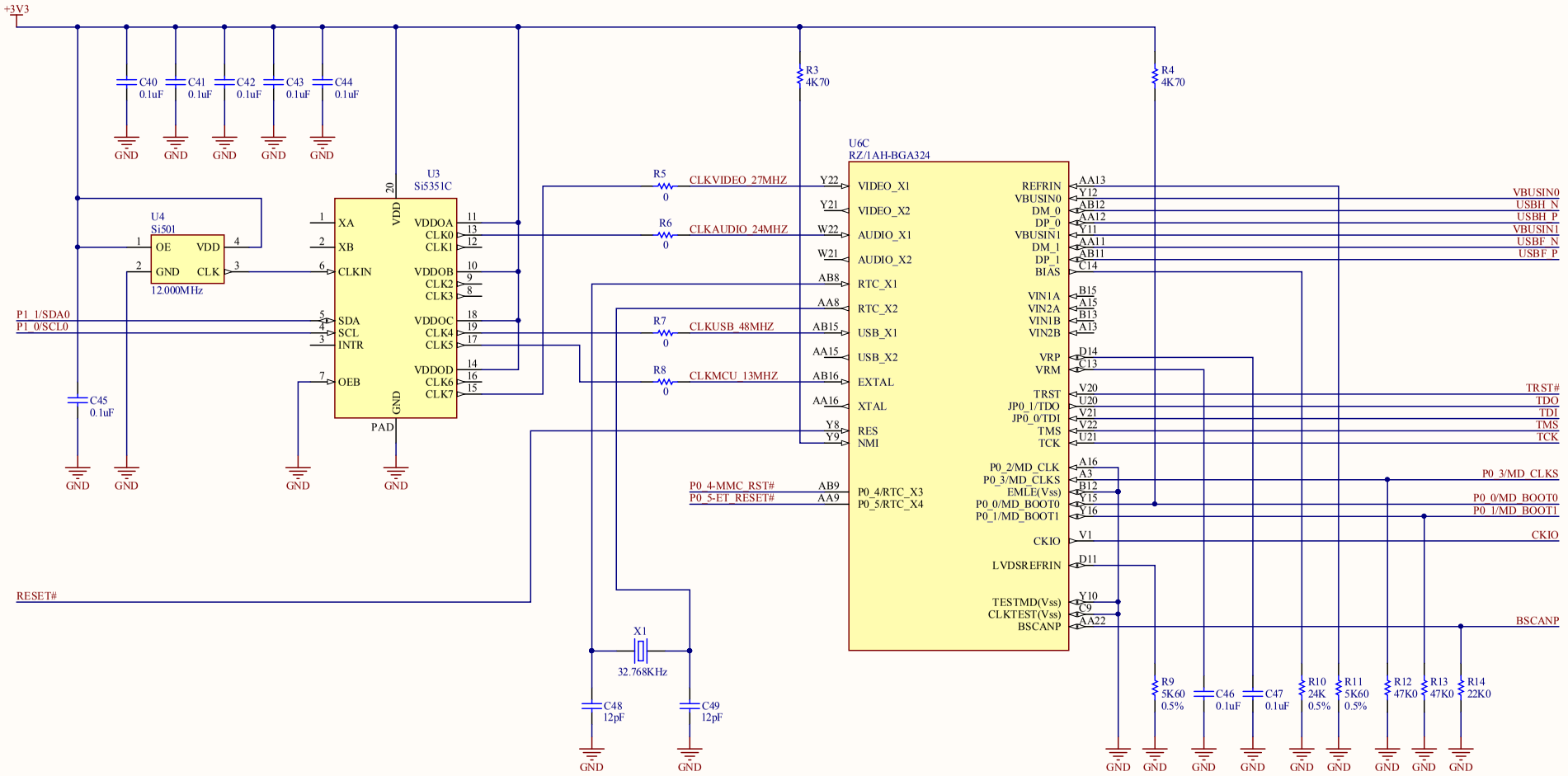
12.2 - RZ Module Schematics

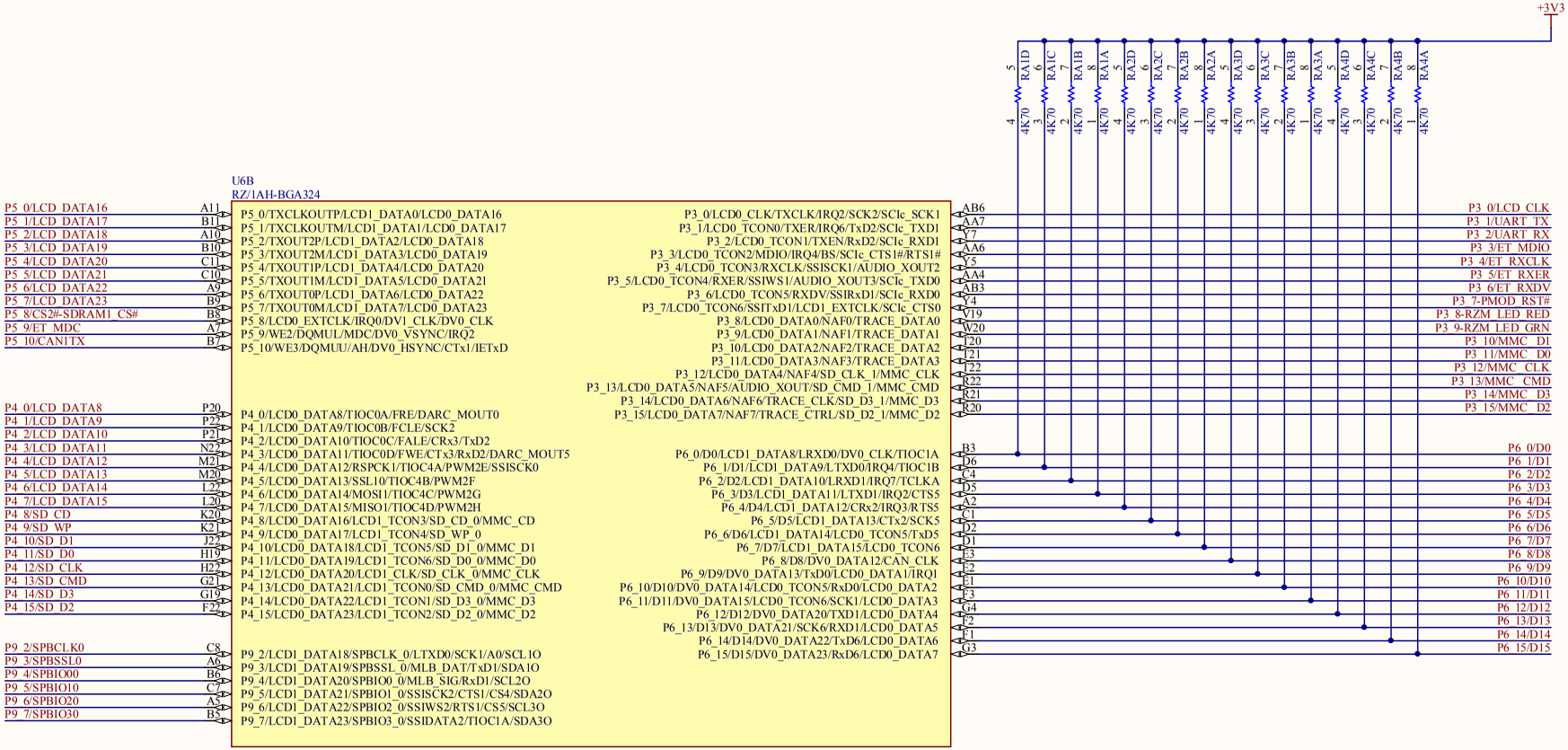


Renesas YLCDRZA1H MCU Module	
Power Supplies and User I/O	am.renesas.com/HiResGUI
Author: *Jorge Amodio*	Revision: v2.1 PCB02
Date: 4/15/2015	Sheet 1 of 8

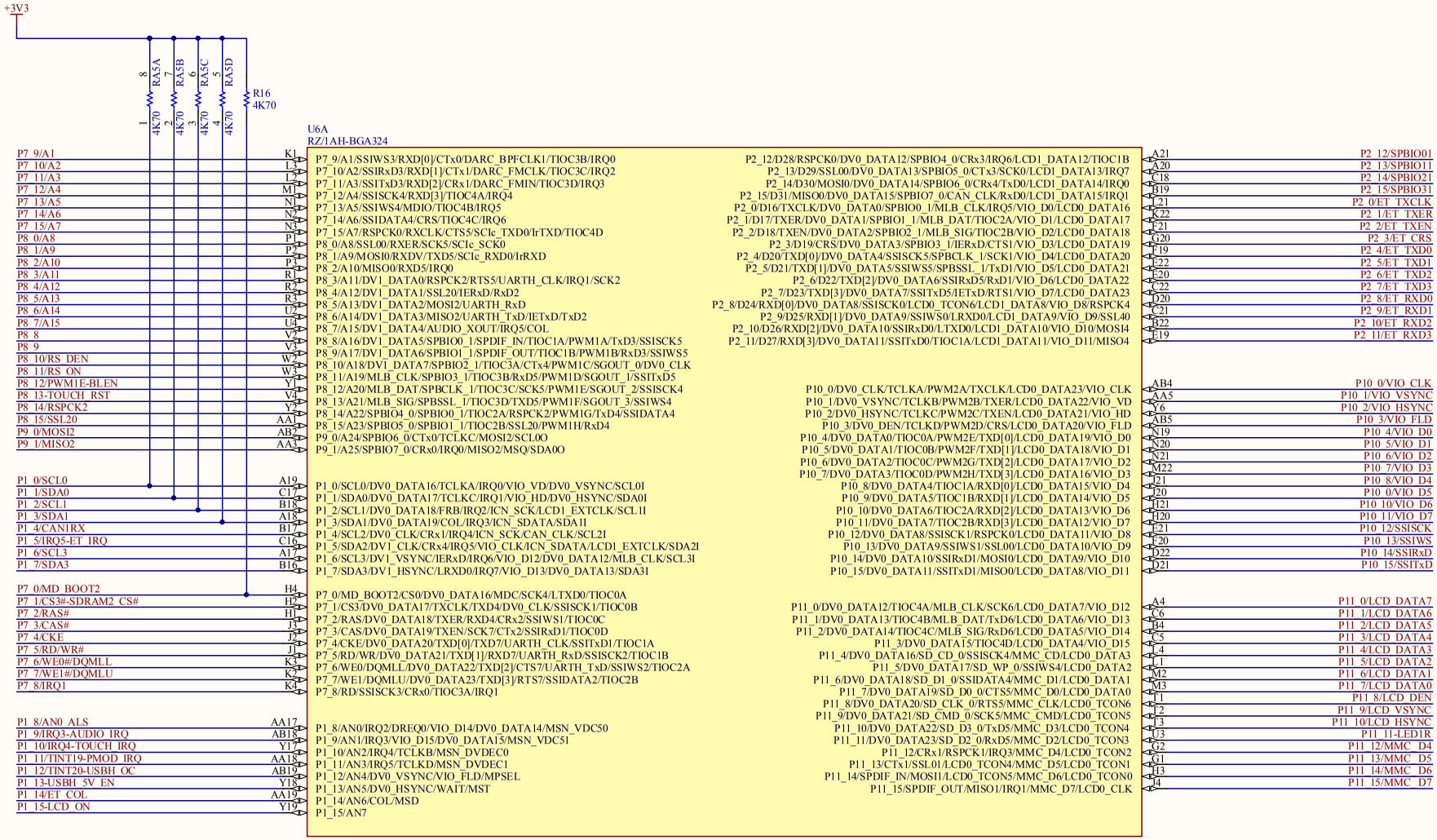


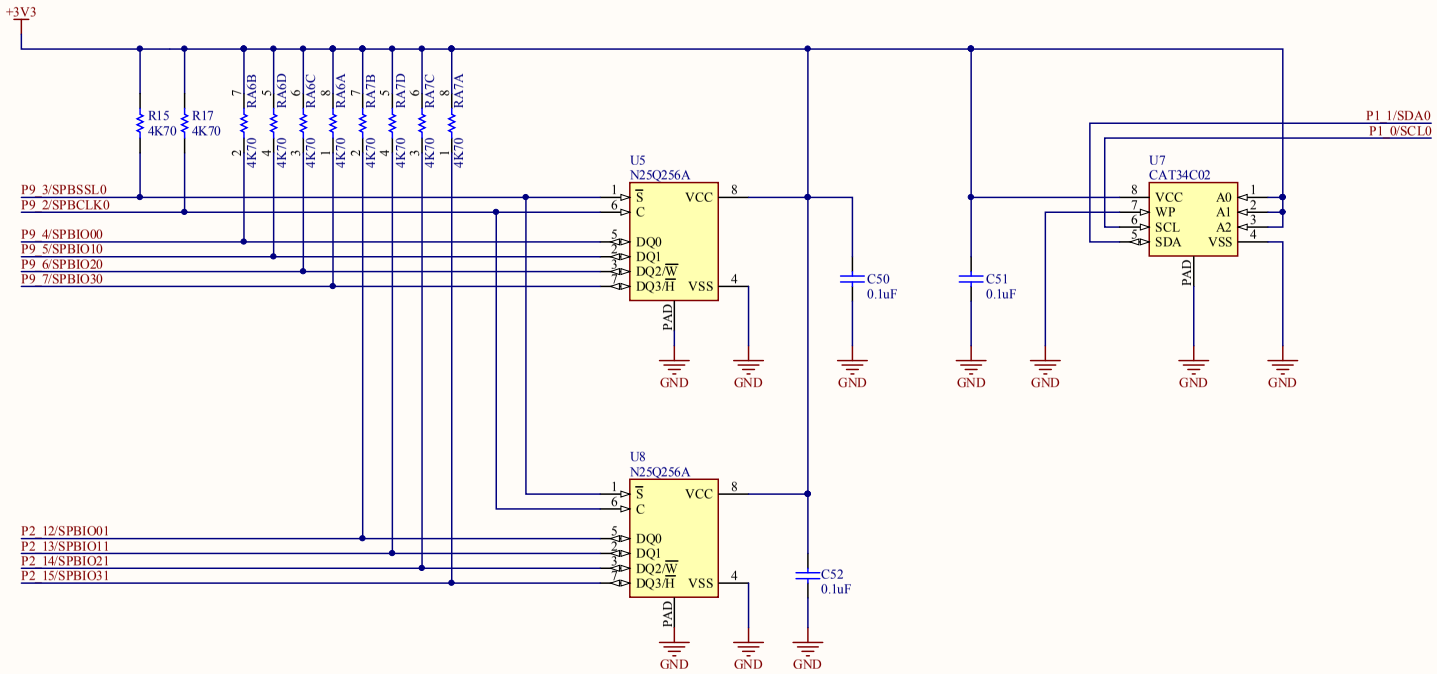
Renesas YLCDRZA1H MCU Module	am.renesas.com/HiResGUI
MCU Power	
Author: *Jorge Amodio*	Revision: v2.1 PCB02
Date: 4/15/2015	Sheet 2 of 8


+3V3
C40 0.1uF
C41 0.1uF
C42 0.1uF
C43 0.1uF
C44 0.1uF
GND
U3
Si5351C
U4
Si501
12.000MHz
C45 0.1uF
P1_1/SDA0
P1_0/SCL0
RESET#
R3 4K70
R4 4K70
R5 0
R6 0
R7 0
R8 0
CLKVIDEO_27MHZ
CLKAUDIO_24MHZ
CLKUSB_48MHZ
CLKMCU_13MHZ
U6C
RZ/1AH-BGA324
VIDEO_X1
VIDEO_X2
AUDIO_X1
AUDIO_X2
RTC_X1
RTC_X2
USB_X1
USB_X2
EXTAL
XTAL
RES
NMI
P0_4/RTC_X3
P0_5/RTC_X4
P0_4-MMC_RST#
P0_5-ET_RESET#
REFRIN
VBUSIN0
DM_0
DP_0
VBUSIN1
DM_1
DP_1
BIAS
VIN1A
VIN2A
VIN1B
VIN2B
VRP
VRM
TRST
JP0_1/TDO
JP0_0/TDI
TMS
TCK
P0_2/MD_CLK
P0_3/MD_CLKS
EMLE(Vss)
P0_0/MD_BOOT0
P0_1/MD_BOOT1
CKIO
LVDSREFRIN
TESTMD(Vss)
CLKTEST(Vss)
BSCANP
VBUSIN0
USBH_N
USBH_P
VBUSIN1
USBF_N
USBF_P
TRST#
TDO
TDI
TMS
TCK
P0_3/MD_CLKS
P0_0/MD_BOOT0
P0_1/MD_BOOT1
CKIO
BSCANP
X1
32.768KHz
C48 12pF
C49 12pF
R9 5K60 0.5%
C46 0.1uF
C47 0.1uF
R10 24K 0.5%
R11 5K60 0.5%
R12 47K0
R13 47K0
R14 22K0
Renesas YLCDRZA1H MCU Module
MCU Clocks & Control Signals
Author: Jorge Amodio
Date: 4/15/2015
Revision: v2.1 PCB02
Sheet 3 of 8
am.renesas.com/HiResGUI

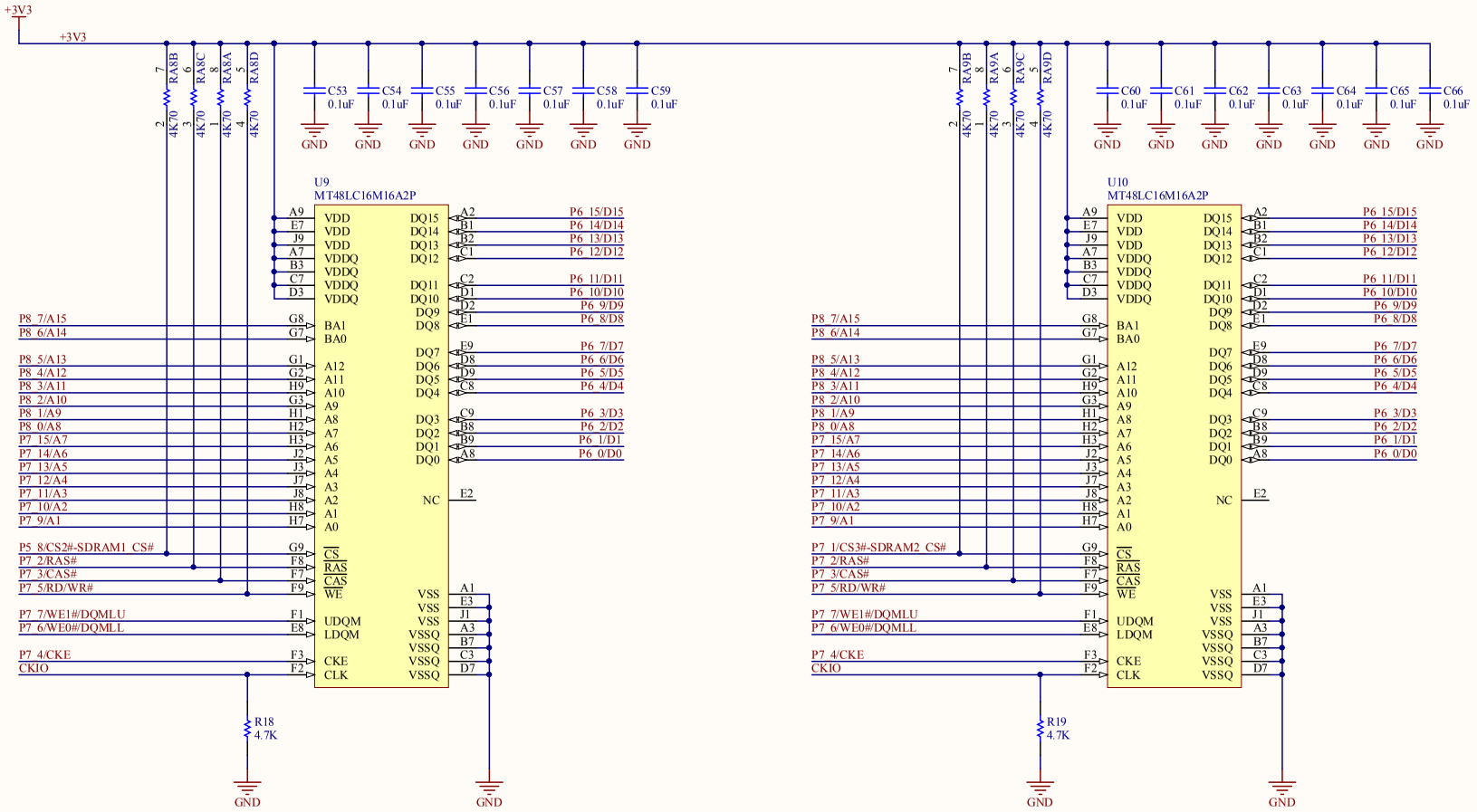


Renesas YLCDRZA1H MCU Module	am.renesas.com/HiResGUI
MCU Data/Address Bus, Serial & LCD Interfaces	
Author: *Jorge Amodio*	Revision: v2.1 PCB02
Date: 4/15/2015	Sheet 4 of 8


+3V3
RA5A
RA5B
RA5C
RA5D
R16
4K70
U6A
RZ/1AH-BGA324
P7_9/A1
P7_10/A2
P7_11/A3
P7_12/A4
P7_13/A5
P7_14/A6
P7_15/A7
P8_0/A8
P8_1/A9
P8_2/A10
P8_3/A11
P8_4/A12
P8_5/A13
P8_6/A14
P8_7/A15
P8_8
P8_9
P8_10/RS_DEN
P8_11/RS_ON
P8_12/PWM1E-BLEN
P8_13-TOUCH_RST
P8_14/RSPCK2
P8_15/SSL20
P9_0/MOSI2
P9_1/MISO2
P1_0/SCL0
P1_1/SDA0
P1_2/SCL1
P1_3/SDA1
P1_4/CAN1RX
P1_5/IRQ5-ET_IRQ
P1_6/SCL3
P1_7/SDA3
P7_0/MD_BOOT2
P7_1/CS3#-SDRAM2_CS#
P7_2/RAS#
P7_3/CAS#
P7_4/CKE
P7_5/RD/WR#
P7_6/WE0#/DQMLL
P7_7/WE1#/DQMLU
P7_8/IRQ1
P1_8/AN0_ALS
P1_9/IRQ3-AUDIO_IRQ
P1_10/IRQ4-TOUCH_IRQ
P1_11/TINT19-PMOD_IRQ
P1_12/TINT20-USBH_OC
P1_13-USBH_5V_EN
P1_14/ET_COL
P1_15-LCD_ON
P7_9/A1/SSIWS3/RXD[0]/CTx0/DARC_BPFCLK1/TIOC3B/IRQ0
P7_10/A2/SSIRxD3/RXD[1]/CTx1/DARC_FMCLK/TIOC3C/IRQ2
P7_11/A3/SSITxD3/RXD[2]/CRx1/DARC_FMIN/TIOC3D/IRQ3
P7_12/A4/SSISCK4/RXD[3]/TIOC4A/IRQ4
P7_13/A5/SSIWS4/MDIO/TIOC4B/IRQ5
P7_14/A6/SSIDATA4/CRS/TIOC4C/IRQ6
P7_15/A7/RSPCK0/RXCLK/CTS5/SCIc_TXD0/IrTXD/TIOC4D
P8_0/A8/SSL00/RXER/SCK5/SCIc_SCK0
P8_1/A9/MOSI0/RXDV/TXD5/SCIc_RXD0/IrRXD
P8_2/A10/MISO0/RXD5/IRQ0
P8_3/A11/DV1_DATA0/RSPCK2/RTS5/UARTH_CLK/IRQ1/SCK2
P8_4/A12/DV1_DATA1/SSL20/IERxD/RxD2
P8_5/A13/DV1_DATA2/MOSI2/UARTH_RxD
P8_6/A14/DV1_DATA3/MISO2/UARTH_TxD/IETxD/TxD2
P8_7/A15/DV1_DATA4/AUDIO_XOUT/IRQ5/COL
P8_8/A16/DV1_DATA5/SPBIO0_1/SPDIF_IN/TIOC1A/PWM1A/TxD3/SSISCK5
P8_9/A17/DV1_DATA6/SPBIO1_1/SPDIF_OUT/TIOC1B/PWM1B/RxD3/SSIWS5
P8_10/A18/DV1_DATA7/SPBIO2_1/TIOC3A/CTx4/PWM1C/SGOUT_0/DV0_CLK
P8_11/A19/MLB_CLK/SPBIO3_1/TIOC3B/RxD5/PWM1D/SGOUT_1/SSITxD5
P8_12/A20/MLB_DAT/SPBCLK_1/TIOC3C/SCK5/PWM1E/SGOUT_2/SSISCK4
P8_13/A21/MLB_SIG/SPBSSL_1/TIOC3D/TXD5/PWM1F/SGOUT_3/SSIWS4
P8_14/A22/SPBIO4_0/SPBIO0_1/TIOC2A/RSPCK2/PWM1G/TxD4/SSIDATA4
P8_15/A23/SPBIO5_0/SPBIO1_1/TIOC2B/SSL20/PWM1H/RxD4
P9_0/A24/SPBIO6_0/CTx0/TCLKC/MOSI2/SCL0O
P9_1/A25/SPBIO7_0/CRx0/IRQ0/MISO2/MSQ/SDA0O
P1_0/SCL0/DV0_DATA16/TCLKA/IRQ0/VIO_VD/DV0_VSYNC/SCL0I
P1_1/SDA0/DV0_DATA17/TCLKC/IRQ1/VIO_HD/DV0_HSYNC/SDA0I
P1_2/SCL1/DV0_DATA18/FRB/IRQ2/ICN_SCK/LCD1_EXTCLK/SCL1I
P1_3/SDA1/DV0_DATA19/COL/IRQ3/ICN_SDATA/SDA1I
P1_4/SCL2/DV0_CLK/CRx1/IRQ4/ICN_SCK/CAN_CLK/SCL2I
P1_5/SDA2/DV1_CLK/CRx4/IRQ5/VIO_CLK/ICN_SDATA/LCD1_EXTCLK/SDA2I
P1_6/SCL3/DV1_VSYNC/IERxD/IRQ6/VIO_D12/DV0_DATA12/MLB_CLK/SCL3I
P1_7/SDA3/DV1_HSYNC/LRXD0/IRQ7/VIO_D13/DV0_DATA13/SDA3I
P7_0/MD_BOOT2/CS0/DV0_DATA16/MDC/SCK4/LTXD0/TIOC0A
P7_1/CS3/DV0_DATA17/TXCLK/TXD4/DV0_CLK/SSISCK1/TIOC0B
P7_2/RAS/DV0_DATA18/TXER/RXD4/CRx2/SSIWS1/TIOC0C
P7_3/CAS/DV0_DATA19/TXEN/SCK7/CTx2/SSIRxD1/TIOC0D
P7_4/CKE/DV0_DATA20/TXD[0]/TXD7/UARTH_CLK/SSITxD1/TIOC1A
P7_5/RD/WR/DV0_DATA21/TXD[1]/RXD7/UARTH_RxD/SSISCK2/TIOC1B
P7_6/WE0/DQMLL/DV0_DATA22/TXD[2]/CTS7/UARTH_TxD/SSIWS2/TIOC2A
P7_7/WE1/DQMLU/DV0_DATA23/TXD[3]/RTS7/SSIDATA2/TIOC2B
P7_8/RD/SSISCK3/CRx0/TIOC3A/IRQ1
P1_8/AN0/IRQ2/DREQ0/VIO_D14/DV0_DATA14/MSN_VDC50
P1_9/AN1/IRQ3/VIO_D15/DV0_DATA15/MSN_VDC51
P1_10/AN2/IRQ4/TCLKB/MSN_DVDEC0
P1_11/AN3/IRQ5/TCLKD/MSN_DVDEC1
P1_12/AN4/DV0_VSYNC/VIO_FLD/MPSEL
P1_13/AN5/DV0_HSYNC/WAIT/MST
P1_14/AN6/COL/MSD
P1_15/AN7
P2_12/D28/RSPCK0/DV0_DATA12/SPBIO4_0/CRx3/IRQ6/LCD1_DATA12/TIOC1B
P2_13/D29/SSL00/DV0_DATA13/SPBIO5_0/CTx3/SCK0/LCD1_DATA13/IRQ7
P2_14/D30/MOSI0/DV0_DATA14/SPBIO6_0/CRx4/TxD0/LCD1_DATA14/IRQ0
P2_15/D31/MISO0/DV0_DATA15/SPBIO7_0/CAN_CLK/RxD0/LCD1_DATA15/IRQ1
P2_0/D16/TXCLK/DV0_DATA0/SPBIO0_1/MLB_CLK/IRQ5/VIO_D0/LCD0_DATA16
P2_1/D17/TXER/DV0_DATA1/SPBIO1_1/MLB_DAT/TIOC2A/VIO_D1/LCD0_DATA17
P2_2/D18/TXEN/DV0_DATA2/SPBIO2_1/MLB_SIG/TIOC2B/VIO_D2/LCD0_DATA18
P2_3/D19/CRS/DV0_DATA3/SPBIO3_1/IERxD/CTS1/VIO_D3/LCD0_DATA19
P2_4/D20/TXD[0]/DV0_DATA4/SSISCK5/SPBCLK_1/SCK1/VIO_D4/LCD0_DATA20
P2_5/D21/TXD[1]/DV0_DATA5/SSIWS5/SPBSSL_1/TxD1/VIO_D5/LCD0_DATA21
P2_6/D22/TXD[2]/DV0_DATA6/SSIRxD5/RxD1/VIO_D6/LCD0_DATA22
P2_7/D23/TXD[3]/DV0_DATA7/SSITxD5/IETxD/RTS1/VIO_D7/LCD0_DATA23
P2_8/D24/RXD[0]/DV0_DATA8/SSISCK0/LCD0_TCON6/LCD1_DATA8/VIO_D8/RSPCK4
P2_9/D25/RXD[1]/DV0_DATA9/SSIWS0/LRXD0/LCD1_DATA9/VIO_D9/SSL40
P2_10/D26/RXD[2]/DV0_DATA10/SSIRxD0/LTXD0/LCD1_DATA10/VIO_D10/MOSI4
P2_11/D27/RXD[3]/DV0_DATA11/SSITxD0/TIOC1A/LCD1_DATA11/VIO_D11/MISO4
P10_0/DV0_CLK/TCLKA/PWM2A/TXCLK/LCD0_DATA23/VIO_CLK
P10_1/DV0_VSYNC/TCLKB/PWM2B/TXER/LCD0_DATA22/VIO_VD
P10_2/DV0_HSYNC/TCLKC/PWM2C/TXEN/LCD0_DATA21/VIO_HD
P10_3/DV0_DEN/TCLKD/PWM2D/CRS/LCD0_DATA20/VIO_FLD
P10_4/DV0_DATA0/TIOC0A/PWM2E/TXD[0]/LCD0_DATA19/VIO_D0
P10_5/DV0_DATA1/TIOC0B/PWM2F/TXD[1]/LCD0_DATA18/VIO_D1
P10_6/DV0_DATA2/TIOC0C/PWM2G/TXD[2]/LCD0_DATA17/VIO_D2
P10_7/DV0_DATA3/TIOC0D/PWM2H/TXD[3]/LCD0_DATA16/VIO_D3
P10_8/DV0_DATA4/TIOC1A/RXD[0]/LCD0_DATA15/VIO_D4
P10_9/DV0_DATA5/TIOC1B/RXD[1]/LCD0_DATA14/VIO_D5
P10_10/DV0_DATA6/TIOC2A/RXD[2]/LCD0_DATA13/VIO_D6
P10_11/DV0_DATA7/TIOC2B/RXD[3]/LCD0_DATA12/VIO_D7
P10_12/DV0_DATA8/SSISCK1/RSPCK0/LCD0_DATA11/VIO_D8
P10_13/DV0_DATA9/SSIWS1/SSL00/LCD0_DATA10/VIO_D9
P10_14/DV0_DATA10/SSIRxD1/MOSI0/LCD0_DATA9/VIO_D10
P10_15/DV0_DATA11/SSITxD1/MISO0/LCD0_DATA8/VIO_D11
P11_0/DV0_DATA12/TIOC4A/MLB_CLK/SCK6/LCD0_DATA7/VIO_D12
P11_1/DV0_DATA13/TIOC4B/MLB_DAT/TxD6/LCD0_DATA6/VIO_D13
P11_2/DV0_DATA14/TIOC4C/MLB_SIG/RxD6/LCD0_DATA5/VIO_D14
P11_3/DV0_DATA15/TIOC4D/LCD0_DATA4/VIO_D15
P11_4/DV0_DATA16/SD_CD_0/SSISCK4/MMC_CD/LCD0_DATA3
P11_5/DV0_DATA17/SD_WP_0/SSIWS4/LCD0_DATA2
P11_6/DV0_DATA18/SD_D1_0/SSIDATA4/MMC_D1/LCD0_DATA1
P11_7/DV0_DATA19/SD_D0_0/CTS5/MMC_D0/LCD0_DATA0
P11_8/DV0_DATA20/SD_CLK_0/RTS5/MMC_CLK/LCD0_TCON6
P11_9/DV0_DATA21/SD_CMD_0/SCK5/MMC_CMD/LCD0_TCON5
P11_10/DV0_DATA22/SD_D3_0/TxD5/MMC_D3/LCD0_TCON4
P11_11/DV0_DATA23/SD_D2_0/RxD5/MMC_D2/LCD0_TCON3
P11_12/CRx1/RSPCK1/IRQ3/MMC_D4/LCD0_TCON2
P11_13/CTx1/SSL01/LCD0_TCON4/MMC_D5/LCD0_TCON1
P11_14/SPDIF_IN/MOSI1/LCD0_TCON5/MMC_D6/LCD0_TCON0
P11_15/SPDIF_OUT/MISO1/IRQ1/MMC_D7/LCD0_CLK
P2_12/SPBIO01
P2_13/SPBIO11
P2_14/SPBIO21
P2_15/SPBIO31
P2_0/ET_TXCLK
P2_1/ET_TXER
P2_2/ET_TXEN
P2_3/ET_CRS
P2_4/ET_TXD0
P2_5/ET_TXD1
P2_6/ET_TXD2
P2_7/ET_TXD3
P2_8/ET_RXD0
P2_9/ET_RXD1
P2_10/ET_RXD2
P2_11/ET_RXD3
P10_0/VIO_CLK
P10_1/VIO_VSYNC
P10_2/VIO_HSYNC
P10_3/VIO_FLD
P10_4/VIO_D0
P10_5/VIO_D1
P10_6/VIO_D2
P10_7/VIO_D3
P10_8/VIO_D4
P10_0/VIO_D5
P10_10/VIO_D6
P10_11/VIO_D7
P10_12/SSISCK
P10_13/SSIWS
P10_14/SSIRxD
P10_15/SSITxD
P11_0/LCD_DATA7
P11_1/LCD_DATA6
P11_2/LCD_DATA5
P11_3/LCD_DATA4
P11_4/LCD_DATA3
P11_5/LCD_DATA2
P11_6/LCD_DATA1
P11_7/LCD_DATA0
P11_8/LCD_DEN
P11_9/LCD_VSYNC
P11_10/LCD_HSYNC
P11_11-LED1R
P11_12/MMC_D4
P11_13/MMC_D5
P11_14/MMC_D6
P11_15/MMC_D7
Renesas YLCDRZA1H MCU Module
MCU e-MMC, SDRAM, I2C linterfaces & GPIO
Author: Jorge Amodio
Date: 4/15/2015
Revision: v2.1 PCB02
Sheet 5 of 8
am.renesas.com/HiResGUI
RENESAS
RZ

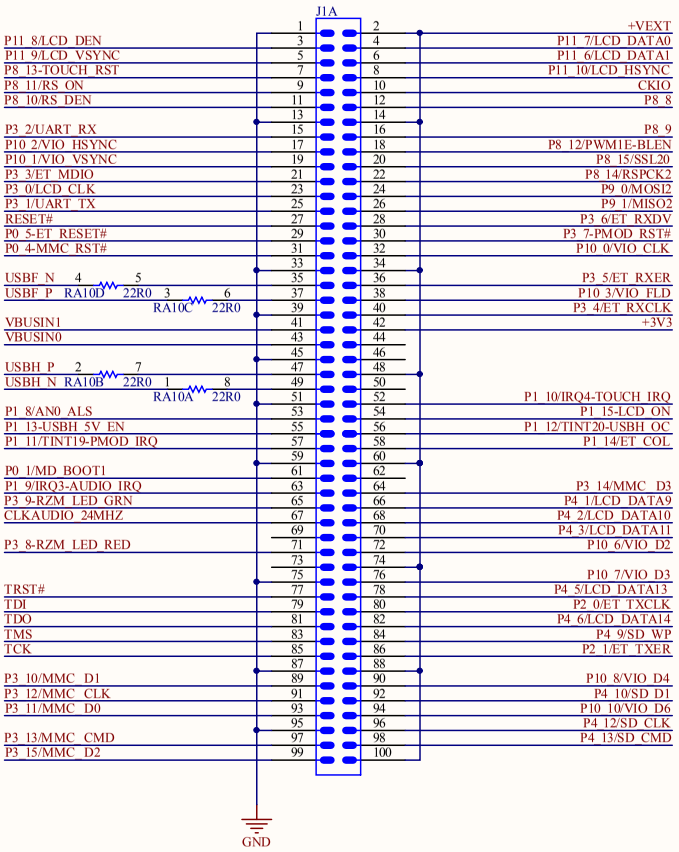


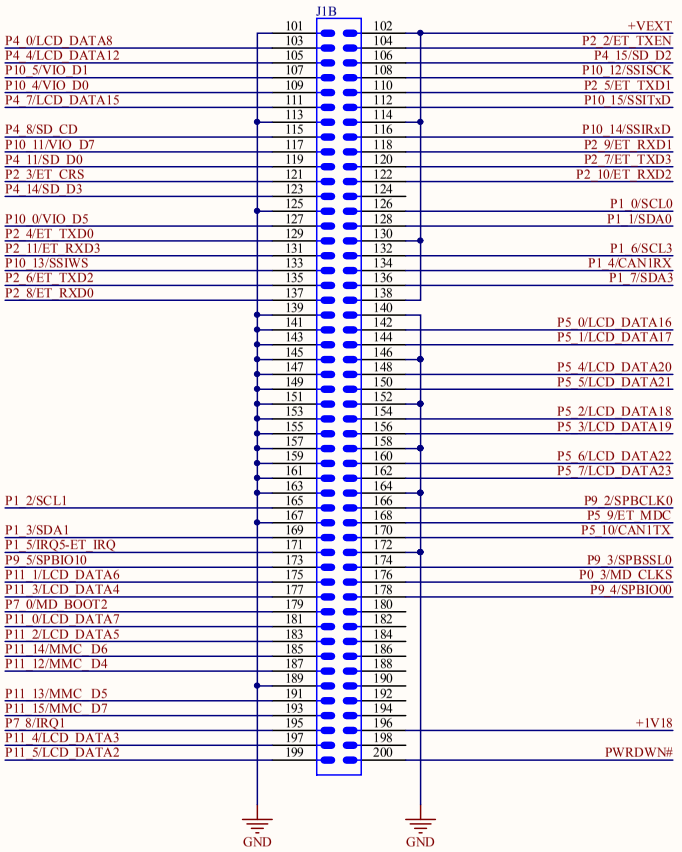
Renesas YLCDRZA1H MCU Module	am.renesas.com/HiResGUI
Dual QSPI FLASH & EEPROM	
Author: *Jorge Amodio*	Revision: v2.1 PCB02
Date: 4/15/2015	Sheet 6 of 8



Renesas YLCDRZA1H MCU Module	
SDRAM	am.renesas.com/HiResGUI
Author: *Jorge Amodio*	Revision: v2.1 PCB02
Date: 4/15/2015	Sheet 7 of 8

Board to Board connections via PCB Edge 200-pin matching DDR2 SODIMM Socket



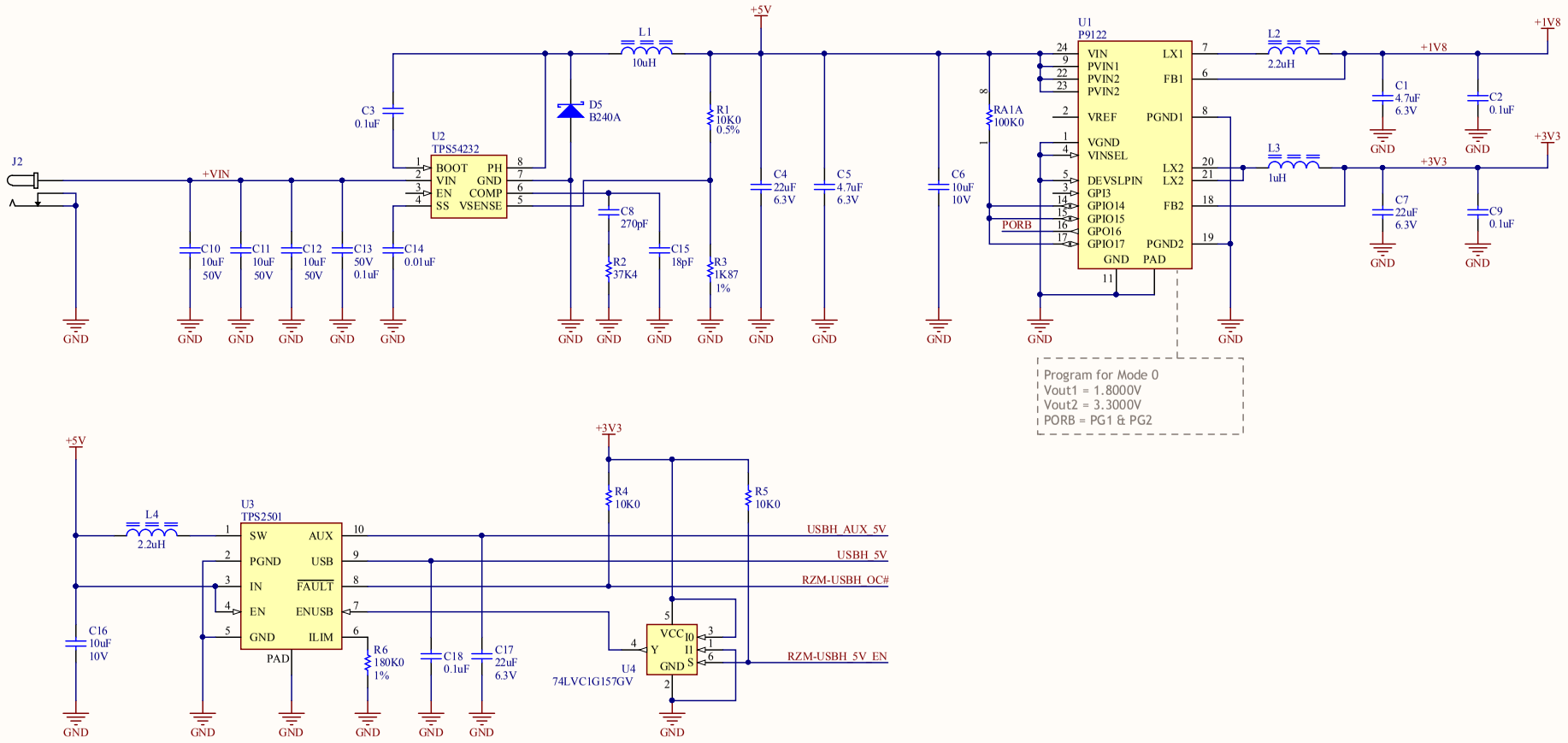


Renesas YLCDRZA1H MCU Module Board to Board Interconnect			am.renesas.com/HiResGUI
Author: *Jorge Amodio*		Revision: v2.1 PCB02	
Date: 4/15/2015		Sheet 8 of 8	

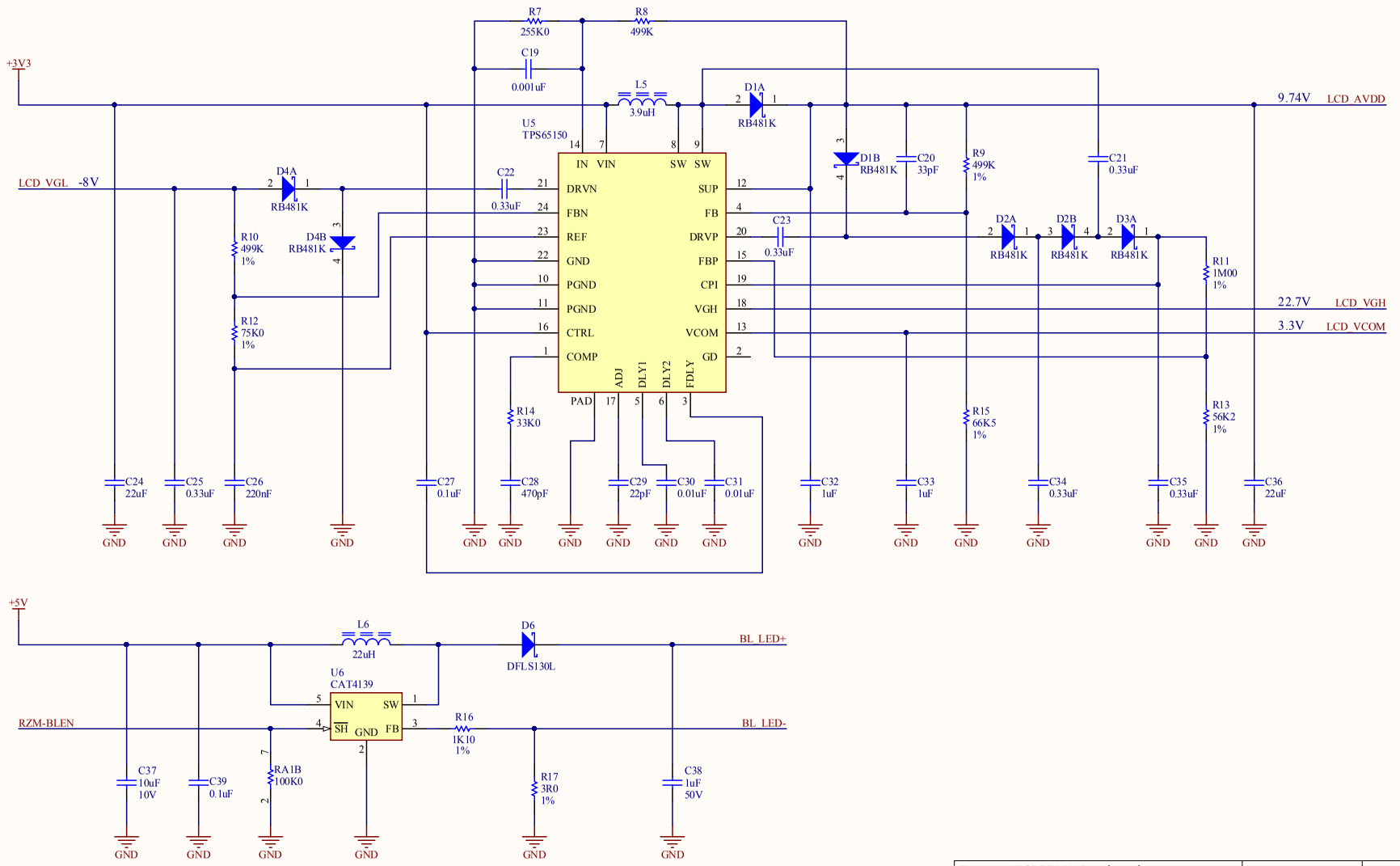
12.3 - RZ Module BOM

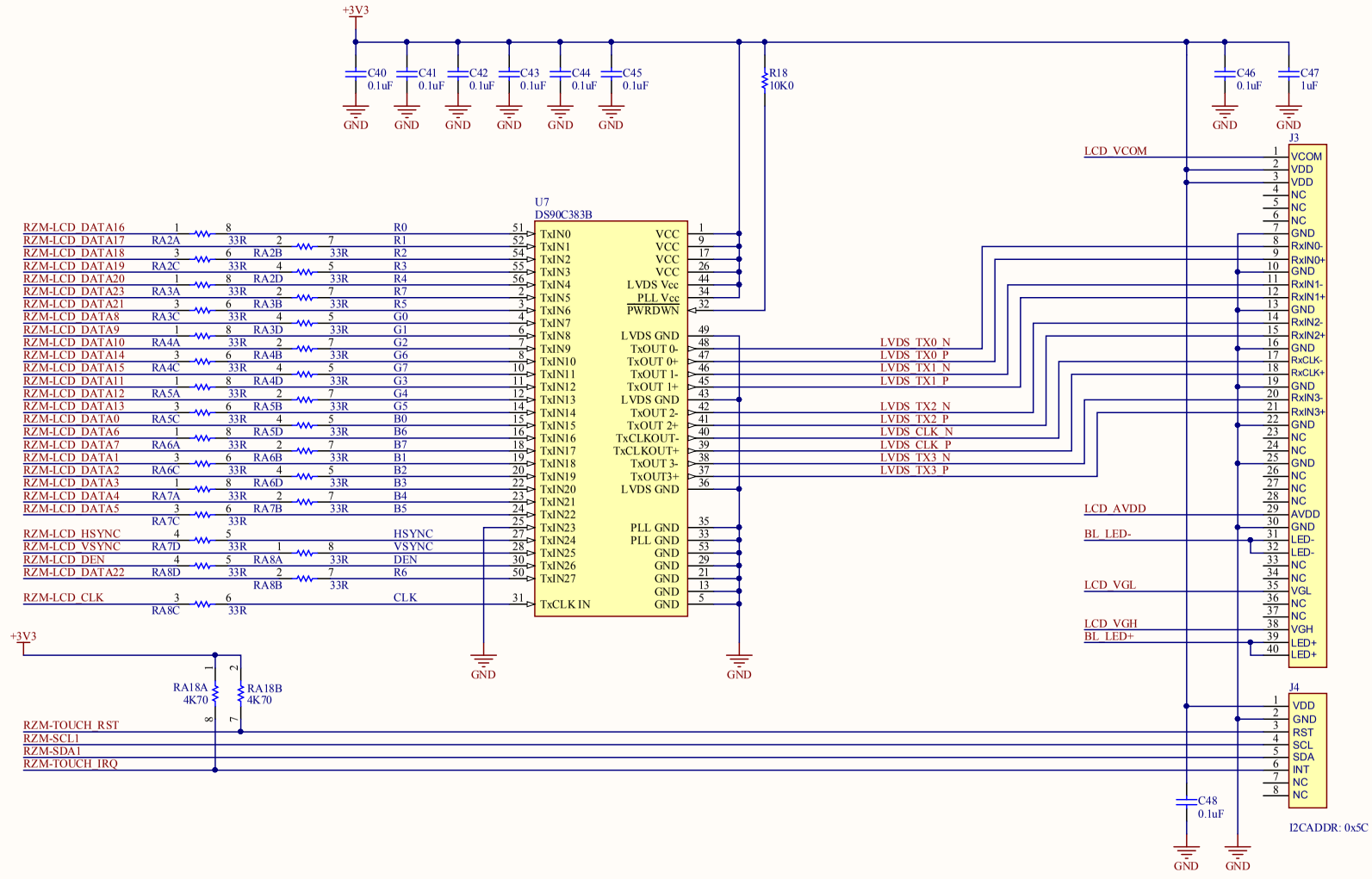
ID	Description	Package
C1	CL10A106KP8NNND [Samsung] Ceramic 10uF 10V 10% X5R	0603
C2	CL05A475MQ5NQNC [Samsung] Ceramic 4u7 6V3 20% X5R	0402
C3-4,C6,C8-20,C23-26,C28-C38,C40-47,C50-66	CL03A104KP3NNNC [Samsung] Ceramic100n0 10V X5R 10%	0201
C48,C49	CL05C120JB5NNNC [Samsung] Ceramic 12p0 50V C0G 5%	0402
C5	CL10A226MQ8NRNC [Samsung] Ceramic 22uF 6.3V X5R 20%	0603
C7,C21-22,C27,C39	CL05A106MQ5NUNC [Samsung] CER 10uF 6.3V X5R 20%	0402
L1	SRN3015-2R2M [Bourns] 2.2uH 1.8A 72mOhm Inductor	SMD
L2	SRN3015-1R0Y [Bourns] 1uH 2.35A Inductor 3x3x1.5mm	SMD
LED1	598-8610-207F [Dialight] LED Bi-Color Red/Green 60/40mcd	1210
R1	ERA-2AED104X [Panasonic] 100K0 0.5% 1/16W 25ppm	0402
R10	ERA-2AED243X [Panasonic] 24k0 0.5% 1/16W 25ppm	0402
R12,R13	ERJ-2RKF4702X [Panasonic] 47k0 1% 1/10W 100ppm	0402
R14	ERA-2AED223X [Panasonic] 22k0 0.5% 1/16W 25ppm	0402
R21	ERA-2AED471X [Panasonic] 470R 0.5% 1/16W 25ppm	0402
R22	ERA-2AED152X [Panasonic] 1K50 0.5% 1/16W 25ppm	0402
R2-4,R15-19	ERA-2AED472X [Panasonic] 4k70 0.5% 1/16W 25ppm	0402
R5-8	CRCW04020000Z0ED [Vishay] 0R00 1/16W	0402
R9,R11	ERA-2AED562X [Panasonic] 5k60 0.5% 1/16W 25ppm	0402
RA10	EXB-28V220JX [Panasonic] IsolArr 22R0 4x 5% 200ppm 1/16W	0804
RA1-9	EXB-28V472JX [Panasonic] IsolArr 4k7 5% 200ppm 1/16W 4x0402	0804
U1	IDTP9122 [IDT] Switcher w/I2C Dual Factory Pgm 1.18[1],3.30[2]	QFN24
U2	STM1818SWX7F [STM] Reset Monitor 2.88V	SOT23
U3	SI5351C [SiLabs] I2C 8 Clock Gen (T/R) Factory Pre-Programmed	QFN20
U4	501AAA-12M0000-DAGR [SiLabs] 12MHz Oscillator 50ppm	2x2.5
U5,U8	N25Q256A13EF840E [Micron] NOR Serial FLASH QSPI 256Mbit	V-PDFN-8/8x6mm
U6	R7S721001VCBG#AC0 [Renesas] RZ A1H MCU 10MB BGA324	PRBG0324GA-A
U7	CAT34C02HU4IGT4A [OnSemi] EEPROM I2C 2KBit w/OTP	UDFN8
U9,U10	MT48LC16M16A2B4-6A IT:G TR [Micron] 32MB SDRAM 133MHz	VFBGA54
X1	ABS07-32.768KHZ-T [Abracon] 32.768 Tuning Fork Crystal	2-SMD

12.4 - Baseboard Schematics

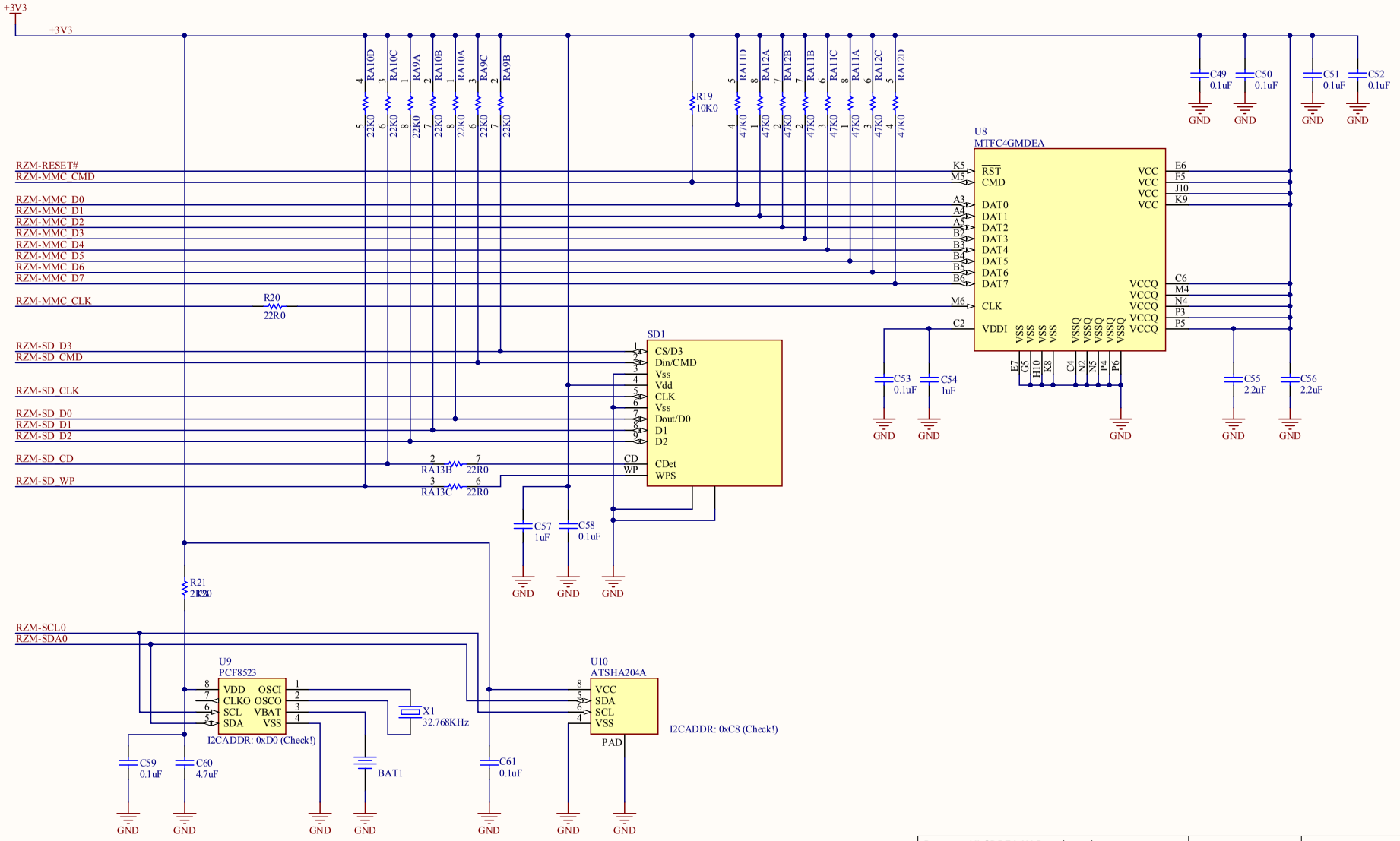


Renesas YLCDRZA1H Baseboard System and USB Host Power Supplies		www.seriousintegrated.com
Author: *Jorge Amodio*	Revision: v2.1 PCB03	
Date: *7/15/2015*	Sheet 1 of 12	


+3V3
R7
255K0
R8
499K
C19
0.001uF
L5
3.9uH
D1A
RB481K
9.74V
LCD_AVDD
U5
TPS65150
IN
VIN
SW
SW
LCD_VGL
-8V
D4A
RB481K
C22
0.33uF
DRVN
FBN
REF
GND
PGND
PGND
CTRL
COMP
SUP
FB
DRVP
FBP
CP1
VGH
VCOM
GD
PAD
ADJ
DLY1
DLY2
FDLY
D1B
RB481K
C20
33pF
R9
499K
1%
C21
0.33uF
C23
0.33uF
D2A
RB481K
D2B
RB481K
D3A
RB481K
R10
499K
1%
D4B
RB481K
R11
1M00
1%
22.7V
LCD_VGH
3.3V
LCD_VCOM
R12
75K0
1%
R14
33K0
R15
66K5
1%
R13
56K2
1%
C24
22uF
C25
0.33uF
C26
220nF
C27
0.1uF
C28
470pF
C29
22pF
C30
0.01uF
C31
0.01uF
C32
1uF
C33
1uF
C34
0.33uF
C35
0.33uF
C36
22uF
GND
+5V
L6
22uH
D6
DFLS130L
BL_LED+
U6
CAT4139
VIN
SW
SH
GND
FB
RZM-BLEN
R16
1K10
1%
BL_LED-
C37
10uF
10V
C39
0.1uF
RA1B
100K0
R17
3R0
1%
C38
1uF
50V
Renesas YLCDRZA1H Baseboard
LCD Power
Author: Jorge Amodio
Date: 7/15/2015
Revision: v2.1 PCB03
Sheet 2 of 12
www.seriousintegrated.com
RENESAS
RZ



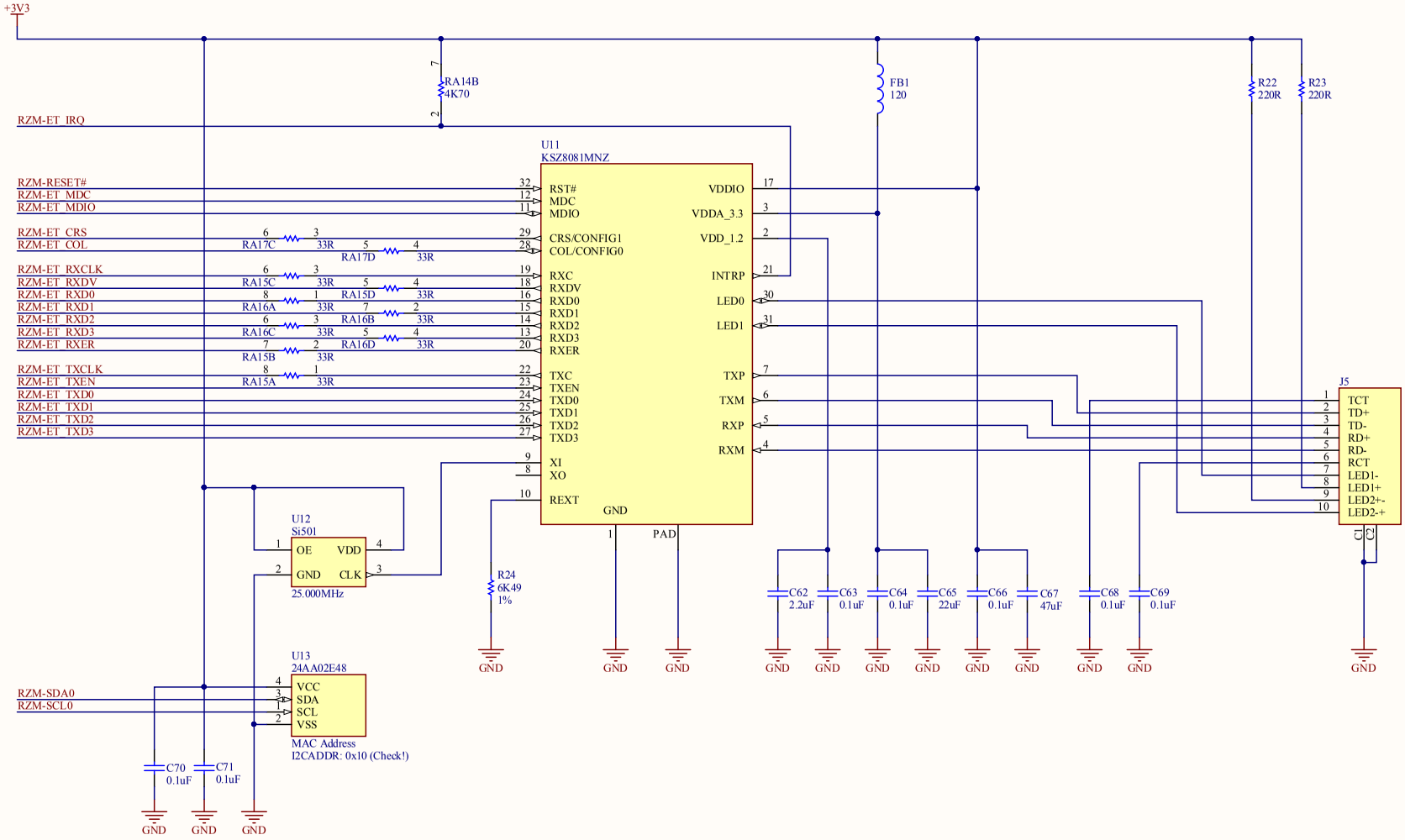
Renesas YLCDRZA1H Baseboard	www.seriousintegrated.com
LCD Interface	
Author: *Jorge Amodio*	Revision: v2.1 PCB03
Date: *7/15/2015*	Sheet 3 of 12



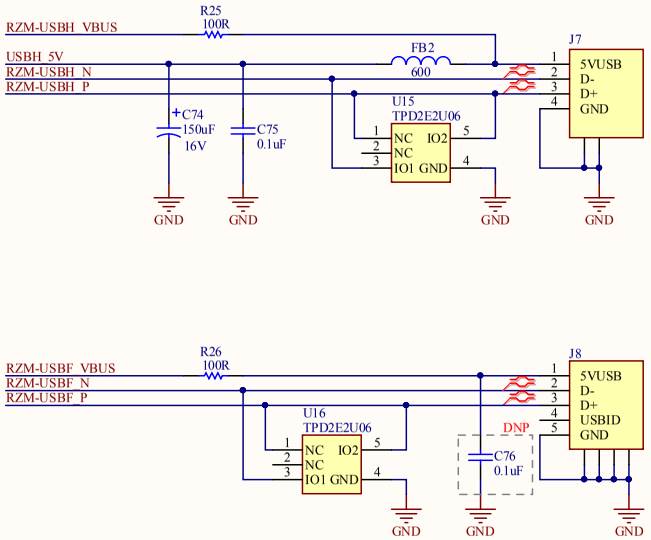
Renesas YLCDRZA1H Baseboard
MMC, SD Card, RTCC, Crypto

Author: *Jorge Amodio*	Revision: v2.1 PCB03
Date: *7/15/2015*	Sheet 4 of 12

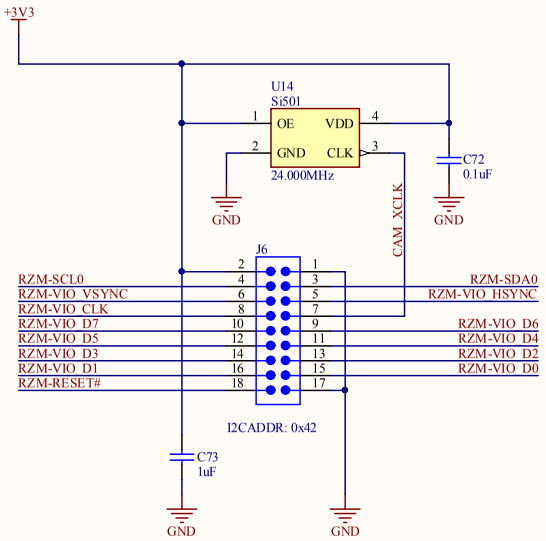
www.seriousintegrated.com



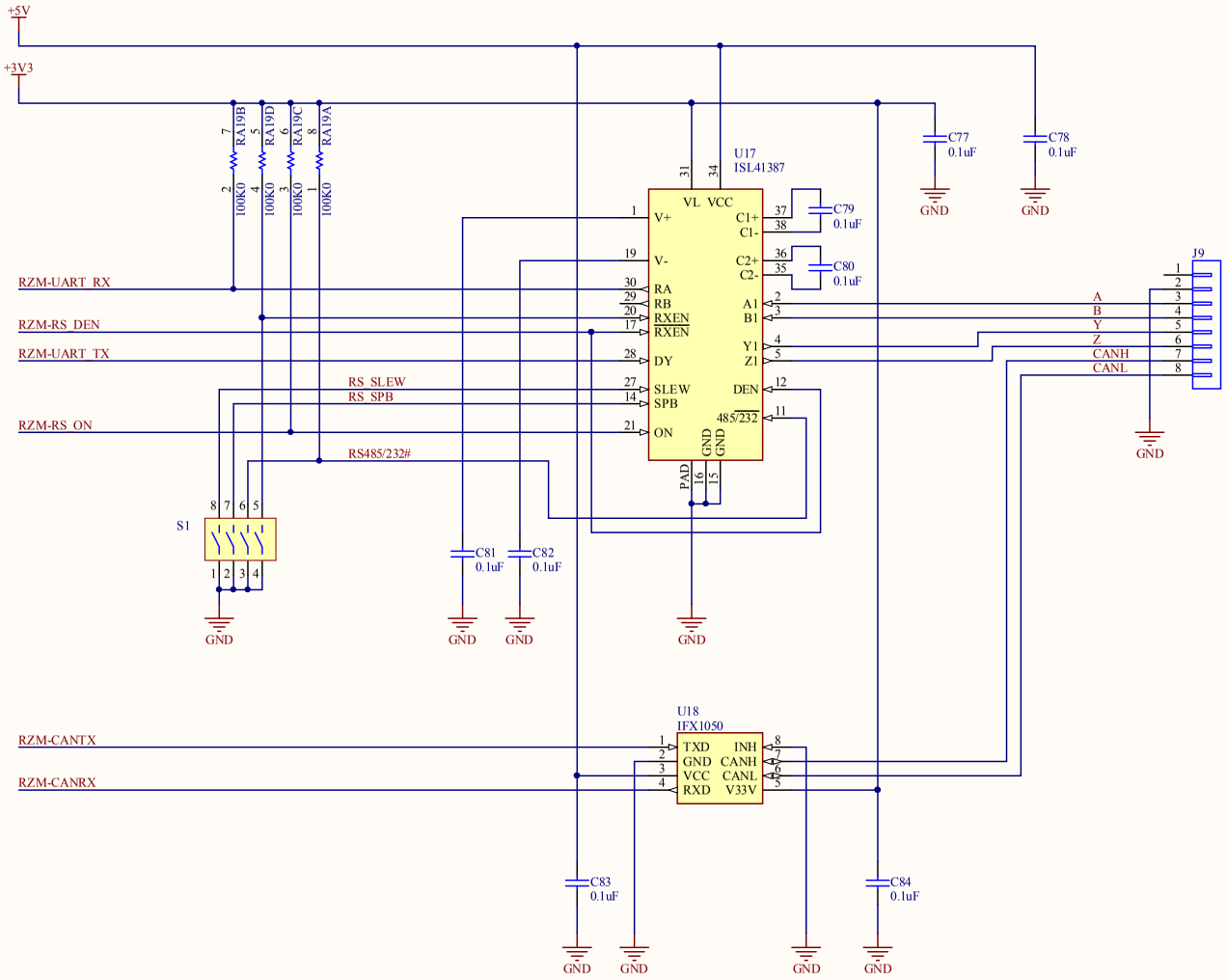
Renesas YLCDRZA1H Baseboard Ethernet		www.seriousintegrated.com
Author: *Jorge Amodio*	Revision: v2.1 PCB03	
Date: *7/15/2015*	Sheet 5 of 12	



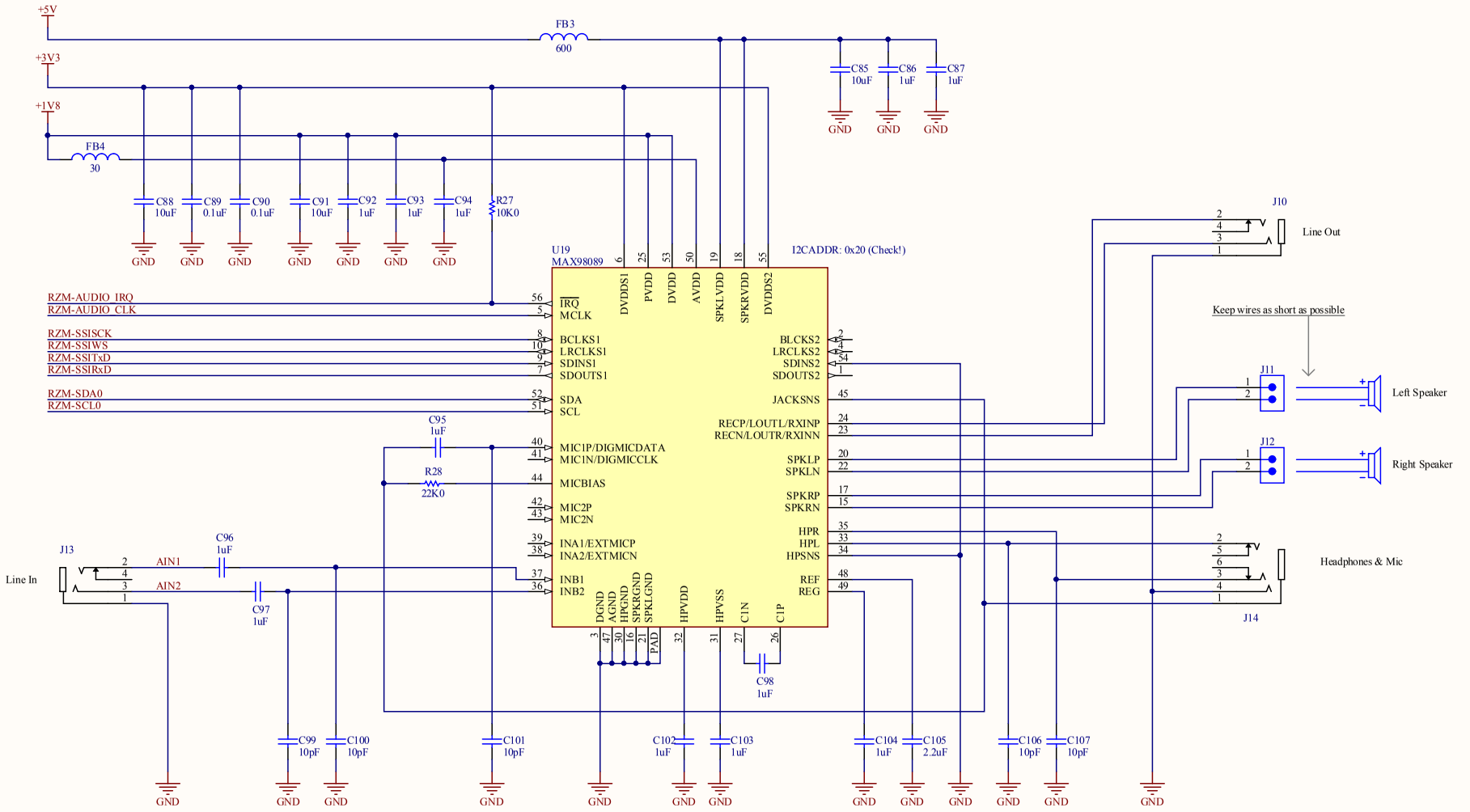
Renesas YLCDRZA1H Baseboard			www.seriousintegrated.com
USB Host & Device			
Author: *Jorge Amodio*		Revision: v2.1 PCB03	
Date: *7/15/2015*		Sheet 6 of 12	



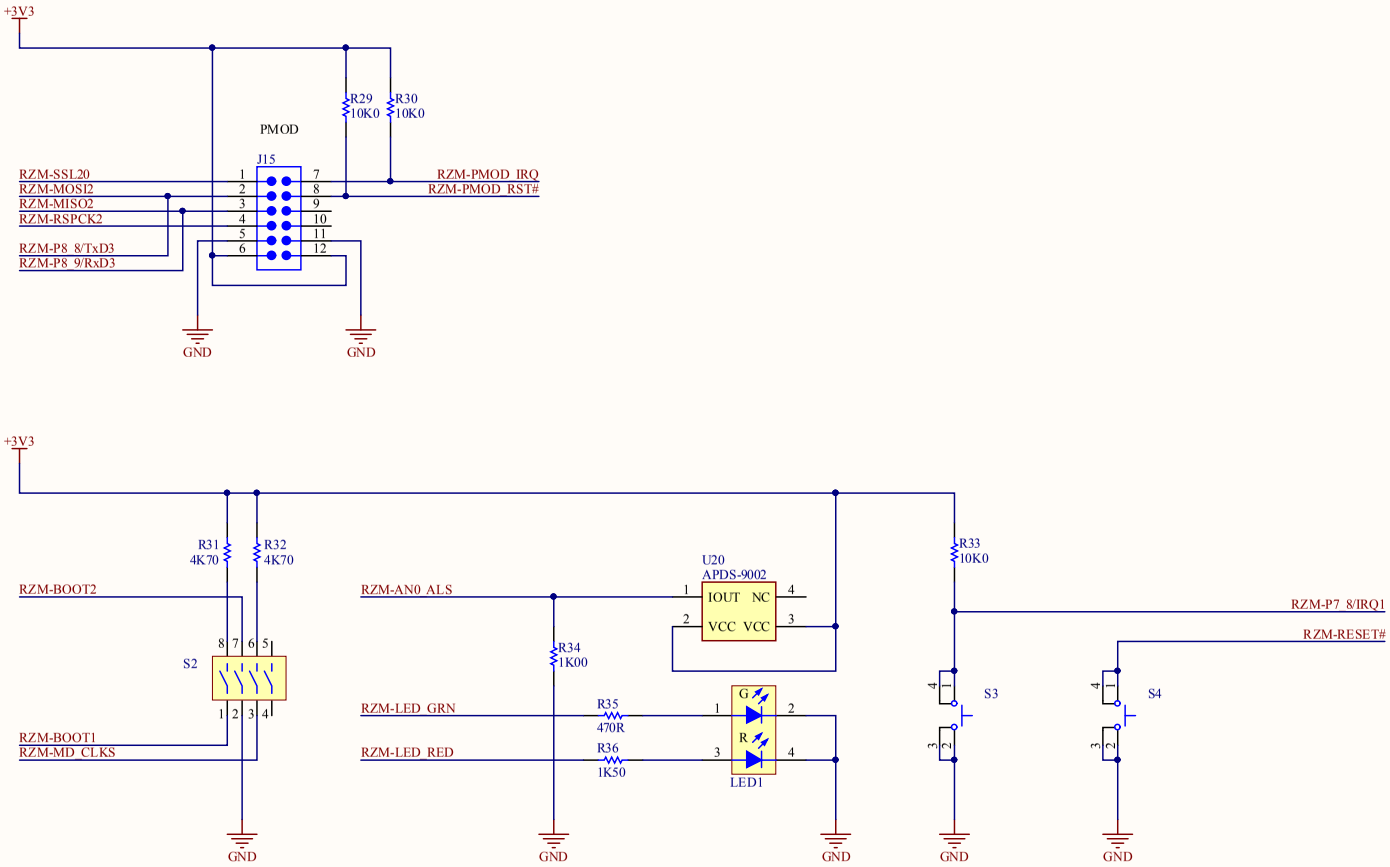
Renesas YLCDRZA1H Baseboard Camera Interface			www.seriousintegrated.com
Author: *Jorge Amodio*		Revision: v2.1 PCB03	
Date: *7/15/2015*		Sheet 7 of 12	



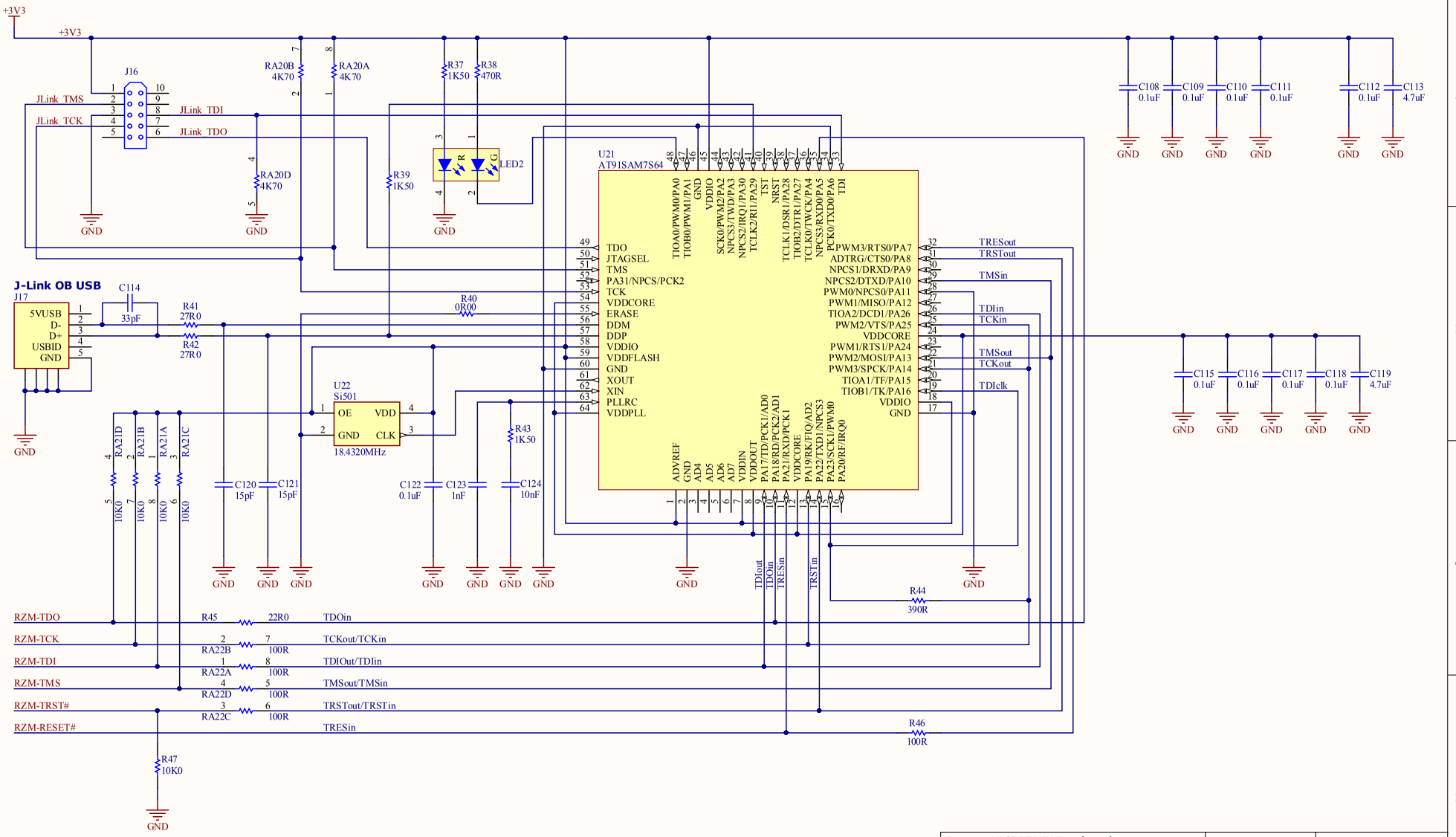
Renesas YLCDRZA1H Baseboard	www.seriousintegrated.com
Industrial Networking RS485/232 & CAN	
Author: *Jorge Amodio*	Revision: v2.1 PCB03
Date: *7/15/2015*	Sheet 8 of 12



Renesas YLCDRZA1H Baseboard Audio			www.seriousintegrated.com
Author: *Jorge Amodio*		Revision: v2.1 PCB03	
Date: *7/15/2015*		Sheet 9 of 12	



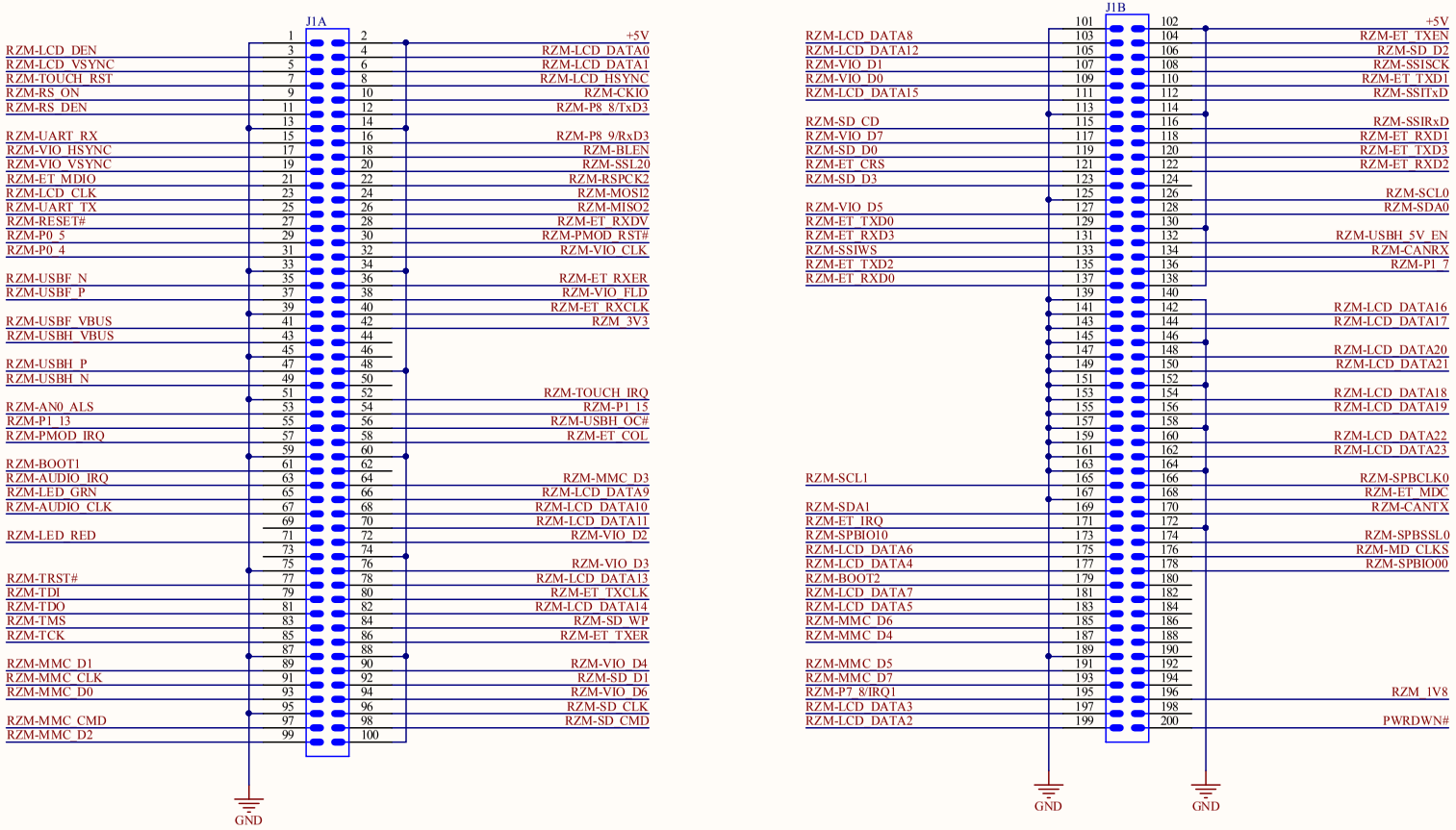
Renesas YLCDRZA1H Baseboard	www.seriousintegrated.com
PMOD, Boot Modes, & User I/O	
Author: *Jorge Amodio*	Revision: v2.1 PCB03
Date: *7/15/2015*	Sheet 10of 12



Renesas YLCDRZA1H Baseboard	
JLink On Board & External JTAG Interface	
Author: *Jorge Amodio*	Revision: v2.1 PCB03
Date: *7/15/2015*	Sheet 11of 12

www.seriousintegrated.com

Board to Board connections via DDR2 SODIMM Socket



SO1 SO2 SO3 SO4 SO5 SO6

Renesas YLCDRZA1H Baseboard Board to Board Interconnect			www.seriousintegrated.com
Author: *Jorge Amodio*		Revision: v2.1 PCB03	
Date: *7/15/2015*		Sheet 12of 12	

12.5 - Baseboard BOM

Designator	Qty	Description
BAT1	1	3030TR [Keystone] CR1025 SMD Coin Cell Holder
C1, C5, C60, C113, C119	5	CL05A475MQ5NQNC [Samsung] Ceramic 4u7 6V3 X5R 20%
C2, C3, C9, C27, C39, C40, C41, C42, C43, C44, C45, C46, C48, C49, C50, C51, C52, C53, C58, C59, C61, C63, C64, C66, C68, C69, C70, C71, C72, C75, C77, C78, C79, C80, C81, C82, C83, C84, C89, C90, C108, C109, C110, C111, C112, C115, C116, C117, C118, C122	50	CL03A104KP3NNNC [Samsung] Ceramic100n0 10V X5R 10%
C4, C7, C17, C65	4	CL10A226MQ8NRNC [Samsung] Ceramic 22uF 6.3V X5R 20%
C6, C16, C37, C88, C91	5	CL10A106KP8NNND [Samsung] Ceramic 10uF 10V 10% X5R
C8	1	CL05B271KB5NNNC [Samsung] Ceramic 270p 50V X7R 10%
C10, C11, C12	3	CL31A106KBHNNNE [Samsung] Ceramic 10u0 50V 10% X5R
C13	1	C1005X7R1H104K050BB [TDK] Ceramic 100n0 50V 10% X7R
C14, C30, C31	3	CL05B103KB5NNNC [Samsung] Ceramic 10n0 50V X7R 10%
C15	1	CL05C180JB5NNNC [Samsung] Ceramic 18p0 50V C0G 5%
C18	1	CL05A104KO5NNNC [Samsung] Ceramic 100n0 16V 10% X7R
C19	1	CL05B102KB5NNNC [Samsung] Ceramic 1n0 50V X7R 10%
C20, C114	2	CL05C330JB5NNNC [Samsung] Ceramic 33p0 50V 5% NP0
C21, C22, C23, C25, C34, C35	6	C1608X5R1H334M080AB [TDK] Ceramic 330n0 50V 20% X5R
C24, C36	2	CL21A226MAQNNNE [Samsung] Ceramic 22u0 25V 20% X5R
C26	1	C1608X7R1H224M080AB [TDK] Ceramic 220n0 50V 20% X7R
C28	1	CL05B471KB5NNNC [Samsung] Ceramic 470p0 50V 10% X7R
C29	1	CL05C220JB5NNNC [Samsung] Ceramic 22p0 50V 5% NP0
C32, C33, C47, C95, C96, C97	6	CL05A105KO5NNNC [Samsung] Ceramic1u0 16V X5R 10%
C38	1	CL31B105KBHNNNE [Samsung] Ceramic 1u0 50V 10% X7R
C54, C57, C73, C86, C87, C92, C93, C94, C98, C102, C103, C104	12	CL03A105MQ3CSNC [Samsung] Ceramic 1u0 6.3V 20% X5R
C55, C56, C62, C105	4	CL05A225MP5NNNC [Samsung] Ceramic 2u2 10V X5R 20%
C67	1	LMK316BJ476ML-T [Taiyo Yuden] Ceramic 47uF 10V 20% X5R
C74	1	TPSD157M016R0150 [AVX] Tant150uF 16V 20%
C76	0	CL03A104KP3NNNC [Samsung] Ceramic100n0 10V X5R 10%
C85	1	CL05A106MQ5NUNC [Samsung] Ceramic10uF 6.3V X5R 20%
C99, C100, C101, C106, C107	5	CL03C100DA3GNNC [Samsung] Ceramic 10p0 25V C0G/NP0 +/-0.5pF
C120, C121	2	C0603C0G1E150J030BA [Murata] Ceramic 15p0 25V C0G 5%
C123	1	CL03B102KA3NNNC [Samsung] Ceramic 1n0 25V 10% X7R
C124	1	CL03A103KP3NNNC [Samsung] Ceramic 10n0 10V 10% X5R
D1, D2, D3, D4	4	RB481KTL [Rohm] Dual Shottky Diode 30V
D5	1	B240A-13-F [Diodes Inc] Schottky 40V 2A
D6	1	DFLS130L-7 [Diodes Zetex] Schottky Diode 30V 310mV@1A
FB1	1	BLM21AG121SN1D [Murata] Ferrite Beads120Ohm 25% 100MHz 800mA
FB2, FB3	2	CIM05U601NC [Samsung] Ferrite Bead 600 Ohm 300mA 0402
FB4	1	CIS10P300AC [Samsung] Ferrite Bead 30R0 6A
J1	1	1473005-4 [TE] 200Pos RA DIMM Socket 0.6mm pitch
J2	1	RASM722PTR13X [Switchcraft] RA, 2.1mm 5A SMT, T/R

J3	1	XF2W-4015-1A [Omron] 40pos 0.5mm pitch FFC Dual
J4	1	XF2W-0815-1A [Omron] 8pos 0.5mm pitch FFC
J5	1	08B0-1X1T-36-F [Bel] MagJack 10/100 AutoMDIX LED G/Y TH
J6	1	CES-109-01-T-D [Samtec] 18pos/2x9 ST F 2.54mm Hdr
J7	1	USB-A-S-F-B-SM2-R-TR [Samtec] USB A 2.0 4Pin
J8, J17	2	10118192-0001LF [FCI] USB Micro B Full SMT
J9	1	20020110-C081A01LF [FCI] Term Block 8pos/1x8 M 3.5mm RA TH
J10	1	SJ-3524-SMT-TR-GR [CUI] 3.5mm SMT Audio Jack Green
J11, J12	2	SM02B-GHS-TB(LF)(SN) [JST] 2Pos/1x2 1.25mm RA
J13	1	SJ-3524-SMT-TR-BE [CUI] 3.5mm SMT Audio Jack Blue
J14	1	SJ-43516-SMT-TR-PI [CUI] 3.5mm SMT Audio Jack Pink/Red
J15	1	SSW-106-02-F-D-RA [Samtec] 2x6 RA 0.1" F Header
J16	0	TC-2050 PCB [Tag-Connect] 10pos/2x5 *NO PART PADS ONLY*
L1	1	SRU1028-100Y [Bourns] 10uH Shielded 2.8A 45mOhm 10x10x2.8mm
L2, L4	2	SRN3015-2R2M [Bourns] 2.2uH 1.8A 72mOhm Inductor
L3	1	SRN3015-1R0Y [Bourns] 1uH 2.35A Inductor 3x3x1.5mm
L5	1	SRR6028-3R9Y [Bourns] Shielded 3.9uH 2.45A SMD Coil
L6	1	SRR5028-220Y [Bourns] 22uH 1.15 30% 120mOHM,5.8x5.8x2.8mm
LED1, LED2	2	598-8610-207F [Dialight] LED BiColor Red/Green 60/40mcd
R1, R4, R5, R18, R19, R27, R29, R30, R33, R47	10	ERA-2AED103X [Panasonic] 10K 0.5% 1/16W 25ppm
R2	1	ERJ-2RKF3742X [Panasonic] 37k4 1% 1/10W 100ppm
R3	1	ERJ-2RKF1871X [Panasonic] 1k87 1% 1/10W 100ppm
R6	1	ERJ-2RKF1803X [Panasonic] 180K Ohm 1% 1/10W ±100ppm
R7	1	ERJ-2RKF2553X [Panasonic] 255k0 1% 1/10W 100ppm AEC-Q200
R8, R9, R10	3	ERJ-2RKF4993X [Panasonic] 499k 1% 1/10W 100ppm
R11	1	ERJ-2RKF1004X [Panasonic] 1m00 1% 1/10W 100ppm
R12	1	ERJ-2RKF7502X [Panasonic] 75k0 1% 1/10W 100ppm
R13	1	ERJ-2RKF5622X [Panasonic] 56k2 1% 1/10W 100ppm
R14	1	ERJ-2RKF3302X [Panasonic] 33k0 1% 1/10W 100ppm
R15	1	ERJ-2RKF6652X [Panasonic] 66k5 1% 1/10W 100ppm
R16	1	NRC04F1101TRF [NIC] 1k1 1/16W 1% 0402
R17	1	CRCW04023R00FKED [Vishay] 3R00 1% 1/16W 100ppm
R20, R45	2	ERJ-2RKF22R0X [Panasonic] 22R0 1% 1/10W 100ppm
R21	1	ERJ-2RKF2201X [Panasonic] 2k2 1% 1/10W 100ppm
R22, R23	2	ERJ-2RKF2200X [Panasonic] 220R 1% 1/10W 100ppm
R24	1	ERJ-2RKF6491X [Panasonic] 6k49 1% 1/10W 100ppm
R25, R26, R46	3	ERA-2AED101X [Panasonic] 100R 0.5% 1/16W 25ppm
R28	1	ERA-2AED223X [Panasonic] 22k0 0.5% 1/16W 25ppm
R31, R32	2	ERA-2AED472X [Panasonic] 4k70 0.5% 1/16W 25ppm
R34	1	ERA-2AED102X [Panasonic] 1k00 0.5% 1/16W 25ppm
R35, R38	2	ERA-2AED471X [Panasonic] 470R 0.5% 1/16W 25ppm
R36, R37, R39, R43	4	ERA-2AED152X [Panasonic] 1K50 0.5% 1/16W 25ppm
R40	1	CRCW04020000Z0ED [Vishay] 0R00 1/16W
R41, R42	2	ERJ-2RKF27R0X [Panasonic] 27R0 1% 1/10W 100ppm
R44	1	ERJ-2RKF3900X [Panasonic] 390R 1% 1/10W 100ppm

RA1, RA19	2	EXB-28V104JX [Panasonic] IsolArr 100k0 5% 200ppm 1/16W 4x040
RA2, RA3, RA4, RA5, RA6, RA7, RA8, RA15, RA16, RA17	10	EXB-28V330JX [Panasonic] IsolArr 33R0 4x 5% 200ppm 1/16W
RA9, RA10	2	EXB-28V223JX [Panasonic] IsolArr 22k0 4x 5% 200ppm 1/16W
RA11, RA12	2	EXB-28V473JX [Panasonic] IsolArr 47k0 4x 5% 200ppm 1/16W
RA13	1	EXB-28V220JX [Panasonic] IsolArr 22R0 4x 5% 200ppm 1/16W
RA14, RA18, RA20	3	EXB-28V472JX [Panasonic] IsolArr 4k7 5% 200ppm 1/16W 4x0402
RA21	1	EXB-28V103JX [Panasonic] IsolArr 10k0 5% 200ppm 1/16W 4x0402
RA22	1	EXB-28V101JX [Panasonic] IsolArr 100R 4x 5% 200ppm 1/16W
S1, S2	2	219-4LPSTR [CTS] DIP Switch 4Pos 2.54mm
S3, S4	2	KSC222J LFS [C&K] Sealed PB Switch 6.2x6.2mm
SD1	1	10067847-001RLF [FCI] SDCard Socket
SO3, SO4, SO5, SO6	4	SMTSO-M4-6ET [PEM] M4 6.0mm Standoff
U1	1	P9122-S2NBGI [IDT] Switcher w/I2C Dual Fact Pgm 1.8, 3.30
U2	1	TPS54232D [TI] Buck Regulator 28V 2A
U3	1	TPS2501DRCR [TI] USB Boost Power Controlller SON10
U4	1	74LVC1G157GV [NXP] Single 2-Input Multiplexer
U5	1	TPS65150RGER [TI] LCD 3-output LCD power controller
U6	1	CAT4139TD-GT3 [OnSemi] LED Backlight Driver
U7	1	DS90CF383BMTX/NOPB [TI] RGB888 to LVDS 65MHz Serializer
U8	1	MTFC4GMDEA-4M IT [Micron] 4GByte eMMC 3v3
U9	1	PCF8523TK/1,118 [NXP] Real Time Clock
U10	1	ATSHA204-MAHDA-T [Atmel] CryptoAuthentication Chip
U11	1	KSZ8081MNXCA TR [Micrel] Ethernet 10/100 MII PHY
U12	1	501AAA25M0000DAGR [SiLabs] 25MHz Oscillator 50ppm 2x2.5mm
U13	1	24AA02E48T-I/OT [Microchip] EEPROM EUI48 MAC I2C
U14	1	501AAA24M0000DAGR [SiLabs] 24MHz Oscillator 50ppm 2x2.5mm
U15, U16	2	TPD2E2U06DRLR [TI] ESD Transient Suppressor Dual 30kV
U17	1	ISL41387IRZ-T [Intersil] RS232/RS485 Dual Mode Transceiver
U18	1	IFX1050GVIOXUMA1 [Infineon] CAN Transceiver 1MBaud
U19	1	MAX98089ETN+ [Maxim] Audio Codec/Amplifier
U20	1	APDS-9002-021 [Avago] Ambient Light Sensor
U21	1	AT91SAM7S64C-MU [Atmel] MCU
U22	1	501AAA18M4320DAGR [SiLabs] 18.432MHz Osc 50ppm 2x2.5mm
X1	1	ABS07-32.768KHZ-T [Abracon] 12.5pF 20ppm

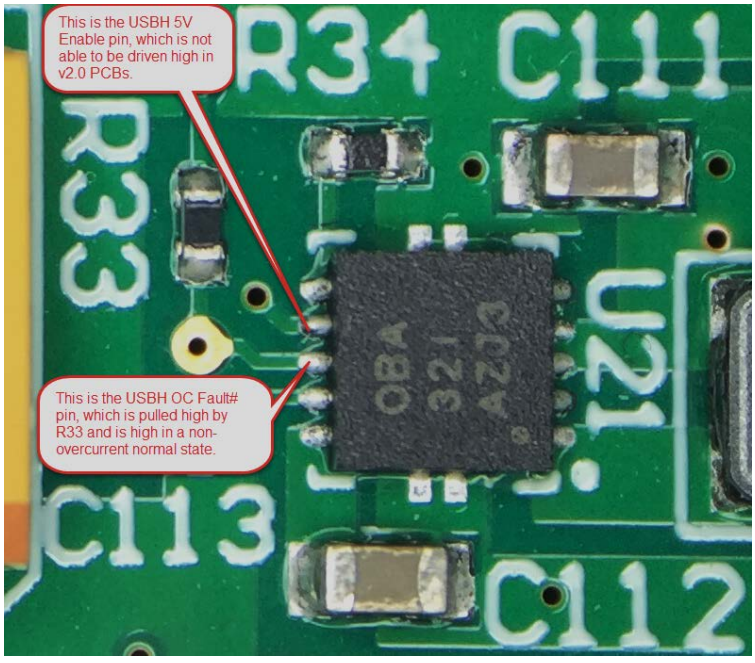
Chapter 13 - Post Production Modifications

13.1 – I/O Baseboard v2.0

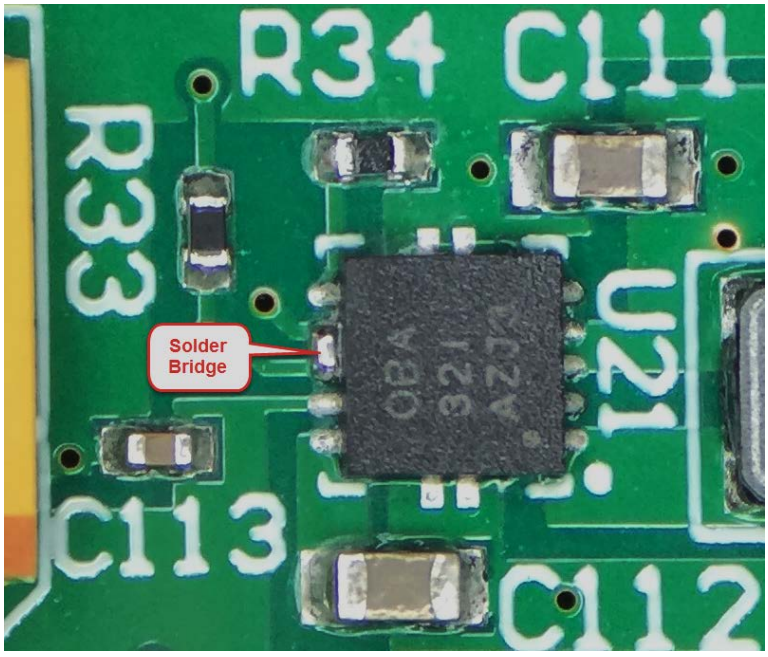
The I/O Baseboard v2.0 has the following post-production modification to address the issue described in the 5.5 - USB Host Power Subsystem section:

> On v2.0 units, P1.6 was incorrectly used to drive the USB Host Power Enable (RZM-USBH_5V_EN on the RZ Module; DIMM pin 132). This port is open drain only on the MCU, and is incapable of driving high and enabling the power supply. All v2.0 units should include a post-production modification connecting U21 pin 7 (ENUSB) to U21 pin 8 (FAULT#) to enable the USB supply during all non-overcurrent situations.

The unmodified v2.0 units have U21 (near the USB Host A Connector) like this:



The modified 2.0 units have the two pins 7 and 8 shorted as described above:



Chapter 14 - Additional Information

Further information available for this product can be found on the Renesas website at:

http://am.renesas.com/HiResGUI

General information on Renesas Microcontrollers can be found on the global Renesas website:

http://www.renesas.com/

Renesas Electronics America, Inc.
2801 Scott Boulevard
Santa Clara, CA 95050-2554, US