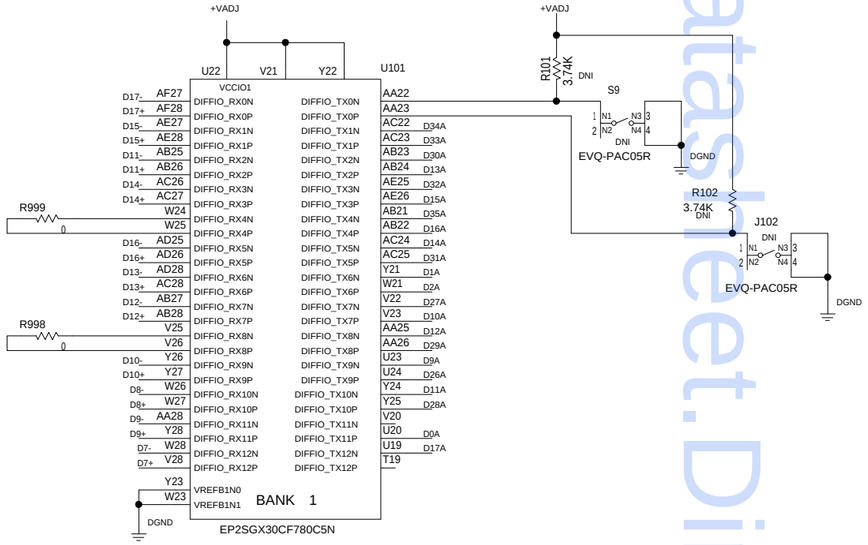
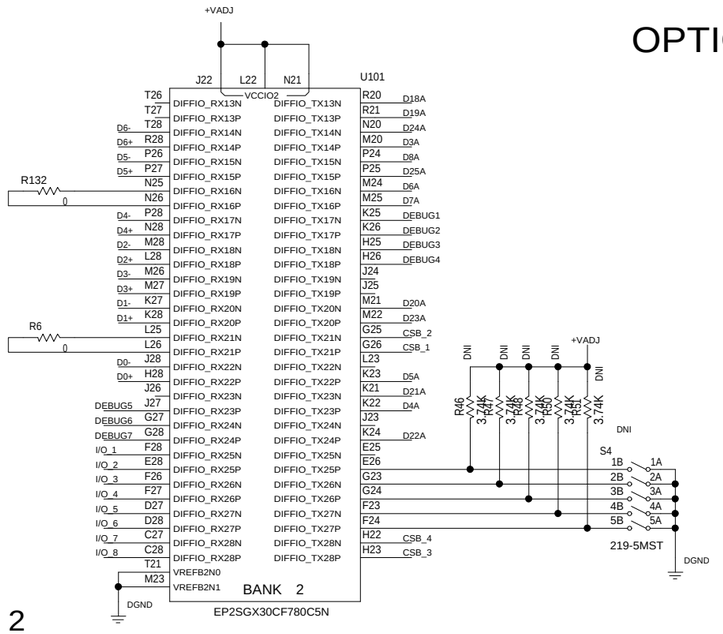
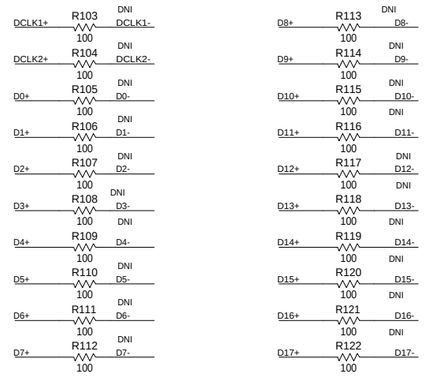
| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| | | | |

# PARALLEL I/O CONNECTIONS



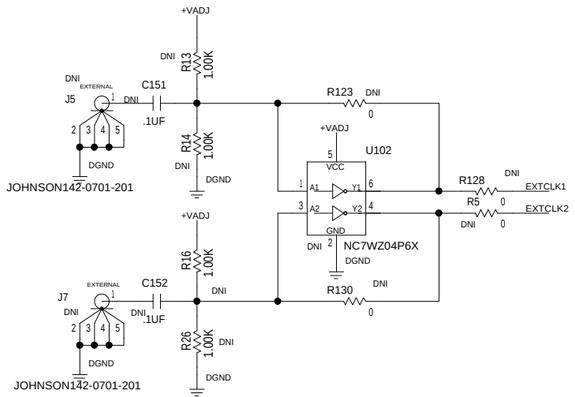




## OPTIONAL LVDS TERMINATIONS

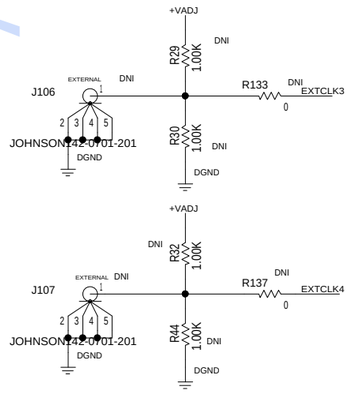



PLACE NEAR TYCO CONNECTORS
UNLESS EASY TO PLACE NEAR FPGA PINS

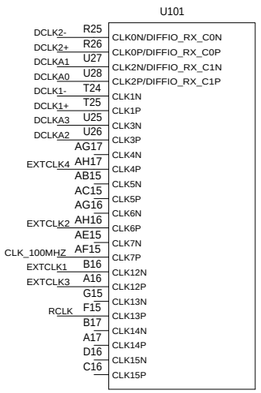
PINOUT IS FLEXIBLE WITHIN BANKS 1 AND 2
MUST OBSERVE POLARITY FOR LVDS +/- PAIRS
LVDS +/- PAIRS MUST BE ON RX PINS

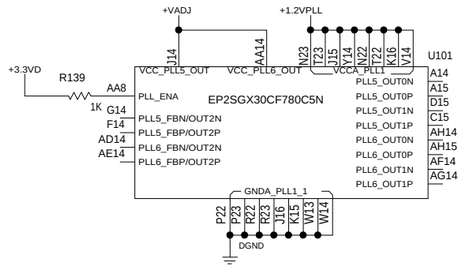



SINEWAVE INPUTS




SQUAREWAVE INPUT OR GENERAL I/O



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| | PTD ENGINEER <PTD_ENGINEER> | SIZE D / SCALE - / SHEET 1 OF 7 |

# SRAM CONNECTIONS

| REVISIONS | | | |
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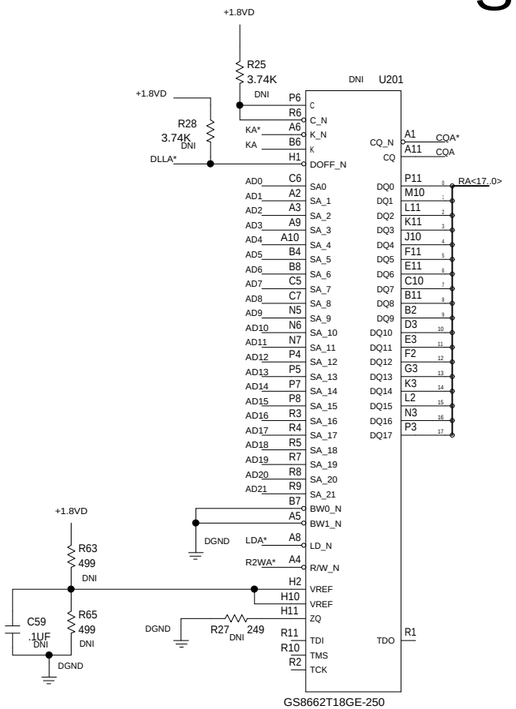
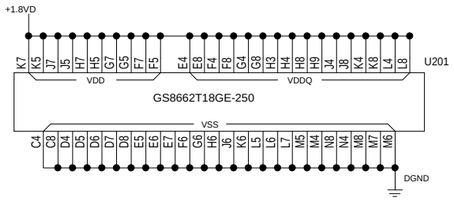
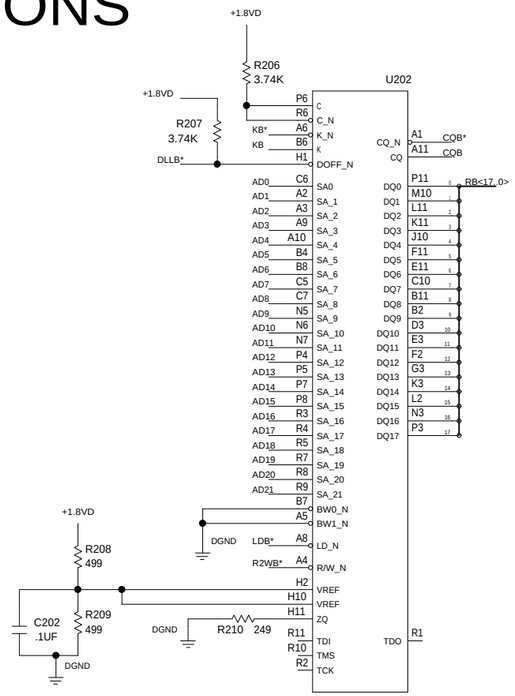
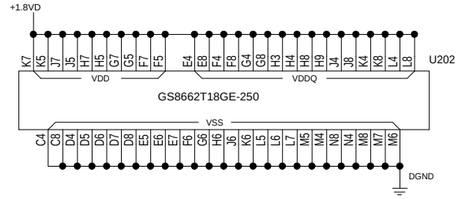
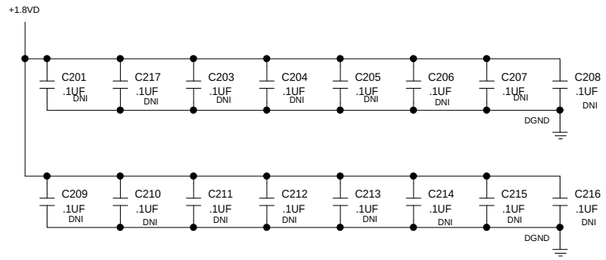
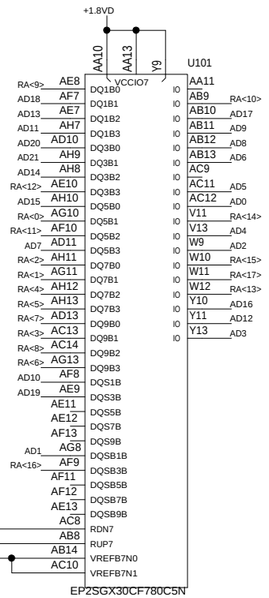


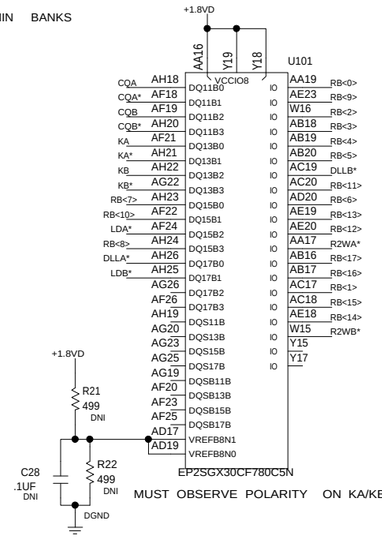



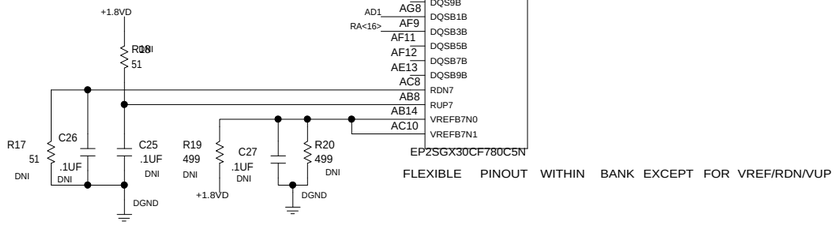




FLEXIBLE PINOUT WITHIN BANKS




MUST OBSERVE POLARITY ON KA/KB/CQA/CQB




FLEXIBLE PINOUT WITHIN BANK EXCEPT FOR VREF/RDN/VUP

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|---|---|---|---|
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| | PTD ENGINEER <PTD_ENGINEER> | SIZE D / SCALE - | SHEET 2 OF 7 |

# FPGA POWER AND DECOUPLING

## COPY DUT FOOTPRINT FROM ALTERA EVAL BOARD

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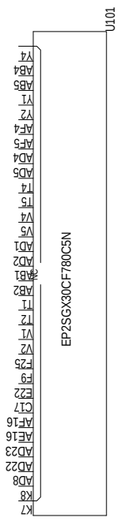
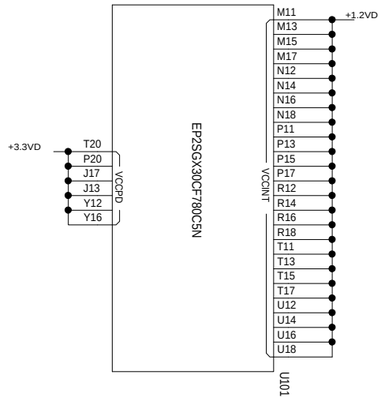
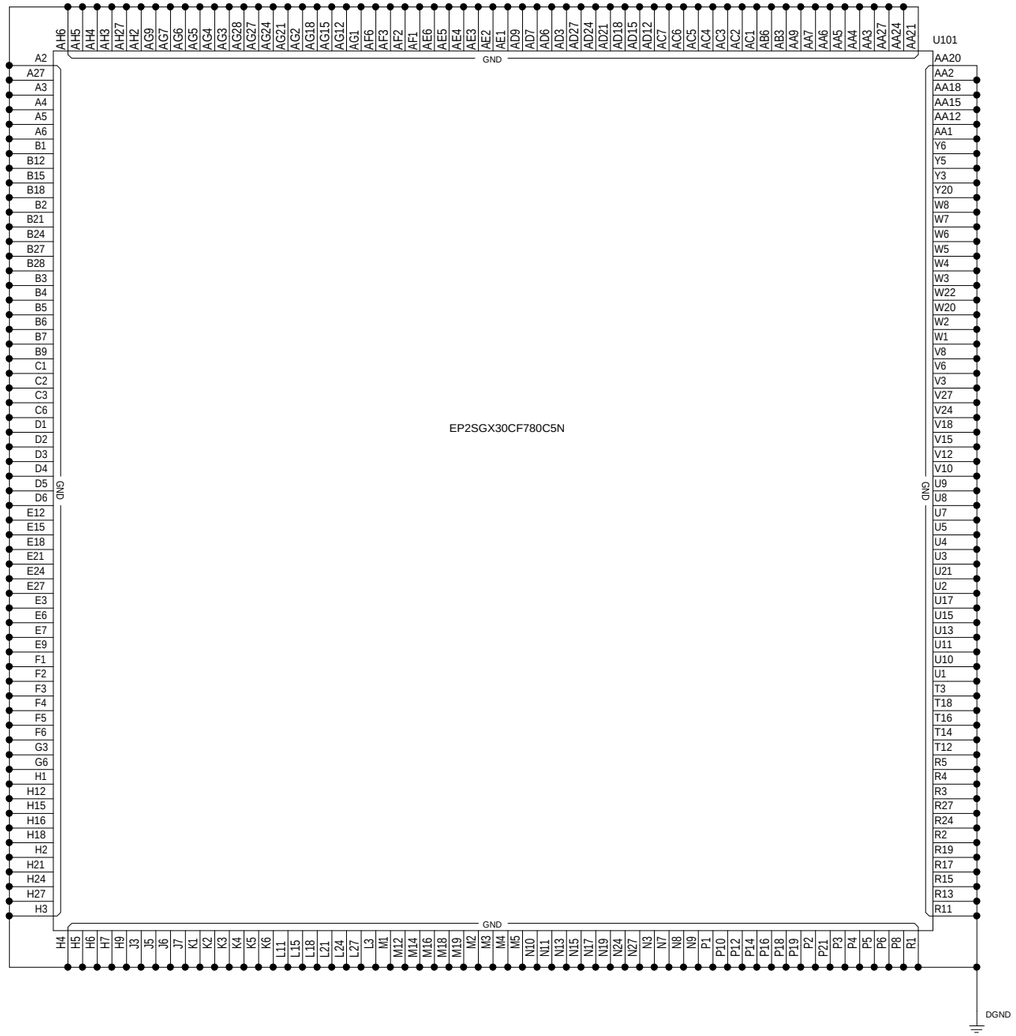
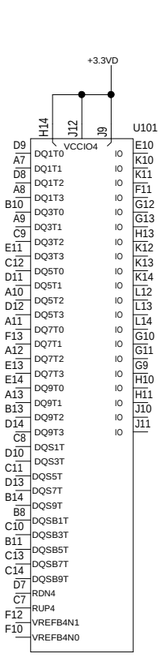
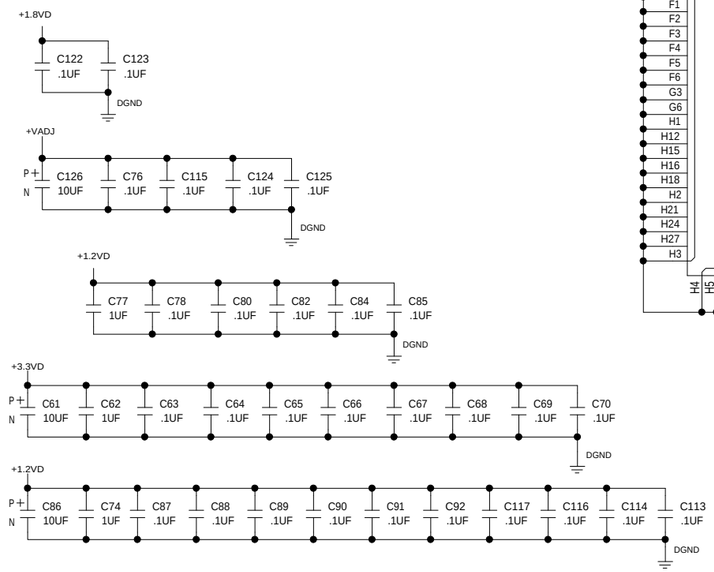



FPGA BYPASS CAP




ANALOG DEVICES



SCHEMATIC

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| DESIGN VIEW | DRAWING NO. | REV |
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| PTD ENGINEER <PTD_ENGINEER> | SIZE D / SCALE - | SHEET 3 OF 7 |

| REVISIONS | | | |
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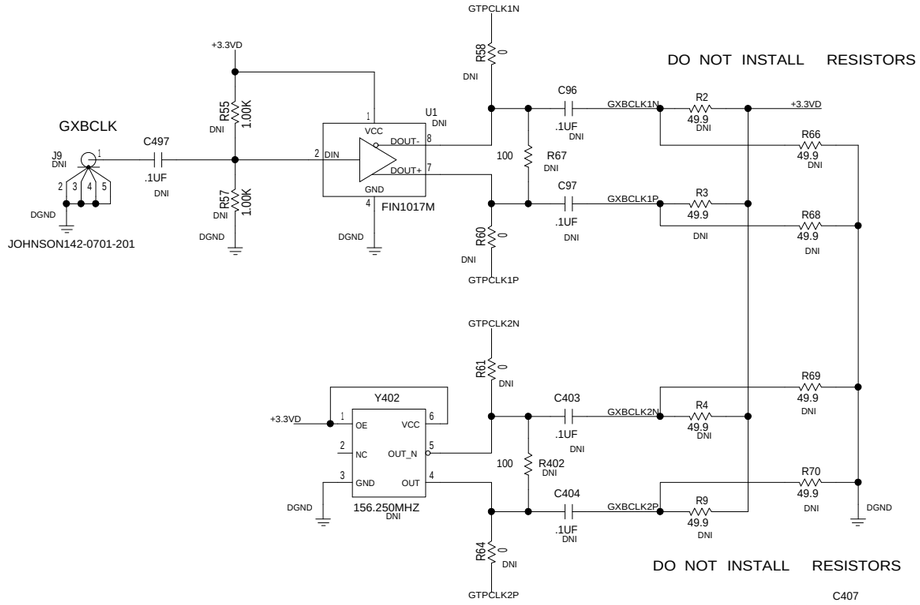
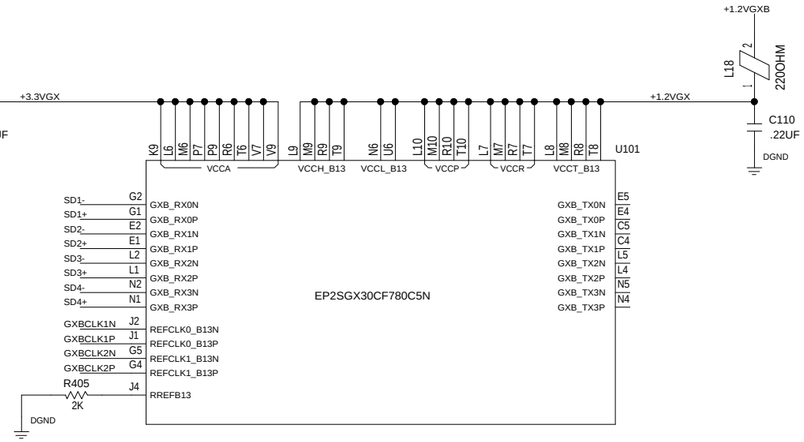
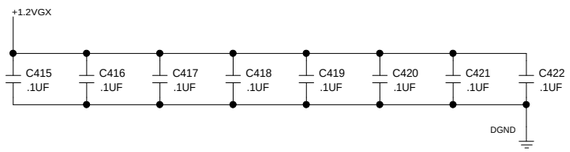
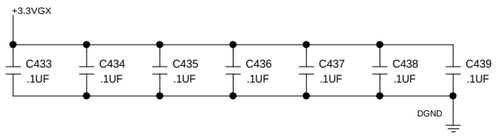
| REV | DESCRIPTION | DATE | APPROVED |
| | | | |

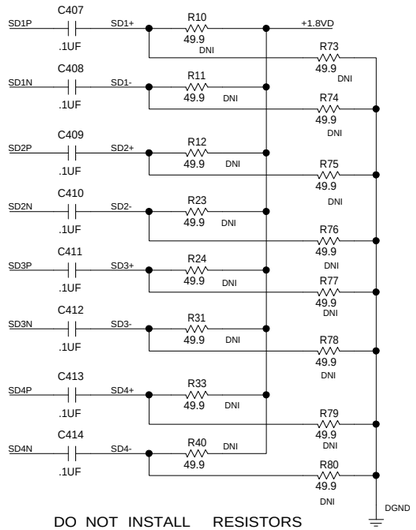
# GXB CONNECTIONS

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| REVISIONS | | | |
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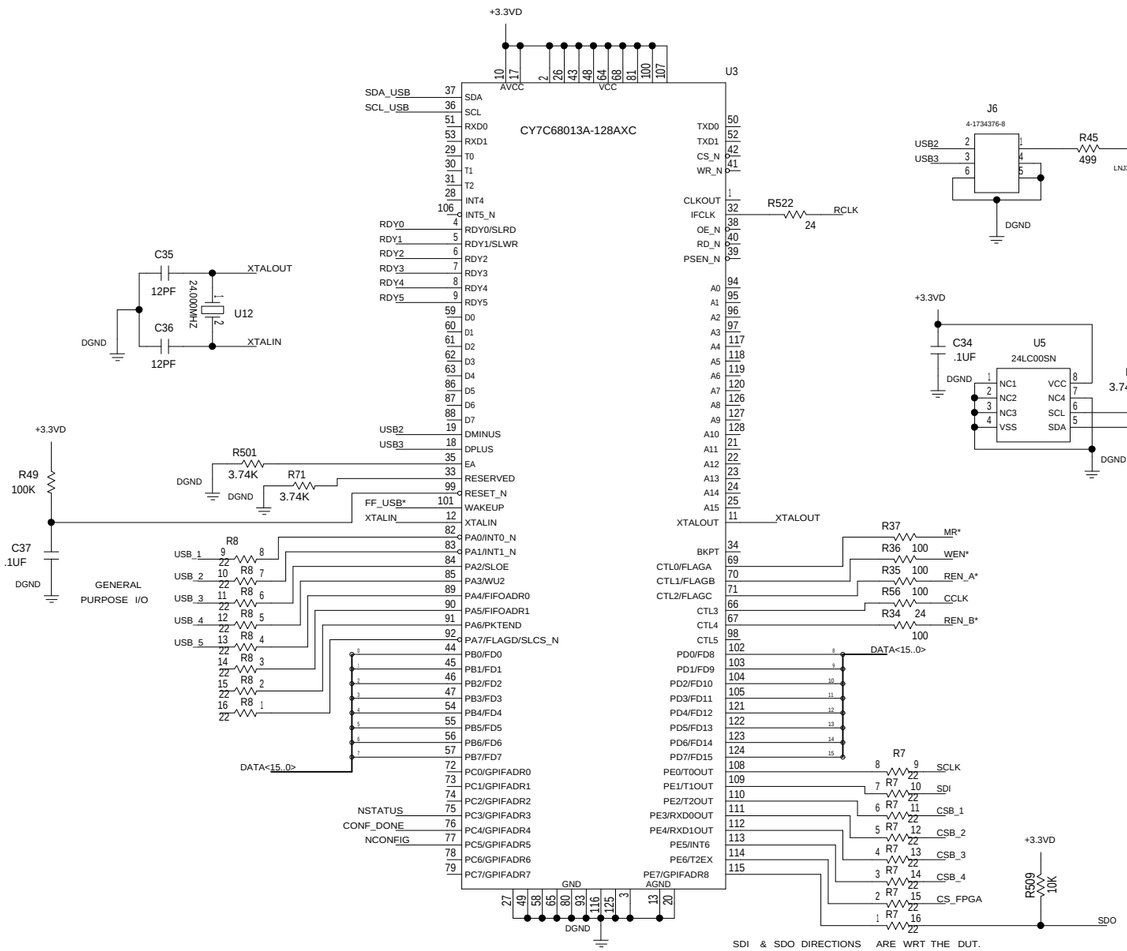
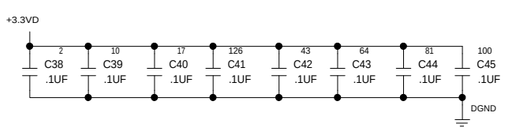
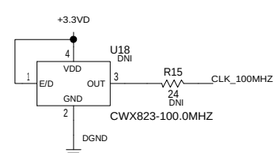
| | | | |

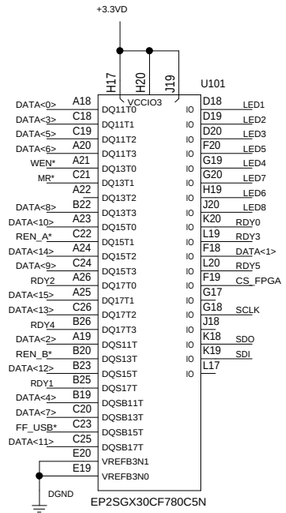
# USB CONNECTIONS



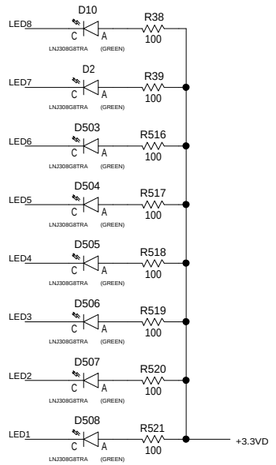




REFCLK OSCILLATOR FOR IDELAYCTRL




FLEXIBLE PINOUT WITHIN BANK

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# TYCO AND MISC FPGA CONNECTIONS

| REVISIONS | | | |
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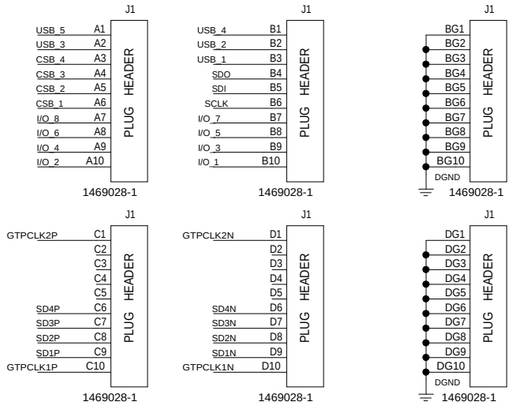


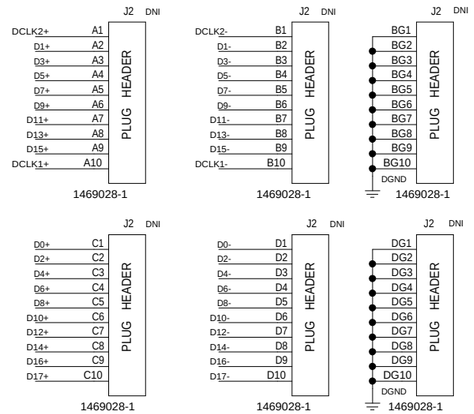


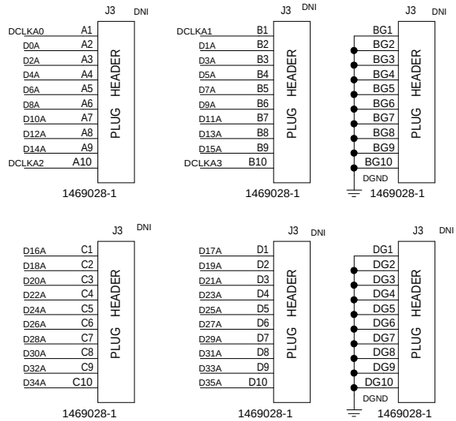


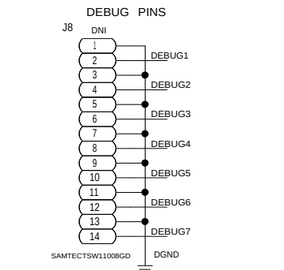


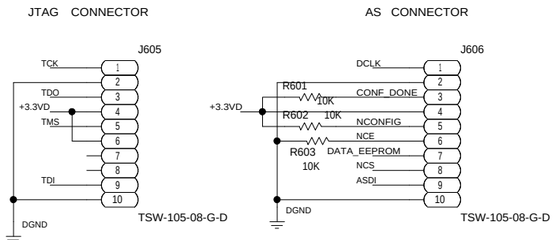


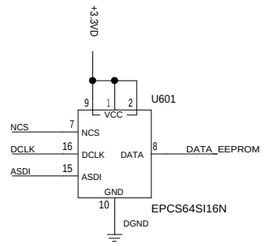


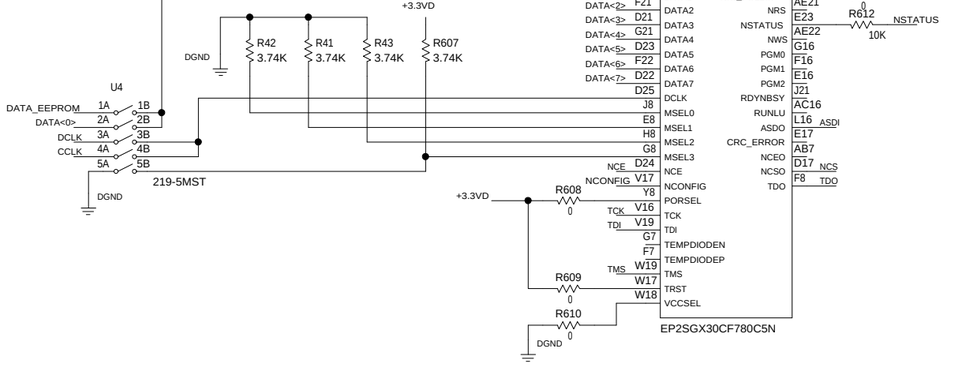




ANALOG DEVICES

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| DESIGN VIEW | DRAWING NO. | REV |
|---|---|---|
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| PTD ENGINEER | SIZE | SCALE | SHEET | OF |
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| <PTD_ENGINEER> | D | - | 6 | 7 |

| REVISIONS | | | |
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| REV | DESCRIPTION | DATE | APPROVED |
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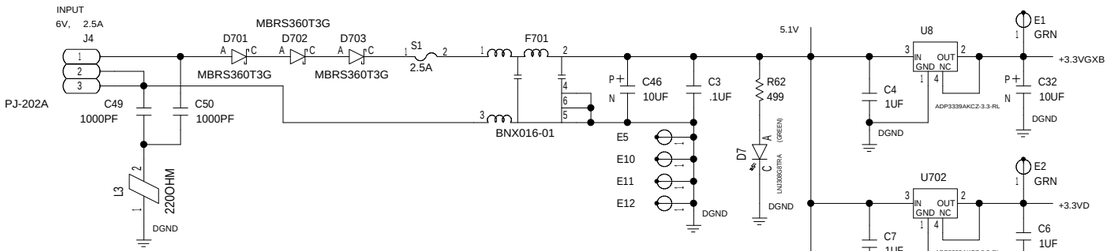
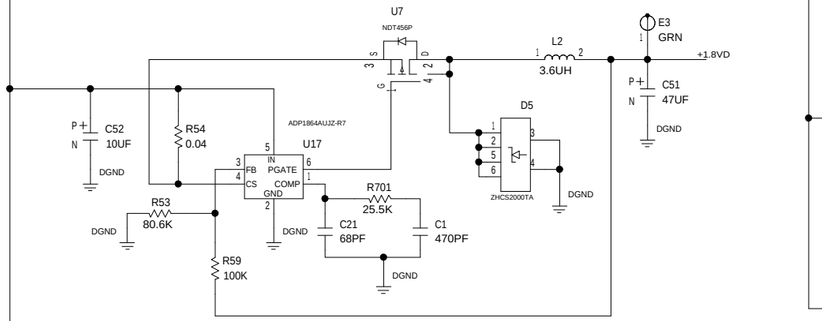
# POWER SUPPLIES

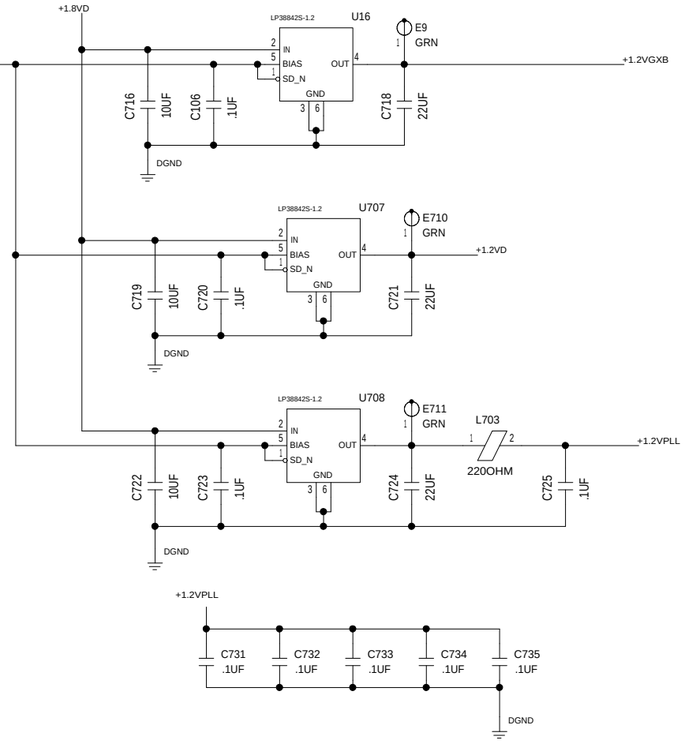



NOTE: PLACE GXB REGULATORS NEAR FPGA
ALL REGULATORS SHOULD BE PLACED NEAR FPGA
GXB REGULATORS HAVE PRIORITY
USE PROPER THERMAL RELIEF ON LAYOUT







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|---|---|---|
| ANALOG DEVICES | SCHEMATIC | |
| | <DRAWING_TITLE_HEADER> . <PRODUCT_1> | |
| DESIGN VIEW <DESIGN_VIEW> | DRAWING NO. - | REV - |
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