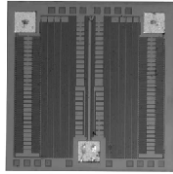


Megohm Center-Tap Chip Resistor



Product may not be to scale

FEATURES

- Wire bondable
- Resistance range total: 200 kΩ to 10 MΩ
- Center tap
- Chip size: 0.040 inches square
- Resistor material: Tantalum nitride, self-passivating
- Moisture resistant

The CTM resistor chips extends the resistance range to 10M in a center tap configuration while keeping the die size relatively small.

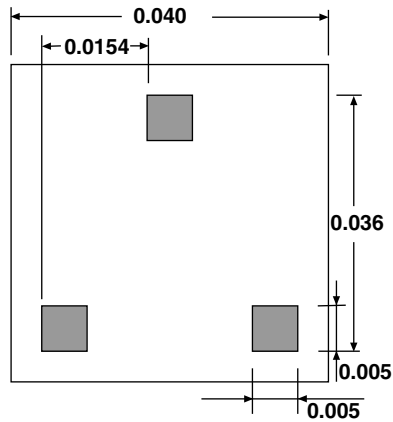
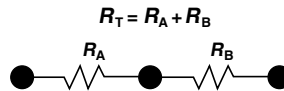
The CTMs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The CTMs are 100 % electrically tested and visually inspected to MIL-STD-883.

APPLICATIONS

Vishay EFI CTM tapped megohm resistor chips are designed for hybrid packages requiring high value, two resistor combinations.

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES AND TOLERANCES													
Tightest Standard Tolerance Available													
<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th colspan="2">PROCESS CODE</th> </tr> <tr> <th>CLASS H*</th> <th>CLASS K*</th> </tr> </thead> <tbody> <tr> <td>100</td> <td>130</td> </tr> <tr> <td>101</td> <td>131</td> </tr> <tr> <td>099</td> <td>129</td> </tr> <tr> <td>098</td> <td>128</td> </tr> </tbody> </table>		PROCESS CODE		CLASS H*	CLASS K*	100	130	101	131	099	129	098	128
PROCESS CODE													
CLASS H*	CLASS K*												
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101	131												
099	129												
098	128												
*MIL-PRF-38534 inspection criteria													

STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR Tracking Between Resistors	± 5 ppm/°C
Ratio/Ratio, R_A/R_B : Tolerance	1 ± 1 % standard
Noise	- 12 dB typ.
Moisture Resistance, MIL-STD-202, Method 106	± 0.5 % max. $\Delta R/R$
Stability, 1000 h, + 125 °C, 10 mW	± 0.5 % max. absolute ± 0.005 % ratio
Operating Temperature Range	- 55 °C to + 125 °C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	± 0.25 % max. $\Delta R/R$
High Temperature Exposure, + 150 °C, 100 h	± 0.5 % max. $\Delta R/R$
Dielectric Voltage Breakdown	200 V
Insulation Resistance	10 ¹² min.
Operating Voltage	100 V max.
DC Power Rating at + 70 °C (Derated to Zero at + 175 °C)	20 mW each resistor
5 x Rated Power Short-Time Overload, + 25 °C, 5 s	± 0.25 % max. $\Delta R/R$

DIMENSIONS in inches

SCHEMATIC


MECHANICAL SPECIFICATIONS in inches	
PARAMETER	
Chip Size	0.040 x 0.040 ± 0.002 (1.02 x 1.02 ± 0.05 mm)
Chip Thickness	0.010 ± 0.002 (0.254 ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Tantalum nitride, self-passivating
Bonding Pad Size	0.005 x 0.005 (0.127 x 0.127 mm)
Number of Pads	3
Pad Material	10 kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

Options: Gold back for eutectic die attach
 Custom ratios available up to 4:1 R_A/R_B - consult Vishay EFI Sales
 Consult Applications Engineer

ORDERING INFORMATION					
Example: 100 % visual, 2 MΩ, ± 1 %, ± 100 ppm/°C TCR, aluminum pads, class H visual inspection					
W	CTM	101	2000	3	F
INSPECTION/ PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
W = 100 % visually inspected parts in matrix trays per MIL-STD-883 X = Sample, visually inspected parts loaded in matrix trays (4 % AQL)		See Process Code table	Use first 4 digits significant digits of the resistance (R_T)	2 = 100 3 = 1000 4 = 10 000	B = 0.1 % C = 0.2 % D = 0.5 % F = 1.0 % G = 2.0 % H = 2.5 % J = 5.0 % K = 10 %



Disclaimer

All product specifications and data are subject to change without notice.

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