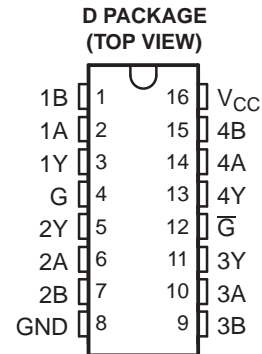


FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendations V.10 and V.11**
- **±7-V Common-Mode Range With ±200-mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typ**
- **Operates From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output-Enable Inputs**
- **Input Impedance . . . 12 kΩ Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32**



- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DESCRIPTION/ORDERING INFORMATION

The AM26LS32A is a quadruple differential line receiver for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs always are high.

The AM26LS32A incorporates an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay, however, this does not affect interchangeability in most applications.

The AM26LS32AM is characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Tape and reel	AM26LS32AMDREP	26LS32EP

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



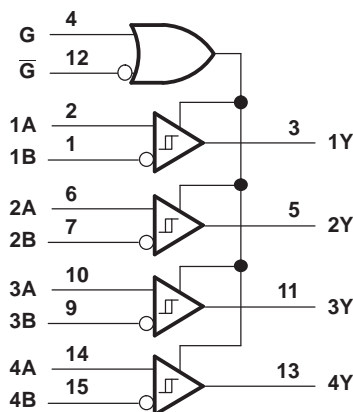
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE⁽¹⁾
 (each receiver)

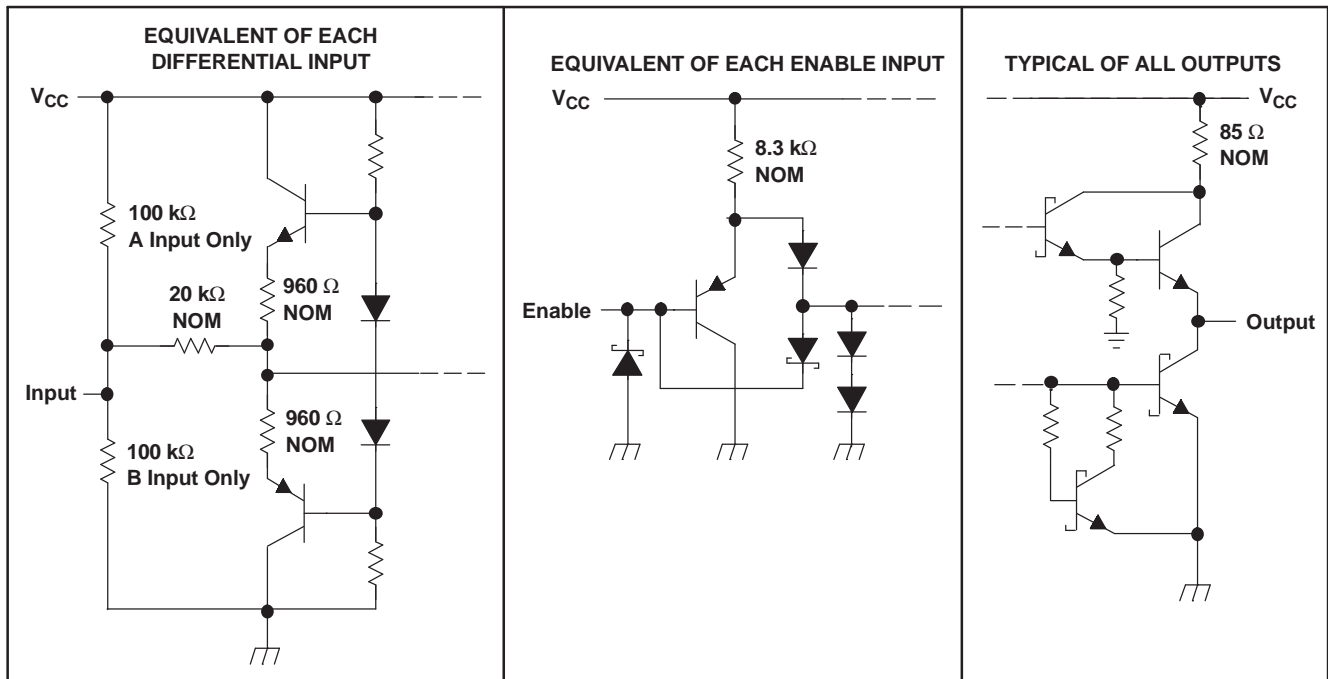
DIFFERENTIAL A – B	ENABLES		OUTPUT Y
	G	\bar{G}	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant,
 Z = high impedance (off)

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS OF INPUTS AND OUTPUTS



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾		7	V
V_I	Input voltage	Any differential input		±25
		Other inputs		7
V_{ID}	Differential input voltage ⁽³⁾		±25	V
Continuous total power dissipation				See Dissipation Rating Table
θ_{JA}	Package thermal impedance ⁽⁴⁾	D package		111.6
T_{stg}	Storage temperature range ⁽⁵⁾	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground terminal.
- (3) Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	1075 mW	8.9 mW/°C	672 mW	179 mW

AM26LS32AM-EP QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS730–OCTOBER 2006

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
V_{IC} Common-mode input voltage			± 7	V
I_{OH} High-level output current			-440	μ A
I_{OL} Low-level output current			8	mA
T_A Operating free-air temperature	-55		125	$^{\circ}$ C

Electrical Characteristics

over recommended ranges of V_{CC} , V_{IC} , and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = V_{OH}$ min, $I_{OH} = -440 \mu$ A			0.2	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.45$ V, $I_{OL} = 8$ mA	-0.2 ⁽²⁾			V
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
V_{IK} Enable-input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18$ mA			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{ID} = 1$ V, $V_{I(G)} = 0.8$ V, $I_{OH} = -440 \mu$ A	2.5			V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{ID} = -1$ V, $V_{I(G)} = 0.8$ V	$I_{OL} = 4$ mA		0.4	V
		$I_{OL} = 8$ mA		0.45	
I_{OZ} Off-state (high-impedance state) output current	$V_{CC} = \text{MAX}$	$V_O = 2.4$ V		20	μ A
		$V_O = 0.4$ V		-20	
I_I Line input current	$V_I = 15$ V,	Other input at -10 V to 15 V		1.2	mA
	$V_I = -15$ V,	Other input at -15 V to 10 V		-1.7	
$I_{I(EN)}$ Enable input current	$V_I = 5.5$ V			100	μ A
I_{IH} High-level enable current	$V_I = 2.7$ V			20	μ A
I_{IL} Low-level enable current	$V_I = 0.4$ V			-0.36	mA
r_I Input resistance	$V_{IC} = -15$ V to 15 V, One input to ac ground	12	15		k Ω
I_{OS} Short-circuit output current ⁽³⁾	$V_{CC} = \text{MAX}$	-15		-85	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, All outputs disabled		52	70	mA

(1) All typical values are at $V_{CC} = 5$ V, $T_A = 25^{\circ}$ C, and $V_{IC} = 0$.

(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

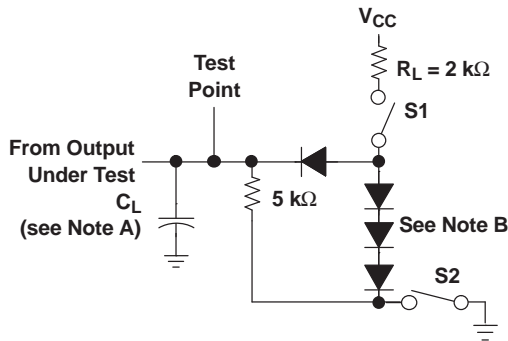
(3) Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics

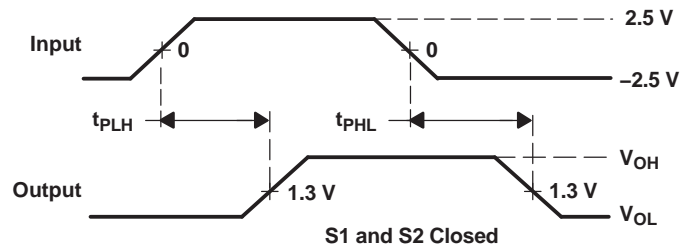
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15\text{ pF}$,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35	
t_{PZH}	Output enable time to high level	$C_L = 15\text{ pF}$,	See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level				20	25	
t_{PHZ}	Output disable time from high level	$C_L = 5\text{ pF}$,	See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level				30	40	

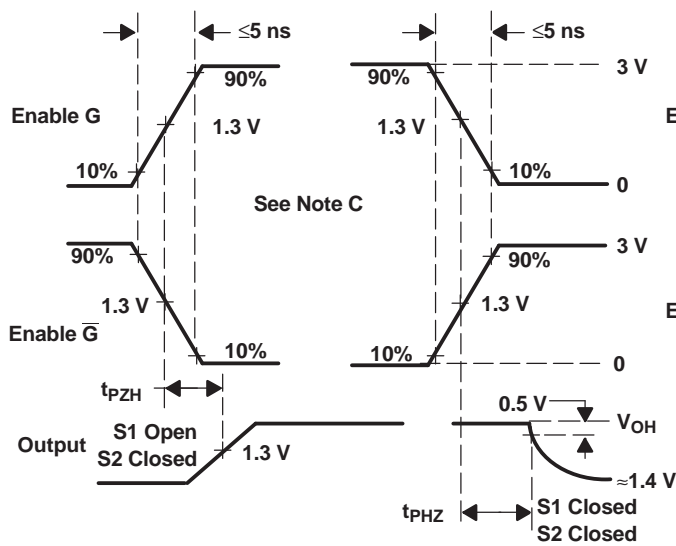
PARAMETER MEASUREMENT INFORMATION



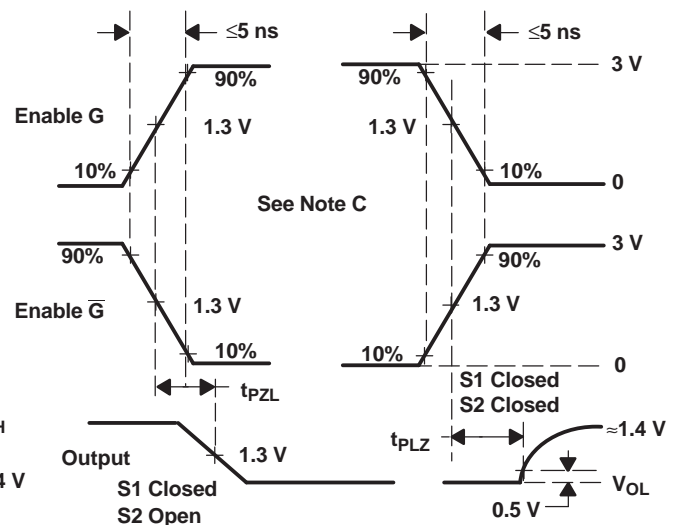
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH} , t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ} , t_{PZH}

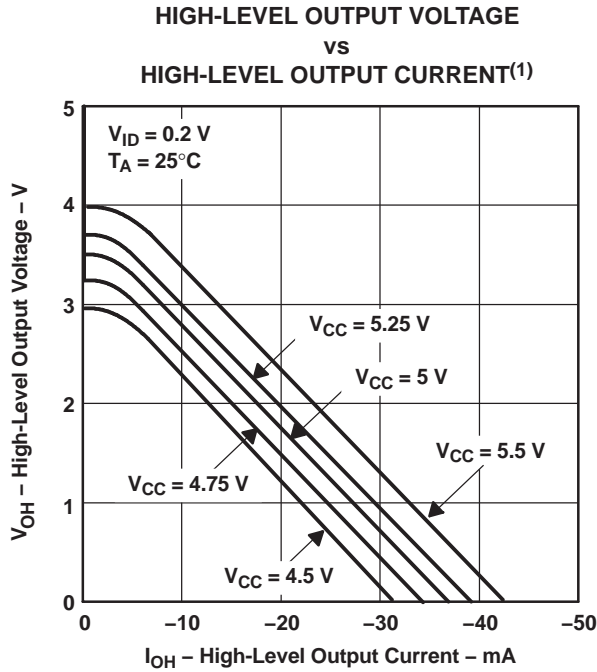


VOLTAGE WAVEFORMS FOR t_{PLZ} , t_{PZL}

- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Enable G is tested with \bar{G} high; \bar{G} is tested with G low.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



(1) $V_{CC} = 5.5$ V and $V_{CC} = 4.5$ V applies to M-suffix devices only.

Figure 2.

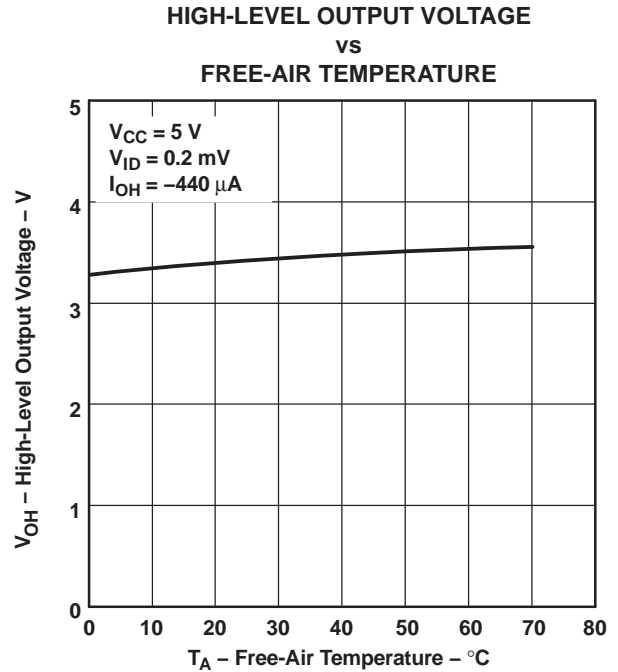


Figure 3.

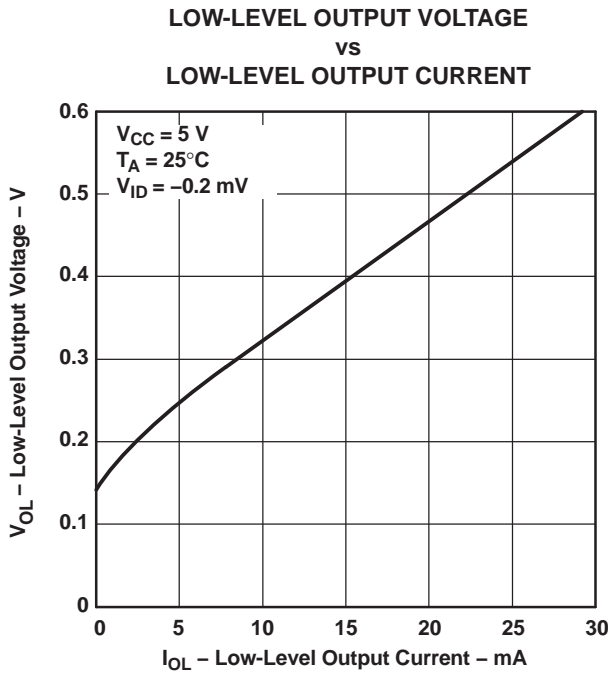


Figure 4.

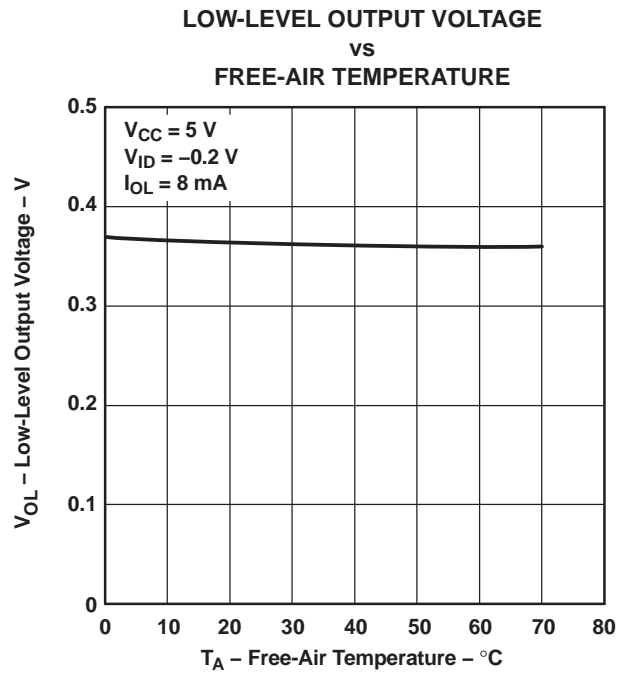


Figure 5.

TYPICAL CHARACTERISTICS (continued)

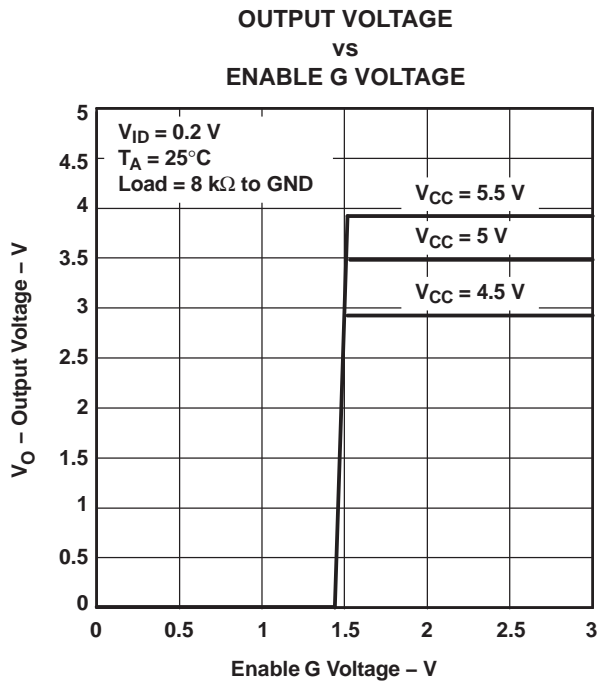


Figure 6.

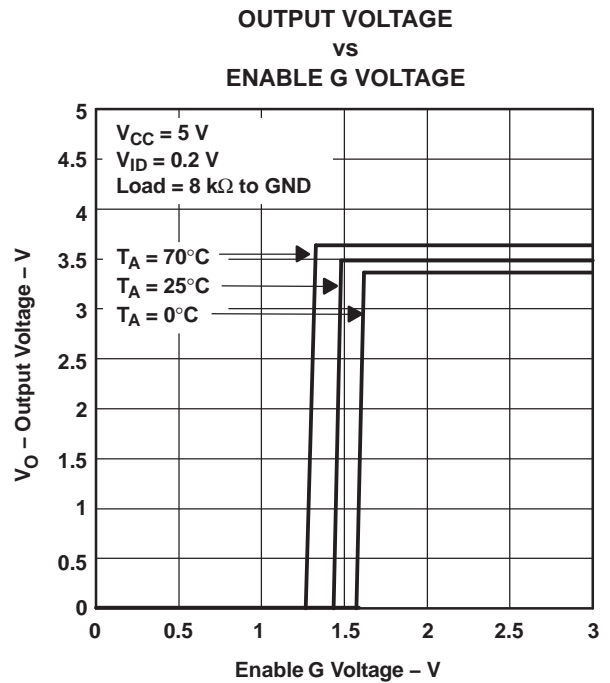


Figure 7.

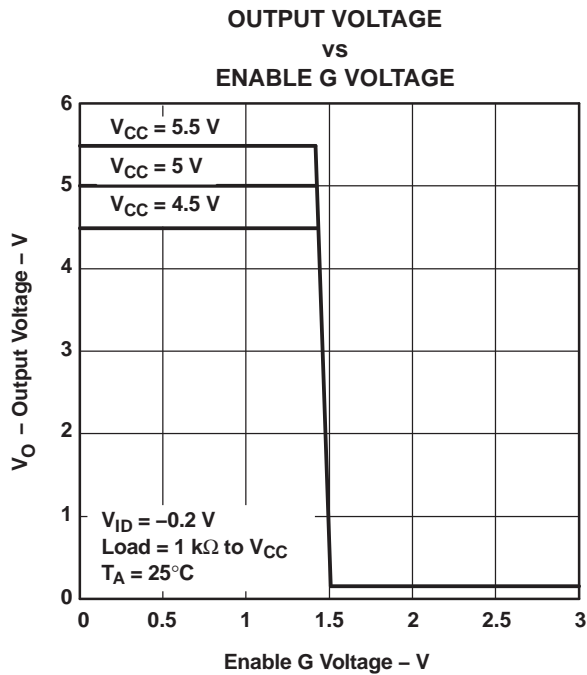


Figure 8.

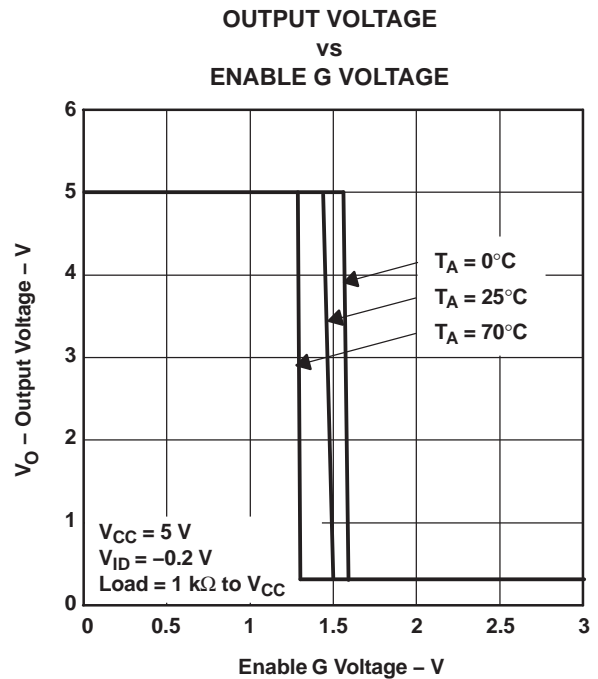


Figure 9.

TYPICAL CHARACTERISTICS (continued)

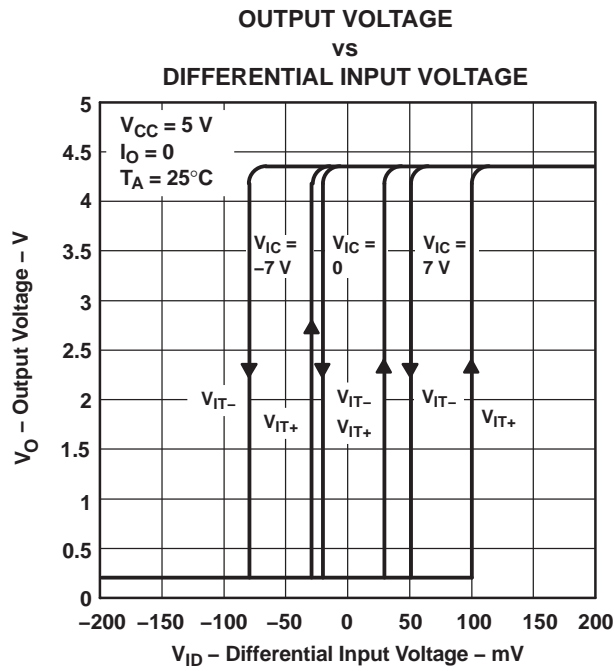


Figure 10.

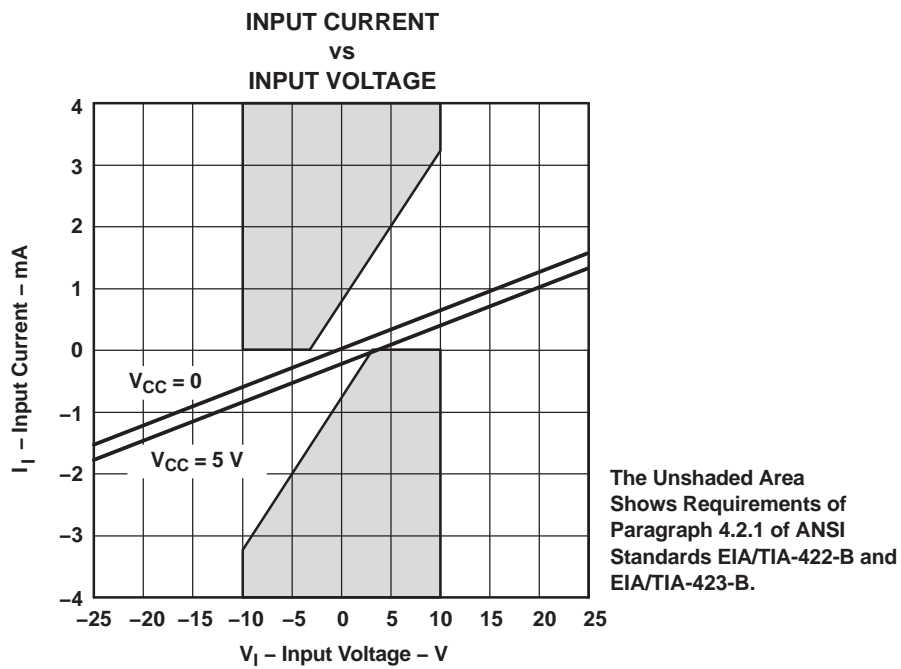


Figure 11.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
AM26LS32AMDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/07603-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

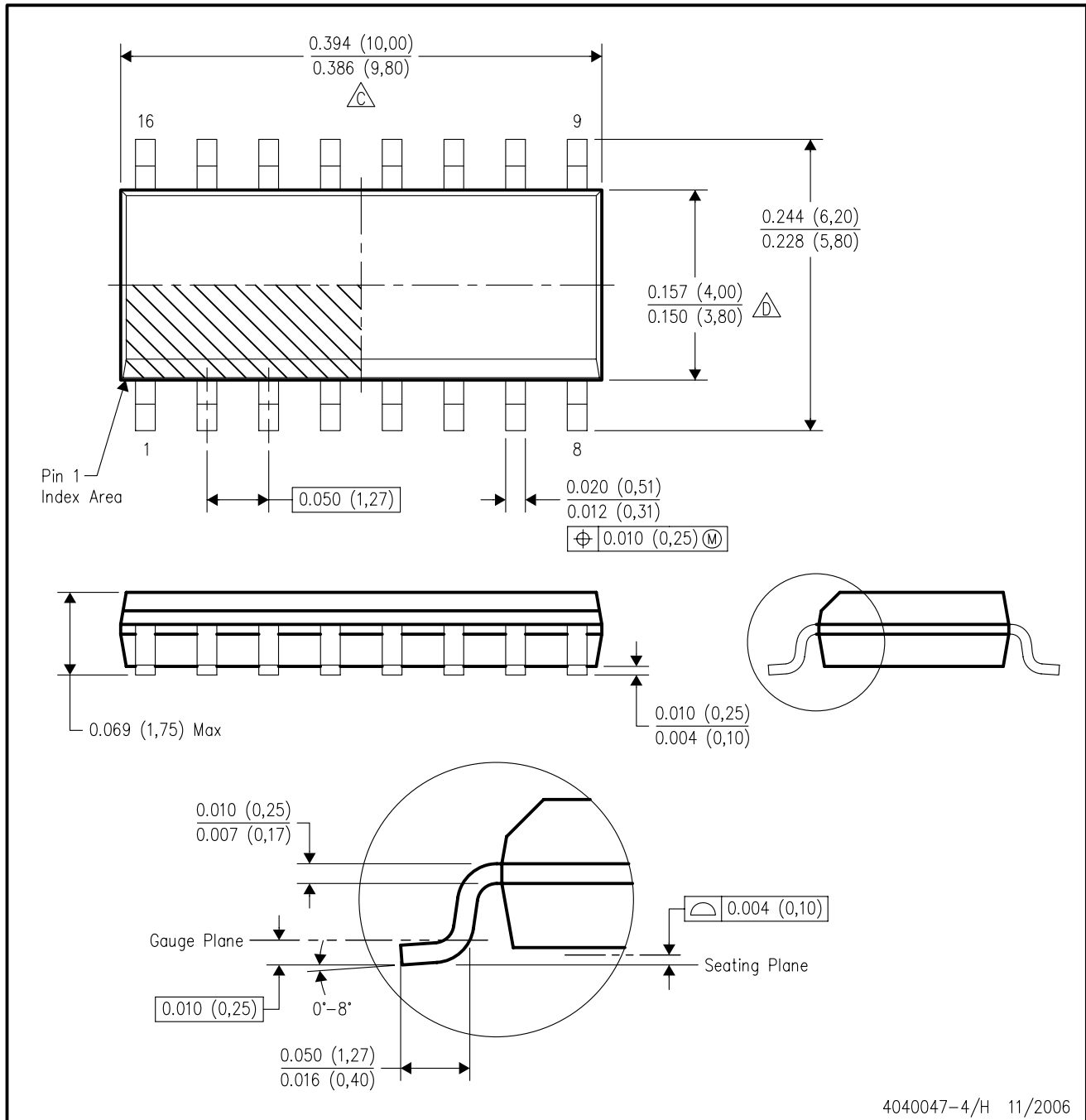
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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