SIEMENS

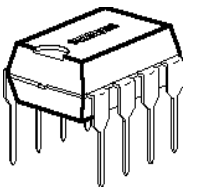
Control IC for Switched-Mode Power Supplies using MOS-Transistors

TDA 4605

Bipolar IC

Features

- Fold-back characteristic provides overload protection for external components
- Burst operation under short-circuit conditions
- Loop error protection
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage compensation of overload point
- Soft-start for quiet start-up
- Chip-over temperature protection (thermal shutdown)
- On-chip parasitic transformer oscillation suppression circuitry



P-DIP-8-1

Type	Ordering Code	Package
TDA 4605	Q67000-A8078	P-DIP-8-1

The IC TDA 4605-1 controls the MOS-power transistor and performs all necessary regulation and monitoring functions in free running flyback converters. Since good load regulation over a wide load range is attained, this IC is applicable tor consumer and industrial power supplies.

The serial circuit of power transistor and primary winding of the flyback transformer is connected to the input voltage. During the switch - on period of the transistor, energy is stored in the transformer and during the switch - off period it is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent ot load variations.

The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period.

In the different load ranges the switched-mode power supply (SMPS) behaves as follow:

No load operation:

The power supply unit oscillates at its resonant frequency typ. 100 kHz to 200 kHz. Depending upon the transformator windings the output voltage can be slightly above nominal value.

Nominal operation:

The switching frequency declines with increasing load and decreasing AC-voltage. The duty factor primarly depends on the AC-voltage. The output voltage is load-dependent only.

Overload point:

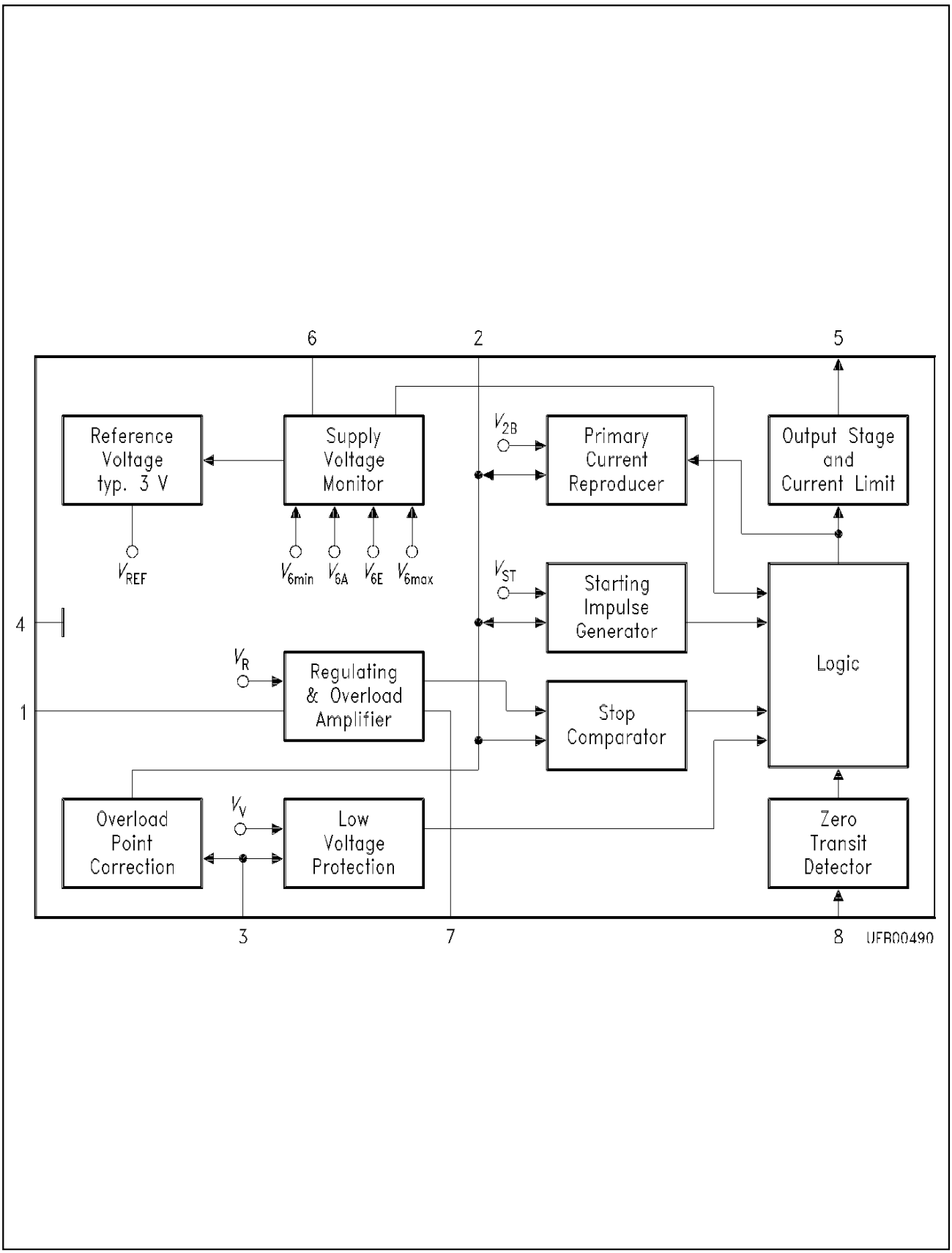
Maximal output power is available at this point ot the output characteristic.

Overload:

The energy transferred per operation cycle is limited at the top. Therefore the output voltage declines by secondary overloading.

Pin Definitions and Functions

Pin No.	Function
1	**Regulating Voltage:** Information input concerning secondary voltage. By comparing the regulating voltage - obtained from the regulating winding ot the transformer - with the internal reference voltage, the output impulse width on pin 5 is adapted to the load ot the secondary side (normal, overload, short-circuit, no load).
2	**Primary Current Simulation:** Information input regarding the primary current. The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means ot external RC-element. When a value is reached that is derived from the regulating voltage at pin 1, the output impulse at pin 5 is terminated. The RC-element serves to set the maximum power at the overload point set.
3	**Input for Primary Voltage Monitoring:** In the normal operation V_3 is moving between the thresholds V_{3H} and V_{3L} $(V_{3H} > V_3 > V_{3L})$. $V_3 < V_{3L}$: SMPS is switched OFF (line voltage too low). $V_3 > V_{3H}$: Compensation of the overload point regulation (controlled by pin 2) starts at $V_{3H} : V_{3L} = 1.7$.
4	**Ground**
5	**Output:** Push-pull-output provides $\pm$ 1 A for rapid charge and discharge of the gate capacitance ot the power MOS-transistor.
6	**Supply Voltage Input:** A stable internal reference voltage V_{REF} is derived from the supply voltage also the switching thresholds V_{6A} , V_{6E} , $V_{6\ max}$ and $V_{6\ min}$ for the supply voltage detector. If $V_6 > V_{6E}$ then V_{REF} is switched on and swiched off when $V_6 < V_{6A}$. In addition the logic is only enable for $V_{6\ min} < V_6 < V_{6\ max}$.
7	**Soft-Start:** Input for soft-start. Start-up will begin with short pulses by connecting a capacitor from pin 7 to ground.
8	**Zero Detector:** Input tor the oscillation feedback. After starting oscillation, every zero transit of the feedback voltage (falling edge) triggers an output impulse at pin 5. The trigger threshold is at + 50 mV typical.



Block Diagram

Circuit Description

Application Circuit

Application circuit shows a flyback converter for video recorders with a power rating of 50 W. The circuit is designed as a wide-range power supply tor AC-line voltages ot 90 to 270 V. The AC-input voltage is rectified by bridge rectifier GR1 and smoothed by C_1 . The NTC limits the rush in current.

In the period before the switch-on threshold is reached the IC is supplied via resistor R_1 ; during the start-up phase it uses the energy stored in C_2 , under steady-state conditions the IC receives its supply voltage from transformer winding n_1 via diode D1. The switching transistor T1 is a BUZ 90. The parallel-connected capacitor C_3 and the inductance ot primary winding 112 determine the system resonance frequency. The R_2 - C_4 - D2 circuitry limits overshoot peaks, and R_3 protects the gate of T1 against static charges.

While T1 conducts, the current rise in the primary winding depends on the winding's inductance and the V_{C1} voltage. A voltage reproduction ot the current rise is tabbed using the R_4 - C_5 network and forwarded into pin 2 ot the IC. The RC-time constant ot R_4 , R_5 must be dimensioned correctly in order to prevent driving the transformer core into saturation.

The R_{10}/R_{11} divider ratio provides the line voltage threshold controlling the undervoltage control circuit in the IC. The voltage present at pin 3 also determines the overload. Detection of overload together with the current characteristic at pin 2 controls the on period ot T1. This keeps the cut-off point stable even with higher AC-line voltages.

Regulation of the switched-mode power supply is via pin 1. The control voltage of winding n_1 during the off-period of T1 is rectified by D3, smoothed by C_6 and stepped down at an adjustable ratio by R_5 , R_6 and R_7 . The R_6 - C_7 network suppresses parasitic overshoots (transformer oscillation). The peak voltage at pin 2, and thus the primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the transformer has supplied its energy to the load, the control voltage passes through zero. The IC detects the zero crossing via series resistors R_9 connected to pin 8. But zero crossings are also produced by transformer oscillation after T1 has turned off if output is short-circuited. Therefore the IC ignores zero crossings occurring within a specitied period of time after T1 turn-off.

The capacitor C_8 connected to pin 7 causes the power supply to be started with shorter pulses to keep the operating ftrequency outside the audible range during start-up.

On the secondary side, tive output voltages are produced across winding n_3 to n_7 rectified by D4 to D8 and smoothed by C_9 to C_{13} . Resistors R_{12} , R_{14} and R_{19} to R_{21} are used as bleeder resistors. Fusable resistors R_{15} to R_{18} protect the rectifiers against short circuits in the output circuits, which are designed to supply only small loads.

Block Diagram

Pin 1

The regulating voltage forwarded to this pin is compared with a stable internal reference voltage V_R in the **regulating and overload amplifier**. The output of this stage is ted to the stop comparator.

Pin 2

A voltage proportional to the drain current ot the switching transistor is generated there by the external RC-combination in conjunction with the **primary current transducer**. The output of this transducer is controlled by the logic and referenced to the internal stable voltage V_{2B} . If the voltage V_2 exceeds the output voltage of the regulating amplifier, the logic is reset by the stop comparator and consequently the output ot pin 5 is switched to low potential. Further inputs tor the logic stage are the output for the **start impulse generator** with the stable reference potential V_{ST} and the **supply voltage monitor**.

Pin 3

The down-divide primary voltage applied there stabilizes the overload point. In addition the logic is disabled in the event of low voltage by comparison with the internal stable voltage V_V in the primary voltage monitor block.

Pin 4

Ground

Pin 5

In the output stage the output signals produced by the logic are shifted to a leved suitable for MOS-power transistors.

Pin 6

From the supply voltage V_6 are derived a stable internal reference V_{REF} and the switching threshold V_{6A} , V_{6E} , $V_{6\,max}$ and $V_{6\,min}$ for the supply voltage monitor. All reference values (V_R , V_{2B} , V_{ST}) are derived from V_{REF} . If $V_6 > V_{VE}$ the V_{REF} is switched on and switched off when $V_6 < V_{6A}$. In addition, the logic is released only for $V_{6\,min} < V_6 < V_{6\,max}$.

Pin 7

The output of the overload amplifier is connected to pin 7. A load on this output causes a reduction in maximal impulse duration. This function can be used to implement a soft start, when pin 7 is connected to ground by a capacitor.

Pin 8

The zero detector controlling the logic block recognizes the transformer being discharged by positive to negative zero crossing of pin 8 voltage and enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse (double-pulsing), because an internal circuit inhibits the zero detector for a finite time t_{UL} after the end of each pulse.

Start-Up Behaviour

The start-up behaviour of the application circuit per sheet 48 is represented on sheet 50 for a line voltage barely above the lower acceptable limit voltage value (without soft-start). After applying the line voltage at the time t_0 to the tollowing voltages built up:

- V_6 corresponding to the half-wave charge current over R_1
- V_2 to $V_{2\,max}$ (typically 6.6 V)
- V_3 to the value determined by the divider R_{10}/R_{11}.

The current drawn by the IC in this case is less than 1.6 mA. If V_6 reaches the threshold V_{6E} (time point t_1), the IC switches on the internal reference voltage. The currentdraw max. rises to 12 mA. The primary current- voltage reproducer regulates V_2 down to V_{2E} and the starting impulse generator generates the starting impulses from time point t_5 to t_6. The feedback to pin 8 starts the next impulse and so on. All impulses including the starting impulse are controlled in width by regulating voltage of pin 1. When switching on this corresponds to a short-circuit event, i.e. $V_1 = 0$. Hence the IC starts up with "short-circuit impulses" to assume a width depending on the regulating voltage feedback (the IC operates in the overload range). The maximum pulse width is reached at time point t_2 ($V_2 = V_{2\,max}$). The IC operates at the overload point. Thereafter the peak values ot V_2 decrease rapidly, as the IC is operating within the regulation range. The regulating loop has built up. If voltage V_6 falls below the switch-off threshold $V_{6\,min}$ before the reversal point is reached, the starting attempt is aborted (pin 5 is switched to low). As the IC remains switched on, V_6 further decreases to V_6. The IC switches off; V_6 can rise again (time point 14) and a new start-up attempt begins at time point t_1. If the rectified alternating line voltage (primary voltage) collapses during load, V_3 can fall below V_{3A}, as is happening at time point t_3 (switch-on attempt when voltage is too low). The primary voltage monitor then clamps V_3 to V_{3S} until the IC switches off ($V_6 < V_{6A}$). Then a new start-up attempt begins at time point t_1.

Regulation, Overload and No-Load Behaviour

When the IC has started up, it is operating in the regulation range. The potential at pin 1 typically is 400 mV. If the output is loaded, the regulation amplifier allows broader impulses (V_5 = H). The peak voltage value at pin 2 increases up to $V_{2S\ max}$. If the secondary load is further increased, the overload amplifier begins to regulate the pulse width downward. This point is referred to as the overload point of the power supply. As the IC supply voltage V_6 is directly proportional to the secondary voltage, it goes down in accordance with the overload regulation behaviour. If V_6 falls below the value $V_{6\ min}$, the IC goes into burst operation. As the time constant of the half-wave charge-up is relatively large, the short-circuit power remains small. The overload amplifier cuts back to the pulse width t_{pk}. This pulse width must remain possible, in order to permit the IC to start-up without problems from the virtual short circuit, which every switching on with V_1 = 0 represents. If the secondary side is unloaded, the loading impulses (V_5 = H) become shorter. The frequency increases up to the resonance frequency of the system. If the load is further reduced, the secondary voltages and V_6 increase. When $V_6 = V_{6\ max}$, the logic is blocked. The IC converts to burst operation. This renders the circuit absolutely safe under no-load conditions.

Behaviour when Temperature Exceeds Limit

An integrated temperature protection disables the logic when the chip temperature becomes too high. The IC automatically interrogates the temperature and starts as soon as the temperature decreases to permissible values.

Absolute Maximum Ratings

T_A = 25 ˚C

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Voltages	pin 1	V_1	– 0.3	3	V	
	pin 2	V_2	– 0.3		V	
	pin 3	V_3	– 0.3		V	
	pin 5	V_5	– 0.3	V_6	V	
	pin 6	V_6	– 0.3	20	V	Supply voltage
	pin 7	V_7	– 0.3	6	V	
Currents	pin 1	V_1		3	mA	
	pin 2	V_2		3	mA	
	pin 3	V_3		3	mA	
	pin 4	V_4	– 1.5		A	$t_p \leq 50$ µs; v ≤ 0.1*)
	pin 5	V_5	– 1.5	1.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 6	V_6		1.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 7	V_7		3	mA	
	pin 8	V_8	– 3	3	mA	
Junction temperature		T_j		125	˚C	
Storage temperature		T_{stg}	– 40	125	˚C	

Operating Range

Supply voltage	V_6	8	14	V	IC "on"
Ambient temperature	T_A	– 20	85	˚C	
Heat resistance					
Junction environment	$R_{th\ JE}$		100	K/W	
Junction case	$R_{th\ JC}$		70	K/W	measured at pin 4

*) t_p= pulse width
v= duty circle

Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Start-Up Hysteresis							
Start-up current	I_{6E0}	0.5	1.1	1.6	mA	$V_6 = V_{6E}$	1
Switch-on voltage	V_{6E}	11	12	13	V		1
Switch-off voltage	V_{6A}	6.4	6.9	7.4	V		1
Switch-on current	I_{6E1}	7	9	12	mA	$V_6 = V_{6E}$	1
Switch-off current	I_{6A1}	6.5	8	10	mA	$V_6 = V_{6A}$	1
Voltage Clamp (V_6 = 10 V, IC switched off)							
At pin 2 ($V_6 \leq V_{6E}$) At pin 3 ($V_6 \leq V_{6E}$)	$V_{2\,max}$ $V_{3\,max}$	5.6 5.6	6.6 6.6	7.6 7.6	V V	I_2 = 1 mA I_3 = 1 mA	1 1
Regulation Range							
Regulation input voltage	V_{1R}	370	400	430	mV		2
Voltage gain regulation range	$-V_R$	47	50	53	dB	V_R = d ($V_{2S} - V_{2B}$)/– dV_1	2
Regulation transmittance	R_R		20		kΩ	R_R = d ($V_{2S} - V_{2B}$)/– dI_1	2
Primary Current Reproducer							
Basic value	V_{2B}	0.90	1.00	1.15	V		2
Input resistance $R_{2B} = \Delta V_{2B}/\Delta I_{2B}$	R_{2B}		25	40	Ω	V_3 = 1.5 V; 1.2 V < V_2 < 3 V 0.1 mA < I_{2B} < 3 mA	2
Slew rate falling edge	dV_2/dt		– 1		V		2

Characteristics (cont'd)
T_A = 25 °C

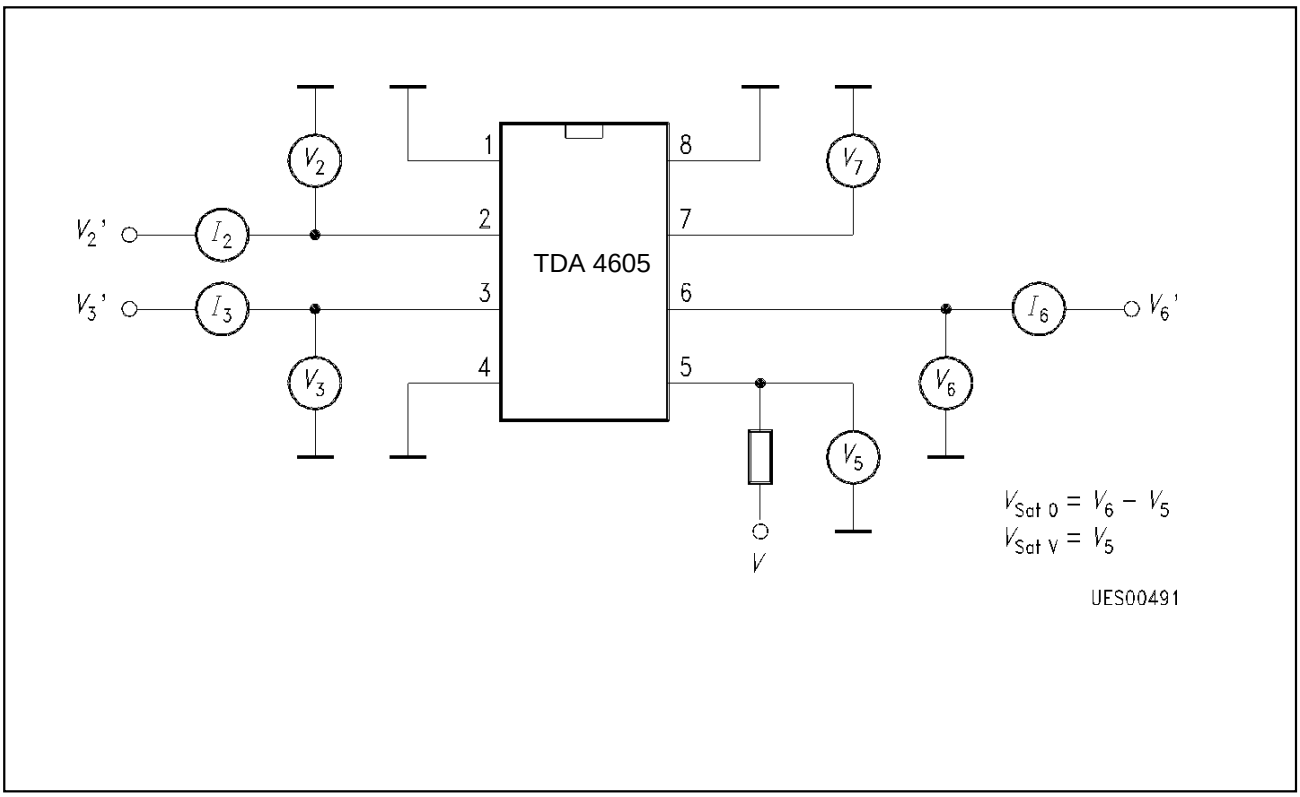
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Overload Range and Short-Circuit Operation							
Overload range lower limit	V_{1U}	60	230	290	mV		2
Voltage gain in overload range	$V_{Ü}$	1	2	3		$V_{Ü}$ = d ($V_{2S} - V_{2B}$)/dV_1	2
Input current in short circuit operation	$-I_1$	90	120	180	µA	V_1 = 0 V	2
Peak value in overload range	$V_{2Ü}$		3.0		V	$V_1 = V_{1R}$ – 10 mV	2
Peak value in short circuit operation	V_{2K}	2.2	2.6	3.0	V	V_1 = 0 V	2
Generally Valid Data (V_6 = 10 V)							
Overload Point Correction							
Overload point correction current	$-I_2$	400	660	850	µA	V_3'= 4 V; V_2'= 0 V	1
Zero Transition Detector Voltage							
Positive clamp	V_{8P}	0.70	0.75	0.80	V	I_8 = 1 mA	2
Negative clamp	V_{8N}	– 0.15	– 0.22	– 0.25	V	I_8 = – 1 mA	2
Threshold value	V_{8S}	40	50		mV		2
Input current	$-I_8$		2	4	µA	V_8 = 0	2
Delay time between V_8 and V_5	t_{d2}	0.2	0.4	0.7	µs		2
Zero detector disable time	t_{UL}	2	2	6	µs		

Characteristics (cont'd)
T_A = 25 °C

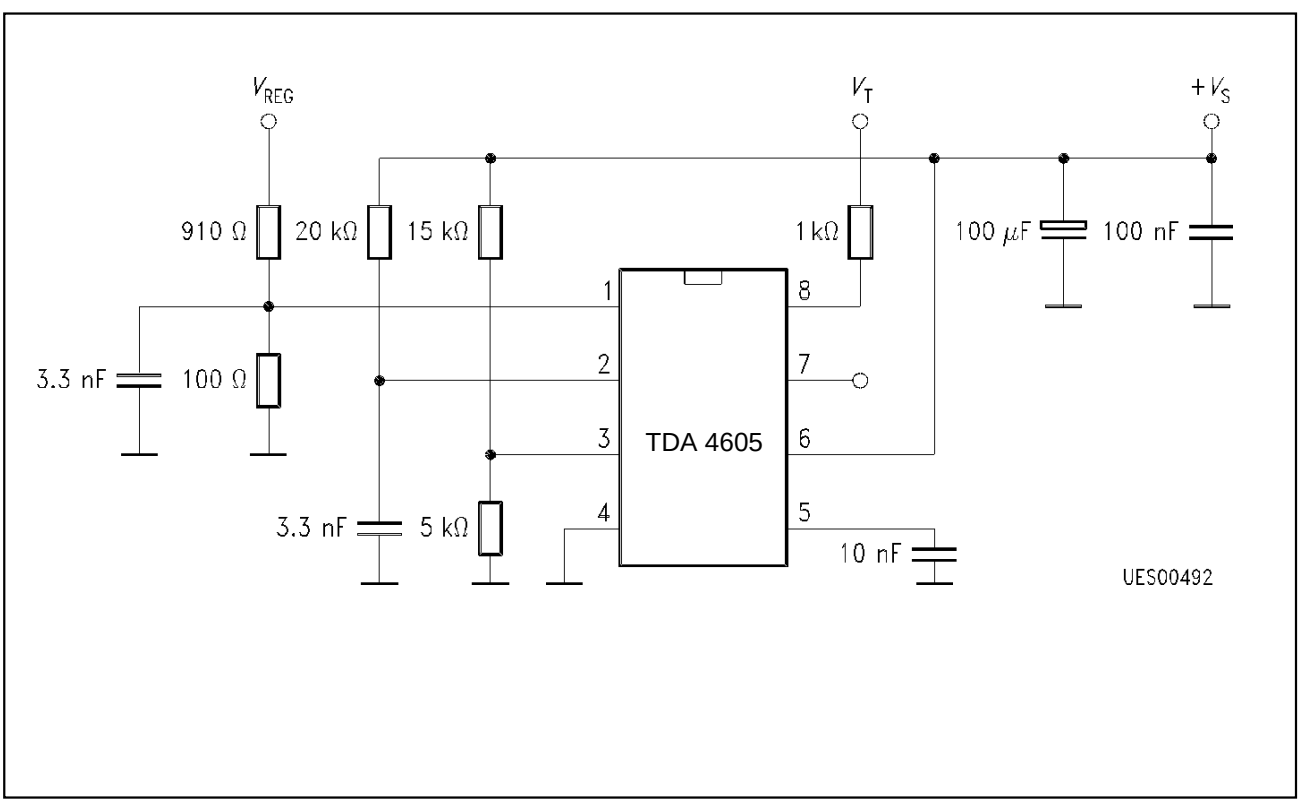
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Output Stage							
Saturation voltages S in position 1							
Output sourcing	V_{Sat0}		1.5	2.0	V	I_5 = – 0.1 A	1
Output sourcing	V_{Sat0}		2.5	3.0	V	I_5 = – 1 A	1
Output sinking	V_{SatV}		1.0	1.2	V	I_5 = 0.1 A	1
Output sinking	V_{SatV}		1.4	1.8	V	I_5 = 0.5 A	1
Output slew rate							
Rising slope	+ dV_5/dt		50		V/µs		2
Falling slope	+ dV_5/dt		80		V/µs		2
Soft-Start							
Open-circuit	V_7	2.2	2.6	2.9	V	V_1 = 0	2
Input resistance	R_{7L}	4	6	9	kΩ	0.5 V ≤ V_7 ≤ 3 V	2
Peak voltage	V_{2S}	1.0	1.2	1.4	V	V_7 = 0	2
Protection Circuit							
Undervoltage protection for V_6 at pin 5 = $V_{5\ min}$ if $V_6 < V_{6\ min}$ (definition: $V_{6\ min} = V_{6A} + \Delta V_6$)	ΔV_6		100		mV		2
Overvoltage protection for V_6 voltage at pin 5 = $V_{5\ min}$ if $V_6 > V_{6\ max}$	$V_{6\ max}$	14	15	16	V		2
Undervoltage protection for V_{AC} voltage at pin 5 = $V_{5\ min}$ if $V_3 < V_{3A}$	V_{3A}	925	1000	1075	mV	V_2' = 0 V	1
Over temperature chip temperature for $V_{5\ min}$	T_j		125		°C	–	2

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Voltage at pin 3 when protection function occurred; (V_3 will be clamped until $V_6 < V_{6A}$)	V_{3S}		0.4	0.8	V	I_3 = 1 mA	1
Burst operation quiescient current	I_6		8		mA	$V_3 = V_2$ = 0 V	1



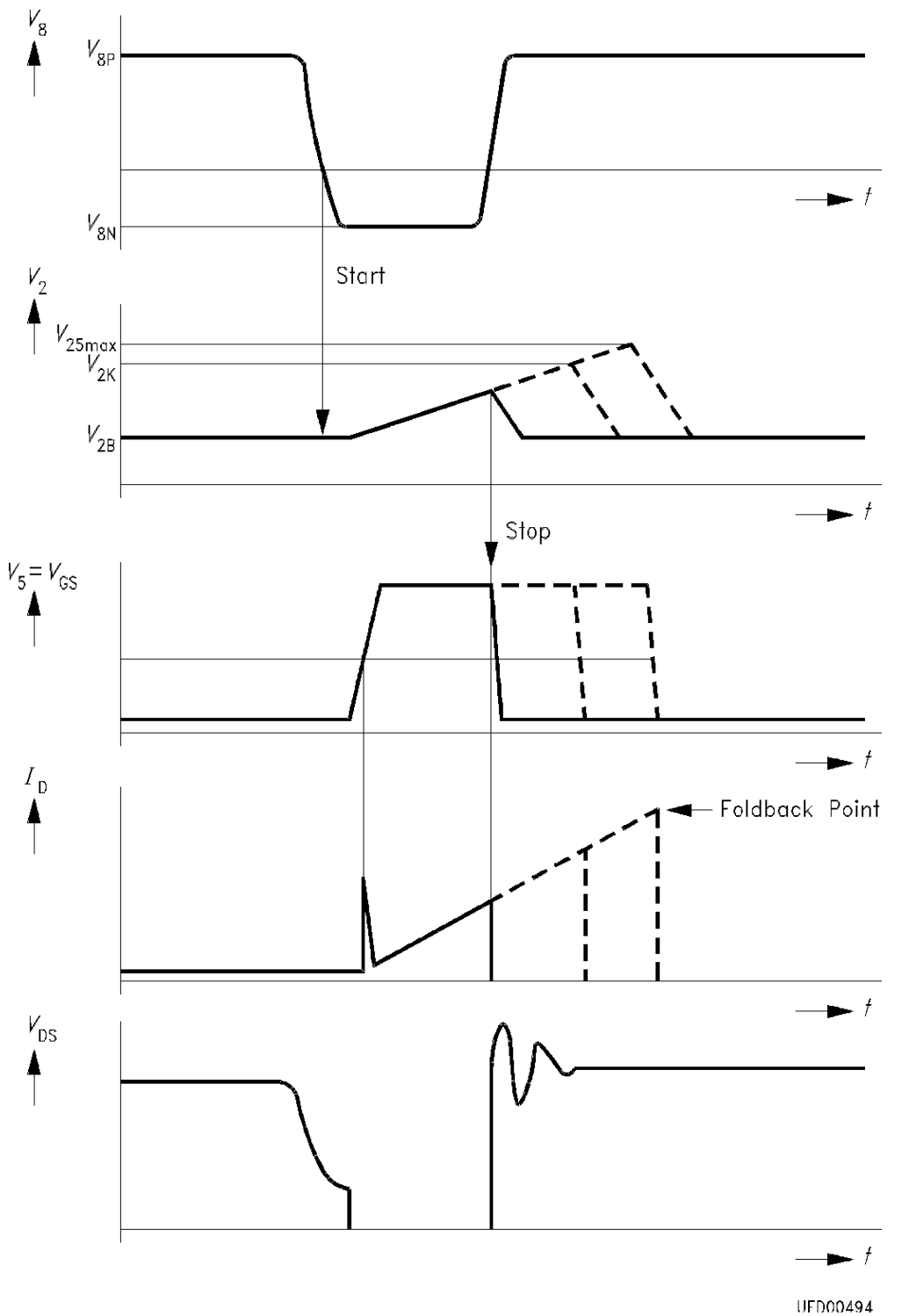
Test Circuit 1

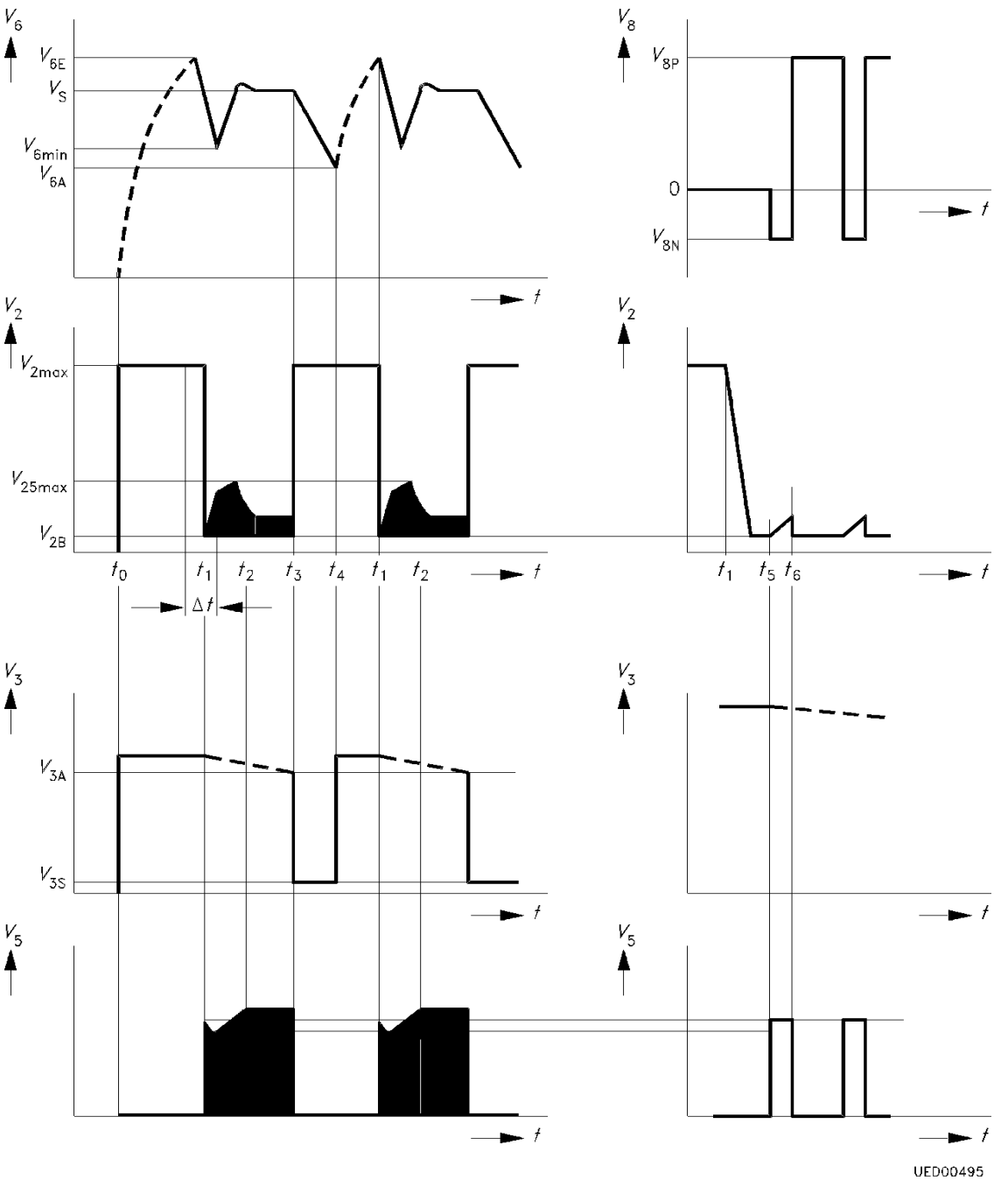


Test Circuit 2

Application Circuit

Diagrams


V_8
V_{8P}
V_{8N}
t
Start
V_2
V_{25max}
V_{2K}
V_{2B}
t
Stop
$V_5 = V_{GS}$
t
I_D
Foldback Point
t
V_{DS}
t
UFD00494


V_6
V_{6E}
V_S
V_{6min}
V_{6A}
t
V_8
V_{8P}
0
V_{8N}
t
V_2
V_{2max}
V_{25max}
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t_0 t_1 t_2 t_3 t_4 t_1 t_2 t
Δt
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t_1 t_5 t_6 t
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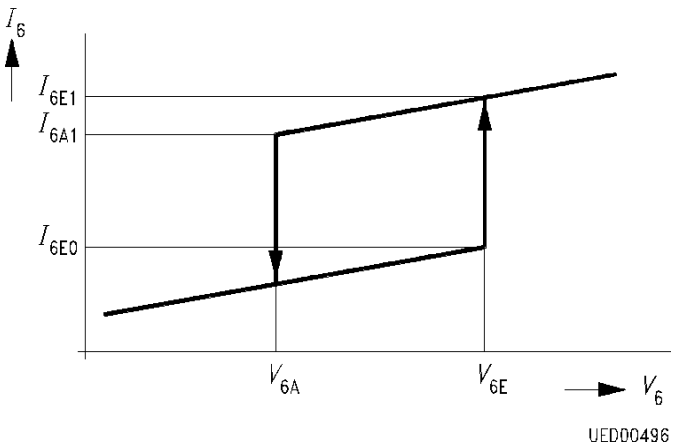
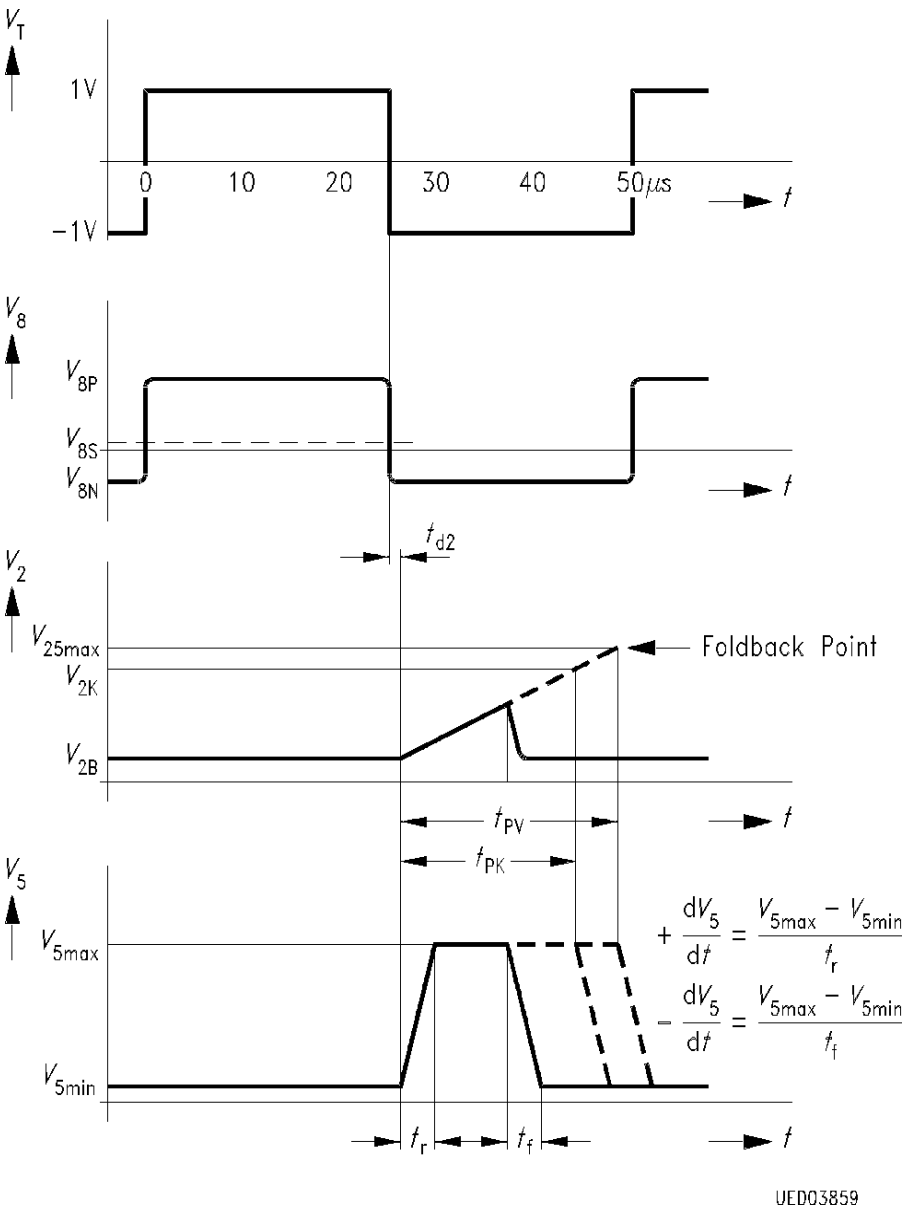
UED00495

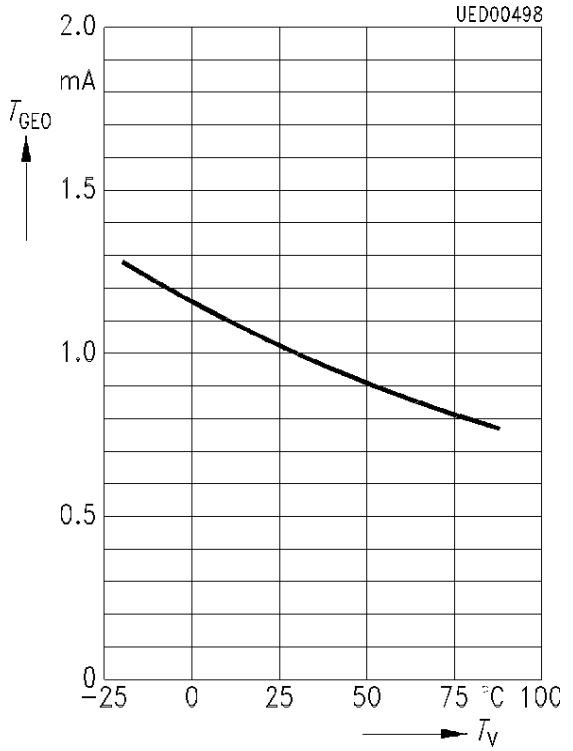


Start-Up Hysteresis

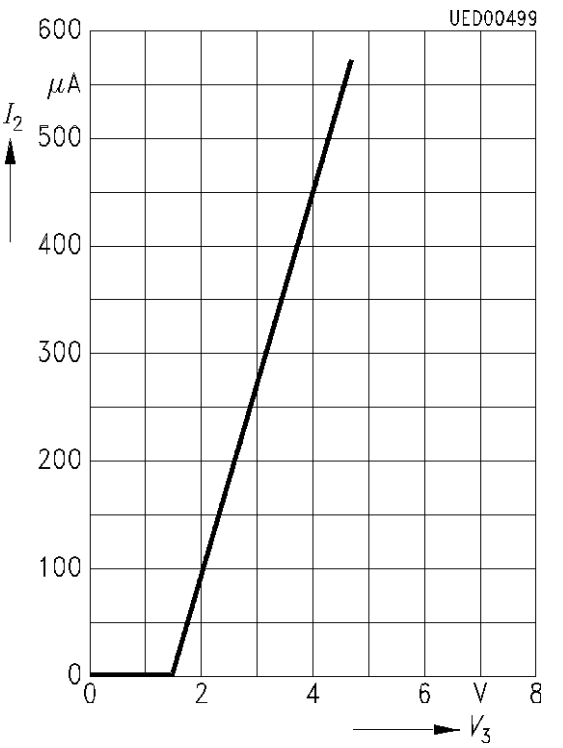


Operation in Test Circuit 2

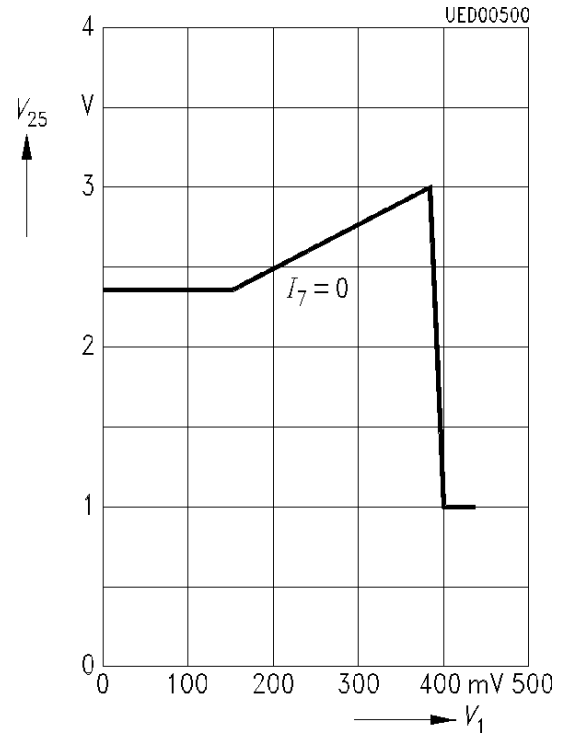
Start-Up Current as a Function of the Ambient Temperature



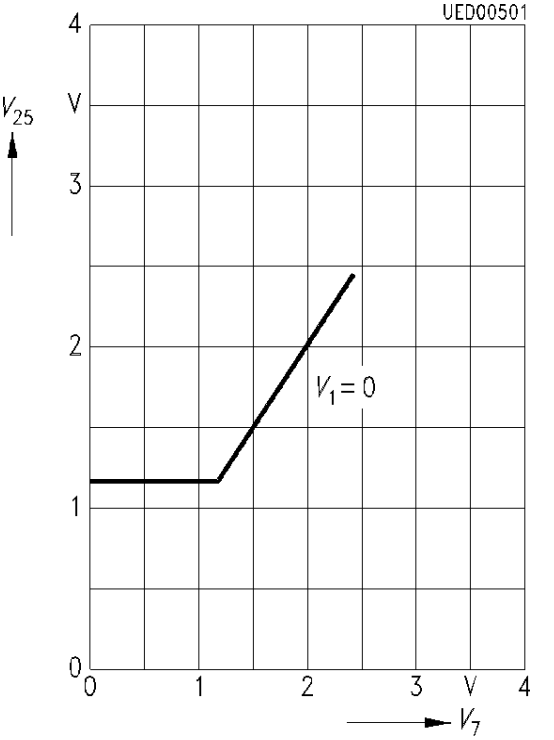
Overload Point Correction as a Function of the Voltage at Pin 3



Peak Value of the Primary Current Reproduction Voltage as a Function of the Regulating Voltage

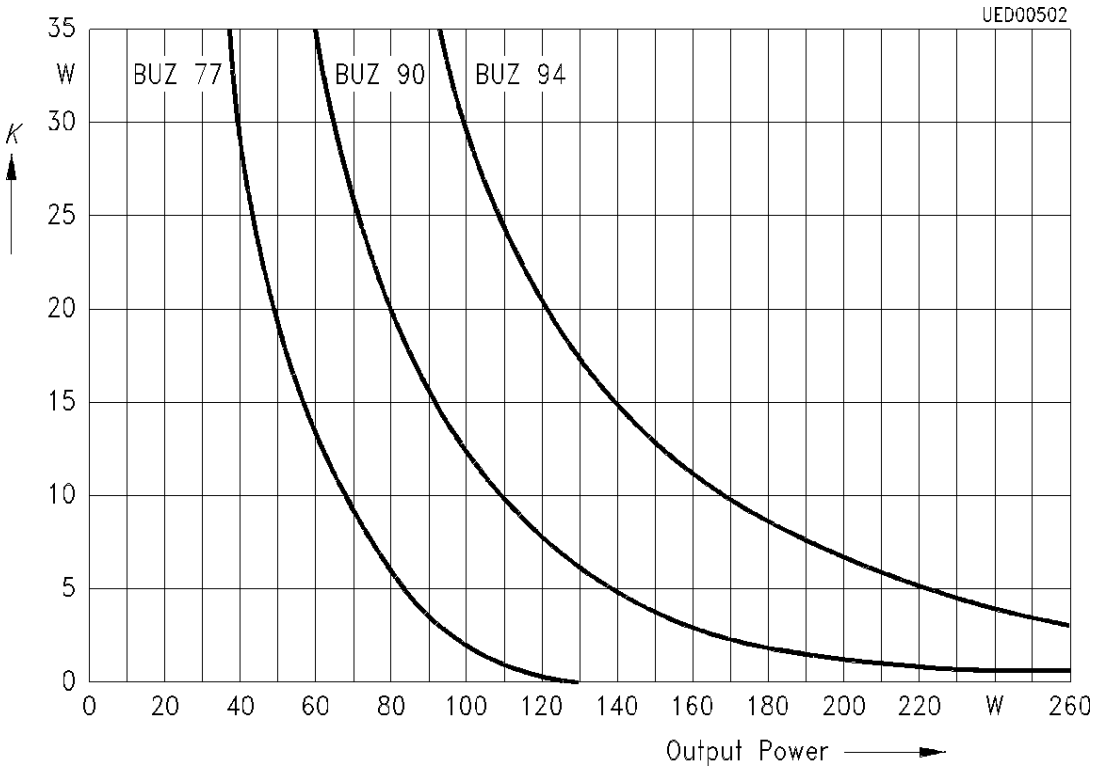


Peak Value of the Primary Current Reproduction Voltage by Loading Pin 7

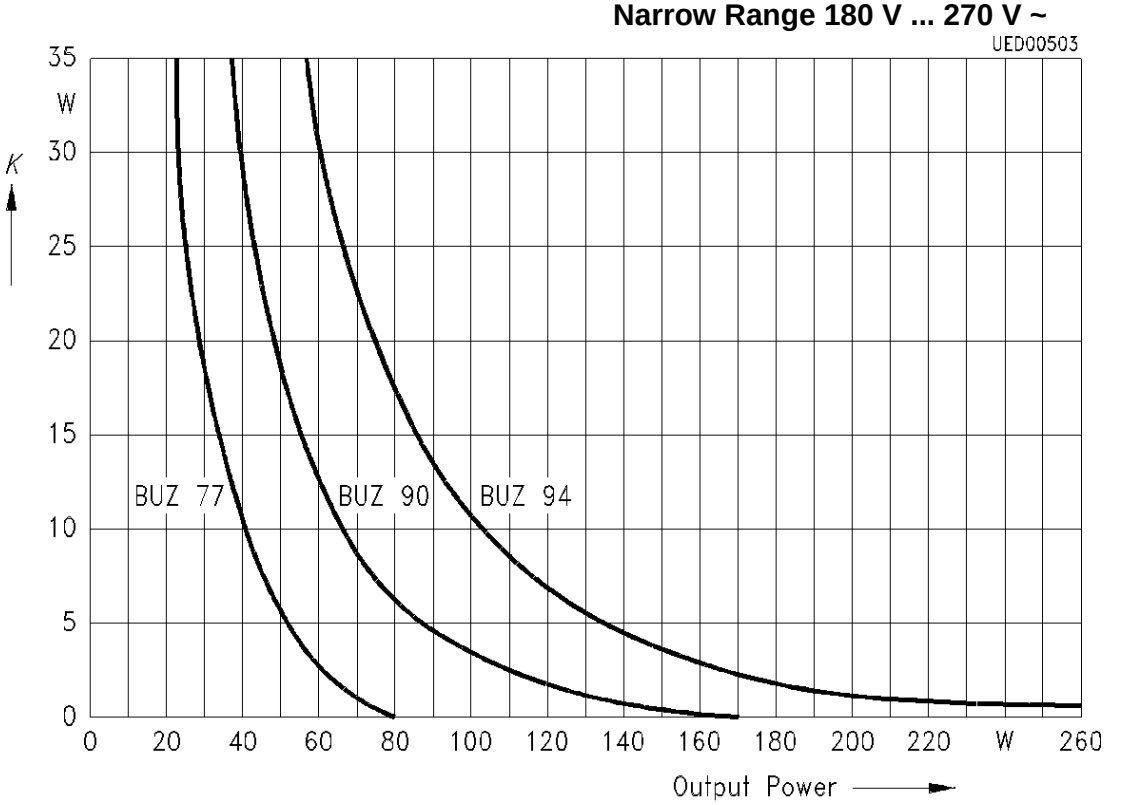


Recommended Heat Sink by 60 ˚C Ambient Temperature

Narrow Range 180 V ... 270 V ~



Narrow Range 180 V ... 270 V ~



SIEMENS

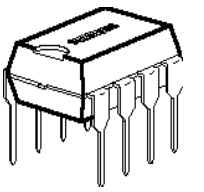
Control IC for Switched-Mode Power Supplies using MOS-Transistors

TDA 4605-2

Bipolar IC

Features

- Fold-back characteristics provides overload protection for external components
- Burst operation under secondary short-circuit condition implemented
- Protection against open or a short of the control loop
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage depending compensation of fold-back point
- Soft-start for quiet start-up without noise generated by the transformer
- Chip-over temperature protection implemented (thermal shutdown)
- On-chip ringing suppression circuit against parasitic oscillations of the transformer



P-DIP-8-1

Type	Ordering Code	Package
TDA 4605-2	Q67000-A5020	P-DIP-8-1

The IC TDA 4605-2 controls the MOS-power transistor and performs all necessary regulation and monitoring functions in free running flyback converters. Because of the fact that a wide load range is achieved, this IC is applicable for consumer as well as industrial power supplies.

The serial circuit and primary winding of the flyback transformer are connected in series to the input voltage. During the switch-on period of the transistor, energy is stored in the transformer. During the switch-off period the energy is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations. The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period. A new cycle will start if the transformer has transferred the stored energy completely into the load.

In the different load ranges the switched-mode power supply (SMPS) behaves as follow:

No load operation

The power supply is operating in the burst mode at typical 20 to 40 kHz. The output voltage can be a little bit higher or lower than the nominal value depending of the design of the transformer and the resistors of the control voltage divider.

Nominal operation

The switching frequency is reduced with increasing load and decreasing AC-voltage. The duty factor primarily depends on the AC-voltage.

The output voltage is only dependent on the load.

Overload point

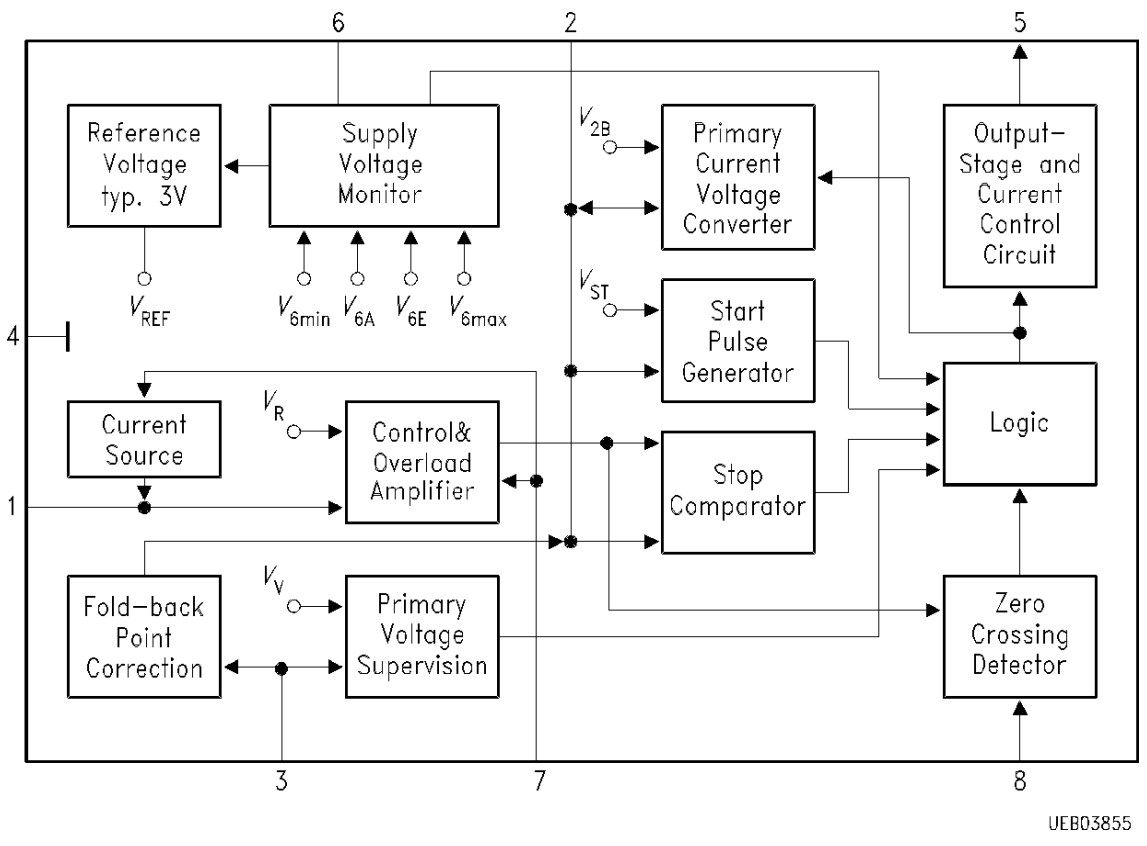
Maximal output power is available at this point of the output characteristic.

Overload

The energy transferred per operation cycle is limited at the top. Therefore the output voltages declines by secondary overloading.

Pin Definitions and Functions

Pin No.	Function
1	**Information Input Concerning Secondary Voltage.** By comparing the regulating voltage - obtained from the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adjusted to the load of the secondary side (normal load, overload, short-circuit, no load).
2	**Information Input Regarding the Primary Current.** The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC-circuit. If a voltage level is reached which is derived from the control voltage at pin 1, the output impulse at pin 5 is terminated. The RC-circuit is used to set the maximum power of the foldback point.
3	**Input for Primary Voltage Monitoring:** In the normal operation V_3 is moving between the thresholds V_{3H} and V_{3L} ($V_{3H} > V_3 > V_{3L}$). $V_3 < V_{3L}$: SMPS is switched OFF (line voltage too low). $V_3 > V_{3H}$: Compensation of the overload point regulation (controlled by pin 2) starts at $V_{3H} : V_{3L} = 1.7$.
4	**Ground**
5	**Output:** Push-pull output for charging or discharging the gate capacity of the power MOSFET-transistor.
6	**Supply Voltage Input.** From the voltage at pin 6 a stable internal reference voltage V_{REF} and the switching thresholds V_{6A} , V_{6E} , $V_{6\,max}$ and $V_{6\,min}$ for the supply voltage detector are derived. If $V_6 > V_{6E}$ then V_{REF} is switched on. The reference voltage will be switched off if $V_6 < V_{6A}$. In addition the logic is only enable, for $V_{6\,min} < V_6 < V_{6\,max}$.
7	**Input for Soft-Start and Integrator Circuit.** The capacitor connected to ground causes a slow increase of the duration of the output pulse during start-up and an integrating response of the control amplifier.
8	**Input for the Feedback of the Oscillator.** After the oscillations of the SMPS started, every transition of the feedback voltage through zero (falling edge) triggers an output pulse at pin 5. The trigger threshold is at + 50 mV typical.



Block Diagram

Circuit Description

Application Circuit

The application circuit shows a flyback converter for video recorders with an output power rating of 70 W. The circuit is designed as a wide-range power supply for AC-line voltages of 180 to 264 V. The AC-input voltage is rectified by the bridge rectifier GR1 and smoothed by C_1 . The NTC limits the rush-in current.

The IC includes an internal circuit to avoid the turn-on of the power transistor T1 because of static charges applied to the transistors gate, during the turn-off state of the IC. The resistor R_{13} helps to limit the spectrum of the radiated noise.

During the conductive phase of the power transistor T1 the current rise in the primary winding depends on the winding inductance and the mains voltage.

The network consisting of R_4-C_5 is used to create a model of the sawtooth shaped rise of the collector current. The resulting control voltage is fed into pin 2 of the IC. The RC-time constant given by R_4-C_5 must be designed that way that driving the transistor core into saturation is avoided.

The ratio of the voltage divider R_{10}/R_{11} is fixing a voltage level threshold. Below this threshold the switching power supply shall stop operation because of the low mains voltage. The control voltage present at pin 3 also determines the correction current for the foldback point.

This current added to the current flowing through R_4 and represents an additional charge to C_5 in order to reduce the turn-on phase of T1. This is done to stabilize the fold-back point even under higher mains voltages.

The control of the switched-mode power supply is done by means of a control voltage applied to pin 1. The control voltage of winding n_1 during the off-period of T1 is rectified by D3 smoothed by C_6 and stepped down at an adjustable ratio by R_5 , R_6 and R_7 . The primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the energy stored in the transformer is transferred into the load the control voltage passes through zero. The IC detects the zero crossing via the series R_9 connected to pin 8. But zero crossings of the control voltage can also be produced by ringing of the transformer after the turn-off of the power transistor for T1 or when a short-circuit is applied to the output of the SMPS.

The capacitor C_8 is connected to pin 7. During the start-up phase this capacitor assures pulses with a shorter duty cycle in order to keep the operating frequency outside the audible frequency range.

On the secondary side of the transformer 3 output voltages are produced using the windings n_2 to n_5 , rectified by D4 to D6 and smoothed by C_9 to C_{11} . The resistor R_{12} is used as a bleeder resistor, the resistors with implemented fuse R_{15} and R_{16} protect the rectifies against short circuits in the output circuits, which are designed to supply only small loads.

Block Diagram

Pin 1

In the control and overload amplifier the control voltage applied to this pin is compared with a stable internal reference voltage V. The output signal of this stage is fed to the "stop" comparator. If the control voltage is rather small at pin 1 an additional current is added by means of current source which is controlled according the level at pin 7. This additional current is virtually reducing the control voltage present at pin 1.

Pin 2

A voltage proportional to the drain current of the switching transistor is generated by means of an external RC-combination in conjunction with the internal functional block **primary current / voltage converter**. The output of this converter is controlled by the internal functional block "logic" and is also connected to the internal reference voltage V_{2B} . If the voltage V_2 exceeds the output voltage of the "control and overload amplifier" the stop comparator will reset the control logic. Consequently the output of pin 5 is switched to low potential. Further inputs for the logic stage are the outputs of the start impulse generator with the stable reference potential V_{ST} , the supply voltage monitoring circuit as well as the primary voltage supervision circuit.

Pin 3

The primary voltage applied here via a voltage divider is used to stabilize the fold-back point. In addition the logic is disable if - in comparison with the internal reference voltage V_V - a mains undervoltage condition is detected.

Pin 4

Ground

Pin 5

In the output stage the output signals from the "logic" block are converted into driving signals suitable for power MOS-transistors.

Pin 6

From the supply voltage V_6 applied to this pin internally a stable reference voltage V_{REF} as well as the switching threshold V_{6A} , V_{6E} , $V_{6\ max}$ and $V_{6\ min}$, for the supply voltage monitor section of the IC. All other inter reference value (V_R , V_{2B} , V_{ST} and V_V) are derived for V_{REF} . If $V_6 > V_{6E}$ the V_{REF} voltage source is switched on and the source is switched off if $V_6 < V_{6A}$. In addition the logic is enable only if $V_{6\ min} < V_6 < V_{6\ max}$.

Pin 7

By means of a resistor pin 7 is connected with the output of the control amplifier. If V_1 is approx. equal to the control voltage V_R the control amplifier has a proportional integrating control characteristics. The response of the control loop is derived from the capacitor connected to pin 7. If V_1 is equal to 0 V the control and overload amplifier is generating a ramp-up function using the capacitor connected to pin 7.

Pin 8

The zero crossing detector controlling the logic block recognizes the complete discharge of the energy stored in the transformator core by detecting the zero crossing the positive to negative voltage transition of the voltage at pin 8. This enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse because of an internal circuit which inhibits the zero detector for a certain dead time t_{UL} after the end of each pulse.

Start-Up Behaviour

The start-up behaviour of the application circuit (which is given on page 68) is explained in the diagrams on page 70 for a line voltage barely above the lower acceptable lower limit of the mains voltage. After applying the mains voltage at the time t_0 the following built up of different voltages can be seen:

- V_6 corresponding to the half-wave charge current over R_1
- V_2 to $V_{2\ max}$ (typically 6.6 V)
- V_3 to the value determined by the divider R_{10}/R_{11}

The current drawn by the IC in this case is less than 0.8 mA.

If V_6 reaches the threshold (at the time t_1 in the diagram), the IC internal reference voltage is switched on. The supply current drawn by the IC rises to 12 mA max.. The primary current/voltage converter reduces V_2 down to V_{2B} and the start pulse generator generates the start pulses from time point t_5 to t_6 in the diagram. The feedback to pin 8 starts the next pulse and so on. The width of all pulses including the start pulse are controlled by means of the control and overload amplifier. After turn on the IC is generating a signal at pin 7 which slowly ramping up. This signal is used to increase the duration of the output pulses slowly (soft-start function). The max. output pulse width is limited by means of the overload amplifier. If the feedback control voltage V_1 is increasing, the overload amplifier allows the generation of output pulses with a wider pulse width. The max. pulse width is reached at time t_2 in the diagram ($V_2 = V_{2S\ max}$). The IC is then operating at the fold-back point. Thereafter the peak values of V_2 decrease rapidly, because of the IC control range. The control loop is in a steady, operational state.

If the voltage V_6 falls below the switch-off threshold $V_{6\ min}$ before the foldback point is reached, the attempt to start the SMPS is aborted (pin 5 is switched to low). As the internal circuits of the IC remain switched on, V_6 further decreases to V_{6A} . The IC switches off; V_6 can rise again (time t_4 in the diagram) and new start-up attempt begins at time t_1 .

If the voltage level of the rectified mains voltage is reduced strongly under the influence of the applied load it can happen that V_3 is below the voltage level V_{3A} - please refer to the time t_3 in the diagram. This is because if an attempt is made to start the SMPS with a too low mains voltage. The internal primary voltage monitor circuit then clamps the voltage V_3 to the voltage level V_{3S} until the IC switches off ($V_6 < V_{6A}$). After this a new attempt to start the SMPS will begin at the time t_1 in the diagram.

Control Range, Overload and No-Load Behaviour

After the IC has started, it is operating in the control range. The voltage level at pin 1 is typically 400 mV. The gain of the control circuit consist of two parts: at first a fixed proportional part which is internally fixed and an integrating part which can be set by means of the external capacitor at pin 7. If the load is applied to the output of the SMPS, the control and overload amplifier allows wider pulses (V_5 = "H") .The peak voltage value at pin 2 increases up to $V_{2S\ max}$. If the secondary load is increased further the overload amplifier begins to reduce the pulse width of the output pulse. This point is referred to as the fold-back point of the power supply. Because of the fact that the IC supply voltage is directly proportional to the secondary voltage, the supply voltage V_6 will be reduced according to the behaviour of the control circuit under the overload condition. If V_6 falls below the value $V_{6\ min}$, the IC will operate in the burst mode. Because of the large time constant of the start-up circuit which is operating with half-wave rectification, only a small output power is transferred into the load during the secondary short-circuit of the SMPS. The overload amplifier reduces the output pulse width down to the pulse width t_{pk} . This pulse width must remain possible in order to permit the IC to start up without problems from the virtual short-circuit, which every switching on with V_1 = 0 is representing.

If no load is applied to the secondary side, the output pulses (V_5 = H) become shorter.

If the pulse width is reduced be low a certain internal limit the IC will suppress some of the output pulses. If the load is reduced further because of the decreasing duty cycle the measurement error of the rectifier network (R_8 , D3, C_6 of the application circuit) is increasing and therefore the secondary output voltage will increase, too. If the IC is operating with small pulse width of the output pulse the control amplifier applies an additional current to the control amplifier in order to reduce the output voltage. The value of the additional current depends on the size of the resistors R_5 , R_8 , R_7 . This can be used to compensate the increase of the secondary voltages.

Behaviour if the Chip Temperature Exceeds Predefined Limits

An integrated protection circuit against over temperature disables the internal logic if the chip temperature is too high. The internal logic automatically checks the chip temperature and restart the SMPS as soon as the temperature decreases to a permissible level.

Absolute Maximum Ratings

T_A = – 20 to 85 °C; all voltages relatives to V_{pp}

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Voltages	pin 1	V_1	– 0.3	3	V	
	pin 2	V_2	– 0.3		V	
	pin 3	V_3	– 0.3		V	
	pin 5	V_5	– 0.3	V_6	V	
	pin 6	V_6	– 0.3	20	V	Supply voltage
	pin 7	V_7	– 0.3		V	
Currents	pin 1	I_1		3	mA	
	pin 2	I_2		3	mA	
	pin 3	I_3		3	mA	
	pin 4	I_4	– 1.5		A	$t_p \leq 50$ µs; v ≤ 0.1*)
	pin 5	I_5	– 0.5	1.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 6	I_6		0.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 7	I_7		3	mA	
	pin 8	I_8	– 5	3	mA	
Junction temperature		T_j		125	°C	
Storage temperature		T_{stg}	– 40	125	°C	

Operating Range

Supply voltage	V_6	7.5	15.5	V	IC "on"
Ambient temperature	T_A	– 20	85	°C	
Heat resistance					
Junction environment	$R_{th\ JE}$		100	K/W	
Junction package	$R_{th\ JG}$		70	K/W	measured at pin 4

*) t_p= pulse width
v= duty circle

Characteristics

T_A = 25 °C; V_S = 10 V

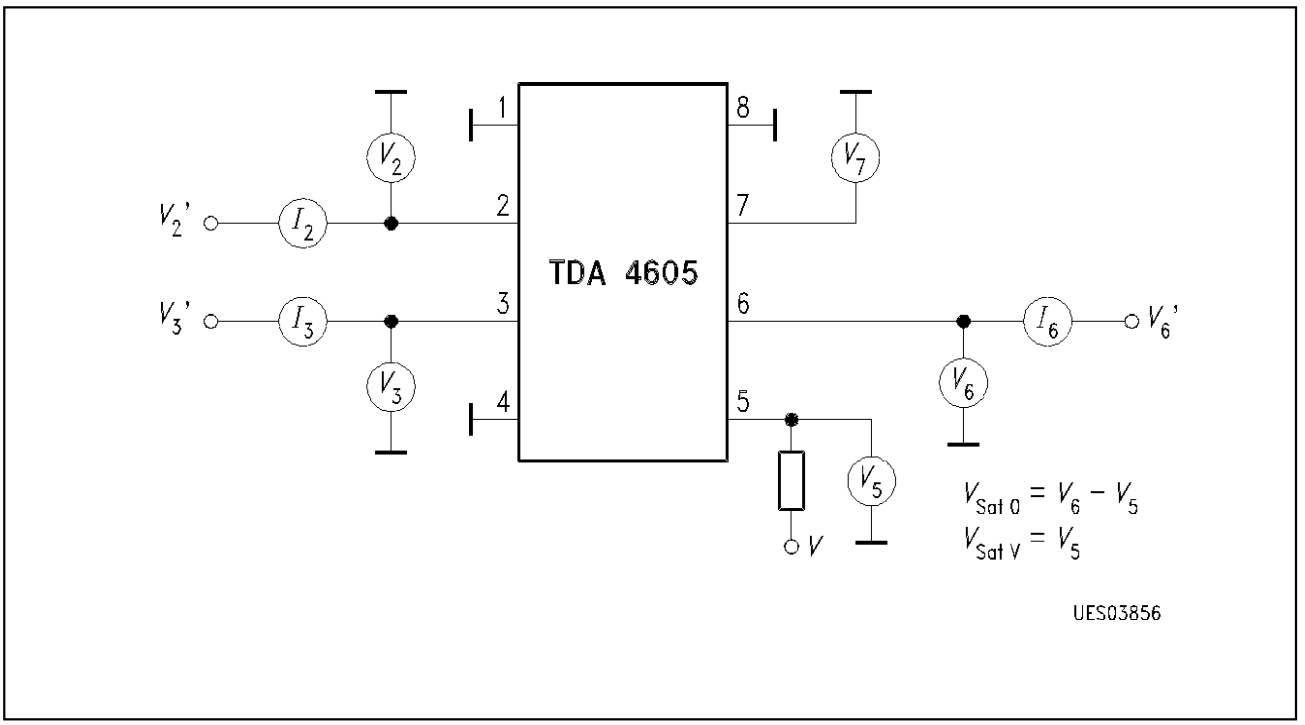
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Start-Up Hysteresis							
Start-up current drain	I_{6E0}		0.6	0.8	mA	$V_6 = V_{6E}$	1
Switch-on voltage	V_{6E}	11	12	13	V		1
Switch-off voltage	V_{6A}	4.5	5	5.5	V		1
Switch-on current	I_{6E1}		11		mA	$V_6 = V_{6E}$	1
Switch-off current	I_{6A1}		10		mA	$V_6 = V_{6A}$	1
Voltage Clamp (V_6 = 10 V, IC switched off)							
At pin 2 ($V_6 \leq V_{6E}$) At pin 3 ($V_6 \leq V_{6E}$)	$V_{2\ max}$ $V_{3\ max}$	5.6 5.6	6.6 6.6	8 8	V V	I_2 = 1 mA I_3 = 1 mA	1 1
Control Range							
Control input voltage	V_{1R}	390	400	410	mV		2
Voltage gain of the control circuit in the control range	$-V_R$		43		dB	V_R = d ($V_{2S} - V_{2B}$)/– dV_1 f = 1 kHz	2
Primary Current Simulation Voltage							
Basic value	V_{2B}	0.97	1.00	1.03	V		2
Overload Range and Short-Circuit Operation							
Peak value in the range of secondary overload	V_{2O}	2.9	3.0	3.1	V	$V_1 = V_{1R}$ – 10 mV	2
Peak value in the range of secondary short-circuit operation	V_{2S}	2.2	2.4	2.6	V	V_1 = 0 V	2
Fold-Back Point Correction							
Fold-back point correction current	$-I_2$	300	500	650	µA	V_3 = 3.7 V	1

Characteristics (cont'd)
T_A = 25 °C; V_S = 10 V

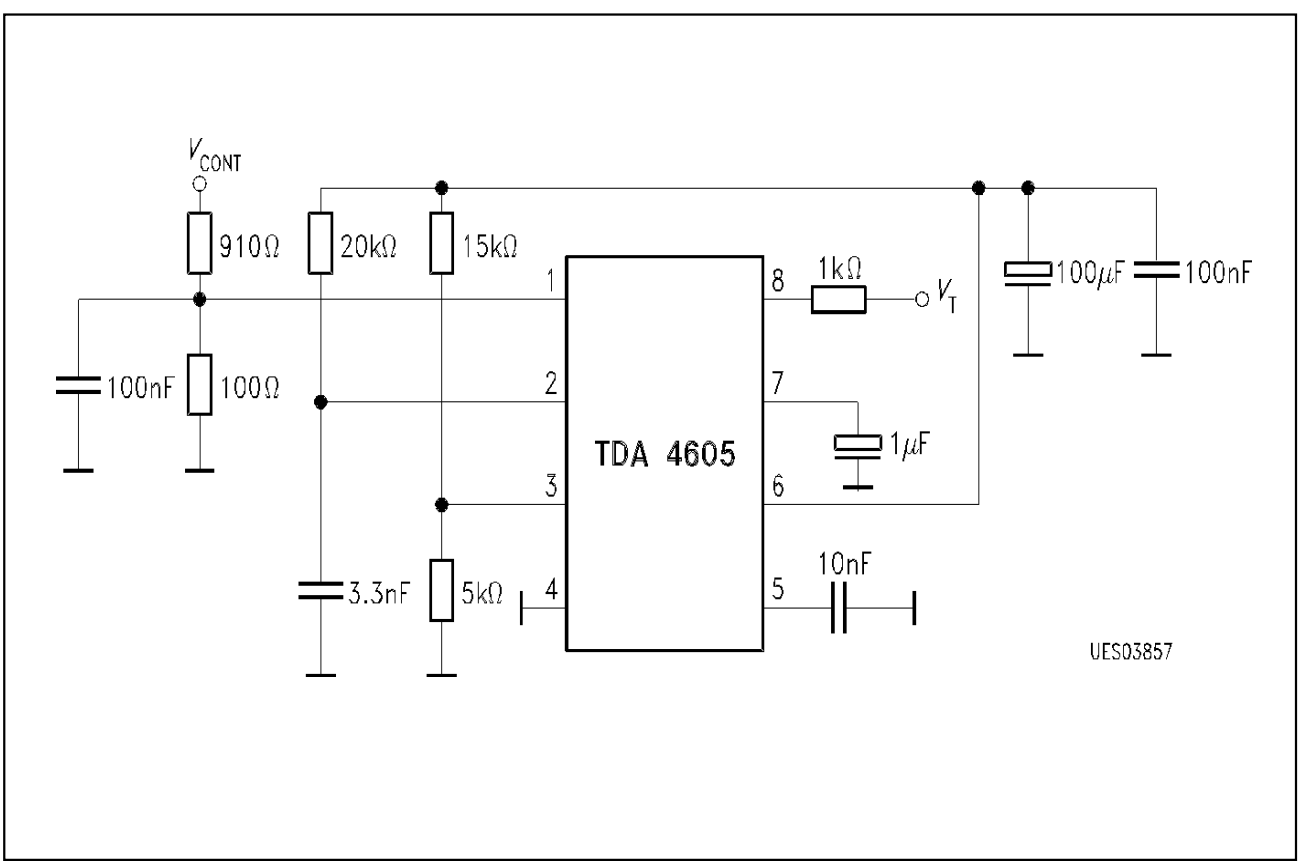
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Generally Valid Data (V_6 = 10 V)							
Voltage of the Zero Transition Detector							
Positive clamping voltage	V_{8P}		0.75		V	I_8 = 1 mA	2
Negative clamping voltage	V_{8N}		– 0.2		V	I_8 = – 1 mA	2
Threshold value	V_{8S}	40	50		mV		2
Suppression of transformer ringing	t_{UL}	4	4.5	5.5	µs		2
Input current	$-I_8$	0		4	µA	V_8 = 0	
Push-Pull Output Stage							
Saturation voltages							
Pin 5 sourcing	V_{Sat0}		1.5	2.0	V	I_5 = – 0.1 A	1
Pin 5 sinking	V_{SatV}		1.0	1.2	V	I_5 = + 0.1 A	1
Pin 5 sinking	V_{SatV}		1.4	1.8	V	I_5 = + 0.5 A	1
Output Slew Rate							
Rising edge	+ dV_5/dt		20		V/µs		2
Falling edge	+ dV_5/dt		50		V/µs		2
Reduction of Control Voltage							
Current to reduce the control voltage	$-I_1$		50		µA	V_7 = 1.1 V	

Characteristics (cont'd)
T_A = 25 °C; V_S = 10 V

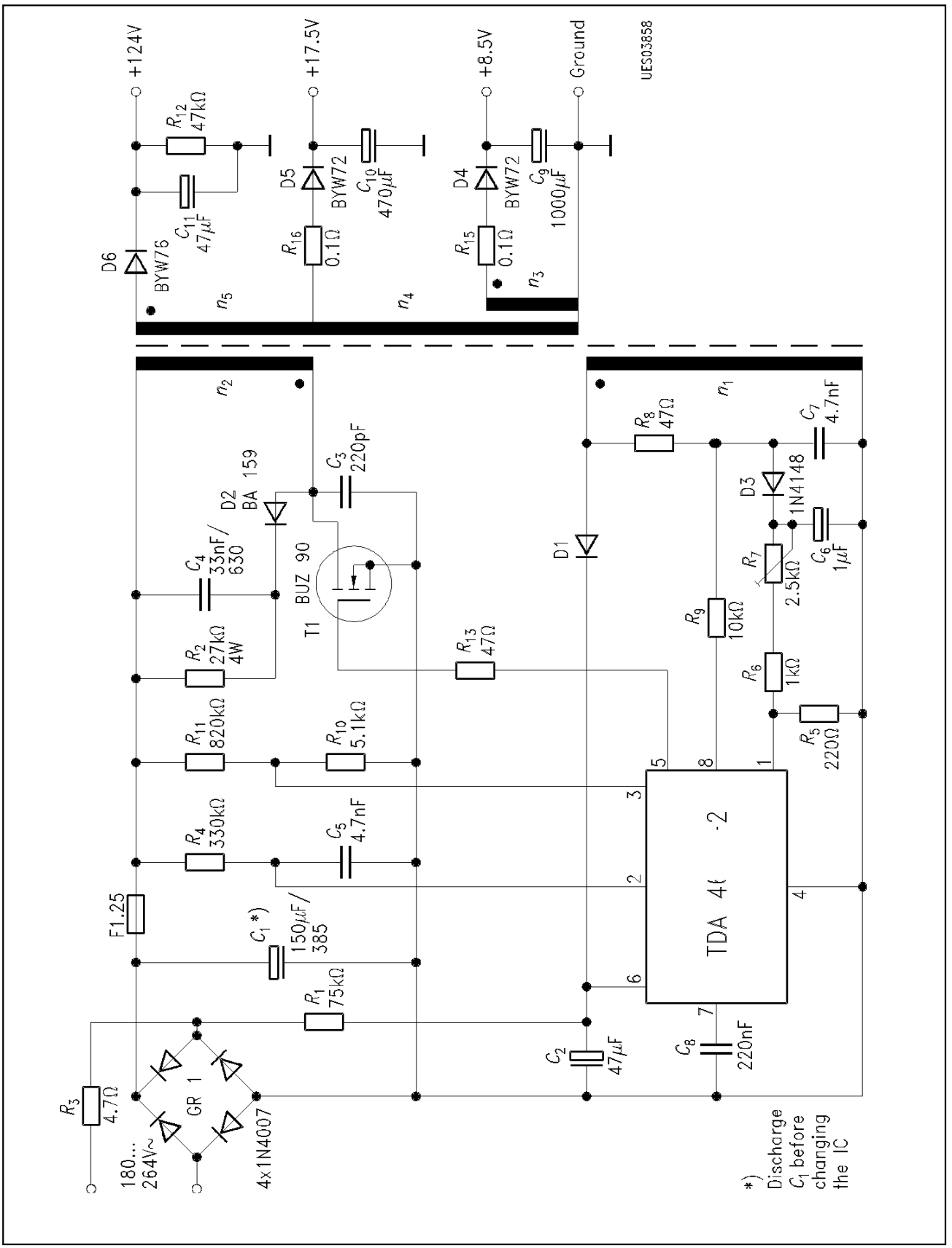
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Protection Circuit							
Undervoltage protection for V_6 : voltage at pin 5 = $V_{5\ min}$ if $V_6 < V_{6\ min}$	$V_{6\ min}$	7.0	7.25	7.5	V		2
Undervoltage protection for V_6 : voltage at pin 5 = $V_{5\ min}$ if $V_6 > V_{6\ max}$	$V_{6\ max}$	15.5	16	16.5	V		2
Undervoltage protection for V_{AC} : voltage at pin 5 = $V_{5\ min}$ if $V_3 < V_{3A}$	V_{3A}	985	1000	1015	mV	V_2 = 0 V	1
Over temperature at the given chip the temperature IC will switch V_5 to $V_{5\ min}$	T_j		150		°C		2
Voltage at pin 3 if one of the protection functions was triggered; (V_3 will be clamped until $V_6 < V_{6A}$)	V_{3Sat}		0.4	0.8	V	I_3 = 750 µA	1
Current drain during burst operation	I_6		8		mA	$V_3 = V_2$ = 0 V	1



Test Circuit 1

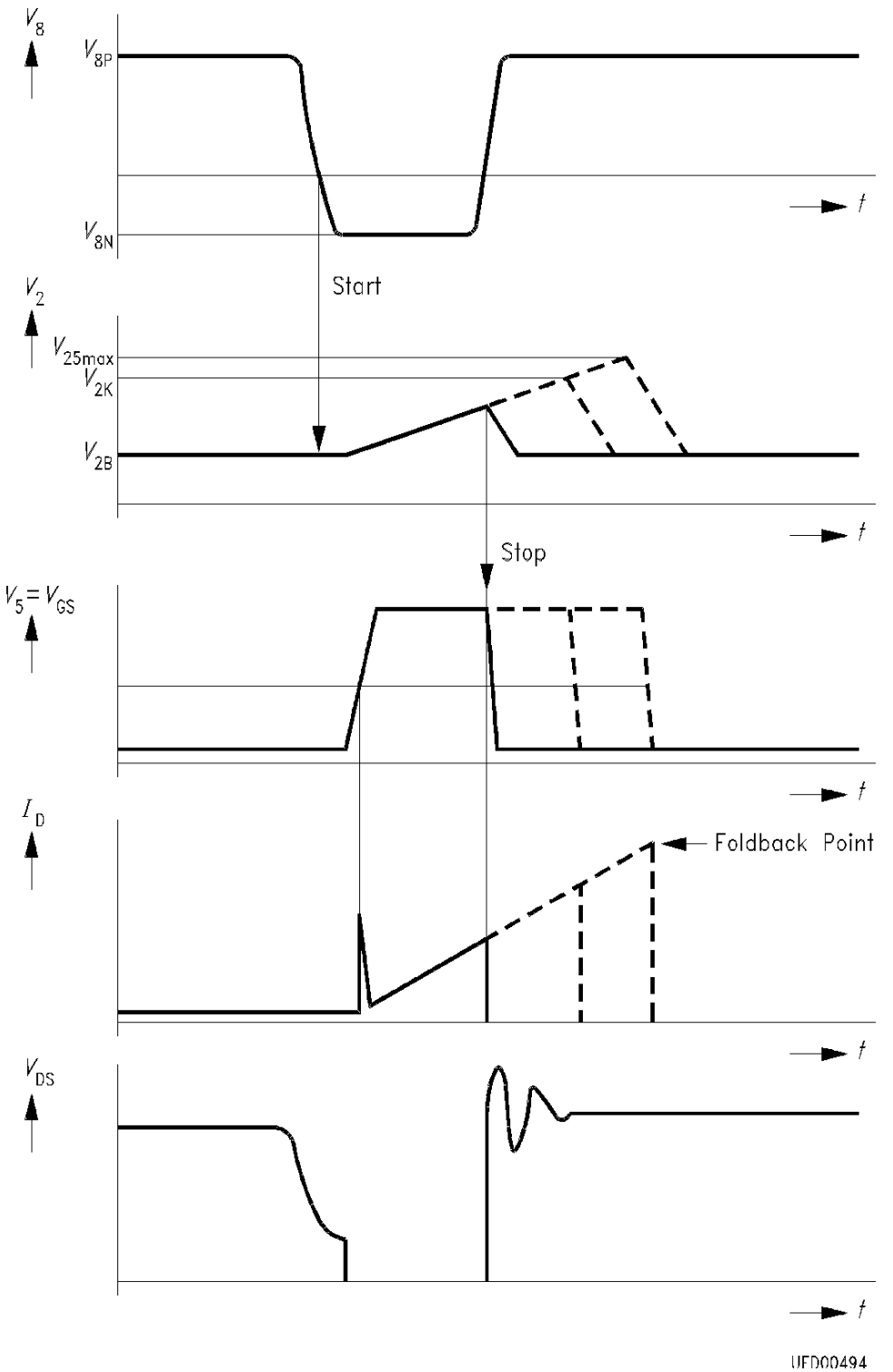


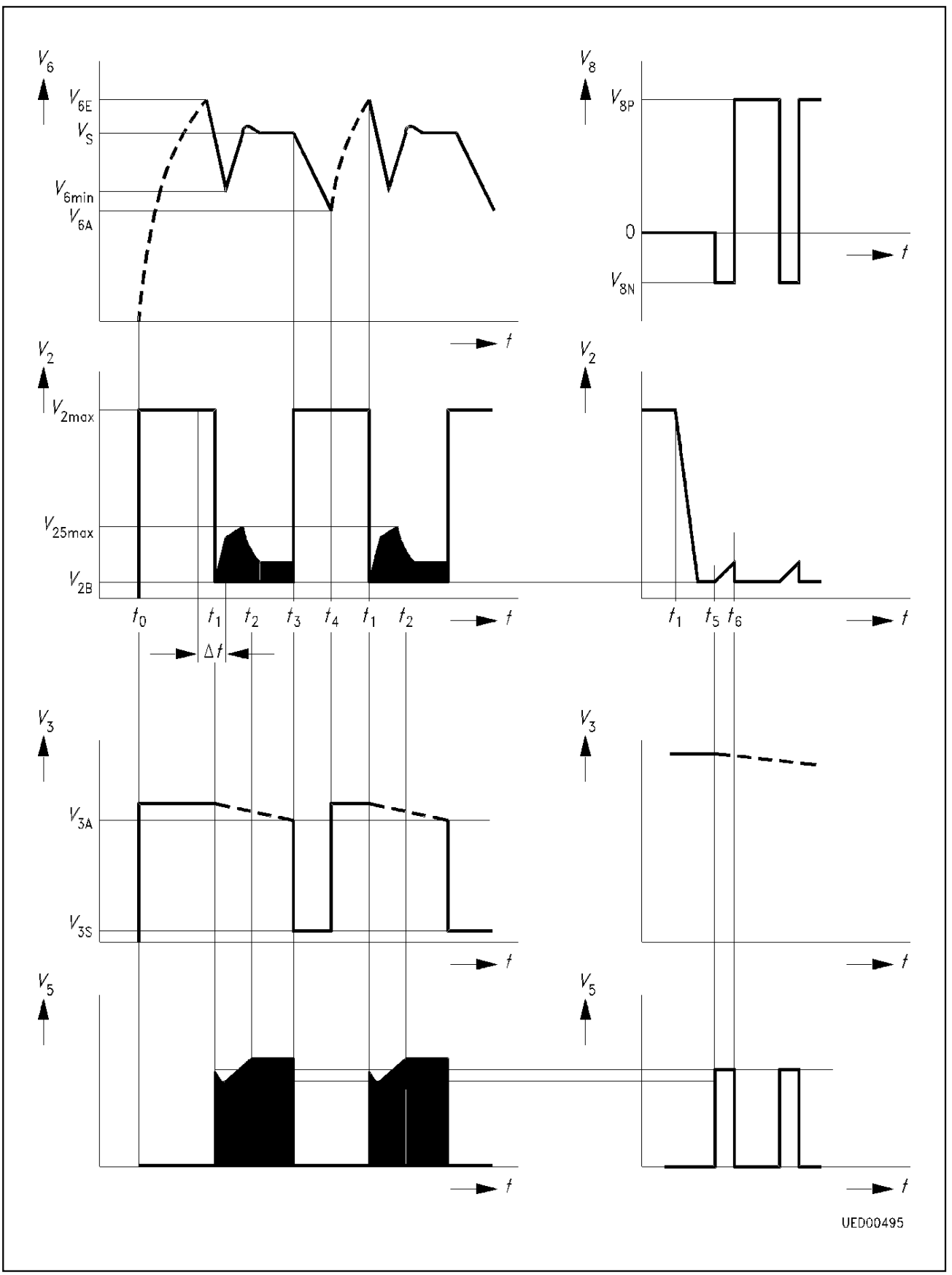
Test Circuit 2



Application Circuit

Diagrams


V_8
V_{8P}
V_{8N}
t
Start
V_2
V_{25max}
V_{2K}
V_{2B}
t
Stop
$V_5 = V_{GS}$
t
I_D
Foldback Point
t
V_{DS}
t
UFD00494


V_6
V_{6E}
V_S
V_{6min}
V_{6A}
t
V_8
V_{8P}
0
V_{8N}
t
V_2
V_{2max}
V_{25max}
V_{2B}
t_0 t_1 t_2 t_3 t_4 t_1 t_2 t
Δt
V_2
t_1 t_5 t_6 t
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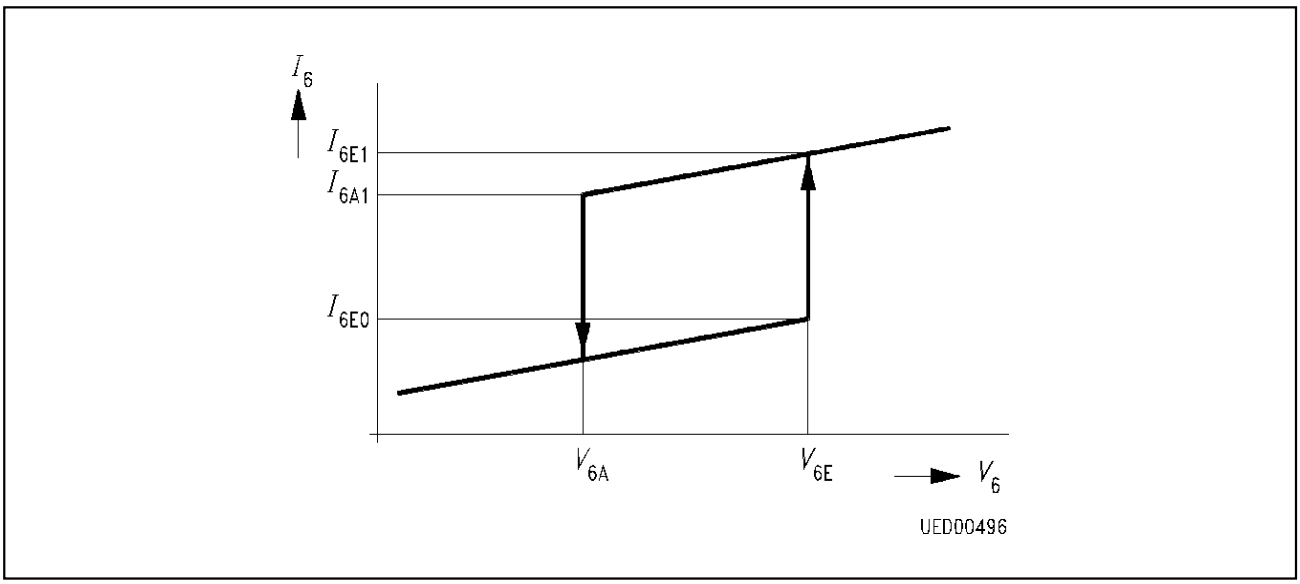
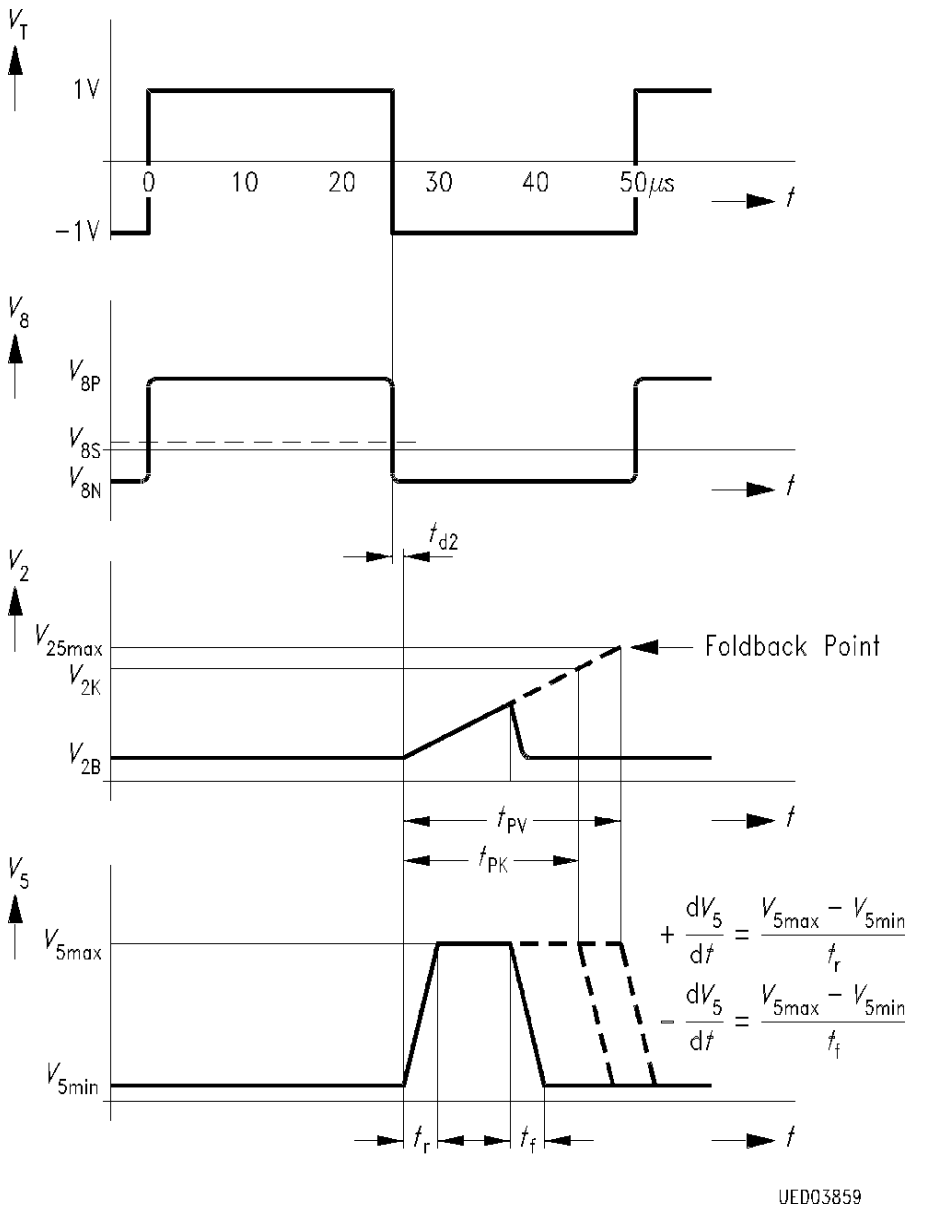
UED00495

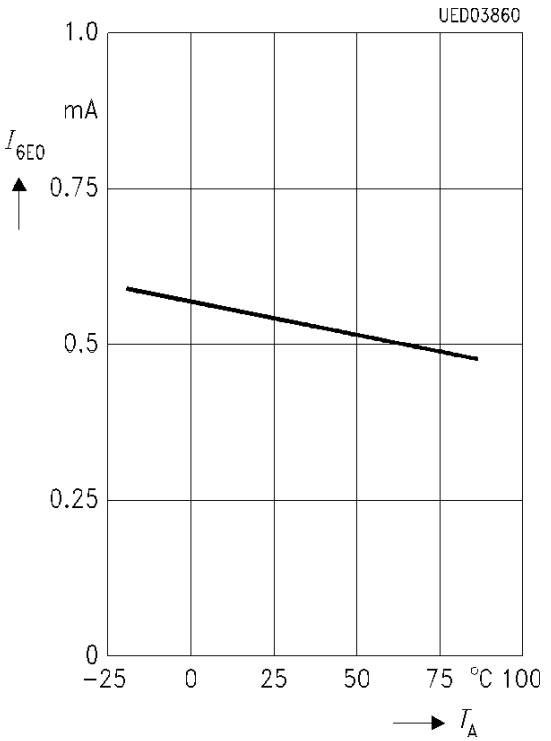


Start-Up Hysteresis

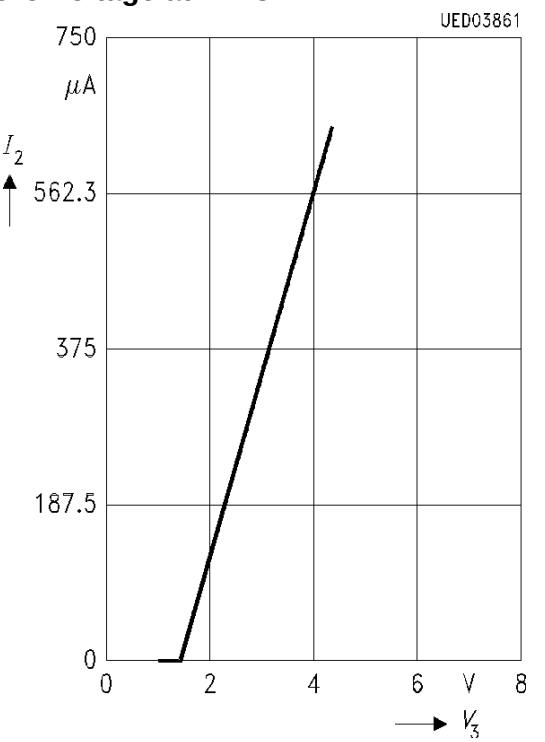


Operation in Test Circuit 2

Start-Up Current as a Function of the Ambient Temperature

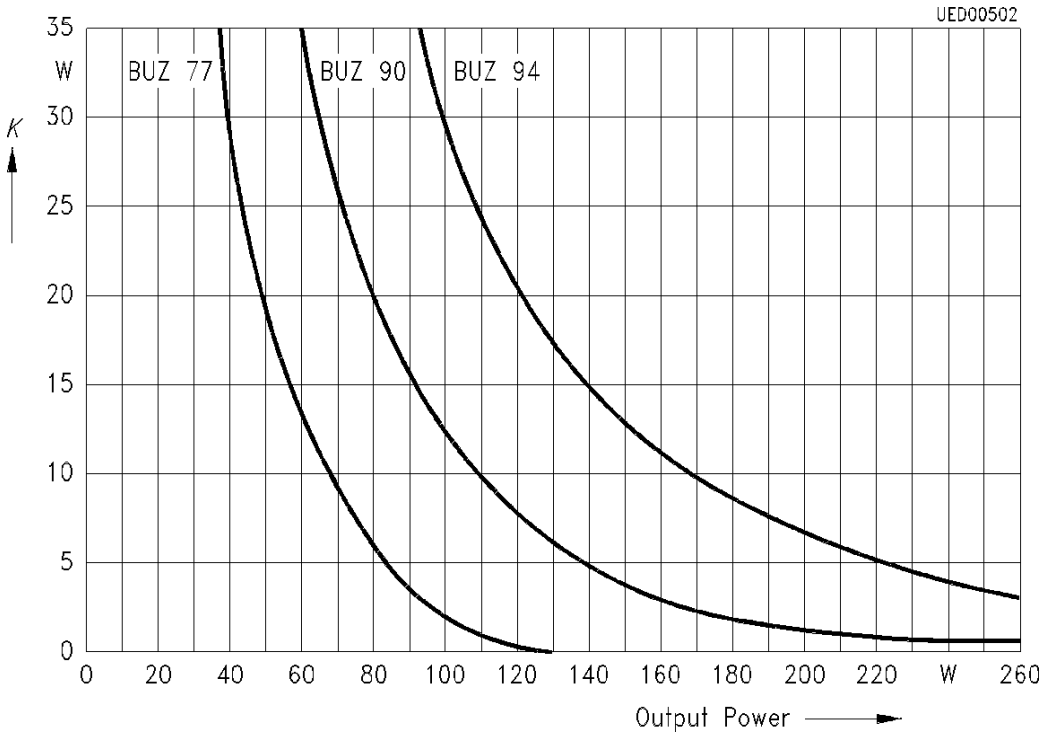


Overload Point Correction as a Function of the Voltage at Pin 3

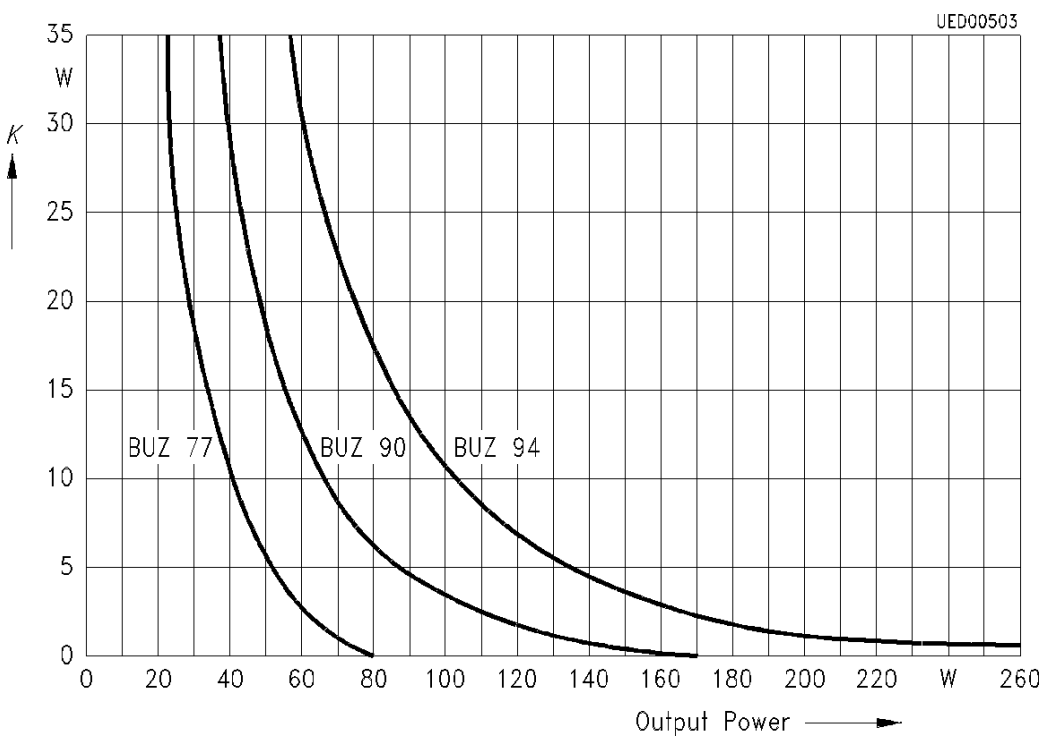


Recommended Heat Sink by 60 °C Ambient Temperature

Narrow Range 180 V ... 120 V ~



Narrow Range 90 V ... 270 V ~



SIEMENS

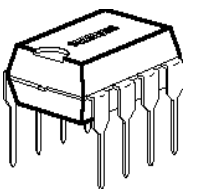
Control IC for Switched-Mode Power Supplies using MOS-Transistor

TDA 4605-3

Bipolar IC

Features

- Fold-back characteristics provides overload protection for external components
- Burst operation under secondary short-circuit condition implemented
- Protection against open or a short of the control loop
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage depending compensation of fold-back point
- Soft-start for quiet start-up without noise generated by the transformer
- Chip-over temperature protection implemented (thermal shutdown)
- On-chip ringing suppression circuit against parasitic oscillations of the transformer
- AGC-voltage reduction at low load



P-DIP-8-1

Type	Ordering Code	Package
TDA 4605-3	Q67000-A5066	P-DIP-8-1

The IC TDA 4605-3 controls the MOS-power transistor and performs all necessary control and protection functions in free running flyback converters. Because of the fact that a wide load range is achieved, this IC is applicable for consumer as well as industrial power supplies.

The serial circuit and primary winding of the flyback transformer are connected in series to the input voltage. During the switch-on period of the transistor, energy is stored in the transformer. During the switch-off period the energy is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations. The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period. A new cycle will start if the transformer has transferred the stored energy completely into the load.

In the different load ranges the switched-mode power supply (SMPS) behaves as follows:

No load operation

The power supply is operating in the burst mode at typical 20 to 40 kHz. The output voltage can be a little bit higher or lower than the nominal value depending of the design of the transformer and the resistors of the control voltage divider.

Nominal operation

The switching frequency is reduced with increasing load and decreasing AC-voltage.
The output voltage is only dependent on the load.

Overload point

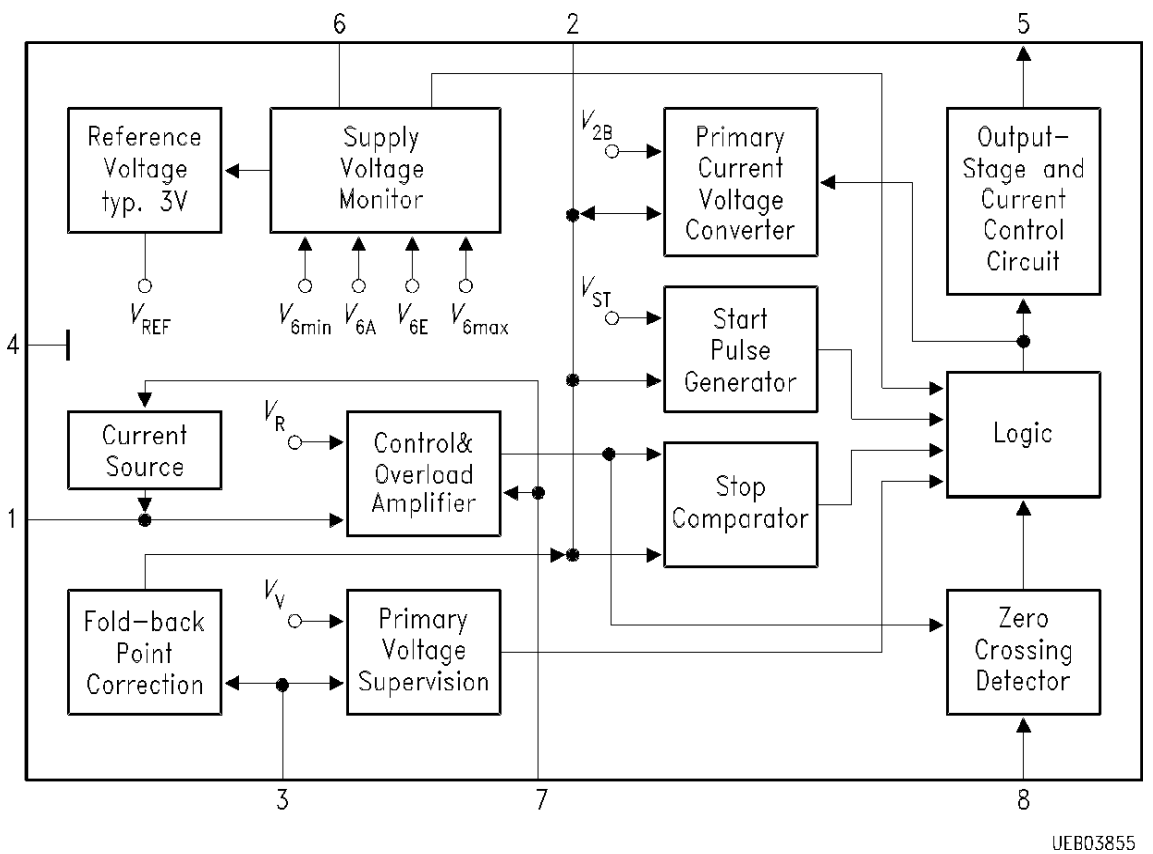
Maximal output power is available at this point of the output characteristic.

Overload

The energy transferred per operation cycle is limited at the top. Therefore the output voltages declines by secondary overloading.

Pin Definitions and Functions

Pin No.	Function
1	**Information Input Concerning Secondary Voltage.** By comparing the regulating voltage - obtained trom the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adjusted to the load of the secondary side (normal, overload, short-circuit, no load).
2	**Information Input Regarding the Primary Current.** The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC-element. When a voltage level is reached thats derived from the regulating voltage at pin 1, the output impulse at pin 5 is terminated. The RC-element serves to set the maximum power at the overload point set.
3	**Input for Primary Voltage Monitoring:** In the normal operation V_3 is moving between the thresholds V_{3H} and V_{3L} ($V_{3H} > V_3 > V_{3L}$). $V_3 < V_{3L}$: SMPS is switched OFF (line voltage too low). $V_3 > V_{3H}$: Compensation of the overload point regulation (controlled by pin 2) starts at $V_{3H} : V_{3L} = 1.7$.
4	**Ground**
5	**Output:** Push-pull output provides $\pm$ 1 A for rapid charge and discharge of the gate capacitance of the power MOS-transistor.
6	**Supply Voltage Input:** A stable internal reference voltage V_{REF} is derived from the supply voltage also the switching thresholds V_{6A} , V_{6E} , $V_{6\ max}$ and $V_{6\ min}$ for the supply voltage detector. If $V_6 > V_{6E}$ then V_{REF} is switched on and swiched off when $V_6 < V_{6A}$. In addition the logic is only enable for $V_{6\ min} < V_6 < V_{6\ max}$.
7	**Input for Soft-Start.** Start-up will begin with short pulses by connecting a capacitor from pin 7 to ground.
8	**Input for the Oscillation Feedback.** After starting oscillation, every zero transition of the feedback voltage (falling edge) through zero (falling edge) triggers an output pulse at pin 5. The trigger threshold is at + 50 mV typical.



Block Diagram

Circuit Description

Application Circuit

The application circuit shows a flyback converter for video recorders with an output power rating of 70 W. The circuit is designed as a wide-range power supply for AC-line voltages of 180 to 264 V. The AC-input voltage is rectified by the bridge rectifier GR1 and smoothed by C_1 . The NTC limits the rush-in current.

In the period before the switch-on threshold is reached the IC is suppled via resistor R_1 ; during the start-up phase it uses the energy stored in C_2 , under steady state conditions the IC receives its supply voltage from transformer winding n_1 via diode D1. The switching transistor T1 is a BUZ 90. The parallel connected capacitor C_3 and the inductance of primary winding n_2 determine the system resonance frequency. The R_2-C_4-D2 circuitry limits overshoot peaks, and R_3 protects the gate of T1 against static charges.

During the conductive phase of the power transistor T1 the current rise in the primary winding depends on the winding inductance and the mains voltage. The network consisting of R_4-C_5 is used to create a model of the sawtooth shaped rise of the collector current. The resulting control voltage is fed into pin 2 of the IC. The RC-time constant given by R_4-C_5 must be designed that way that driving the transistor core into saturation is avoided.

The ratio of the voltage divider R_{10}/R_{11} is fixing a voltage level threshold. Below this threshold the switching power supply shall stop operation because of the low mains voltage. The control voltage present at pin 3 also determines the correction current for the fold-back point. This current added to the current flowing through R_4 and represents an additional charge to C_5 in order to reduce the turn-on phase of T1. This is done to stabilize the fold-back point even under higher mains voltages.

Regulation of the switched-mode power supplies via pin 1. The control voltage of winding n_1 during the off period of T1 is rectified by D3, smoothed by C_6 and stepped down at an adjustable ratio by R_5 , R_6 and R_7 . The R_8-C_7 network suppresses parasitic overshoots (transformer oscillation). The peak voltage at pin 2, and thus the primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the transformer has supplied its energy to the load, the control voltage passes through zero. The IC detects the zero crossing via series resistors R_9 connected to pin 8. But zero crossings are also produced by transformer oscillation after T1 has turned off if output is short-circuited. Therefore the IC ignores zero crossings occurring within a specified period of time after T1 turn-off.

The capacitor C_8 connected to pin 7 causes the power supply to be started with shorter pulses to keep the operating frequency outside the audible range during start-up.

On the secondary side, five output voltages are produced across winding n_3 to n_7 rectified by D4 to D8 and smoothed by C_9 to C_{13} . Resistors R_{12} , R_{14} and R_{19} to R_{21} are used as bleeder resistors. Fusable resistors R_{15} to R_{18} protect the rectifiers against short circuits in the output circuits, which are designed to supply only small loads.

Block Diagram

Pin 1

The regulating voltage forwarded to this pin is compared with a stable internal reference voltage V_R in the **regulating and overload amplifier**. The output of this stage is fed to the stop comparator. If the control voltage is rather small at pin 1 an additional current is added by means of current source which is controlled according the level at pin 7. This additional current is virtually reducing the control voltage present at pin 1.

Pin 2

A voltage proportional to the drain current of the switching transistor is generated there by the external RC-combination in conjunction with the **primary current transducer**. The output of this transducer is controlled by the logic and referenced to the internal stable voltage V_{2B} . If the voltage V_2 exceeds the output voltage of the regulations amplifier, the logic is reset by the stop comparator and consequently the output of pin 5 is switched to low potential. Further inputs for the logic stage are the output for the **start impulse generator** with the stable reference potential V_{ST} and the **supply voltage motor**.

Pin 3

The down divided primary voltage applied there stabilizes the overload point. In addition the logic is disabled in the event of low voltage by comparison with the internal stable voltage V_V in the **primary voltage monitor** block.

Pin 4

Ground

Pin 5

In the output stage the output signals produced by the logic are shifted to a level suitable for MOS-power transistors.

Pin 6

From the supply voltage V_6 are derived a stable internal references V_{REF} and the switching threshold V_{6A} , V_{6E} , $V_{6\,max}$ and $V_{6\,min}$ for the **supply voltage monitor**. All references values (V_R , V_{2B} , V_{ST}) are derived from V_{REF} . If $V_6 > V_{VE}$, the V_{REF} is switched on and switched off when $V_6 < V_{6A}$. In addition, the logic is released only for $V_{6\,min} < V_6 < V_{6\,max}$.

Pin 7

The output of the overload amplifier is connected to pin 7. A load on this output causes a reduction in maximal impulse duration. This function can be used to implement a soft start, when pin 7 is connected to ground by a capacitor.

Pin 8

The zero detector controlling the logic block recognizes the transformer being discharged by positive to negative zero crossing of pin 8 voltage and enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse (double pulsing), because an internal circuit inhibits the zero detector for a finite time t_{UL} after the end of each pulse.

Start-Up Behaviour

The start-up behaviour of the application circuit per sheet 88 is represented an sheet 90 for a line voltage barely above the lower acceptable limit time t_0 the following voltages built up:

- V_6 corresponding to the half-wave charge current over R_1
- V_2 to $V_{2\,max}$ (typically 6.6 V)
- V_3 to the value determined by the divider R_{10}/R_{11}.

The current drawn by the IC in this case is less than 1.6 mA.

If V_6 reaches the threshold V_{6E} (time point t_1), the IC switches on the internal reference voltage. The current draw max. rises to 12 mA. The primary current- voltage reproducer regulates V_2 down to V_{2B} and the starting impulse generator generates the starting impulses from time point t_5 to t_6. The feedback to pin 8 starts the next impulse and so on. All impulses including the starting impulse are controlled in width by regulating voltage of pin 1. When switching on this corresponds to a short-circuit event, i.e. V_1 = 0. Hence the IC starts up with "short-circuit impulses" to assume a width depending on the regulating voltage feedback (the IC operates in the overload range). The IC operates at the overload point. Thereafter the peak values of V_2 decrease rapidly, as the starting attempt is aborted (pin 5 is switched to low). As the IC remains switched on, V_6 further decreases to V_6. The IC switches off; V_6 can rise again (time point t_4) and a new start-up attempt begins at time point t_1. If the rectified alternating line voltage (primary voltage) collapses during load, V_3 can fall below V_{3A}, as is happening at time point t_3 (switch-on attempt when voltage is too low). The primary voltage monitor then clamps V_3 to V_{3S} until the IC switches off ($V_6 < V_{6A}$). Then a new start-up attempt begins at time point t_1.

Regulation, Overload and No-Load Behaviour

When the IC has started up, it is operating in the regulation range. The potential at pin 1 typically is 400 mV. If the output is loaded, the regulation amplifier allows broader impulses (V_5 = H). The peak voltage value at pin 2 increases up to $V_{2S\ max}$. If the secondary load is further increased, the overload amplifier begins to regulate the pulse width downward. This point is referred to as the overload point of the power supply. As the IC-supply voltage V_6 is directly proportional to the secondary voltage, it goes down in accordance with the overload regulation behaviour. If V_6 falls below the value $V_{6\ min}$, the IC goes into burst operation. As the time constant of the half-wave charge-up is relatively large, the short-circuit power remains small. The overload amplifier cuts back to the pulse width t_{pk}. This pulse width must remain possible, in order to permit the IC to start-up without problems from the virtual short-circuit, which every switching on with V_1 = 0 represents. If the secondary side is unloaded, the loading impulses (V_5 = H) become shorter. The frequency increases up to the resonance frequency of the system. If the load is further reduced, the secondary voltages and V_6 increase. When $V_6 = V_{6\ max}$ the logic is blocked. The IC converts to burst operation.This renders the circuit absolutely safe under no-load conditions.

Behaviour when Temperature Exceeds Limit

An integrated temperature protection disables the logic when the chip temperature becomes too high. The IC automatically interrogates the temperature and starts as soon as the temperature decreases to permissible values.

Absolute Maximum Ratings

T_A = – 20 to 85 °C

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Voltages	pin 1	V_1	– 0.3	3	V	
	pin 2	V_2	– 0.3		V	
	pin 3	V_3	– 0.3		V	
	pin 5	V_5	– 0.3	V_6	V	
	pin 6	V_6	– 0.3	20	V	Supply voltage
	pin 7	V_7	– 0.3		V	
Currents	pin 1	I_1		3	mA	
	pin 2	I_2		3	mA	
	pin 3	I_3		3	mA	
	pin 4	I_4	– 1.5		A	$t_p \leq 50$ µs; v ≤ 0.1*)
	pin 5	I_5	– 0.5	1.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 6	I_6		0.5	A	$t_p \leq 50$ µs; v ≤ 0.1
	pin 7	I_7		3	mA	
	pin 8	I_8	– 5	3	mA	
Junction temperature		T_j		125	°C	
Storage temperature		T_{stg}	– 40	125	°C	

Operating Range

Supply voltage	V_6	7.5	15.5	V	IC "on"
Ambient temperature	T_A	– 20	85	°C	
Heat resistance					
Junction to environment	$R_{th\ JE}$		100	K/W	
Junction case	$R_{th\ JC}$		70	K/W	measured at pin 4

*) t_p= pulse width
v= duty circle

Characteristics

T_A = 25 °C; V_S = 10 V

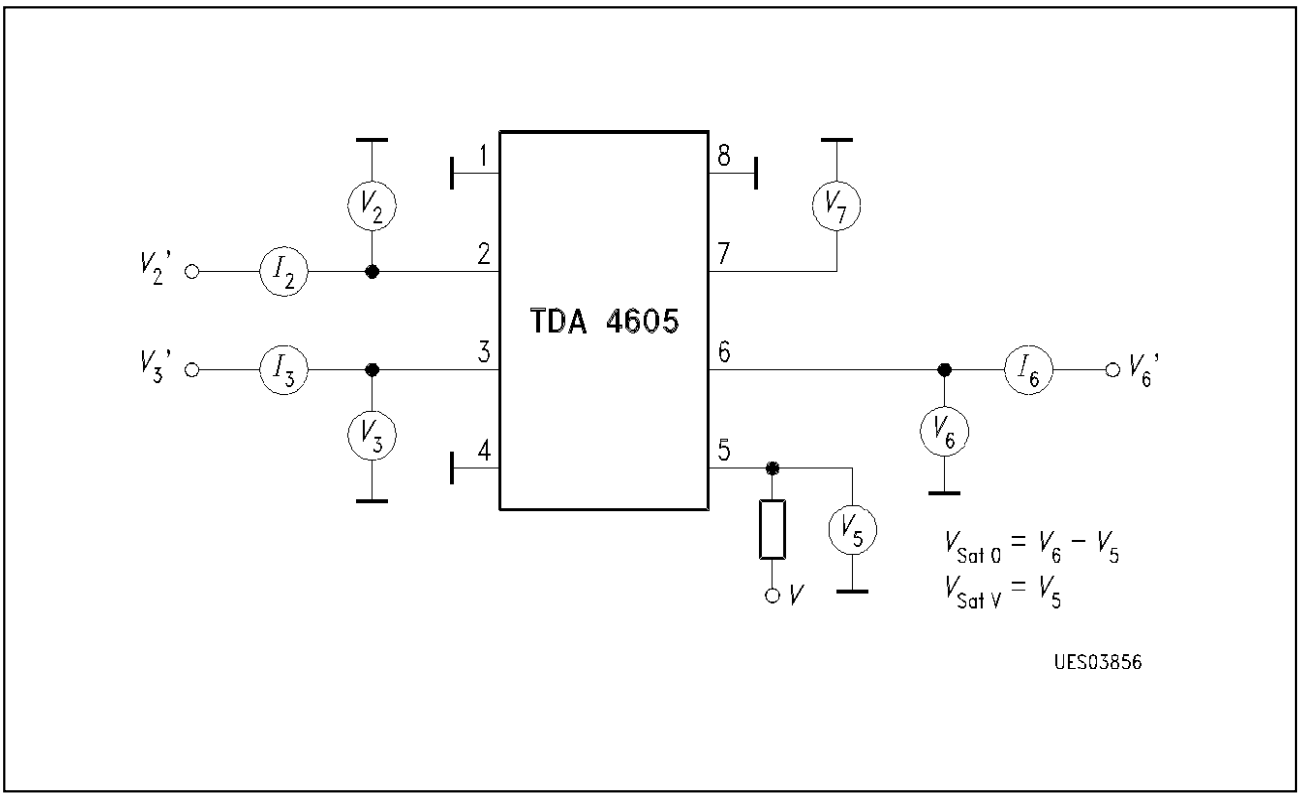
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Start-Up Hysteresis							
Start-up current drain	I_{6E0}		0.6	0.8	mA	$V_6 = V_{6E}$	1
Switch-on voltage	V_{6E}	11	12	13	V		1
Switch-off voltage	V_{6A}	4.5	5	5.5	V		1
Switch-on current	I_{6E1}	7	11	14	mA	$V_6 = V_{6E}$	1
Switch-off current	I_{6A1}	5	10	13	mA	$V_6 = V_{6A}$	1
Voltage Clamp (V_6 = 10 V, IC switched off)							
At pin 2 ($V_6 \leq V_{6E}$) At pin 3 ($V_6 \leq V_{6E}$)	$V_{2\ max}$ $V_{3\ max}$	5.6 5.6	6.6 6.6	8 8	V V	I_2 = 1 mA I_3 = 1 mA	1 1
Control Range							
Control input voltage	V_{1R}	390	400	410	mV		2
Voltage gain of the control circuit in the control range	$-V_R$	30	43	60	dB	V_R = d $(V_{2S} - V_{2B})$ / – dV_1 f = 1 kHz	2
Primary Current Simulation Voltage							
Basic value	V_{2B}	0.97	1.00	1.03	V		2
Overload Range and Short-Circuit Operation							
Peak value in the range of secondary overload	V_{2B}	2.9	3.0	3.1	V	$V_1 = V_{1R}$ – 10 mV	2
Peak value in the range of secondary short-circuit operation	V_{2K}	2.2	2.4	2.6	V	V_1 = 0 V	2
Fold-Back Point Correction							
Fold-back point correction current	$-I_2$	300	500	650	µA	V_3 = 3.7 V	1

Characteristics (cont'd)
T_A = 25 °C; V_S = 10 V

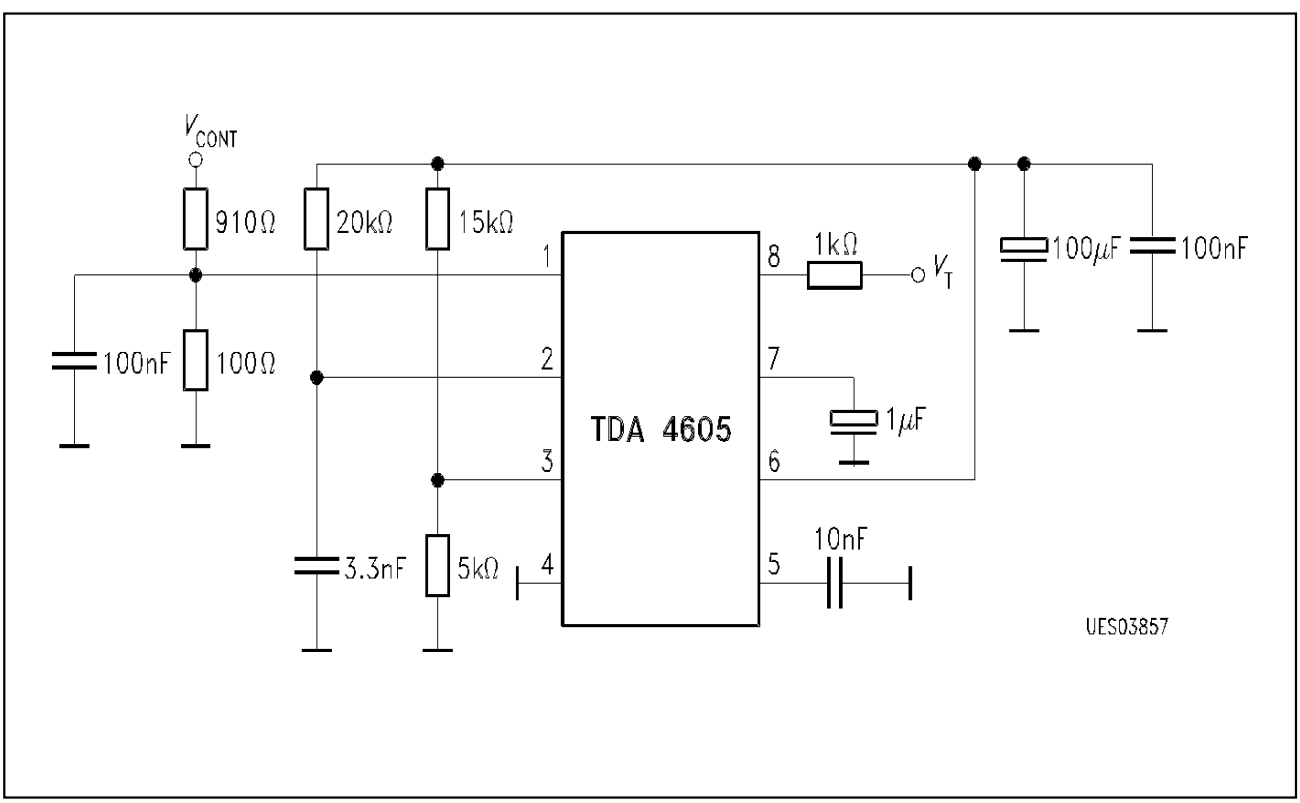
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Generally Valid Data (V_6 = 10 V)							
Voltage of the Zero Transition Detector							
Positive clamping voltage	V_{8P}	0.7	0.75	0.82	V	I_8 = 1 mA	2
Negative clamping voltage	V_{8N}	– 0.25	– 0.2	– 0.15	V	I_8 = – 1 mA	2
Threshold value	V_{8S}	40	50	76	mV		2
Suppression of transformer ringing	t_{UL}	3.0	3.5	3.8	µs		2
Input current	$-I_8$	0		4	µA	V_8 = 0	2
Push-Pull Output Stage							
Saturation voltages							
Pin 5 sourcing	V_{Sat0}		1.5	2.0	V	I_5 = – 0.1 A	1
Pin 5 sinking	V_{SatV}		1.0	1.2	V	I_5 = + 0.1 A	1
Pin 5 sinking	V_{SatV}		1.4	1.8	V	I_5 = + 0.5 A	1
Output Slew Rate							
Rising edge	+ dV_5/dt		70		V/µs		2
Falling edge	+ dV_5/dt		100		V/µs		2
Reduction of Control Voltage							
Current to reduce the control voltage	$-I_1$		50	130	µA	V_7 = 1.1 V, V_1 = 0.4 V	

Characteristics (cont'd)
T_A = 25 °C; V_S = 10 V

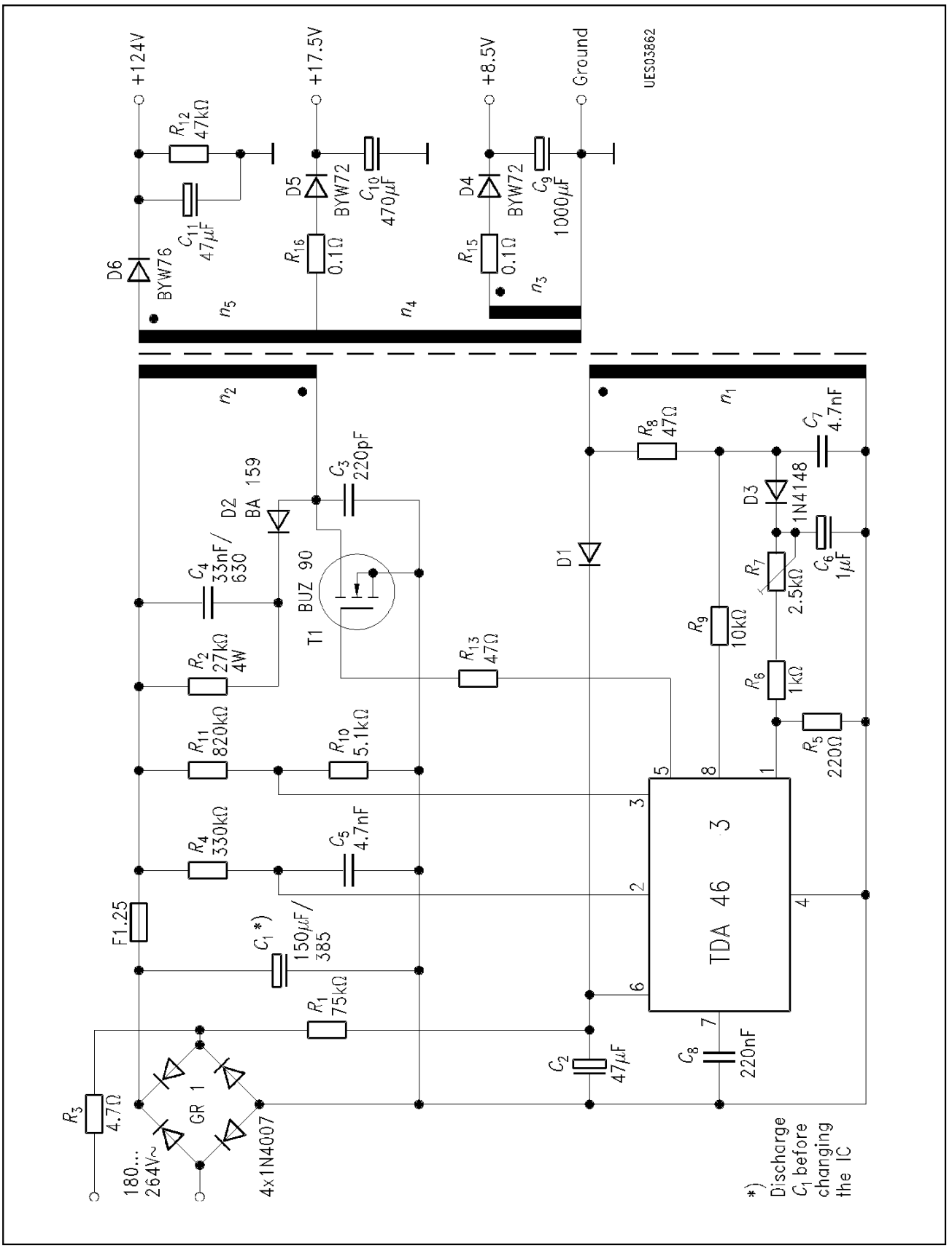
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Protection Circuit							
Undervoltage protection for V_6 : voltage at pin 5 = $V_{5\ min}$ if $V_6 < V_{5\ min}$	$V_{6\ min}$	7.0	7.25	7.5	V		2
Undervoltage protection for V_6 : voltage at pin 5 = $V_{5\ min}$ if $V_6 > V_{6\ max}$	$V_{6\ max}$	15.5	16	16.5	V		2
Undervoltage protection for V_{AC} : voltage at pin 4 = $V_{5\ min}$ if $V_3 < V_{3A}$	V_{3A}	985	1000	1015	mV	V_2 = 0 V	1
Over temperature at the given chip temperature the IC will switch V_5 to $V_{5\ min}$	T_j		150		°C		2
Voltage at pin 3 if one of the protection function was triggered; (V_3 will be clamped until $V_6 < V_{6A}$)	V_{3Sat}		0.4	0.8	V	I_3 = 750 µA	1
Current drain during burst operation	I_6		8		mA	$V_3 = V_2$ = 0 V	1



Test Circuit 1

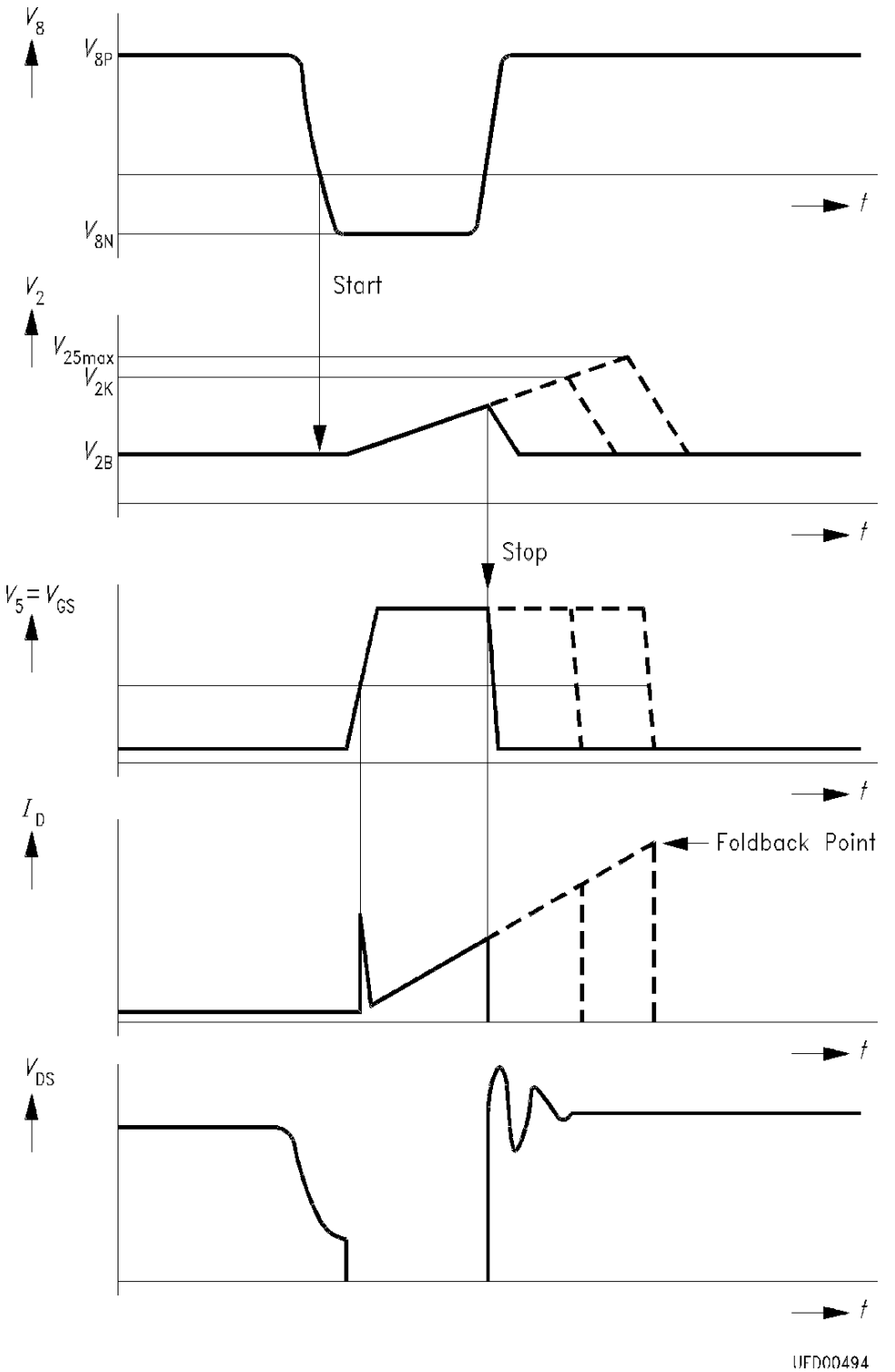


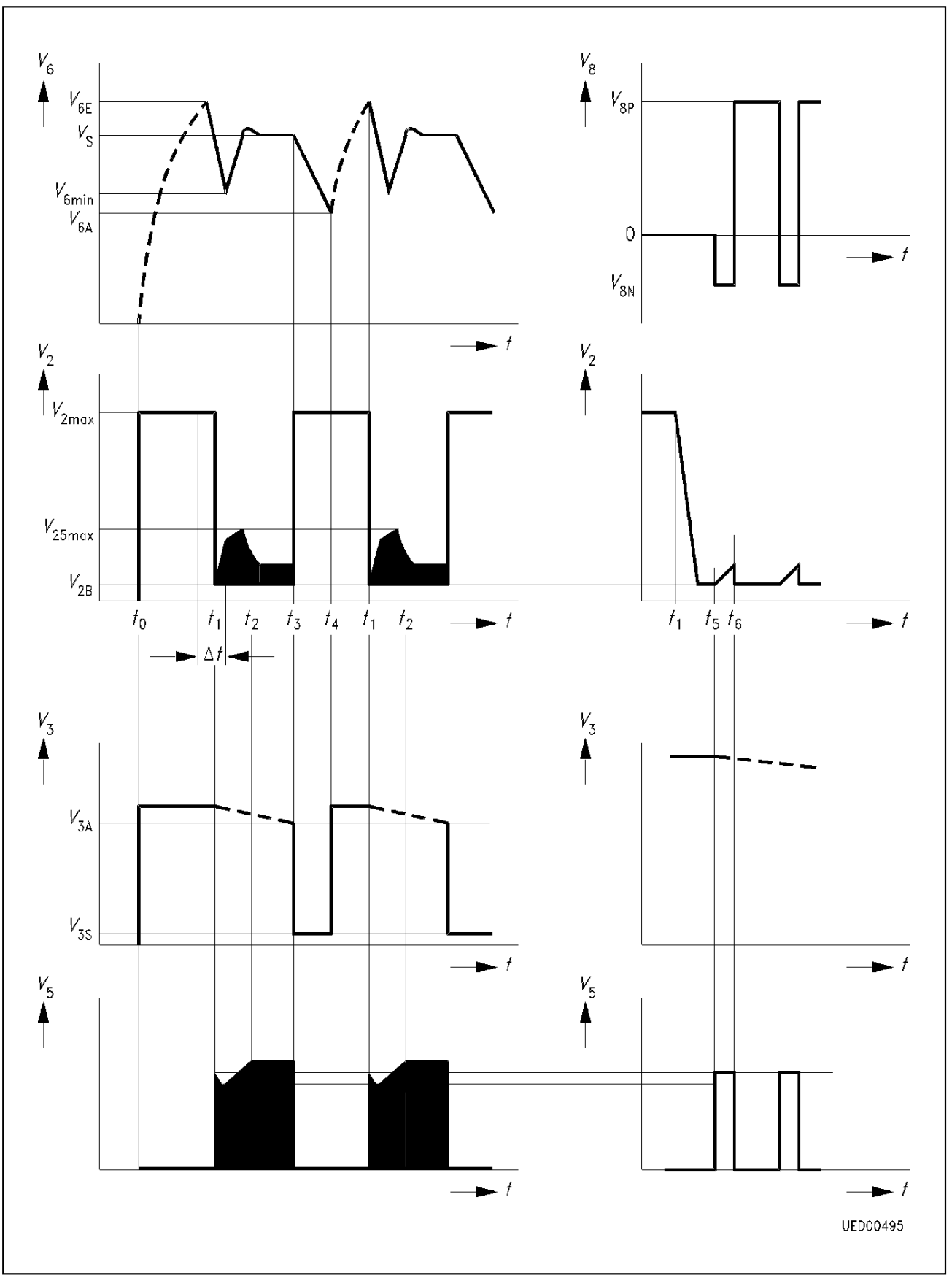
Test Circuit 2



Application Circuit

Diagrams


V_8
V_{8P}
V_{8N}
t
Start
V_2
V_{25max}
V_{2K}
V_{2B}
t
Stop
$V_5 = V_{GS}$
t
I_D
Foldback Point
t
V_{DS}
t
UFD00494


V6
V6E
VS
V6min
V6A
t
V8
V8P
0
V8N
t
V2
V2max
V25max
V2B
t0
t1
t2
t3
t4
t1
t2
Δt
t
V2
t1
t5
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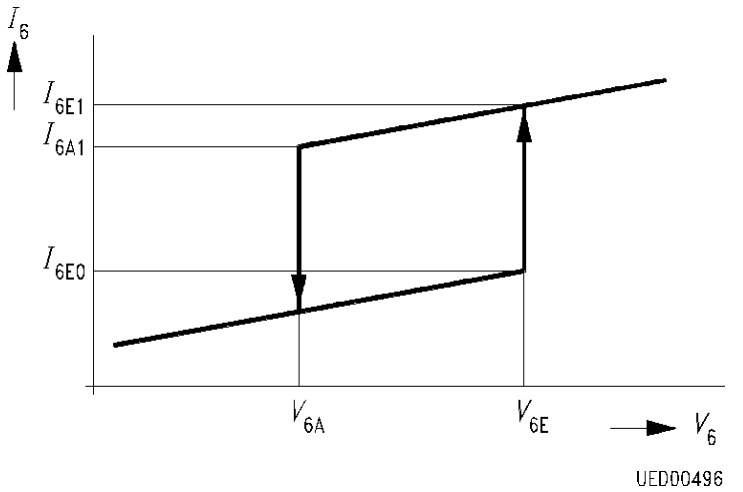
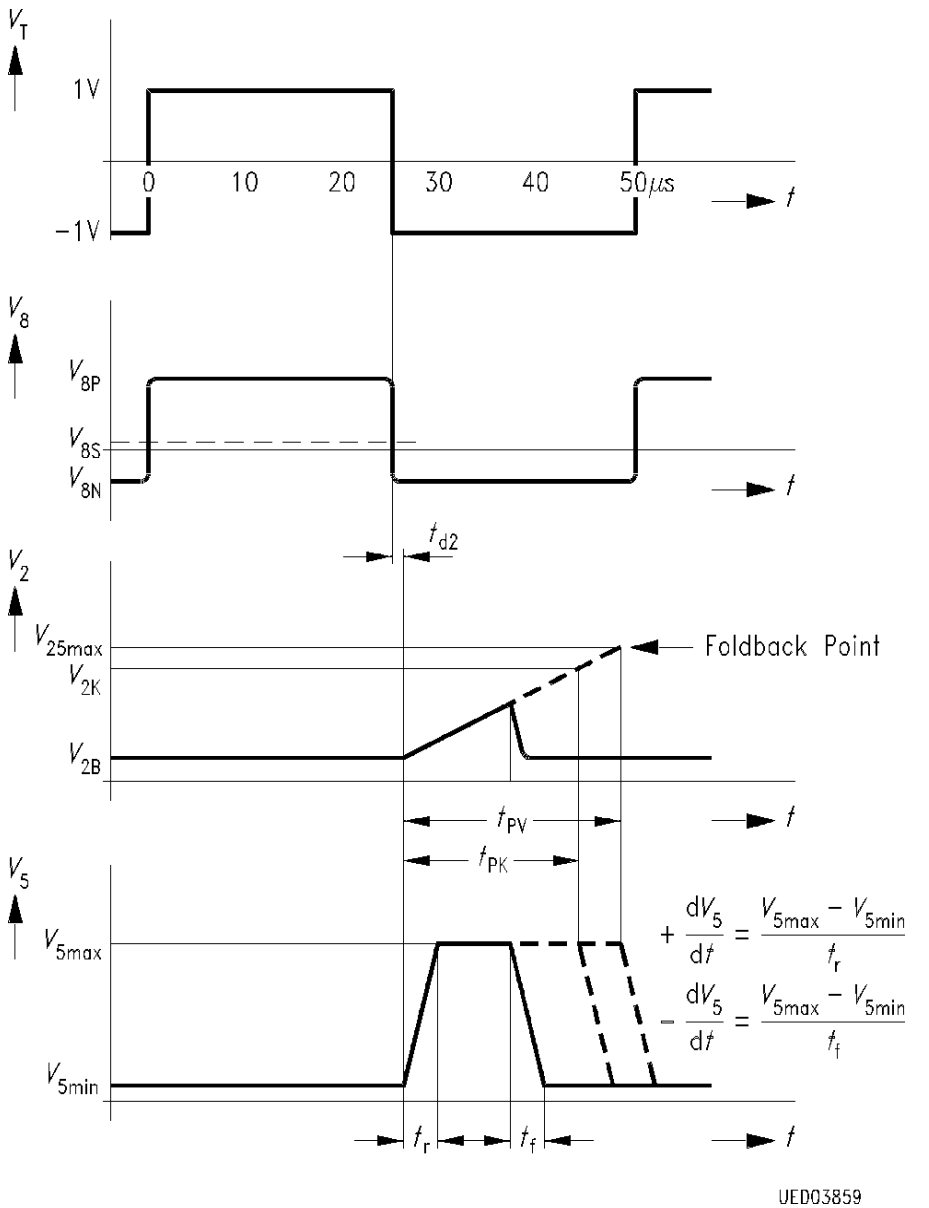
V3
V3A
V3S
t
V3
t
V5
t
V5
t
UED00495

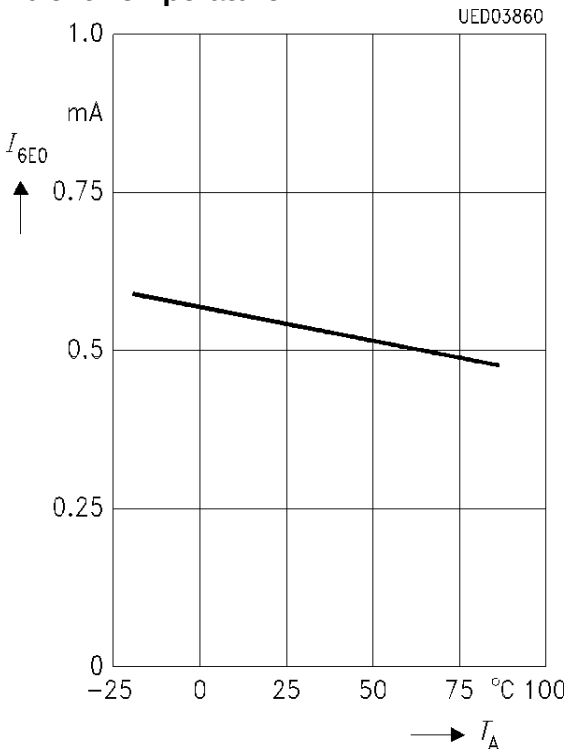


Start-Up Hysteresis

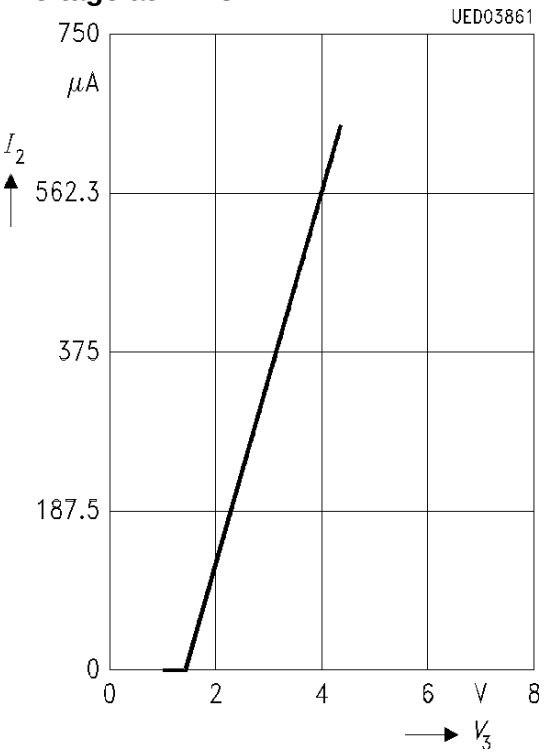


Operation in Test Circuit 2

Start-Up Current as a Function of the Ambient Temperature

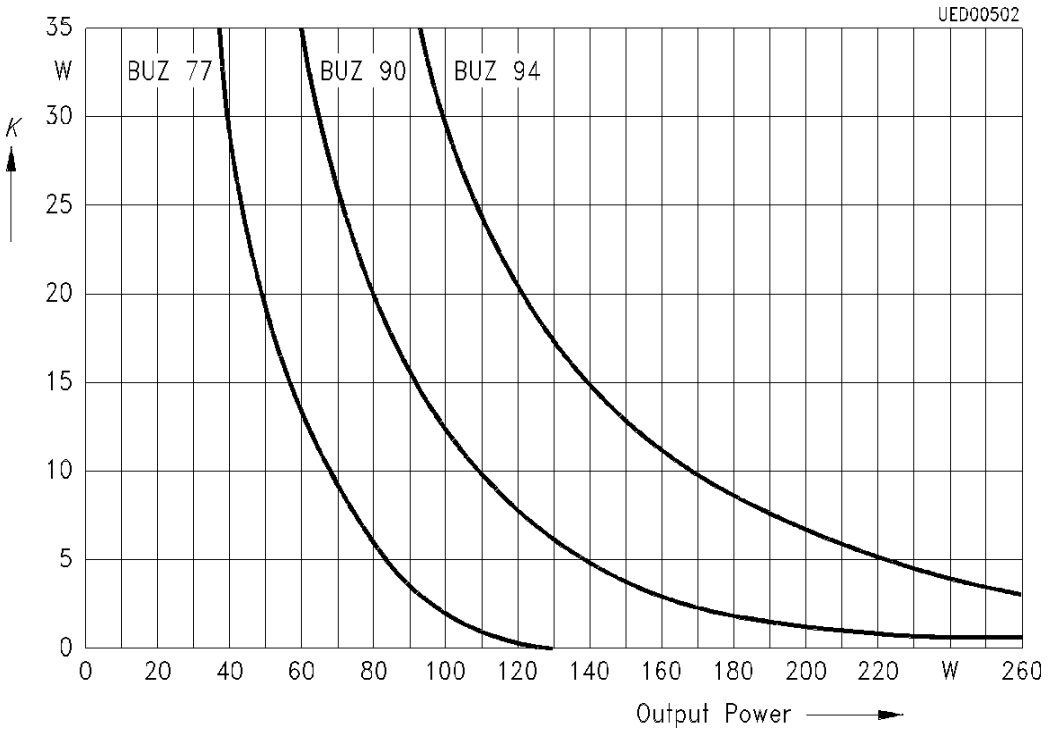


Overload Point Correction as a Function of the Voltage at Pin 3

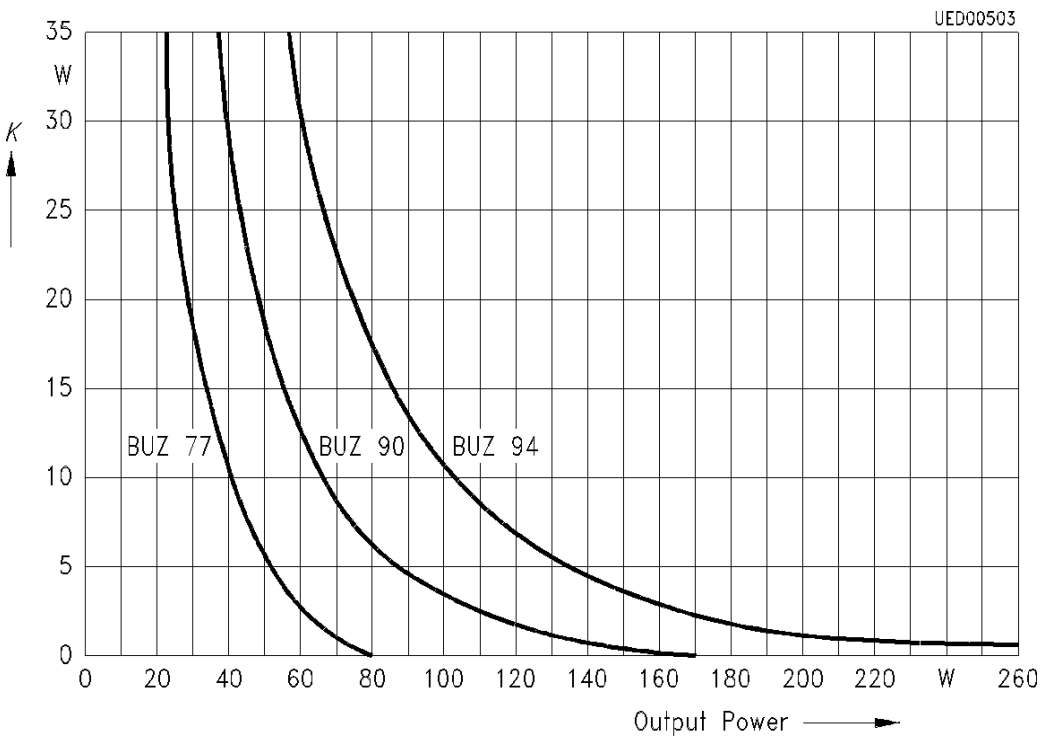


Recommended Heat Sink by 60 ˚C Ambient Temperature

Narrow Range 180 V ... 120 V ~



Narrow Range 90 V ... 270 V ~



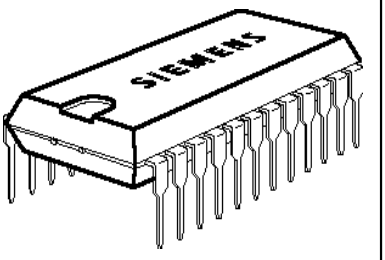
SIEMENS

Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies (SMPS)

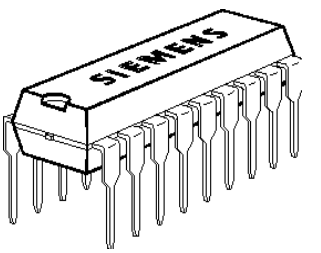
TDA 4700
TDA 4718

Features

- Feed-forward control (line hum suppression)
- Symmetry inputs for push-pull converter (TDA 4700)
- Push-pull outputs
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression



P-DIP-24-1



P-DIP-18-1

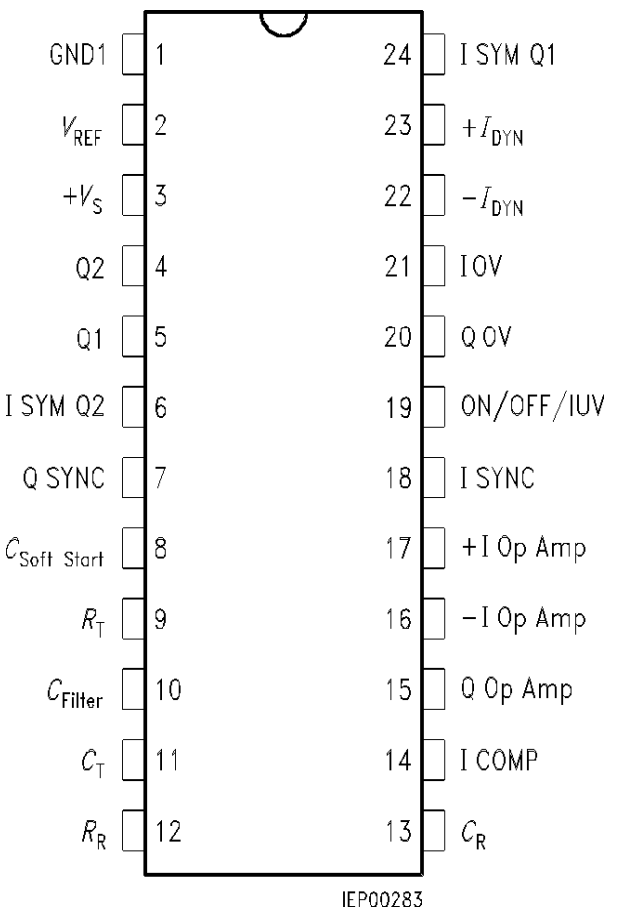
■ Type	Ordering Code	Package	Temp.-Range
TDA 4700 A	Q67000-Y594	P-DIP-24-1	– 0 to 70 °C
TDA 4718 A	Q67000-Y639	P-DIP-18-1	– 0 to 70 °C

■ Not for new design

These versatile SMPS control ICs comprise digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers, which activate protective functions.

[1] Is now available for temperature range – 25 to 85 °C.

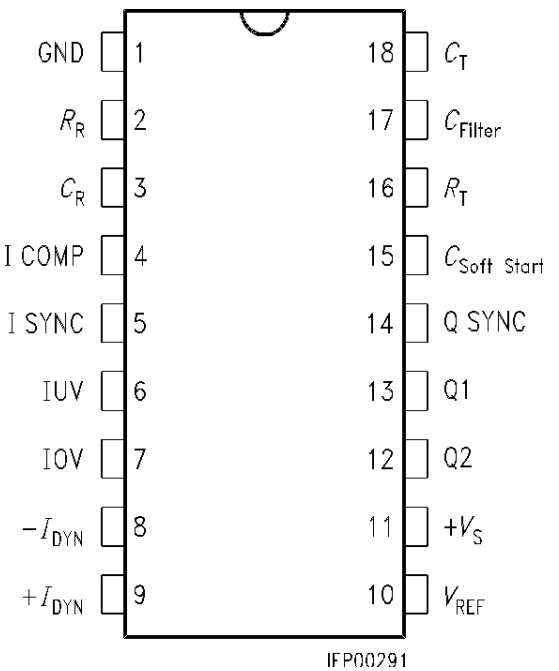
Pin Configuration (TDA 4700)
(top view)



Pin Definitions and Functions (TDA 4700)

Pin	Symbol	Function
1	GND	Ground 0 V
2	+ V_{REF}	Reference voltage
3	+ V_S	Supply voltage
4	Q2	Output Q2
5	Q1	Output Q1
6	I SYM Q2	Symmetry Q2
7	Q SYNC	Sync. output
8	$C_{soft\ start}$	Soft start
9	R_T	VCO R_T
10	C_{filter}	Capacitance
11	C_T	VCO C_T
12	R_R	Ramp generator R_R
13	C_R	Ramp generator C_R
14	I COMP	Comparator input
15	Q Op Amp	Operational amplifier output
16	– I Op Amp	Operational amplifier input (–)
17	+ I Op Amp	Operational amplifier input (+)
18	I SYNC	Sync. input
19	ON/OFF/IUV	ON/OFF, undervoltage
20	QOV	Overvoltage output
21	IOV	Overvoltage input
22	– I_{DYN}	Dynamic current limitation (–)
23	+ I_{DYN}	Dynamic current limitation (+)
24	I SYM Q1	Symmetry

Pin Configuration (TDA 4718)
(top view)



Pin Definitions and Functions (TDA 4718)

Pin	Symbol	Function
1	GND	Ground 0 V
2 3	R_R C_R	Ramp generator R_R Ramp generator C_R
4 5	I COMP I SYNC	+ Input comparator K2 Sync. input
6 7	IUV IOV	Input undervoltage, ON/OFF Input overvoltage
8 9	$-I_{DYN}$ $+I_{DYN}$	Input dynamic current limitation (–) Input dynamic current limitation (+)
10 11	$+V_{REF}$ $+V_S$	Reference voltage Supply voltage
12 13	Q 2 Q 1	Output Q2 Output Q1
14 15	Q SYNC $C_{soft\ start}$	Sync. output Soft start
16 17 18	R_T C_{filter} C_T	VCO R_T Capacitance VCO C_T

Circuit Description

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a DC voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called “feed-forward control”, is utilized to compensate for known interference such as ripple on the input voltage.

Phase Comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. The component can be frequency-synchronized, but not phase-synchronized, with the sync input. The duty cycle of the squarewave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active outputs is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier K1 (TDA 4700; A)

The K1 op amp is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and + 5 V.

Pulse-Turn-OFF Flipflop

The pulse turn-OFF flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2) to a maximum of + 5 V. The voltage at the ramp generator output may, however rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{\text{R}}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, cause the component to switch on again by the soft start.

Comparator K5, K6, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

K7 has a common-mode range covers 0 V and + 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Symmetry (TDA 4700; A)

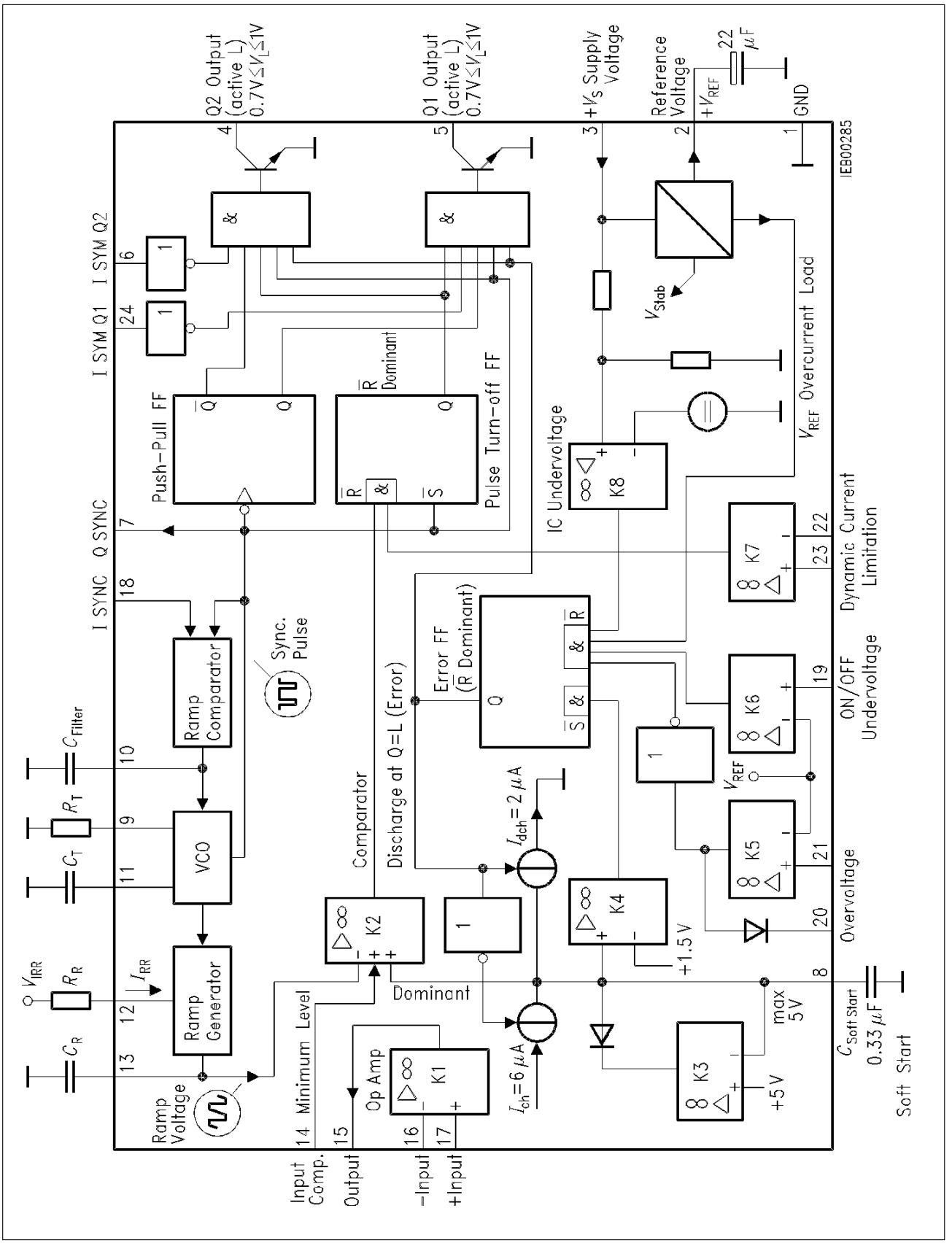
In push-pull converters, a saturation of the transformer core must be prevented. The degree of saturation of the transformer can be determined with an external circuit, thus the active periods of the outputs can be decreased unsymmetrically at the symmetry inputs.

Outputs

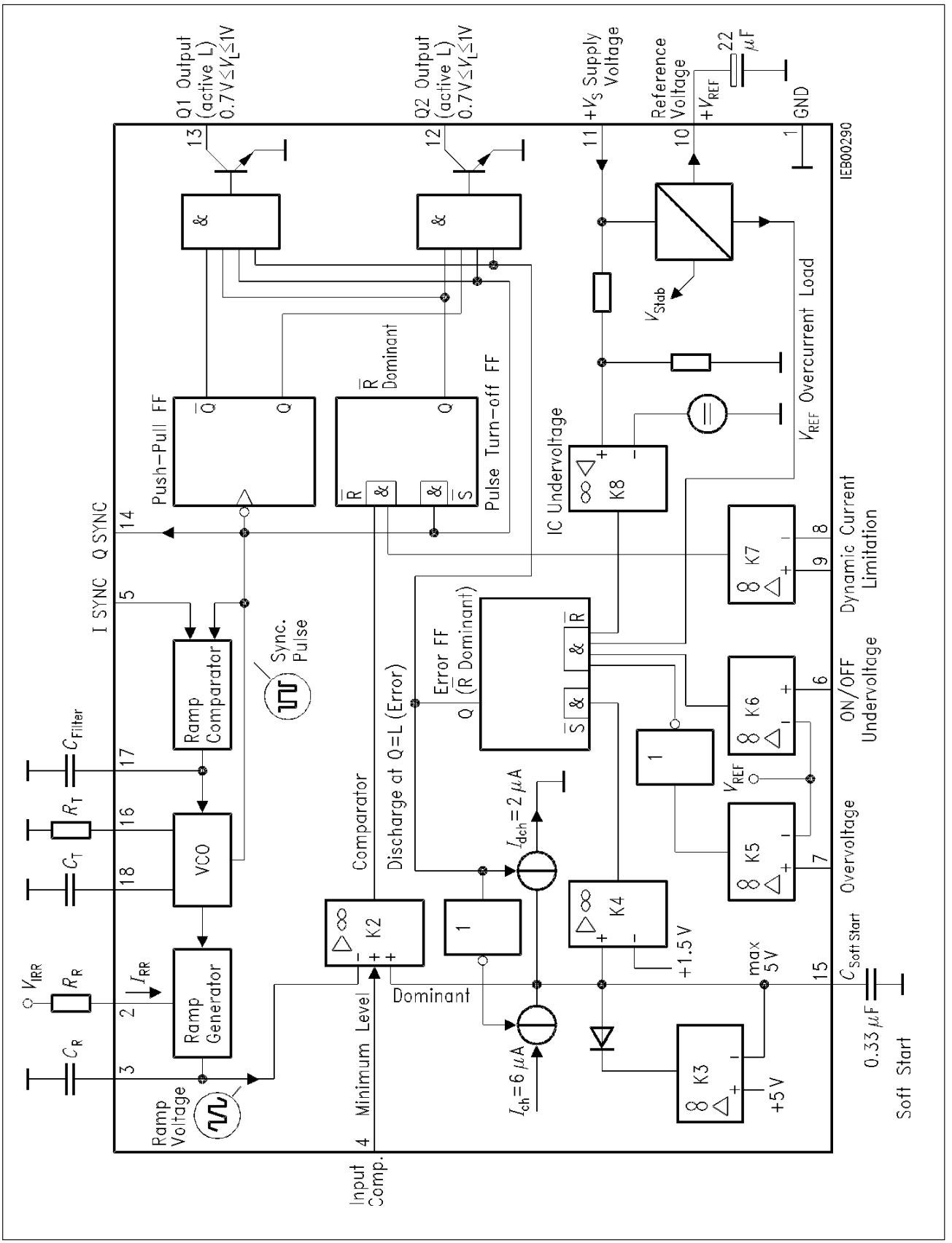
Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.



Block Diagram (TDA 4700)



Block Diagram (TDA 4718)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	– 0.3	33	V	
Voltage at Q1, Q2	V_Q	– 0.3	33	V	Q1, Q2 high
Current at Q1, Q2	I_Q		70	mA	Q1, Q2 low
Symmetry 1, 2 TDA 4700; A	V_{SYM}	– 0.3	33	V	
Sync output	$V_{SYNC\ Q}$	– 0.3	7	V	SYNC Q high
	$I_{SYNC\ Q}$	0	10	mA	SYNC Q low
Sync input	$V_{SYNC\ I}$	– 0.3	33	V	
Input C_{filter}	$V_{I\ Cf}$	– 0.3	7	V	
Input R_T	$V_{I\ RT}$	– 0.3	7	V	
Input C_T	$V_{I\ CT}$	– 0.3	7	V	
Input R_R	$V_{I\ RR}$	– 0.3	7	V	
Input C_R	$I_{I\ CR}$	– 10	10	mA	
Input comparator K2, K5, K6, K7	$V_{I\ K}$	– 0.3	33	V	
Output K5	$V_{Q\ K5}$	– 0.3	33	V	
Input op amp TDA 4700; A	$V_{I\ Op\ Amp}$	– 0.3	33	V	
Output op amp TDA 4700; A	$V_{Q\ Op\ Amp}$	– 0.3	V_S – 1	V	
			max. 7	V	
Reference voltage	V_{REF}	– 0.3	V_{REF}	V	
Input $C_{soft\ start}$	$V_{I\ soft\ start}$	– 0.3	7	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Thermal resistance system - air TDA 4700; A	$R_{th\ SA}$		65	K/W	
TDA 4718	$R_{th\ SA}$		70	K/W	
TDA 4718 A	$R_{th\ SA}$		60	K/W	

Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	10.5	30	V	
Ambient temperature TDA 4700 TDA 4718 TDA 4700 A TDA 4718 A	 T_A T_A	 – 25 0	 85 70	 °C °C	
VCO frequency Ramp generator frequency	f f_{RG}	40 40	250 000 250 000	Hz Hz	

Characteristics

V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_S	8		20	mA	C_T = 1 nF f_{VCO} = 100 kHz
Reference						
Reference voltage	V_{REF}	2.35	2.5	2.65	V	0 mA < I_{REF} < 5 mA
Reference voltage change	ΔV_{REF}		8		mV	14 V ± 20 %
Reference voltage change	ΔV_{REF}		15		mV	25 V ± 20 %
Reference voltage change	ΔV_{REF}			15[1)]	mV	0 mA < I_{REF} < 5 mA
Temperature coefficient	TC		0.25	0.4	mV/K	
Response threshold of I_{REF} overcurrent	I_{REF}		10		mA	

1) At T_A = 0 to 70 °C, this value falls to max. 5 mV

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator (VCO)						
Frequency range	f_{VCO}	40		100 000	Hz	
Frequency change	$\Delta f/f_{VCO}$		0.5		%	14 V ± 20 %
Frequency change	$\Delta f/f_{VCO}$	– 1		1	%	25 V ± 20 %
Tolerance	$\Delta f/f_{VCO}$	– 7		7	%	$\Delta R_T = 0$; $\Delta C_T = 0$
Fall time sawtooth	t		1		µs	C_T = 1 nF
	t		10		µs	C_T = 10 nF
RC combination	C_T	0.82		47	nF	
VCO	R_T	5		700	kΩ	
Ramp Generator						
Frequency range	f	40		100 000	Hz	
Maximum voltage at C_R	V_H		5.5		V	
Minimum voltage at C_R	V_L		1.8		V	
Input current through R_R	I_{RR}	0		400	µA	
Current transformation ratio	I_{RR}/I_{CR}		1/4			
Synchronization						
Sync output	$V_{Q\,H}$	4			V	$I_{Q\,H}$ = – 200 µA
	$V_{Q\,L}$			0.4	V	$I_{Q\,L}$ = 1.6 mA
Sync input	$V_{I\,H}$	2			V	
	$V_{I\,L}$			0.8	V	
Input current	$-I_I$			5	µA	

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Comparator K2						
Input current	$-I_{I\,K2}$			2	µA	
Turn-OFF delay[1]	$t_{D\,OFF}$			500	ns	
Input voltage	$V_{I\,K2}$					for duty cycle
			1.8		V	D = 0
			5		V	D = max.
Common-mode input voltage range	$V_{I\,C}$	0		5.5	V	
Soft Start K3, K4						
Charge current for $C_{soft\ start}$	I_{ch}		6		µA	
Discharge current for $C_{soft\ start}$	I_{dch}		2		µA	
Upper limiting voltage	V_{lim}		5		V	
Switching voltage K4	V_{K4}		1.5		V	
Operational Amplifier K1 (TDA 4700; TDA 4700 A)						
Open-loop voltage gain	G_{V0}	60	80		dB	
Input offset voltage	V_{IO}	– 10		10	mV	
Temperature coefficient of V_{IO}	TC	– 30		30	µV/K	
Input current	$-I_I$			2	µA	
Common-mode input voltage range	V_{IC}	0		5	V	
Output current	I_Q	– 3		1.5	mA	
Rise time of output voltage	$\Delta V/\Delta t$		1		V/µs	
Transition frequency	f_T		3		MHz	
Phase at f_T	φ_T		120		deg.	
Output voltage	$V_{Q\,H/L}$	1.5		5.5	V	$-3\,mA < I < 1.5\,mA$

[1] At the input: step function ΔV = – 100 mV ⌐► ΔV = + 100 mV

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Symmetry (TDA 4700; TDA 4700 A)						
Input voltage	$V_{I\,H}$	2.0			V	
	$V_{I\,L}$			0.8	V	
Input current	$-I_I$			2	µA	
Output Stages Q1, Q2						
Output voltage	$V_{Q\,H}$			30	V	
	$V_{Q\,L}$			1.1	V	I_Q = 20 mA
Output leakage current	I_Q			2	µA	$V_{Q\,H}$ = 30 V
ON, OFF, Undervoltage K6						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Turn-OFF delay time[1]	$t_{D\,OFF}$		250		ns	
Error detection time[1]	t		50		ns	
Dynamic Current Limitation K7						
Common-mode input voltage range	V_{IC}	0		4	V	
Input offset voltage	V_{IO}	– 10		10	mV	
Input current	$-I_I$			2	µA	
Turn-OFF delay time[2]	$t_{D\,OFF}$		250		ns	
Error detection time[2]	t		50		ns	
Overvoltage K5						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Output current	$-I_Q$	0		200	µA	$V_{QH\ min}$ = 5 V
Turn-OFF delay time[1]	$t_{D\,OFF}$		250		ns	
Error detection time[1]	t		50		ns	

[1] At the input: step function $\Delta V = V_{REF}$ – 100 mV ⌐→ V_{REF} + 100 mV
[2] At the input: step function ΔV = – 100 mV ⌐→ ΔV = + 100 mV

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

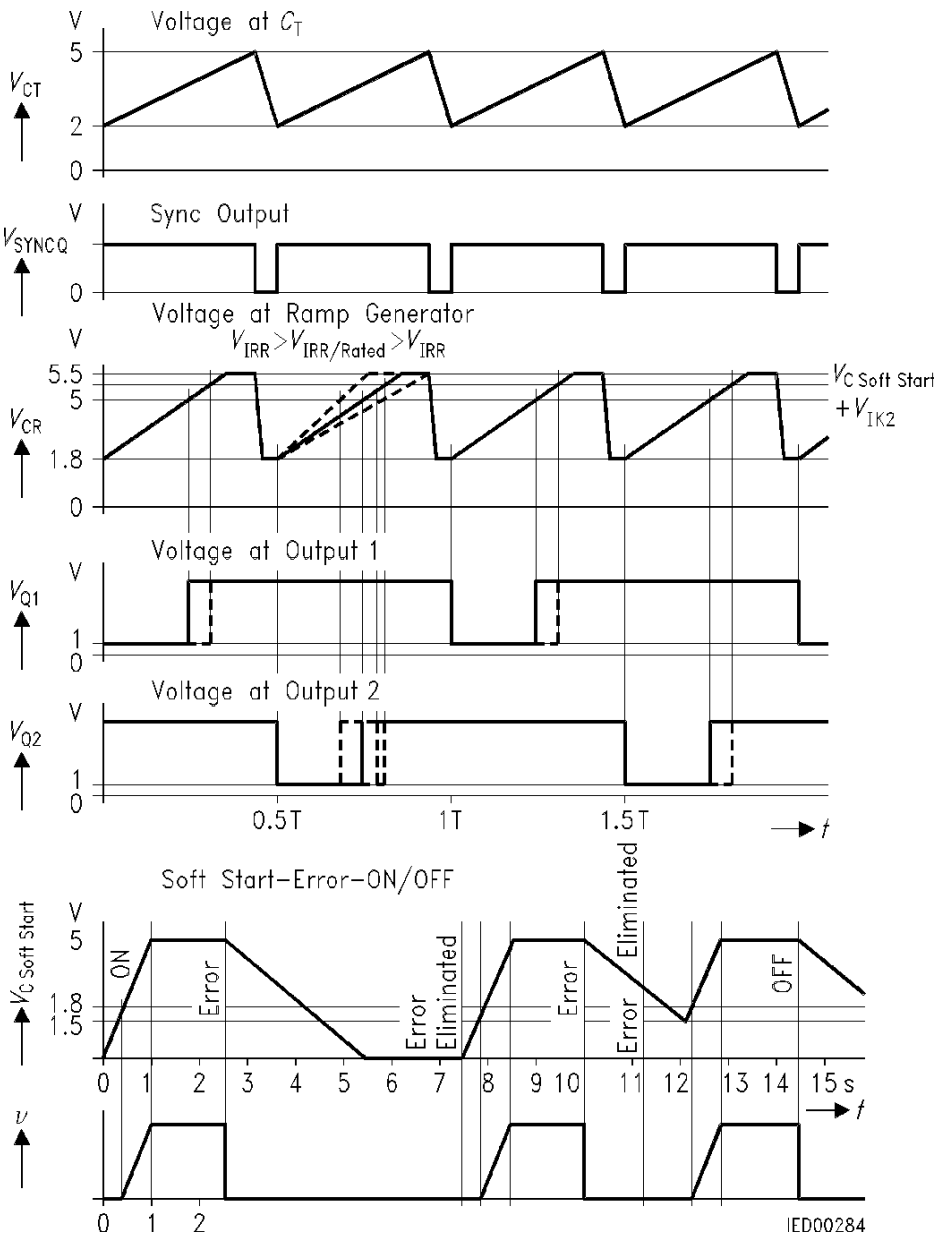
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Undervoltage						
Turn-ON threshold for V_S rising	V_S	8.8		11 10.5	V V	0 °C < T_A < 70 °C
Turn-OFF threshold for V_S falling	V_S	8.5		10.5 10	V V	0 °C < T_A < 70 °C
Input C_{filter}						
Rated voltage for rated frequency	V_R		4		V	
Frequency approx. proportional to voltage within the range	V_R	3		5	V	
Voltage at open sync input	$V_{C\ filter}$		1.6		V	

Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\ start}$.
5. In the case of a free-running VCO: connect sync output with sync input.
6. Wiring of the op amp according to the dynamic requirements and connection of its output with the free input of K2. (TDA 4700; TDA 4700 A)
7. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

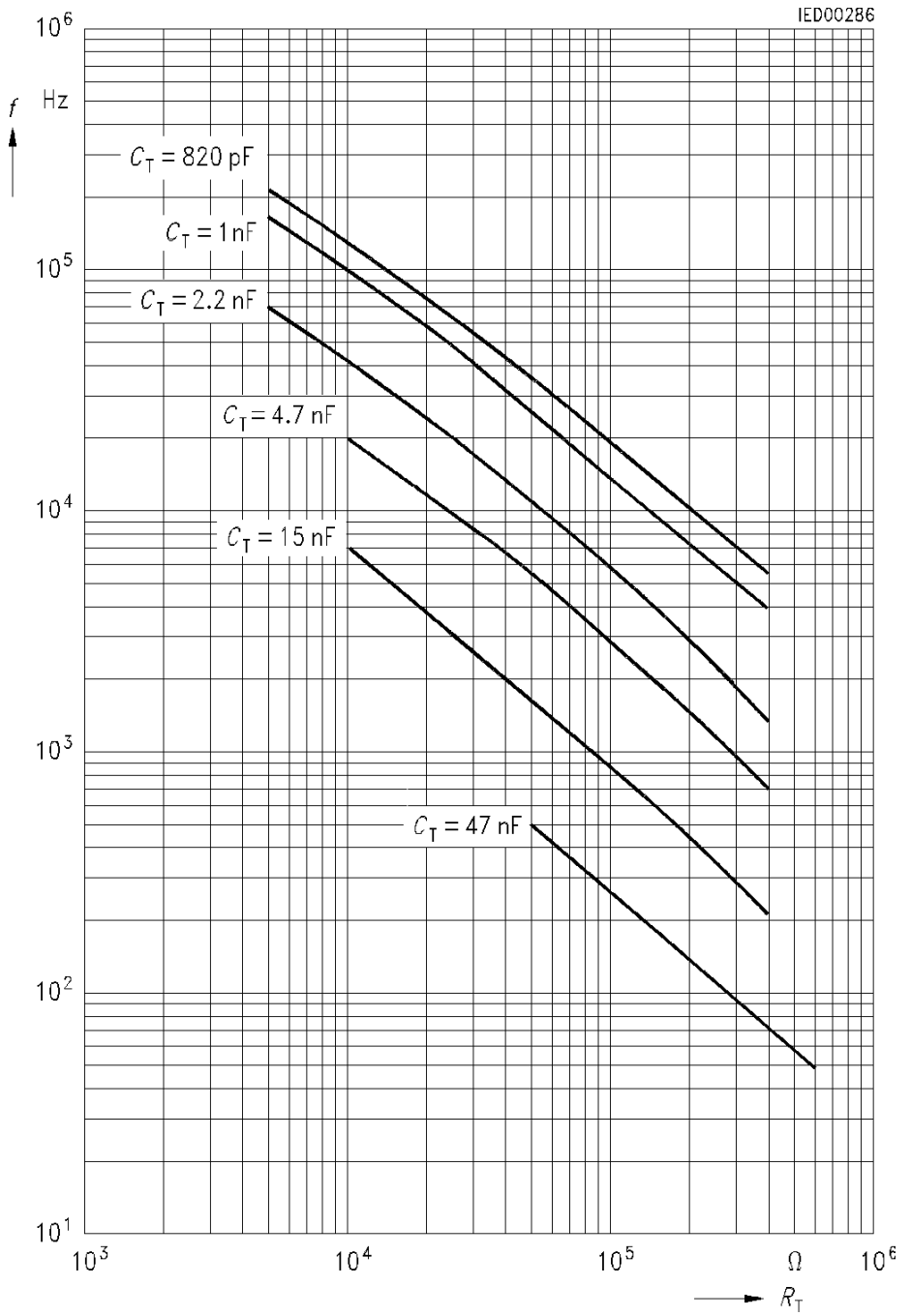
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favourable:	10 nF	1µF



Pulse Diagram

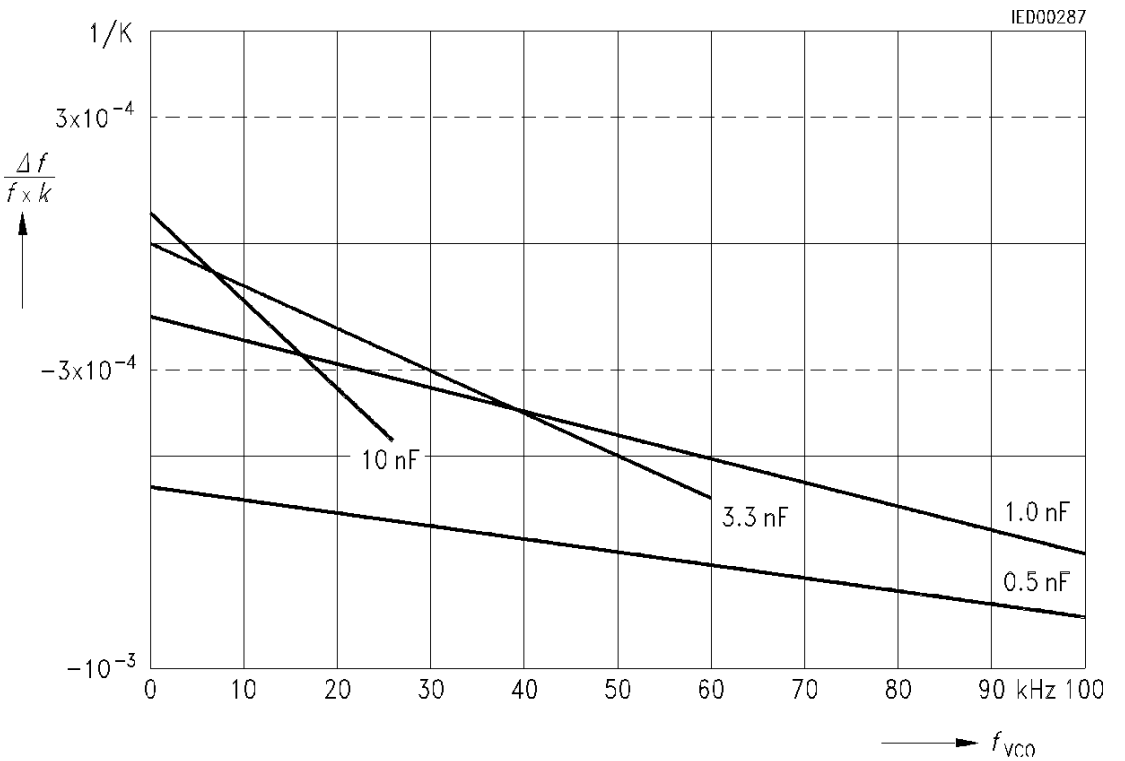
VCO Frequency versus R_T and C_T



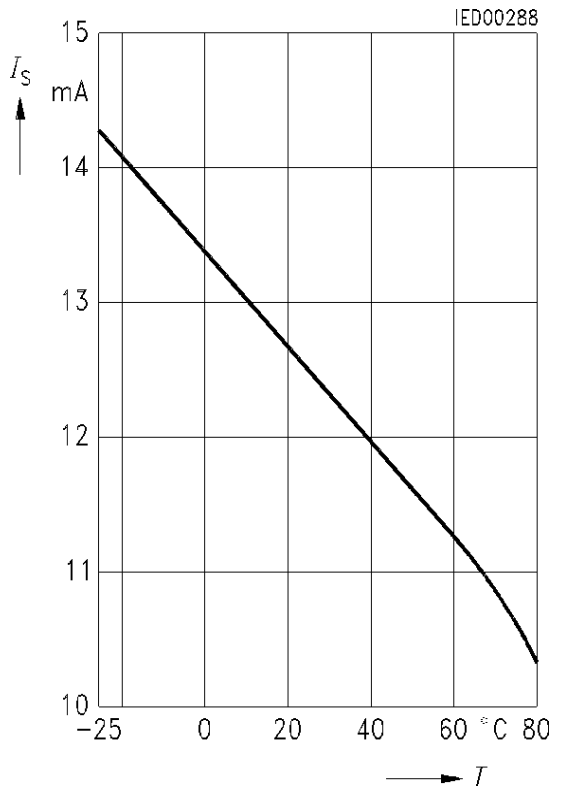
VCO Temperature Response

V_S = 12 V; D = max.

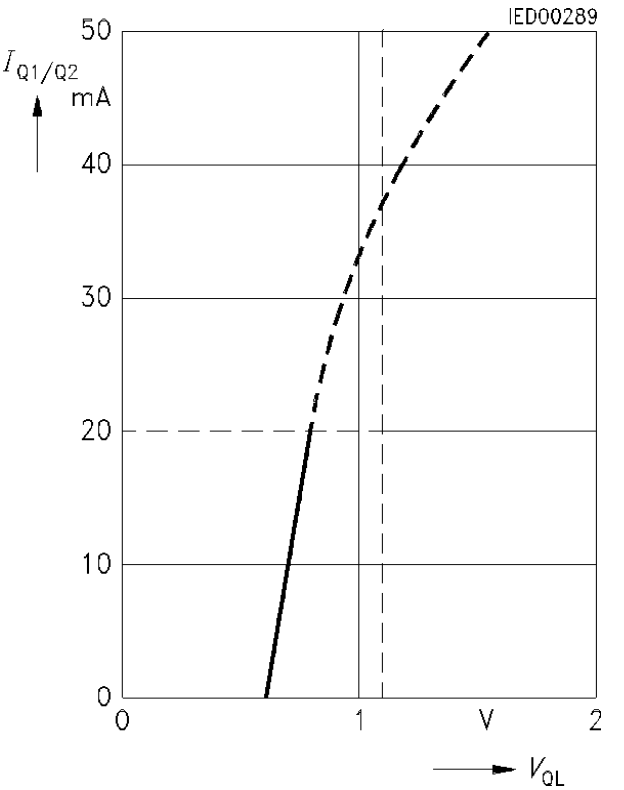
$\frac{\Delta f_{VCO}}{f_K \times K}[1/K]$ with C_T as parameter



Current Consumption versus Temperature



Output Current versus Output Voltage



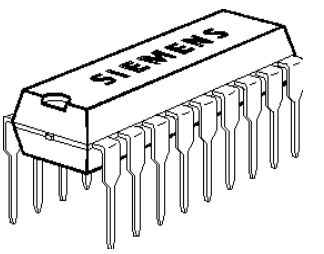
SIEMENS

Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies (SMPS)

TDA 4718 A

Features

- Feed-forward control (line hum suppression)
- Push-pull outputs
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression

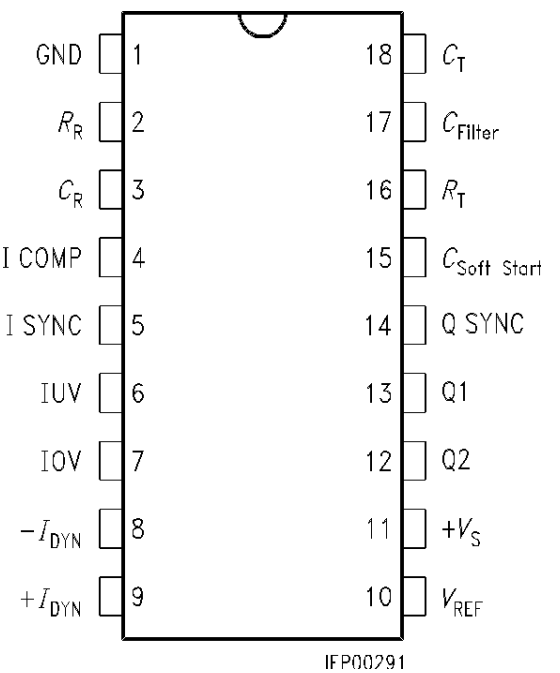


P-DIP-18-1

Type	Ordering Code	Package	Temp.-Range
TDA 4718 A	Q67000-Y639	P-DIP-18-1	– 25 to 85 °C

These versatile SMPS control ICs comprise digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers, which activate protective functions.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground 0 V
2 3	R_R C_R	Ramp generator R_R Ramp generator C_R
4 5	I COMP I SYNC	+ Input comparator K2 Sync. input
6 7	IUV IOV	Input undervoltage, ON/OFF Input overvoltage
8 9	$-I_{DYN}$ $+I_{DYN}$	Input dynamic current limitation (–) Input dynamic current limitation (+)
10 11	$+V_{REF}$ $+V_S$	Reference voltage Supply voltage
12 13	Q 2 Q 1	Output Q2 Output Q1
14 15	Q SYNC $C_{soft\ start}$	Sync. output Soft start
16 17 18	R_T C_{filter} C_T	VCO R_T Capacitance VCO C_T

Circuit Description

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a DC voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called “feed-forward control”, is utilized to compensate for known interference such as ripple on the input voltage.

Phase Comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. The component can be frequency-synchronized, but not phase-synchronized, with the sync input. The duty cycle of the squarewave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active outputs is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse-Turn-OFF Flipflop

The pulse turn-OFF flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2) to a maximum of + 5 V. The voltage at the ramp generator output may, however rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{\text{R}}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, cause the component to switch on again by the soft start.

Comparator K5, K6, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

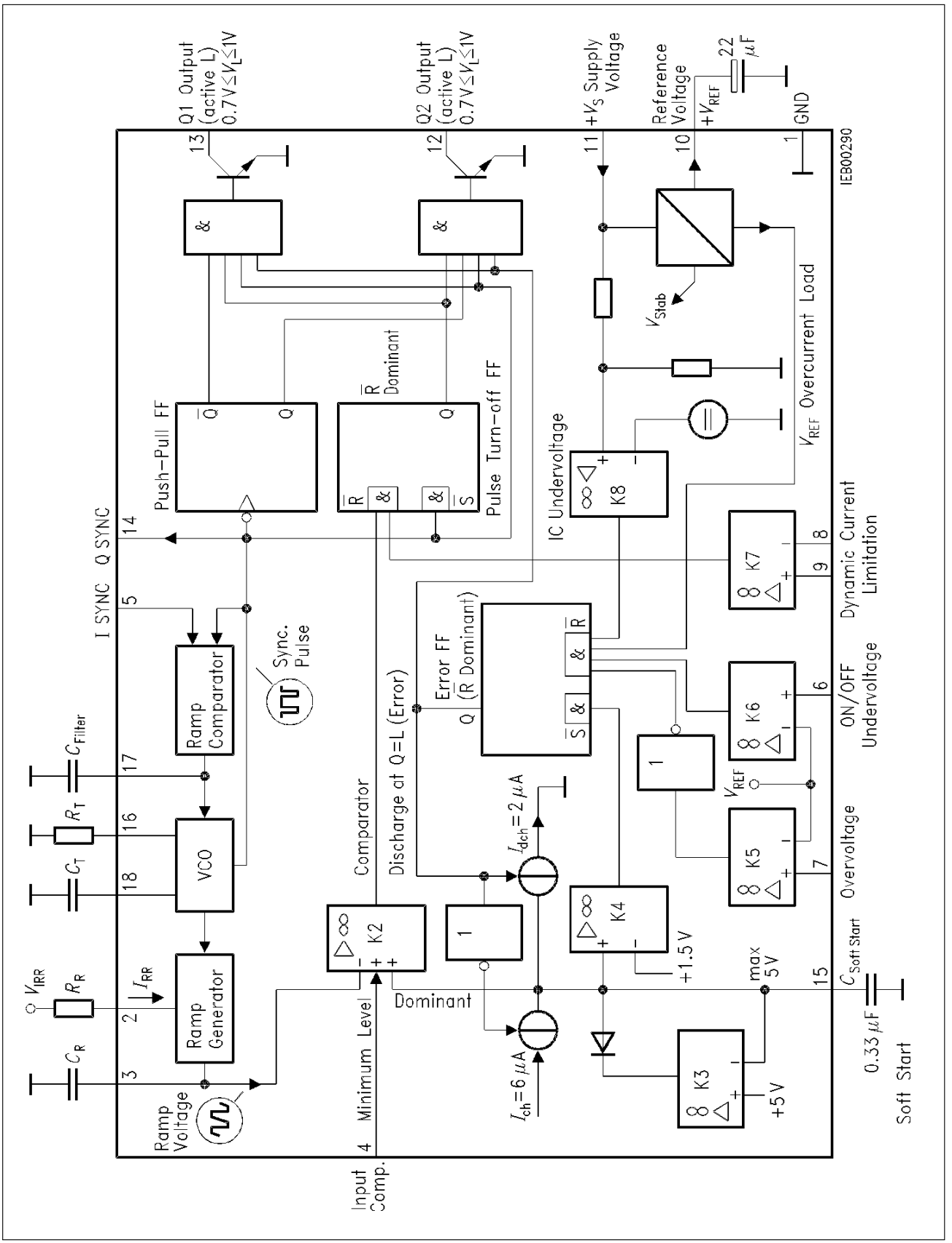
K7 has a common-mode range covers 0 V and + 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	– 0.3	33	V	
Voltage at Q1, Q2	V_Q	– 0.3	33	V	Q1, Q2 high
Current at Q1, Q2	I_Q		70	mA	Q1, Q2 low
Sync output	$V_{SYNC\ Q}$	– 0.3	7	V	SYNC Q high
	$I_{SYNC\ Q}$	0	10	mA	SYNC Q low
Sync input	$V_{SYNC\ I}$	– 0.3	33	V	
Input C_{filter}	$V_{I\ Cf}$	– 0.3	7	V	
Input R_T	$V_{I\ RT}$	– 0.3	7	V	
Input C_T	$V_{I\ CT}$	– 0.3	7	V	
Input R_R	$V_{I\ RR}$	– 0.3	7	V	
Input C_R	$I_{I\ CR}$	– 10	10	mA	
Input comparator K2, K5, K6, K7	$V_{I\ K}$	– 0.3	33	V	
Output K5	$V_{Q\ K5}$	– 0.3	33	V	
Reference voltage	V_{REF}	– 0.3	V_{REF}	V	
Input $C_{soft\ start}$	$V_{I\ soft\ start}$	– 0.3	7	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Thermal resistance system-air	$R_{th\ SA}$		60	K/W	

Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	10.5	30	V	
Ambient temperature	T_A	– 25	85	°C	
VCO frequency Ramp generator frequency	f f_{RG}	40 40	250 000 250 000	Hz Hz	

Characteristics

V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_S	8		20	mA	C_T = 1 nF f_{VCO} = 100 kHz
Reference						
Reference voltage	V_{REF}	2.35	2.5	2.65	V	$0\,mA < I_{REF} < 5\,mA$
Reference voltage change	ΔV_{REF}		8		mV	14 V ± 20 %
Reference voltage change	ΔV_{REF}		15		mV	25 V ± 20 %
Reference voltage change	ΔV_{REF}			15	mV	$0\,mA < I_{REF} < 5\,mA$
Temperature coefficient	TC		0.25	0.4	mV/K	
Response threshold of I_{REF} overcurrent	I_{REF}		10		mA	

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator (VCO)						
Frequency range	f_{VCO}	40		100 000	Hz	
Frequency change	$\Delta f/f_{VCO}$		0.5		%	14 V ± 20 %
Frequency change	$\Delta f/f_{VCO}$	– 1		1	%	25 V ± 20 %
Tolerance	$\Delta f/f_{VCO}$	– 7		7	%	ΔR_T = 0; ΔC_T = 0
Fall time sawtooth	t		1		µs	C_T = 1 nF
	t		10		µs	C_T = 10 nF
RC combination	C_T	0.82		47	nF	
VCO	R_T	5		700	kΩ	
Ramp Generator						
Frequency range	f	40		100 000	Hz	
Maximum voltage at C_R	V_H		5.5		V	
Minimum voltage at C_R	V_L		1.8		V	
Input current through R_R	I_{RR}	0		400	µA	
Current transformation ratio	I_{RR}/I_{CR}		1/4			
Synchronization						
Sync output	$V_{Q\,H}$	4			V	$I_{Q\,H}$ = – 200 µA
	$V_{Q\,L}$			0.4	V	$I_{Q\,L}$ = 1.6 mA
Sync input	$V_{I\,H}$	2			V	
	$V_{I\,L}$			0.8	V	
Input current	$-I_I$			5	µA	

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Comparator K2						
Input current	$-I_{I\,K2}$			2	µA	
Turn-OFF delay [1]	$t_{D\,OFF}$			500	ns	
Input voltage	$V_{I\,K2}$					for duty cycle
			1.8		V	D = 0
			5		V	D = max.
Common-mode input voltage range	$V_{I\,C}$	0		5.5	V	
Soft Start K3, K4						
Charge current for $C_{soft\ start}$	I_{ch}		6		µA	
Discharge current for $C_{soft\ start}$	I_{dch}		2		µA	
Upper limiting voltage	V_{lim}		5		V	
Switching voltage K4	V_{K4}		1.5		V	
Output Stages Q1, Q2						
Output voltage	$V_{Q\,H}$			30	V	
	$V_{Q\,L}$			1.1	V	I_Q = 20 mA
Output leakage current	I_Q			2	µA	$V_{Q\,H}$ = 30 V
ON, OFF, Undervoltage K6						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Turn-OFF delay time [2]	$t_{D\,OFF}$		250		ns	
Error detection time [2]	t		50		ns	

[1] At the input: step function ΔV = – 100 mV ⌟→ ΔV = + 100 mV
[2] At the input: step function $\Delta V = V_{REF}$ – 100 mV ⌟→ V_{REF} + 100 mV

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic Current Limitation K7						
Common-mode input voltage range	V_{IC}	0		4	V	
Input offset voltage	V_{IO}	– 10		10	mV	
Input current	$-I_I$			2	µA	
Turn-OFF delay time [1]	$t_{D\ OFF}$		250		ns	
Error detection time [1]	t		50		ns	
Overvoltage K5						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Output current	$-I_Q$	0		200	µA	$V_{QH\ min}$ = 5 V
Turn-OFF delay time [2]	$t_{D\ OFF}$		250		ns	
Error detection time [2]	t		50		ns	
Supply Undervoltage						
Turn-ON threshold for V_S rising	V_S	8.8		11	V	
Turn-OFF threshold for V_S falling	V_S	8.5		10.5	V	
Input C_{filter}						
Rated voltage for rated frequency	V_R		4		V	
Frequency approx. proportional to voltage within the range	V_R	3		5	V	
Voltage at open sync input	$V_{C\ filter}$		1.6		V	

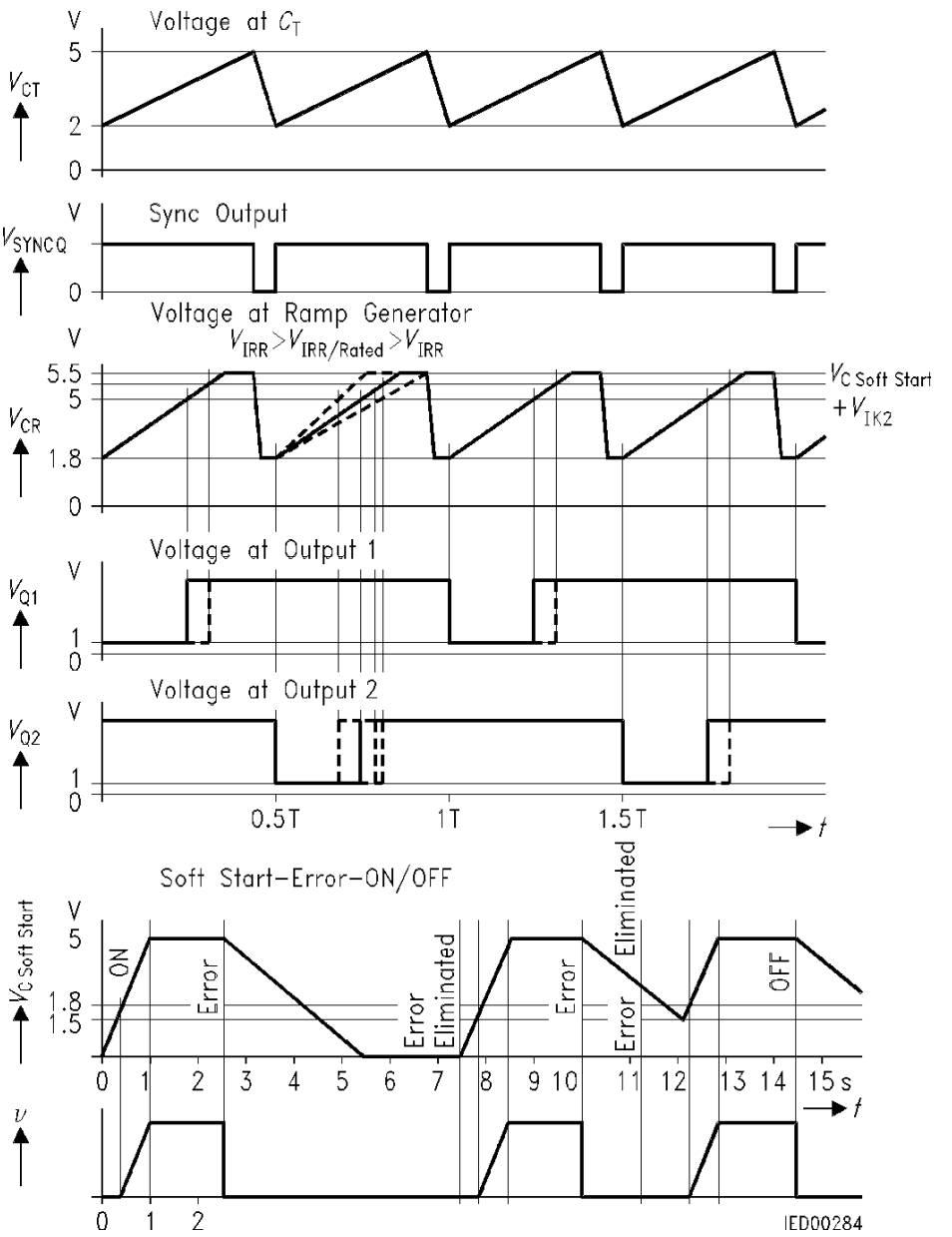
[1] At the input: step function ΔV = – 100 mV ⌐→ ΔV = + 100 mV
[2] At the input: step function $\Delta V = V_{REF}$ – 100 mV ⌐→ V_{REF} + 100 mV

Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\ start}$.
5. In the case of a free-running VCO: connect sync output with sync input.
6. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

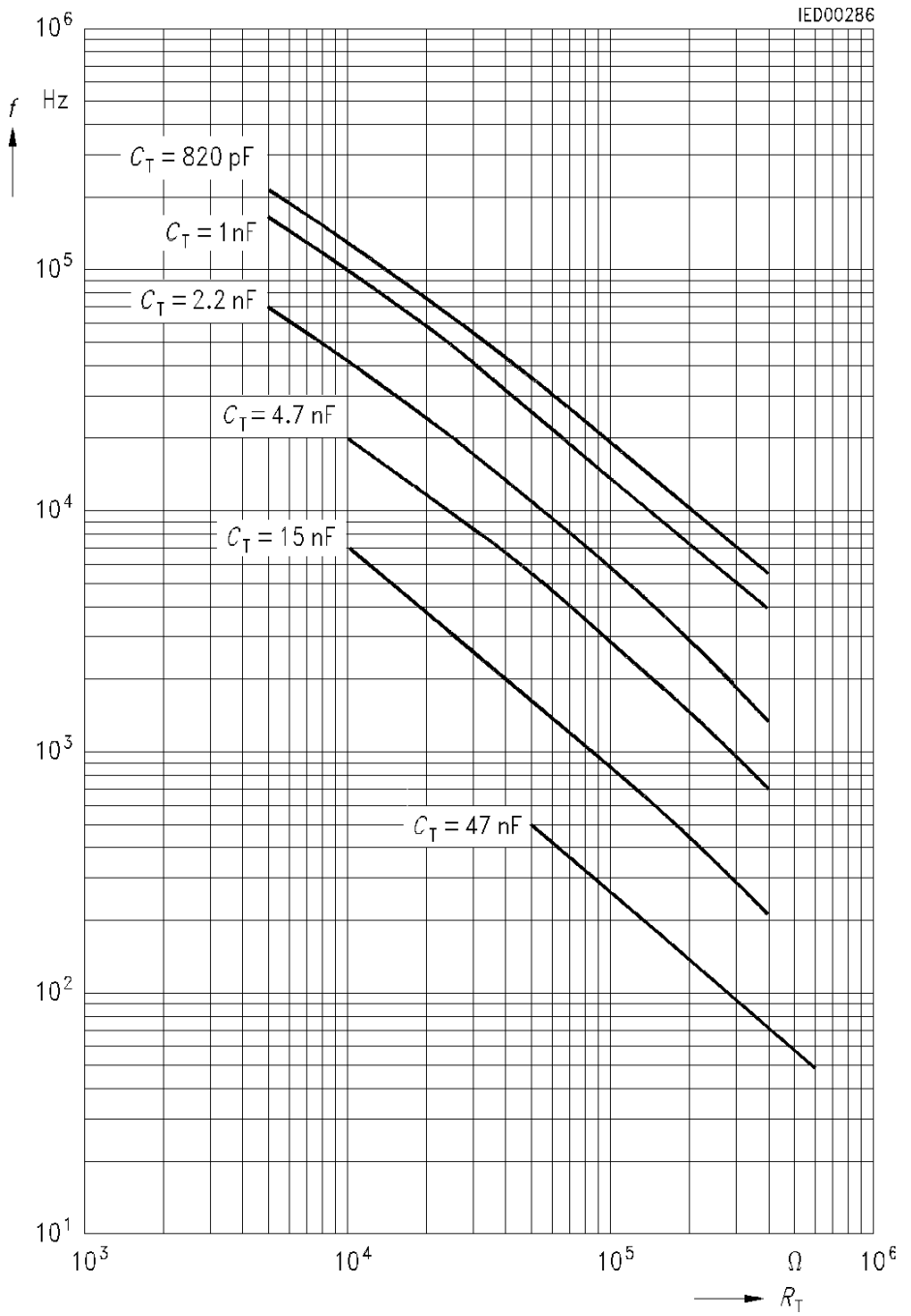
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favourable:	10 nF	1µF



Pulse Diagram

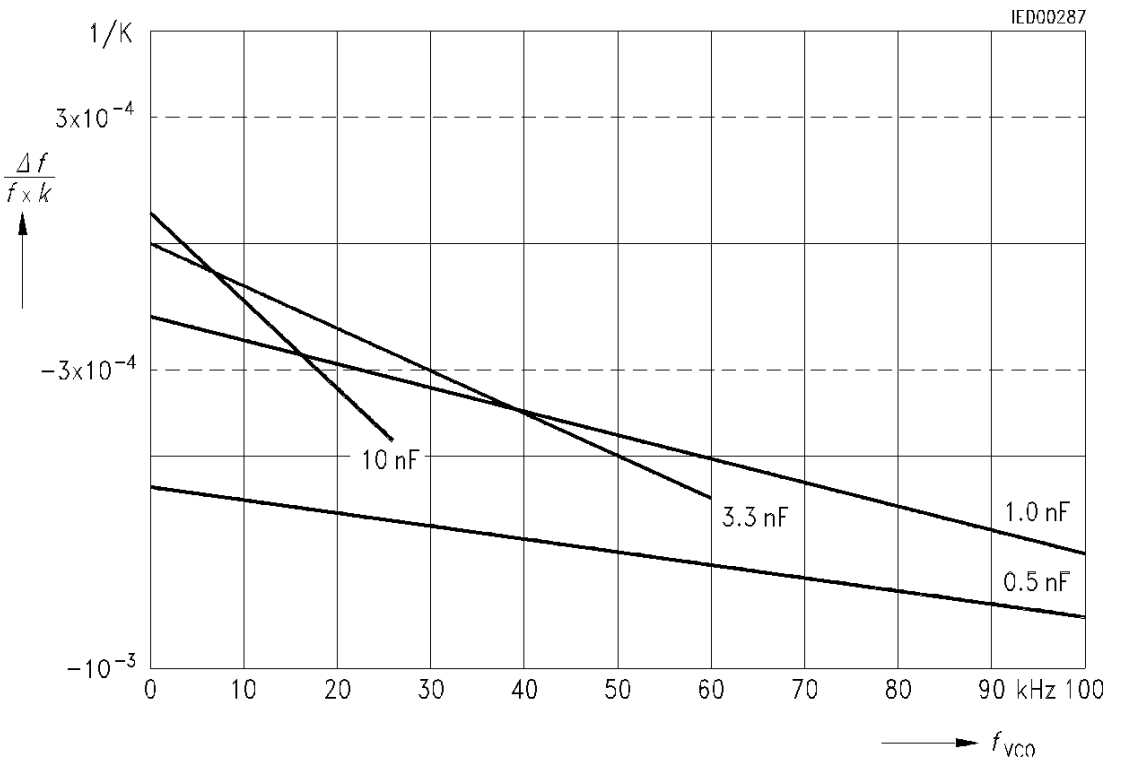
VCO Frequency versus R_T and C_T



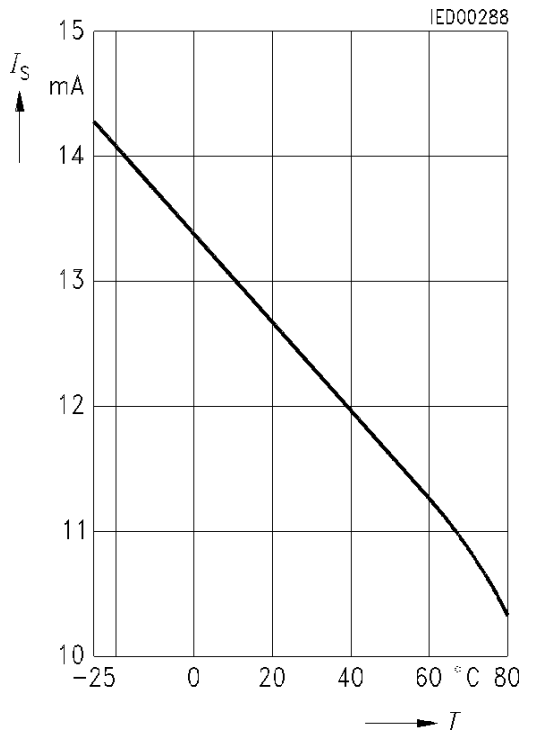
VCO Temperature Response

V_S = 12 V; D = max.

$\frac{\Delta f_{VCO}}{f_K \times K}[1/K]$ with C_T as parameter



Current Consumption versus Temperature



Output Current versus Output Voltage