REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

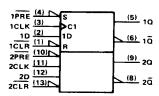
The SN54' family is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74' family is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE

	INPUT	s		OUT	PUTS
PRE	CLR	CLK	D	a	ā
L	Н	×	х	Н	L
Н	L	х	X	L	н
L	L	×	X	нt	H†
н	н	1	н	н	ᆫᆫ
н	н	1	L	L	н
н	Н	L	X	Q ₀	_ ರೄ

[†] The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

SN5474, SN54H74, SN54L74 . . . J PACKAGE SN54LS74A, SN54S74 . . . J OR W PACKAGE SN7474, SN74H74 . . . J OR N PACKAGE SN74LS74A, SN74S74 . . . D, J OR N PACKAGE (TOP VIEW)

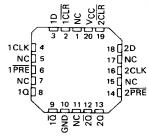
1CLR []	U14 VCC
1D 🗖 2	13 2 CLR
1CLK □3	12 2D
1PRE ☐4	11D2CLK
10 🛛 5	10 2 PRE
10 🗖 6	9 🕽 2 Q
GND ☐ 7	8 🗖 2 🔽

SN5474, SN54H74 . . . W PACKAGE (TOP VIEW)

SN54LS74A, SN54S74 . . . FK PACKAGE SN74LS74A, SN74S74 . . . FN PACKAGE (TOP VIEW)

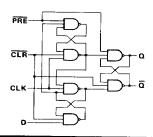
8 2PRE

2CLK 17



NC - No internal connection

logic diagram



PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



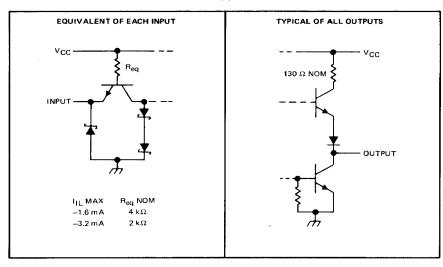
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3

TTL DEVICES

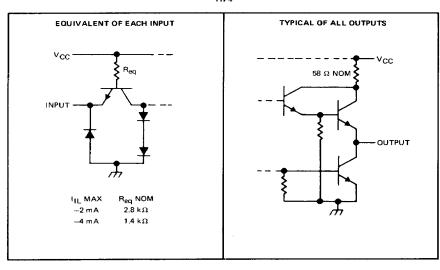
74



3

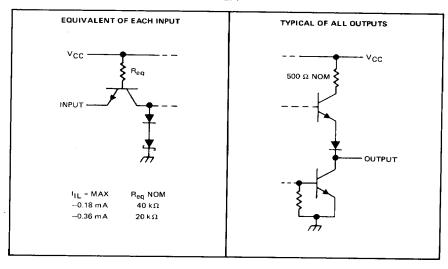
TTL DEVICES

Ή74

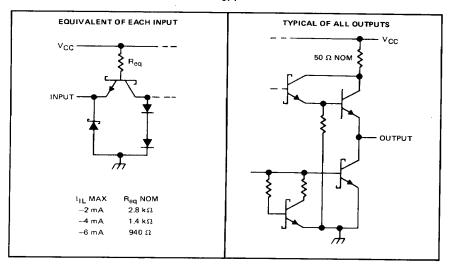




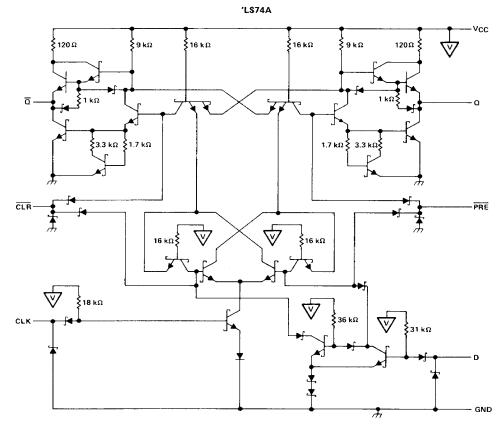
'L74



'\$74



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		7 V
Input voltage: '74, 'H74, 'L74, 'S74 .		5.5 V
′LS74A		7 V
	SN54'	
	SN74'	0°C to 70°C
Storage temperature range		- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



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TYPES \$N5474, \$N7474 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

				SN547	4		SN7474		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			v
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				- 0.4			0.4	mA
JOL	Low-level output current		1		16			16	mΑ
		CLK high	30			30			
tw	Pulse duration	CLK low	37			37			ns
		PRE or CLR low	30			30			i
t _{su}	Input setup time before CLK †		20			20			ns
th	Input hold time-data after CLK f		5			5			ns
TA	Operating free-air temperature		- 55		125	0		70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDITIONS†		SN5474		1	SN7474		
					TYP#	MAX	MIN	TYP‡	MAX	UNIT
v_{IK}		VCC = MIN,	I _‡ = - 12 mA			- 1.5	T		1.5	V
۷он		V _{CC} = MIN, I _{OH} = - 0.4 mA	V _{IH} = 2 V, V _{IL} = 0.	3 V, 2.4	3,4		2.4	3.4		ν
VOL		V _{CC} ≈ MIN, I _{OL} = 16 mA	V _{IH} = 2 V, V _{IL} = 0.	ЗV,	0.2	0.4		0.2	0.4	V
t _l		V _{CC} = MAX,	V _I = 5.5 V			1			1	mA
	D					40			40	
۱н	CLR	V _{CC} = MAX,	V. = 24 V			120			120	mA
	All Other	100	V 2,4 V			80			80	1
	D					- 1.6			1.6	
I _I L	PRE★	V _{CC} = MAX,	V ₁ = 0.4 V			- 1.6			- 1.6	١.
12	CLR★	1 .00	V ₁ 0 V			- 3.2			- 3.2	mA
	CLK					- 3.2			- 3.2	
los§		V _{CC} = MAX		- 20		- 57	- 18		- 57	mA
lcc		V _{CC} = MAX,	See Note 2		8.5	15		8.5	15	mA

- † For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
- ‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
- * Clear is tested with preset high and preset is tested with clear high,
- \S Not more than one output should be shorted at a time.
- NOTE 2: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
fmax					15	25		MHz
tPLH .	PRE or CLR	Q or $\overline{\mathbf{Q}}$					25	ns
^t PHL	THE OF CERT	2012	R _L = 400 Ω,	C _L = 15 pF			40	ns
[†] PLH	CLK	Q or $\overline{\overline{\mathbf{Q}}}$				14	25	ns
^t PHL	OLK	Q Or Q				20	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



recommended operating conditions

				SN54H	74		SN74H7	4	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	l v
v_{IH}	High-level input voltage		2			2			T v
VIL	Low-level input voltage			_	0.8	†		8.0	l v
Юн	High-level output current		1		- 1	t	•	- 1	mA
loL	Law-level autput current				20			20	mA
		CLK high	15			15			
tw	Pulse duration	CLK low	13.5			13.5			ns
		CLR or PRE low	25			25			1
t _{su}	Setup time-before CLK 1	High-level data	10			10			
•su	——————————————————————————————————————	Low-level data	15			15			ns
th	Hold time - data after CLK†		5			5	•		ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	1	EST CONDITIO	nne†		SN54H7	4		SN74H7	4	
		<u>.</u>	EST CONDITIO	JNG.	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
v_{IK}		VCC = MIN,	I _I = - 8 mA				- 1.5			- 1.5	V
νон		V _{CC} = MIN, I _{OH} = 1 mA		V _{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
VOL		V _{CC} = MIN, I _{OL} = 20 mA	V _{IH} = 2 V,	V _{IL} = 0.8 V,		0.2	0.4		0.2	0.4	v
11		V _{CC} = MAX,	V _I = 5.5 V			-	1			1	mA
	D					-	50			50	
ΙЩ	CLR	V _{CC} = MAX,	V = 2.4 V				150			150	μΑ
	PRE or CLK						100			100	
	D						- 2			- 2	Γ
L	CLR★	V _{CC} ≃ MAX,	V: = 0.4 V				4			-4	
ΙL	PRE★	ACC_ MICAY,	V - 0.4 V	,			– 2			-2	mA
	CLK			•			– 4			-4	
los §		V _{CC} = MAX			- 40		- 100	40		100	mA
1cc		V _{CC} = MAX,	See Note 2			15	21		15	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

* Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open, ICC is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST COND	ITIONS	MIN	ТУР	MAX	UNIT
f _{max}					35	43		MHz
^t PLH	PRE or CLR	Q or $\overline{\mathbf{Q}}$					20	ns
^t PHL	PREGICER	u or u	RL = 280 Ω,	C _L = 25 pF			30	ns
^t PLH	CLK	Q or <u>Q</u>				8.5	15	กร
tPHL .	02	4014				13	20	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
VIL	Low-level input voltage				0.7	 `
Іон	High-level output current				- 0.1	mA
loL	Low-level output current				2	mA
	Pulse duration	CLK high or low	200			
tw	ruse duration	CLR or PRE low	100			ns
t _{su}	Setup time before CLK f		50			ns
th	Hold time data after CLK †		15			ns
TA	Operating free-air temperature	1.	- 55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TES	ST CONDITIONS†		MIN	TYP‡	MAX	UNIT
Voн	-	V _{CC} = MIN,	V _{IH} = 2 V,	V _{IL} = 0.7 V,	I _{OH} = 0.1 mA	2.4	3.3		V
VOL		V _{CC} = MIN,	V _{IH} = 2 V,	V _{IL} = 0.7 V,	I _{OL} = 2 mA		0.15	0.3	v
	D						-	0.1	
1 1	CLR	V _{CC} = MAX,	$V_1 = 5.5 V$					0.3	mA
	PRE or CLK							0.2	ĺ
	D							10	
ΉН	CLR	V _{CC} = MAX,	V = 2.4 V					30	μΑ
	PRE or CLK							20	,,,,
	D or PRE					_		- 0.18	
IIL	CLR or CLK	V _{CC} = MAX,	V _I = 0.3 V			_		- 0.36	μΑ
los		V _{CC} = MAX				-3		- 15	mA
Icc		V _{CC} = MAX,	See Note 2			+	0.8	1.5	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. ‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ} \text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
fmax					2.5	3		MHz
tPLH .	PRE or CLR	Q or Ω			**	50	75	ns
	PRE or CLR (CLK high)	Q or Q	D - 416			80	150	
^t PHL	PRE or CLR (CLK low)	u or u	$R_L = 4 k\Omega$,	C _L = 50 pF		80	150	ns
tPLH	Clock	Q or Q			15	65	100	ns
tPHL	CIOCK	4874			15	65	150	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



NOTE 2: With all outputs open, ICC is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is

TYPES SN54LS74A, SN74LS74A DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			St	V54LS7	4A		SN74LS	74A	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current		1		- 0.4			- 0.4	mA
^I OL	Low-level output current				4	· · · · · ·		8	mA
fclock	Clock frequency		0		25	0		25	MHz
		CLK high	25			25			******
tw	Pulse duration	PRE or CLR low	25			25			ns
	Satura time before Class	High-level data	20			20			
t _{su}	Setup time-before CLK↑	Low-level data	20			20		25	ns
th	Hold time-data after CLK↑		5			5			ns
TA	Operating free-air temperature		- 55	•	125	0		70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CONDITIONS†		SN54LS74A			SN74LS74A				
	Anameren	153	T COMBITTONS		MIN	TYP#	MAX	MIN TYP# MAX		UNIT	
v_{iK}		V _{CC} = MIN,	lj = 18 mA				- 1.5			- 1.5	V
V _{OH}		V _{CC} = MIN, I _{DH} = - 0.4 mA	V _{IH} = 2 V,	V _{IL} = MAX,	2.5	3.4		2.7	3.4		V
VOL		V _{CC} = MIN, I _{OL} = 4 mA	VIL = MAX,	V _{IH} = 2 V,		0.25	0.4		0.25	0.4	V
VOL		V _{CC} = MIN, I _{OL} = 8 mA	VIL = MAX,	V _{IH} = 2 V,					0.35	0.5	
4	D or CLK	V _{CC} = MAX,	V ₁ = 7 V		1		0.1			0.1	
'1	CLR or PRE	ACC - MYY	V - / V				0.2	i		0.2	mA
Ιн	D or CLK	V _{CC} = MAX,	V ₁ = 2.7 V				20	<u> </u>		20	
'IH	CLR or PRE	ACC - MUYY	V - 2.7 V				40		•	40	μA
1	D or CLK	V _{CC} = MAX,	V ₁ = 0.4 V			-	- 0.4			- 0.4	
ΊL	CLR or PRE	ACC - MAY	V - 0.4 V			-	- 0.8		,	- 0.8	mA
los§		V _{CC} = MAX,	See Note 4		- 20		- 100	20		- 100	mA
Icc		V _{CC} = MAX,	See Note 2		1	4	8		4	8	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ} \text{C}$.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_Q = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, VCC = 5 V, TA = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CO	TEST CONDITIONS				UNIT
f _{max}					25	33		MHz
tPLH .	CLR, PRE or CLK	Q or Q	$R_L = 2 k\Omega$,	C _L = 15 pF		13	25	ns
tPHL	3211,1 112 ST 3211	40.4				25	40	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

				SN54S7	4	:	SN74S7	4	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	יואטן
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH		and the same of th	2			2			V
VIL					8.0			0.8	V
IOH	High-level output current				1			- 1	mA
IOL	Low-level output current				20			20	mA
	High-level input voltage Low-level input voltage High-level output current Low-level output current Pulse duration Setup time, before CLK † Input hold time - data after CLK †	CLK high	6			6			1
tw		CLK low	7.3			7.3			ns
-00		CLR or PRE low	7			7			<u> </u>
		High-level data	3			3			ns
tsu	Setup time, before CLK 1	Low-level data	3			3			1
t _h	Input hold time - data after CLK ↑		2			2			ns
TA	Operating free-air temperature		_ 55		125	0		70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	T					SN54S7	4	:	SN74S7	4	UNIT
PAR	AMETER		TEST CONDITIO	NS T	MIN	TYP‡	MAX	MIN	түр‡	MAX	UNIT
VIK		V _{CC} = MIN,	I ₁ = - 18 mA,				- 1.2			- 1.2	V
Voн		V _{CC} = MIN,	V _{IH} = 2 V,	V _{IL} = 0.8 V,	2.5	3.4		2.7	3.4		٧
VOL		V _{CC} = MIN, I _{OL} = 20 mA	V _{IH} = 2 V,	V _{IL} = 0.8 V,			0.5			0.5	٧
T _L		V _{CC} = MAX	V ₁ = 5.5 V				1			1	mA
	T D						50			50]
чн	CLR	$V_{CC} = MAX$,	V ₁ = 2.7 V				150			150	mA
'IH	PRE or CLK		·				100			0.5 1 50	
	D						– 2			– 2]
	CLR★						- 6			- 6	Ι.
l _{IL}	PRE*	V _{CC} = MAX,	V ₁ = 0.5 V				- 4			- 4	mA
	CLK						4	1		4	<u> </u>
1os§	1 02	VCC = MAX			- 40		100	- 40		- 100	mA
Icc		V _{CC} = MAX,	See Note 2			15	25		15	25	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 \ddagger All typical values are at V_{CC} = 5 V, T_{A} = $25^{\circ}C.$

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	мах	UNIT
fmax					75	110		MHz
tPLH	PRE or CLR	Qorā				4	6	ns
	PRE or CLR (CLK high)	ā or a	$R_1 = 280 \Omega_1$	C ₁ = 15 pF		9	13.5	ns
^t PHL	PRE or CLR (CLK low)		11[- 200 32,			5	8	
t _{PLH}						6	9	ns
tPHL	CLK	Q or Q				6	9	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.



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[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

 $[\]alpha$ Clear is tested with preset high and preset is tested with clear high.

NOTE 2: All outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is