

# NE5517, NE5517A, AU5517

## Dual Operational Transconductance Amplifier

The AU5517 and NE5517 contain two current-controlled transconductance amplifiers, each with a differential input and push-pull output. The AU5517/NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal-to-noise improvement referenced to 0.5% THD. The AU5517/NE5517 is suited for a wide variety of industrial and consumer applications.

Constant impedance of the buffers on the chip allow general use of the AU5517/NE5517. These buffers are made of Darlington transistors and a biasing network that virtually eliminate the change of offset voltage due to a burst in the bias current  $I_{ABC}$ , hence eliminating the audible noise that could otherwise be heard in high quality audio applications.

### Features

- Constant Impedance Buffers
- $\Delta V_{BE}$  of Buffer is Constant with Amplifier  $I_{BIAS}$  Change
- Excellent Matching Between Amplifiers
- Linearizing Diodes
- High Output Signal-to-Noise Ratio

### Applications

- Multiplexers
- Timers
- Electronic Music Synthesizers
- Dolby™ HX Systems
- Current-controlled Amplifiers, Filters
- Current-controlled Oscillators, Impedances

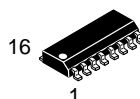


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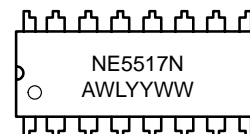
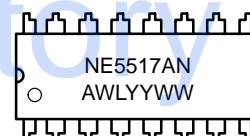
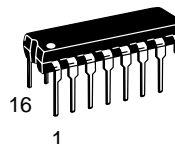
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### MARKING DIAGRAMS

SOIC-16  
D SUFFIX  
CASE 751B



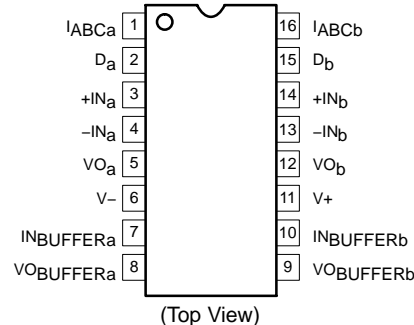
PDIP-16  
N SUFFIX  
CASE 648



A = Assembly Location  
WL = Wafer Lot  
YY, Y = Year  
WW = Work Week

### PIN CONNECTIONS

#### N, D Packages



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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## PIN DESCRIPTION

Pin No.	Symbol	Description
1	$I_{ABCa}$	Amplifier Bias Input A
2	$D_a$	Diode Bias A
3	$+IN_a$	Non-inverted Input A
4	$-IN_a$	Inverted Input A
5	$VO_a$	Output A
6	$V-$	Negative Supply
7	$IN_{BUFFERa}$	Buffer Input A
8	$VO_{BUFFERa}$	Buffer Output A
9	$VO_{BUFFERb}$	Buffer Output B
10	$IN_{BUFFERb}$	Buffer Input B
11	$V+$	Positive Supply
12	$VO_b$	Output B
13	$-IN_b$	Inverted Input B
14	$+IN_b$	Non-inverted Input B
15	$D_b$	Diode Bias B
16	$I_{ABCb}$	Amplifier Bias Input B

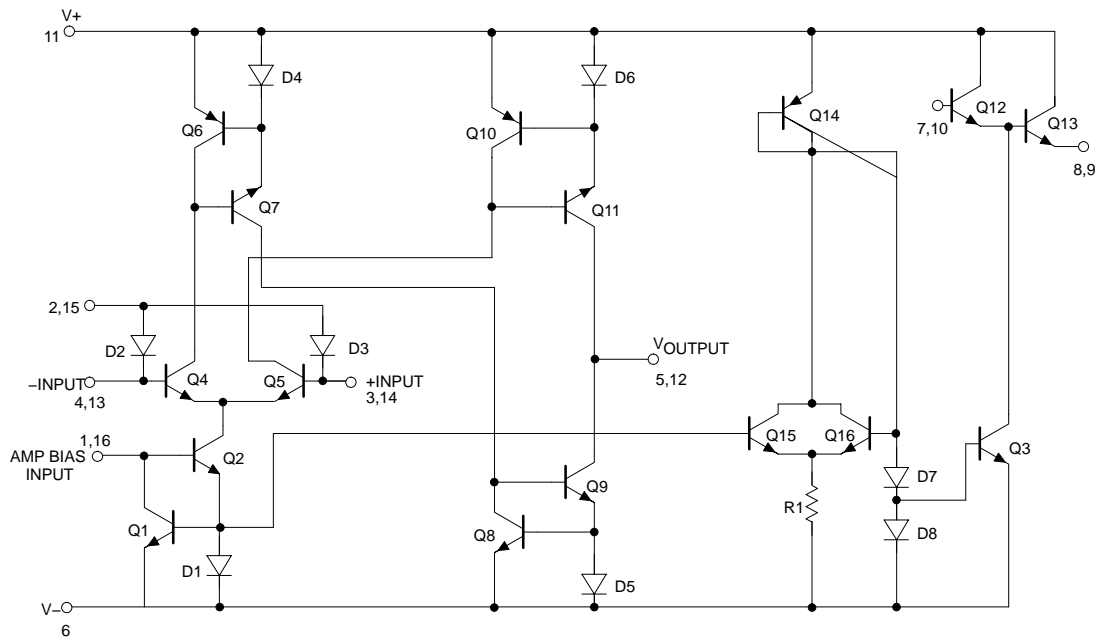
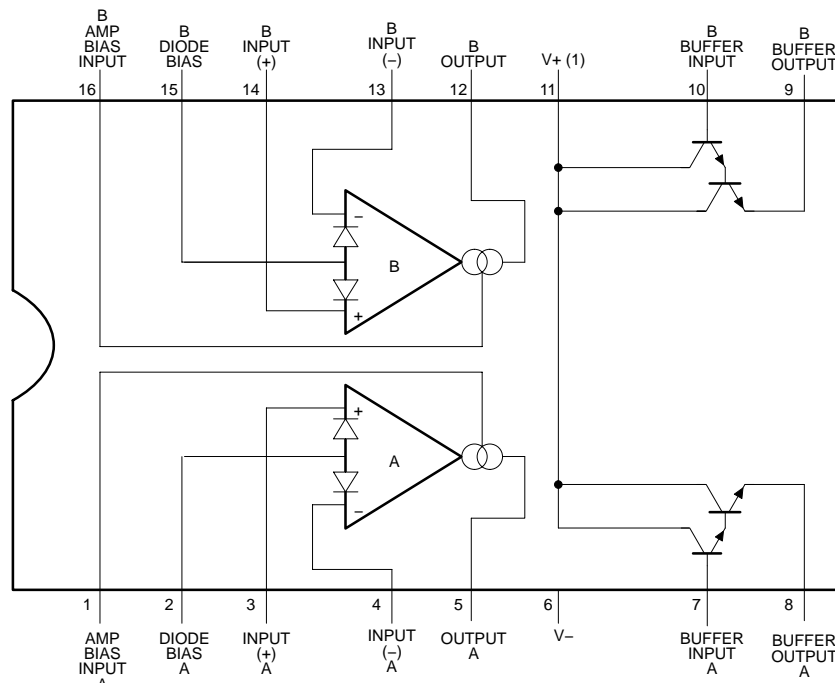


Figure 1. Circuit Schematic

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NOTE: V+ of output buffers and amplifiers are internally connected.

**Figure 2. Connection Diagram**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	$V_S$	44 $V_{DC}$ or $\pm 22$	V
Power Dissipation, $T_{amb} = 25^\circ C$ (Still Air) (Note 2) NE5517N, NE5517AN NE5517D, AU5517D	$P_D$	1500 1125	mW
Thermal Resistance, Junction-to-Ambient D Package N Package	$R_{\theta JA}$	140 94	$^\circ C/W$
Differential Input Voltage	$V_{IN}$	$\pm 5.0$	V
Diode Bias Current	$I_D$	2.0	mA
Amplifier Bias Current	$I_{ABC}$	2.0	mA
Output Short-Circuit Duration	$I_{SC}$	Indefinite	
Buffer Output Current (Note 3)	$I_{OUT}$	20	mA
Operating Temperature Range NE5517N, NE5517AN AU5517T	$T_{amb}$	$0^\circ C$ to $+70^\circ C$ $-40^\circ C$ to $+125^\circ C$	$^\circ C$
Operating Junction Temperature	$T_J$	150	$^\circ C$
DC Input Voltage	$V_{DC}$	$+V_S$ to $-V_S$	
Storage Temperature Range	$T_{stg}$	$-65^\circ C$ to $+150^\circ C$	$^\circ C$
Lead Soldering Temperature (10 sec max)	$T_{slid}$	230	$^\circ C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- For selections to a supply voltage above  $\pm 22$  V, contact factory.
- The following derating factors should be applied above  $25^\circ C$   
N package at  $10.6 \text{ mW}/^\circ C$   
D package at  $7.1 \text{ mW}/^\circ C$ .
- Buffer output current should be limited so as to not exceed package dissipation.

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## DC ELECTRICAL CHARACTERISTICS (Note 4)

Characteristic	Symbol	Test Conditions	AU5517/NE5517			NE5517A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$	Overtemperature Range $I_{ABC} = 500 \mu A$		0.4 0.3	5.0 5.0		0.4 0.3	2.0 5.0 2.0	mV
$\Delta V_{OS}/\Delta T$		Avg. TC of Input Offset Voltage		7.0			7.0		$\mu V/^{\circ}C$
$V_{OS}$ Including Diodes		Diode Bias Current ( $I_D$ ) = 500 $\mu A$		0.5	5		0.5	2.0	mV
Input Offset Change	$V_{OS}$	$5.0 \mu A \leq I_{ABC} \leq 500 \mu A$		0.1			0.1	3.0	mV
Input Offset Current	$I_{OS}$			0.1	0.6		0.1	0.6	$\mu A$
$\Delta I_{OS}/\Delta T$		Avg. TC of Input Offset Current		0.001			0.001		$\mu A/^{\circ}C$
Input Bias Current	$I_{BIAS}$	Overtemperature Range		0.4 1.0	5.0 8.0		0.4 1.0	5.0 7.0	$\mu A$
$\Delta I_B/\Delta T$		Avg. TC of Input Current		0.01			0.01		$\mu A/^{\circ}C$
Forward Transconductance	$g_M$	Overtemperature Range	6700 5400	9600	1300	7700 4000	9600	1200	$\mu mho$
$g_M$ Tracking				0.3			0.3		dB
Peak Output Current	$I_{OUT}$	$R_L = 0, I_{ABC} = 5.0 \mu A$ $R_L = 0, I_{ABC} = 500 \mu A$ $R_L = 0$	350 300	5.0 500	650	3.0 350 300	5.0 500	7.0 650	$\mu A$
Peak Output Voltage Positive Negative	$V_{OUT}$	$R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$ $R_L = \infty, 5.0 \mu A \leq I_{ABC} \leq 500 \mu A$	+12 -12	+14.2 -14.4		+12 -12	+14.2 -14.4		V
Supply Current	$I_{CC}$	$I_{ABC} = 500 \mu A$ , both channels		2.6	4.0		2.6	4.0	mA
$V_{OS}$ Sensitivity Positive Negative		$\Delta V_{OS}/\Delta V_+$ $\Delta V_{OS}/\Delta V_-$		20 20	150 150		20 20	150 150	$\mu V/V$
Common-mode Rejection Ration	CMRR		80	110		80	110		dB
Common-mode Range			$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$		V
Crosstalk		Referred to Input (Note 5) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	$I_{IN}$	$I_{ABC} = 0$ , Input = $\pm 4.0$ V		0.02	100		0.02	10	nA
Leakage Current		$I_{ABC} = 0$ (Refer to Test Circuit)		0.2	100		0.2	5.0	nA
Input Resistance	$R_{IN}$		10	26		10	26		k $\Omega$
Open-loop Bandwidth	$B_W$			2.0			2.0		MHz
Slew Rate	SR	Unity Gain Compensated		50			50		V/ $\mu s$
Buffer Input Current	$I_{BUFFER}$	5		0.4	5.0		0.4	5.0	$\mu A$
Peak Buffer Output Voltage	$V_{O_{BUFFER}}$	5	10			10			V
$\Delta V_{BE}$ of Buffer		Refer to Buffer $V_{BE}$ Test Circuit (Note 6)		0.5	5.0		0.5	5.0	mV

- These specifications apply for  $V_S = \pm 15$  V,  $T_{amb} = 25^{\circ}C$ , amplifier bias current ( $I_{ABC}$ ) = 500  $\mu A$ , Pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
- These specifications apply for  $V_S = \pm 15$  V,  $I_{ABC} = 500 \mu A$ ,  $R_{OUT} = 5.0$  k $\Omega$  connected from the buffer output to  $-V_S$  and the input of the buffer is connected to the transconductance amplifier output.
- $V_S = \pm 15$ ,  $R_{OUT} = 5.0$  k $\Omega$  connected from Buffer output to  $-V_S$  and  $5.0 \mu A \leq I_{ABC} \leq 500 \mu A$ .

TYPICAL PERFORMANCE CHARACTERISTICS

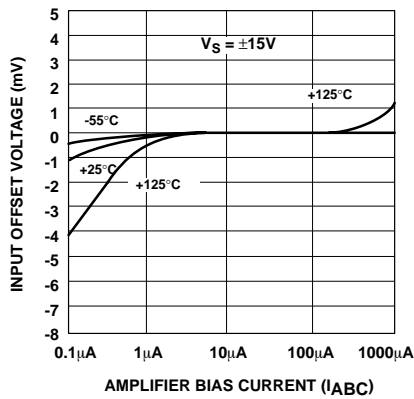


Figure 3. Input Offset Voltage

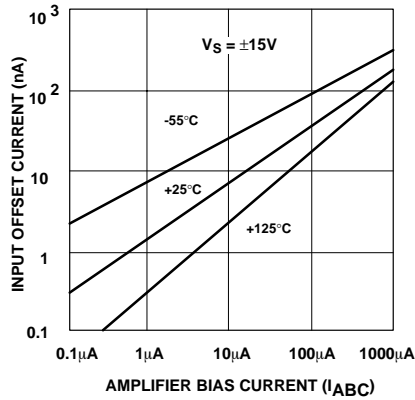


Figure 4. Input Bias Current

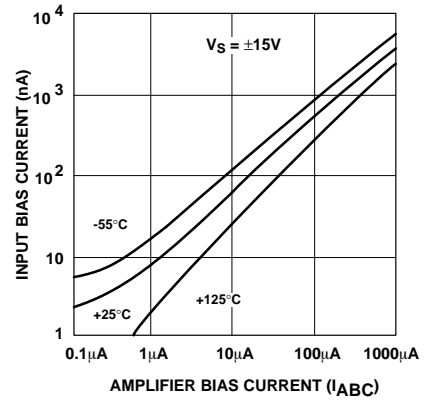


Figure 5. Input Bias Current

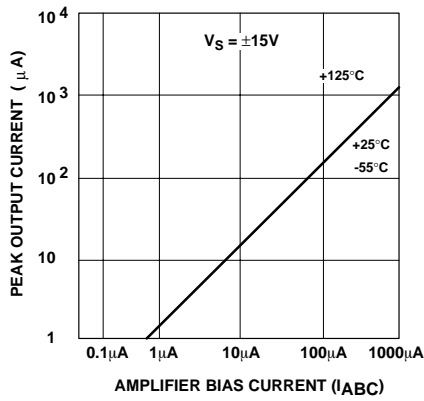


Figure 6. Peak Output Current

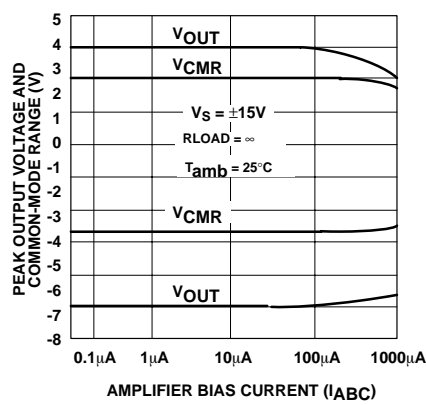


Figure 7. Peak Output Voltage and Common-Mode Range

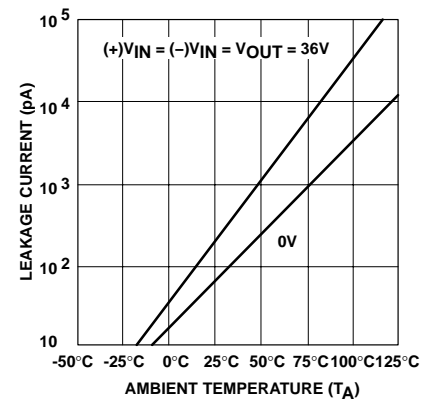


Figure 8. Leakage Current

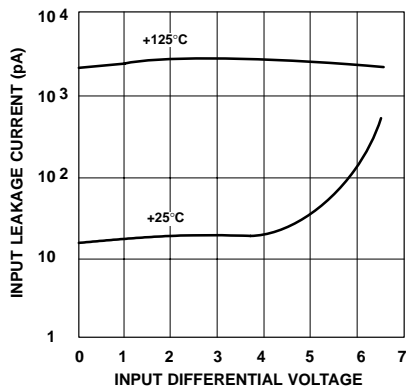


Figure 9. Input Leakage

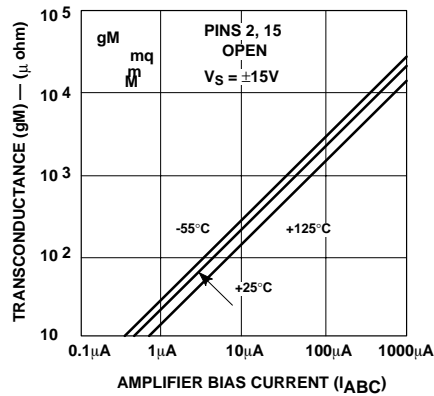


Figure 10. Transconductance

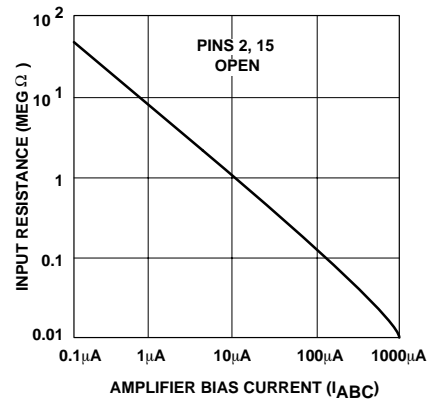


Figure 11. Input Resistance

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

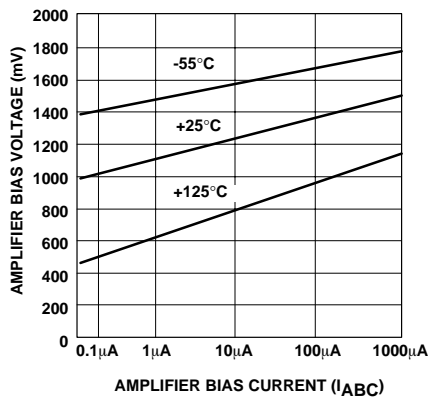


Figure 12. Amplifier Bias Voltage vs. Amplifier Bias Current

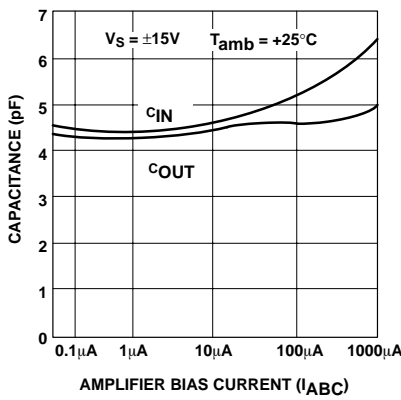


Figure 13. Input and Output Capacitance

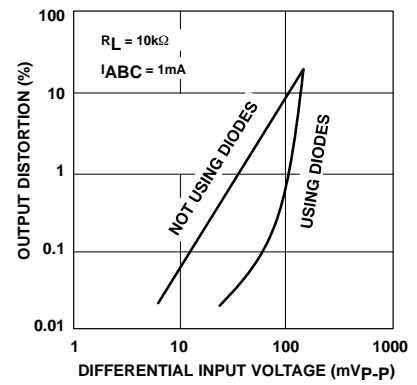


Figure 14. Distortion vs. Differential Input Voltage

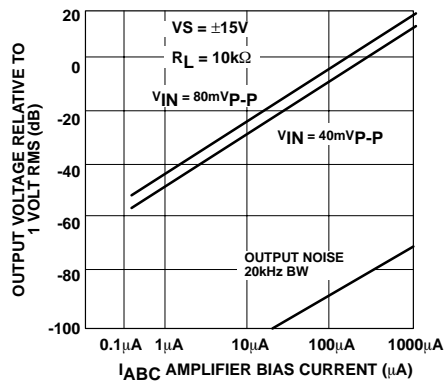


Figure 15. Voltage vs. Amplifier Bias Current

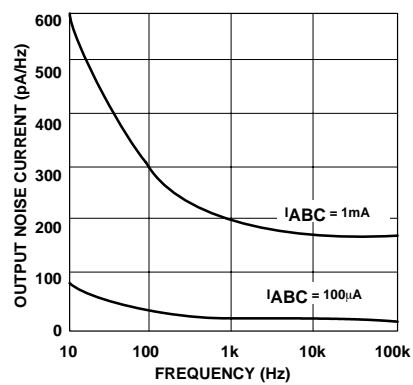


Figure 16. Noise vs. Frequency

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## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

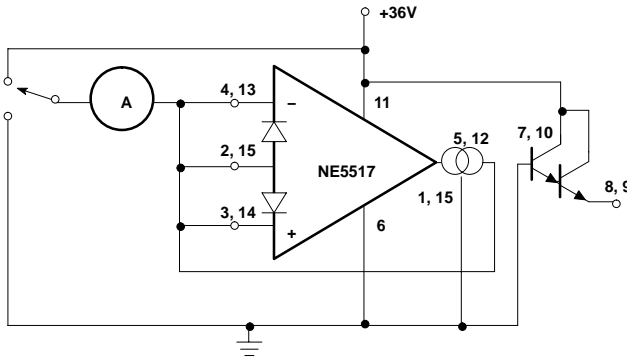


Figure 17. Leakage Current Test Circuit

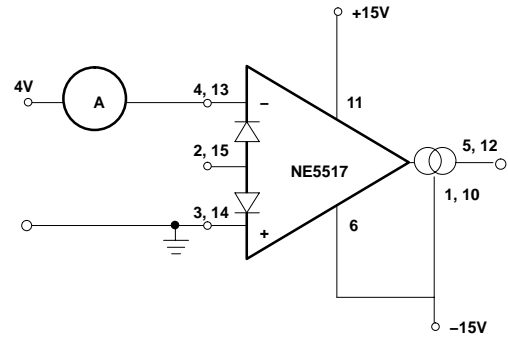


Figure 18. Differential Input Current Test Circuit

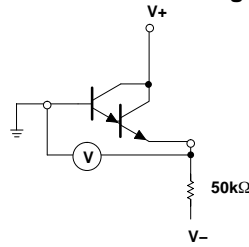


Figure 19. Buffer  $V_{BE}$  Test Circuit

## APPLICATIONS

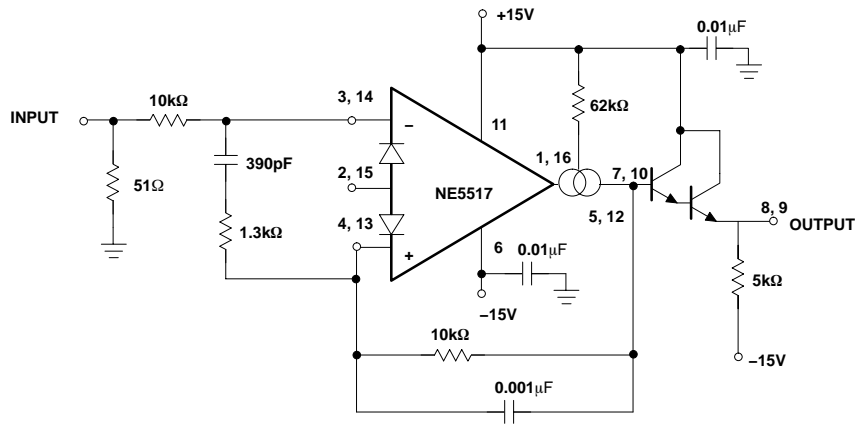


Figure 20. Unity Gain Follower

### CIRCUIT DESCRIPTION

The circuit schematic diagram of one-half of the AU5517/NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 21.

#### Transconductance Amplifier

The transistor pair, Q<sub>4</sub> and Q<sub>5</sub>, forms a transconductance stage. The ratio of their collector currents (I<sub>4</sub> and I<sub>5</sub>, respectively) is defined by the differential input voltage, V<sub>IN</sub>, which is shown in Equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (\text{eq. 1})$$

Where V<sub>IN</sub> is the difference of the two input voltages

KT ≅ 26 mV at room temperature (300°K).

Transistors Q<sub>1</sub>, Q<sub>2</sub> and diode D<sub>1</sub> form a current mirror which focuses the sum of current I<sub>4</sub> and I<sub>5</sub> to be equal to amplifier bias current I<sub>B</sub>:

$$I_4 + I_5 = I_B \quad (\text{eq. 2})$$

If V<sub>IN</sub> is small, the ratio of I<sub>5</sub> and I<sub>4</sub> will approach unity and the Taylor series of ln function can be approximated as

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (\text{eq. 3})$$

$$\text{and } I_4 \cong I_5 \cong I_B$$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{1/2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN} \quad (\text{eq. 4})$$

$$I_5 - I_4 = V_{IN} \frac{(I_B)^q}{2KT}$$

The remaining transistors (Q<sub>6</sub> to Q<sub>11</sub>) and diodes (D<sub>4</sub> to D<sub>6</sub>) form three current mirrors that produce an output current equal to I<sub>5</sub> minus I<sub>4</sub>. Thus:

$$V_{IN} \left( I_B \frac{q}{2KT} \right) = I_O \quad (\text{eq. 5})$$

The term  $\frac{(I_B)^q}{2KT}$  is then the transconductance of the amplifier and is proportional to I<sub>B</sub>.

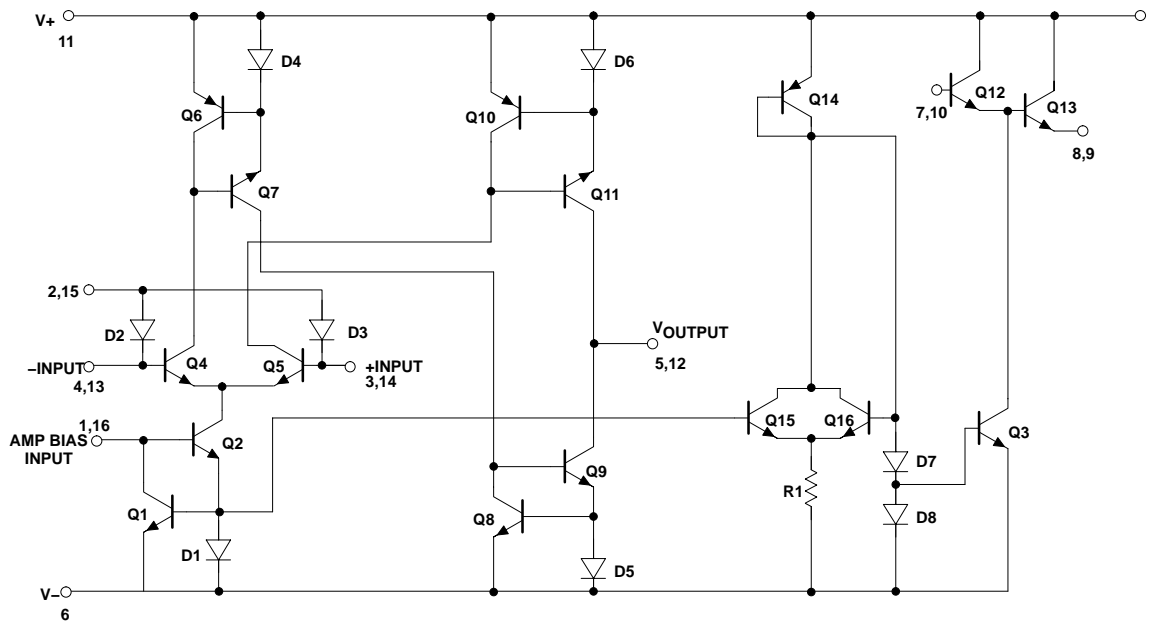


Figure 21. Circuit Diagram of NE5517



### Linearizing Diodes

For  $V_{IN}$  greater than a few millivolts, Equation 3 becomes invalid and the transconductance increases non-linearly. Figure 22 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume  $D_2$  and  $D_3$  are biased with current sources and the input signal current is  $I_S$ . Since  $I_4 + I_5 = I_B$  and  $I_5 - I_4 = I_0$ , that is:  $I_4 = (I_B - I_0)$ ,  $I_5 = (I_B + I_0)$

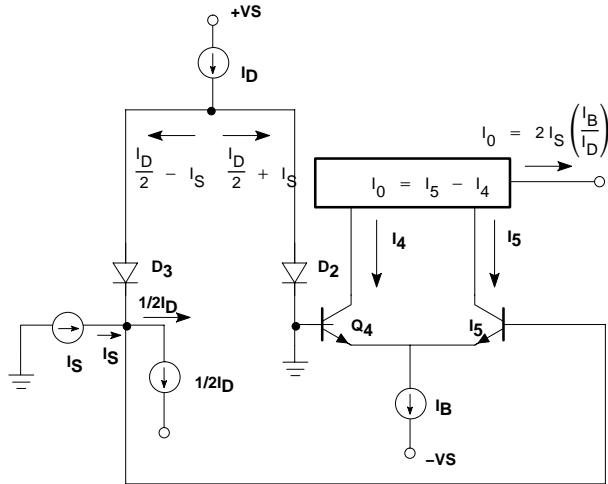


Figure 22. Linearizing Diode

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equation is true:

$$\frac{T}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_0)}{1/2(I_B - I_0)} \quad (\text{eq. 6})$$

$$I_0 = I_S \frac{2I_B}{I_D} \text{ for } |I_S| < \frac{I_D}{2}$$

The only limitation is that the signal current should not exceed  $I_D$ .

### Impedance Buffer

The upper limit of transconductance is defined by the maximum value of  $I_B$  (2.0 mA). The lowest value of  $I_B$  for which the amplifier will function therefore determines the overall dynamic range. At low values of  $I_B$ , a buffer with very low input bias current is desired. A Darlington amplifier with constant-current source ( $Q_{14}$ ,  $Q_{15}$ ,  $Q_{16}$ ,  $D_7$ ,  $D_8$ , and  $R_1$ ) suits the need.

## APPLICATIONS

### Voltage-Controlled Amplifier

In Figure 23, the voltage divider  $R_2$ ,  $R_3$  divides the input-voltage into small values (mV range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \cdot \frac{R_3}{R_2 + R_3} \cdot g_M$$

$$V_{OUT} = I_{OUT} \cdot R_L$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} \cdot g_M \cdot R_L$$

$$(3) g_M = 19.2 I_{ABC}$$

$$(g_M \text{ in } \mu\text{mhos for } I_{ABC} \text{ in mA})$$

Since  $g_M$  is directly proportional to  $I_{ABC}$ , the amplification is controlled by the voltage  $V_C$  in a simple way.

When  $V_C$  is taken relative to  $-V_{CC}$  the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1}$$

The 1.2 V is the voltage across two base-emitter baths in the current mirrors. This circuit is the base for many applications of the AU5517/NE5517.

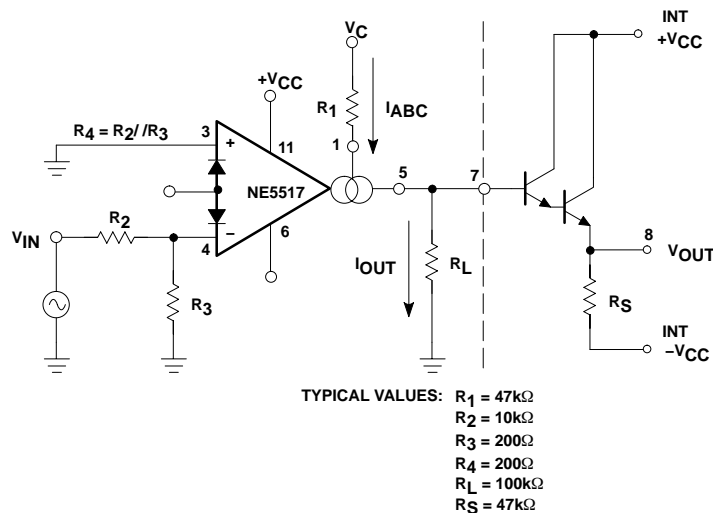


Figure 23.

## Stereo Amplifier With Gain Control

Figure 24 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3 dB is easy to achieve. With the potentiometer,  $R_P$ , the offset can be adjusted. For AC-coupled amplifiers, the potentiometer may be replaced with two 510  $\Omega$  resistors.

## Modulators

Because the transconductance of an OTA (Operational Transconductance Amplifier) is directly proportional to  $I_{ABC}$ , the amplification of a signal can be controlled easily. The output current is the product from transconductance  $\times$  input voltage. The circuit is effective up to approximately 200 kHz. Modulation of 99% is easy to achieve.

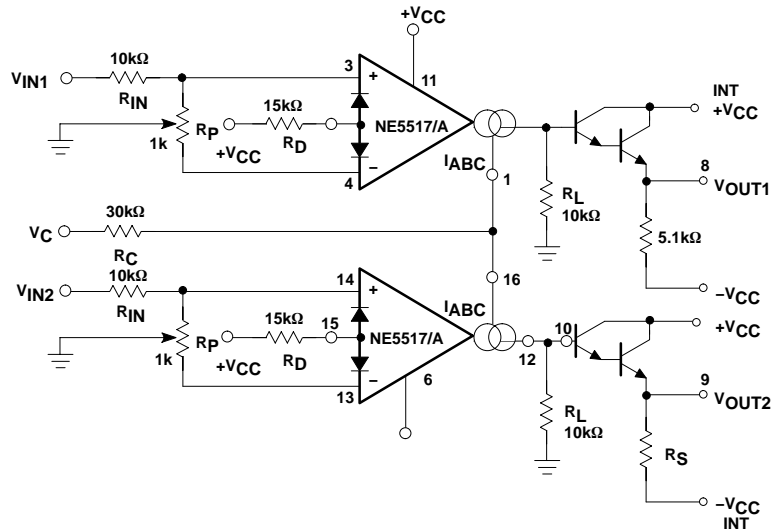


Figure 24. Gain-Controlled Stereo Amplifier

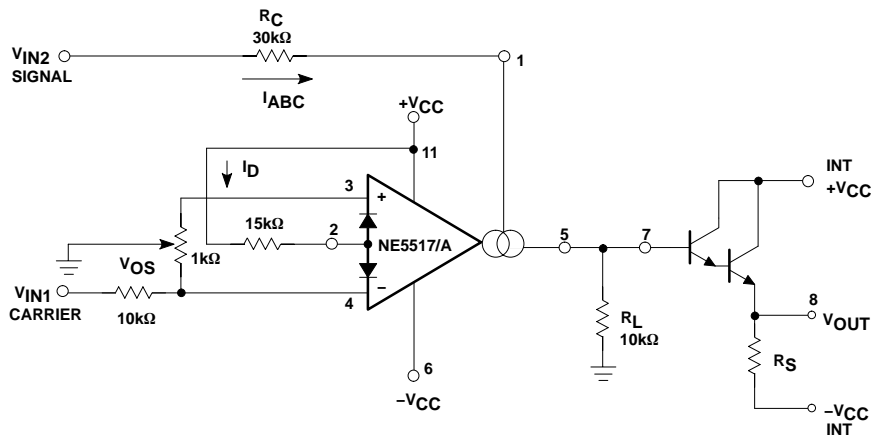


Figure 25. Amplitude Modulator

### Voltage-Controlled Resistor (VCR)

Because an OTA is capable of producing an output current proportional to the input voltage, a voltage variable resistor can be made. Figure 26 shows how this is done. A voltage presented at the  $R_X$  terminals forces a voltage at the input. This voltage is multiplied by  $g_M$  and thereby forces a current through the  $R_X$  terminals:

$$R_x = \frac{R + R_A}{g_M + \frac{R_A}{R}}$$

where  $g_M$  is approximately 19.21  $\mu$ MHOs at room temperature. Figure 27 shows a Voltage Controlled Resistor using linearizing diodes. This improves the noise performance of the resistor.

### Voltage-Controlled Filters

Figure 28 shows a Voltage Controlled Low-Pass Filter. The circuit is a unity gain buffer until  $X_C/g_M$  is equal to  $R/R_A$ . Then, the frequency response rolls off at a 6dB per octave with the -3 dB point being defined by the given equations. Operating in the same manner, a Voltage Controlled High-Pass Filter is shown in Figure 29. Higher order filters can be made using additional amplifiers as shown in Figures 30 and 31.

### Voltage-Controlled Oscillators

Figure 32 shows a voltage-controlled triangle-square wave generator. With the indicated values a range from 2.0 Hz to 200 kHz is possible by varying  $I_{ABC}$  from 1.0 mA to 10  $\mu$ A.

The output amplitude is determined by  $I_{OUT} \times R_{OUT}$ .

Please notice the differential input voltage is not allowed to be above 5.0 V.

With a slight modification of this circuit you can get the sawtooth pulse generator, as shown in Figure 33.

### APPLICATION HINTS

To hold the transconductance  $g_M$  within the linear range,  $I_{ABC}$  should be chosen not greater than 1.0 mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a PNP transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 to -2.0 mA. In this application, however, the current range is set through  $R_{REF}$  (10 k $\Omega$ ) to 0 to -1.0 mA.

$$I_{DACMAX} = 2 \cdot \frac{V_{REF}}{R_{REF}} = 2 \cdot \frac{5V}{10k\Omega} = 1mA$$

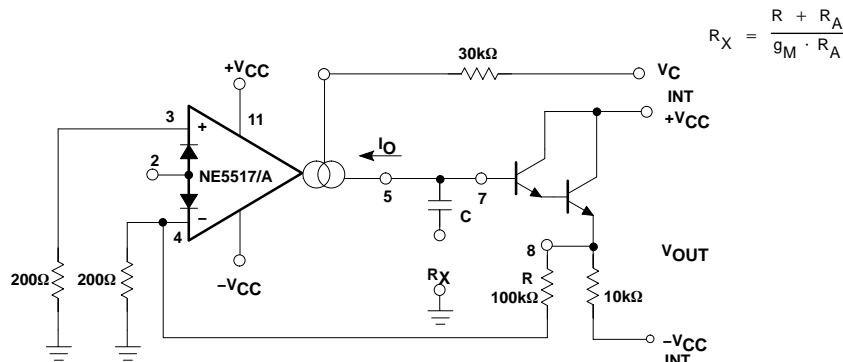


Figure 26. VCR

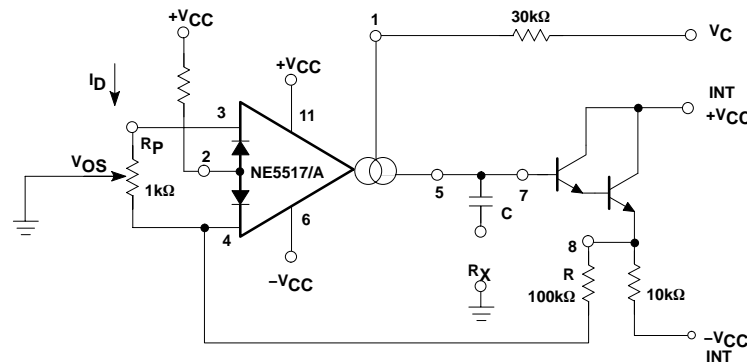
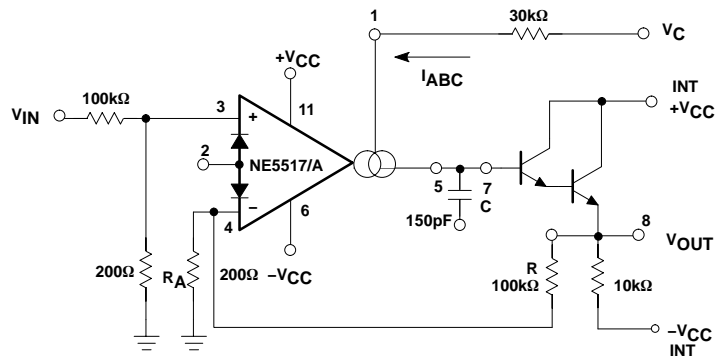


Figure 27. VCR with Linearizing Diodes

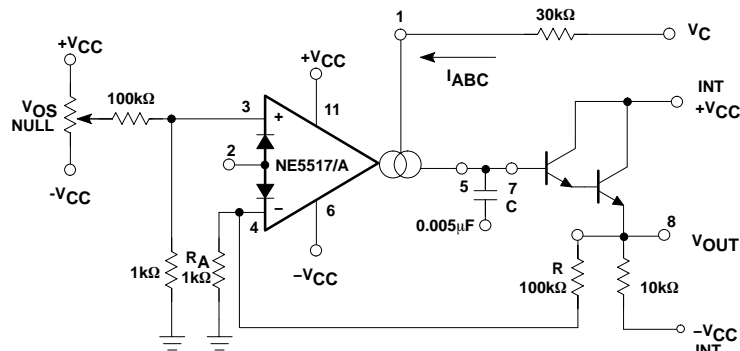
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NOTE:

$$f_O = \frac{R_A 9M}{g(R + R_A) 2\pi C}$$

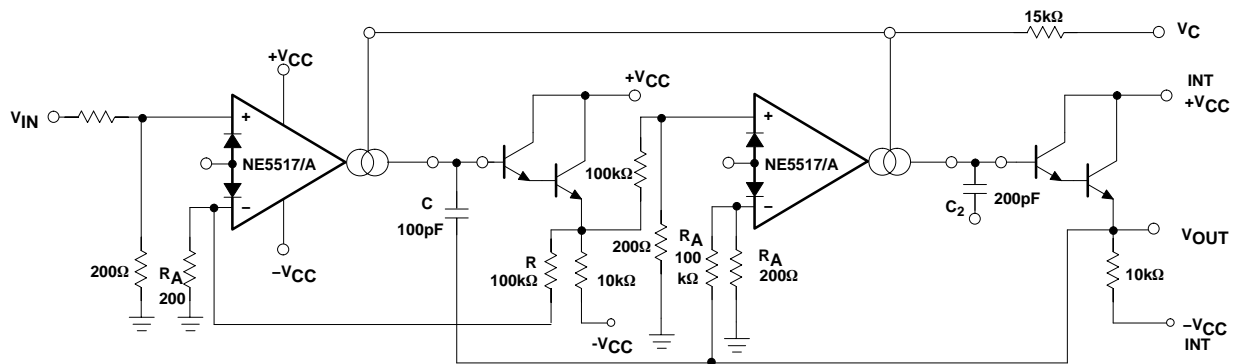
Figure 28. Voltage-Controlled Low-Pass Filter



NOTE:

$$f_O = \frac{R_A 9M}{g(R + R_A) 2\pi C}$$

Figure 29. Voltage-Controlled High-Pass Filter



NOTE:

$$f_O = \frac{R_A 9M}{(R + R_A) 2\pi C}$$

Figure 30. Butterworth Filter – 2nd Order

## NE5517, NE5517A, AU5517

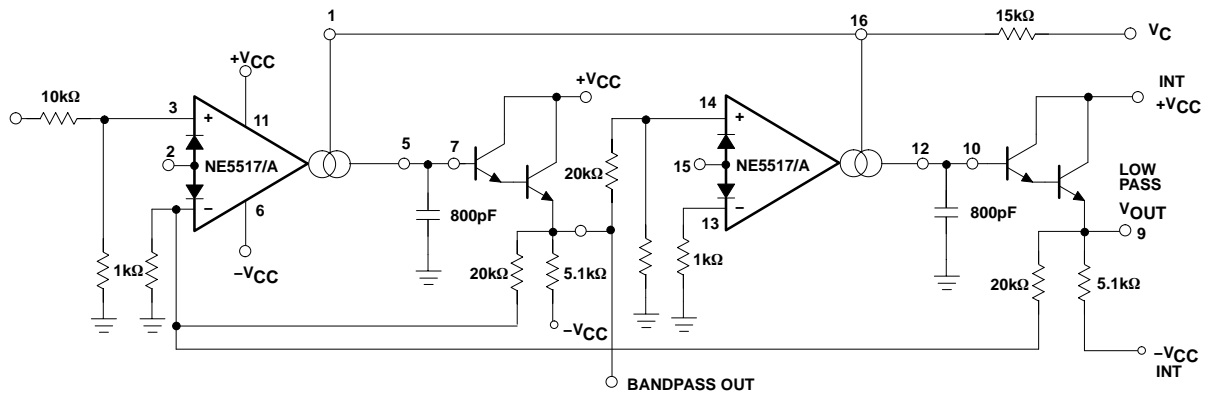


Figure 31. State Variable Filter

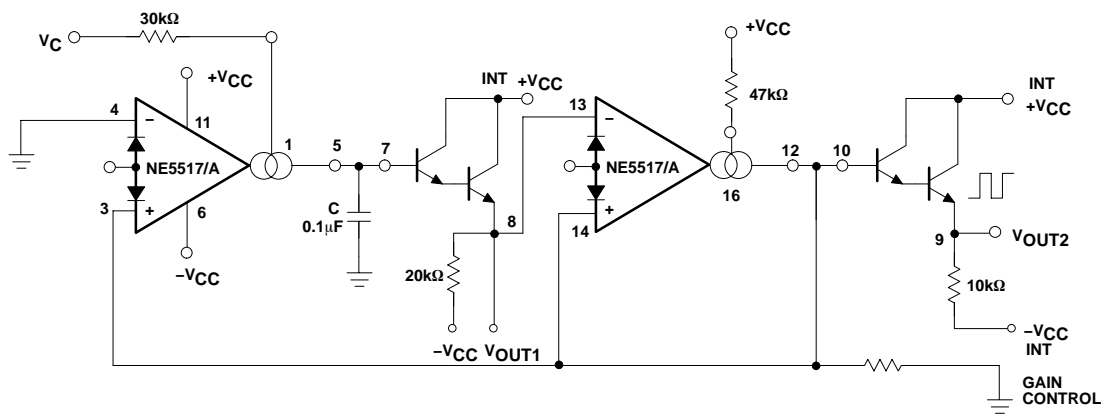


Figure 32. Triangle-Square Wave Generator (VCO)

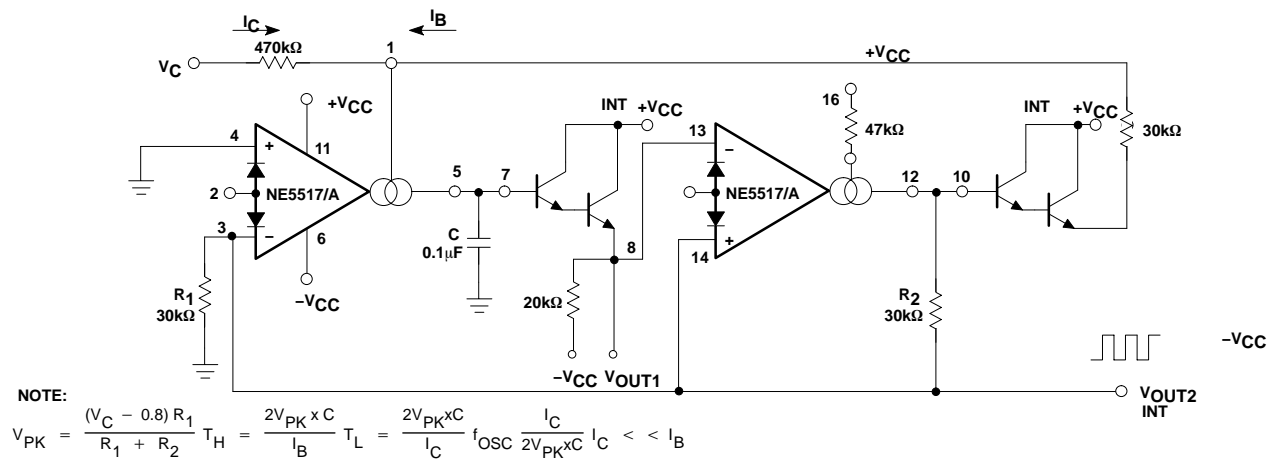


Figure 33. Sawtooth Pulse VCO

## NE5517, NE5517A, AU5517

### ORDERING INFORMATION

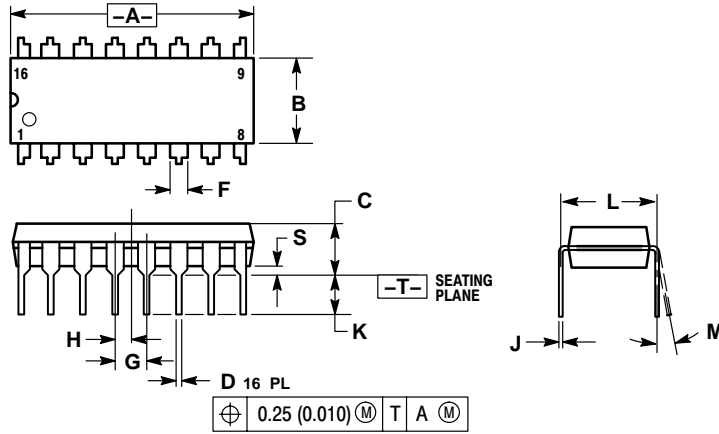
Device	Description	Temperature Range	Shipping†
AU5517DR2	16-Pin Small Outline (SO) Package	–40 to +125 °C	2500 Tape & Reel
NE5517D	16-Pin Small Outline (SO) Package	0 to +70 °C	48 Units/Rail
NE5517DR2	16-Pin Small Outline (SO) Package	0 to +70 °C	2500 Tape & Reel
NE5517N	16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	25 Units/Rail
NE5517AN	16-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	25 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NE5517, NE5517A, AU5517

## PACKAGE DIMENSIONS

PDIP-16  
N SUFFIX  
CASE 648-08  
ISSUE R



### NOTES:

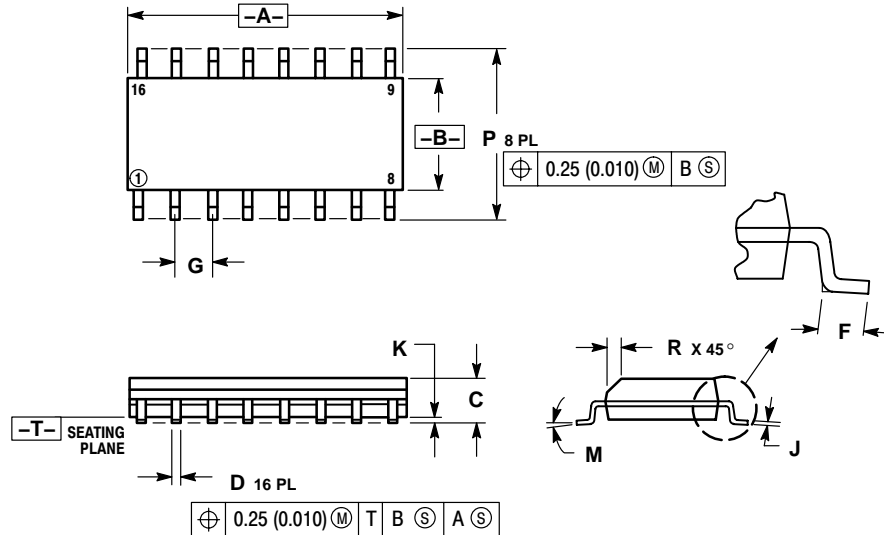
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

# NE5517, NE5517A, AU5517

## PACKAGE DIMENSIONS

SO-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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