

2N7002

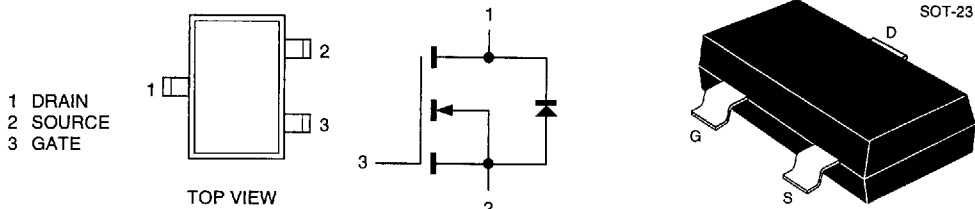
DESCRIPTION

Calogic's 2N7002 device type is a vertical DMOS FET transistor housed in a surface mount SOT-23 for micro-assembly applications. The device is an excellent choice for switching applications where breakdown (B_v) and low on-resistance are important.

ORDERING INFORMATION

Part	Package	Temperature Range
2N7002	Plastic SOT-23 Package	-55°C to +150°C
X2N7002	Sorted Chips in Carriers	-55°C to +150°C

PIN CONFIGURATION



CD5

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	7.5	0.115

PRODUCT MARKING	
2N7002	V02

■ 1844322 0000992 073 ■

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETERS	LIMITS	UNITS	TEST CONDITIONS
V _{DS}	Drain-Source Voltage	60	V	
V _{GS}	Gate-Source Voltage	±40		
I _D	Continuous Drain Current	0.115	A	T _A = 25°C
		0.073		T _A = 100°C
I _{DM}	Pulsed Drain Current ¹	0.8		
P _D	Power Dissipation	200	mW	T _A = 25°C
		80		T _A = 100°C
T _J	Operating Junction Temperature Range	-55 to 150	°C	
T _{stg}	Storage Temperature Range	-55 to 150		
T _L	Lead Temperature (1/16" from case for 10 sec.)	300		

THERMAL RESISTANCE RATINGS

SYMBOL	THERMAL RESISTANCE	LIMITS	UNITS
R _{thJA}	Junction-to-Ambient	625	K/W

NOTE: 1. Pulse width limited by maximum junction temperature.

SPECIFICATIONS¹

SYMBOL	PARAMETER	MIN	TYP ²	MAX	UNIT	TEST CONDITIONS
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	60	70		V	I _D = 10µA, V _{GS} = 0V
V _{GS(th)}	Gate-Threshold Voltage	1	1.9	2.5		V _{DS} = V _{GS} , I _D = 0.25mA
I _{GSS}	Gate-Body Leakage			±100	nA	V _{GS} = ±20V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current			1	µA	V _{DS} = 60V, V _{GS} = 0V T _C = 125°C
				500		
I _{D(ON)}	On-State Drain Current ³	500	1000		mA	V _{DS} = ≥2V _{DS(ON)} , V _{GS} = 10V
r _{DS(ON)}	Drain-Source On-Resistance ³		5	7.5	Ω	V _{GS} = 5V, I _D = 50mA T _C = 125°C
			9	13.5		V _{GS} = 10V, I _D = 0.5A T _C = 125°C
			2.5	7.5		
			4.4	13.5		
V _{DS(ON)}	Drain-Source On-Voltage ³		0.25	0.375	V	V _{GS} = 5V, I _D = 50mA
			1.25	3.75		V _{GS} = 10V, I _D = 0.5A
			2.2	6.75		T _C = 125°C ⁴
g _{FS}	Forward Transconductance ³	80	170		mS	V _{DS} = 10V, I _D = 0.2A
g _{OS}	Common Source Output Conductance ^{3, 4}		500		µS	V _{DS} = 5V, I _D = 50mA
DYNAMIC						
C _{iss}	Input Capacitance		16	50	pF	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz
C _{oss}	Output Capacitance ⁴		11	25		
C _{rss}	Reverse Transfer Capacitance		2	5		
SWITCHING						
t _{ON}	Turn-On Time		7	20	nS	V _{DD} = 30V, R _L = 150Ω, I _D = 0.2A V _{GEN} = 10V, R _G = 25Ω (Switching time is essentially independent of operating temperature)
t _{OFF}	Turn-Off Time		7	20		

- NOTES: 1. T_A = 25°C unless otherwise specified.
 2. For design aid only, not subject to production testing.
 3. Pulse test; PW = ≤80µS, duty cycle ≤1%.
 4. This parameter not registered with JEDEC.