

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

08/03/04

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
C		338723	PRODUCTION RELEASED	DATE	DATE
				08/04/04	?

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3	3	POWER BLOCK DIAGRAM	
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30	26	CPU STRAPS	
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32	28	CPU BYPASS	
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45	37	PARALLEL TERMINATION	
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48	39	U3LITE AGP	
49	40	GPU AGP	
50	41	GRAPHICS VREGS (GPU CORE & 1.5V)	

TOP

PROCESSOR

MEMORY

GRAPHICS

\* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

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53	44	FRAME BUFFER TERMINATION	
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55	46	GRAPHICS DDR SDRAM B	
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60	51	U3LITE HYPERTRANSPORT	
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64	53	HYPERTRANSPORT LA CONNECTORS	
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84*	61	SHASTA ETHERNET	
87	62	ETHERNET PHY & CONNECTORS	
88*	63	SHASTA FIREWIRE	
90	64	FIREWIRE A PHY & CONNECTORS	
91*	65	USB HOST INTERFACE	
92	66	USB DEVICE INTERFACE	
94	67	MODEM CONNECTOR	
95*	68	PCM3052 AUDIO CODEC	
96*	69	LINE IN AMP	
98*	70	LINE OUT AMP	
100*	71	SPEAKER AMP	
101*	72	AUDIO CONNECTORS	
102*	73	AUDIO POWER SUPPLIES	
103*	74	S/PDIF TRANSMITTER	

GRAPHICS

HT

PCI

DISK

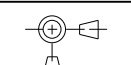
ETHERNET

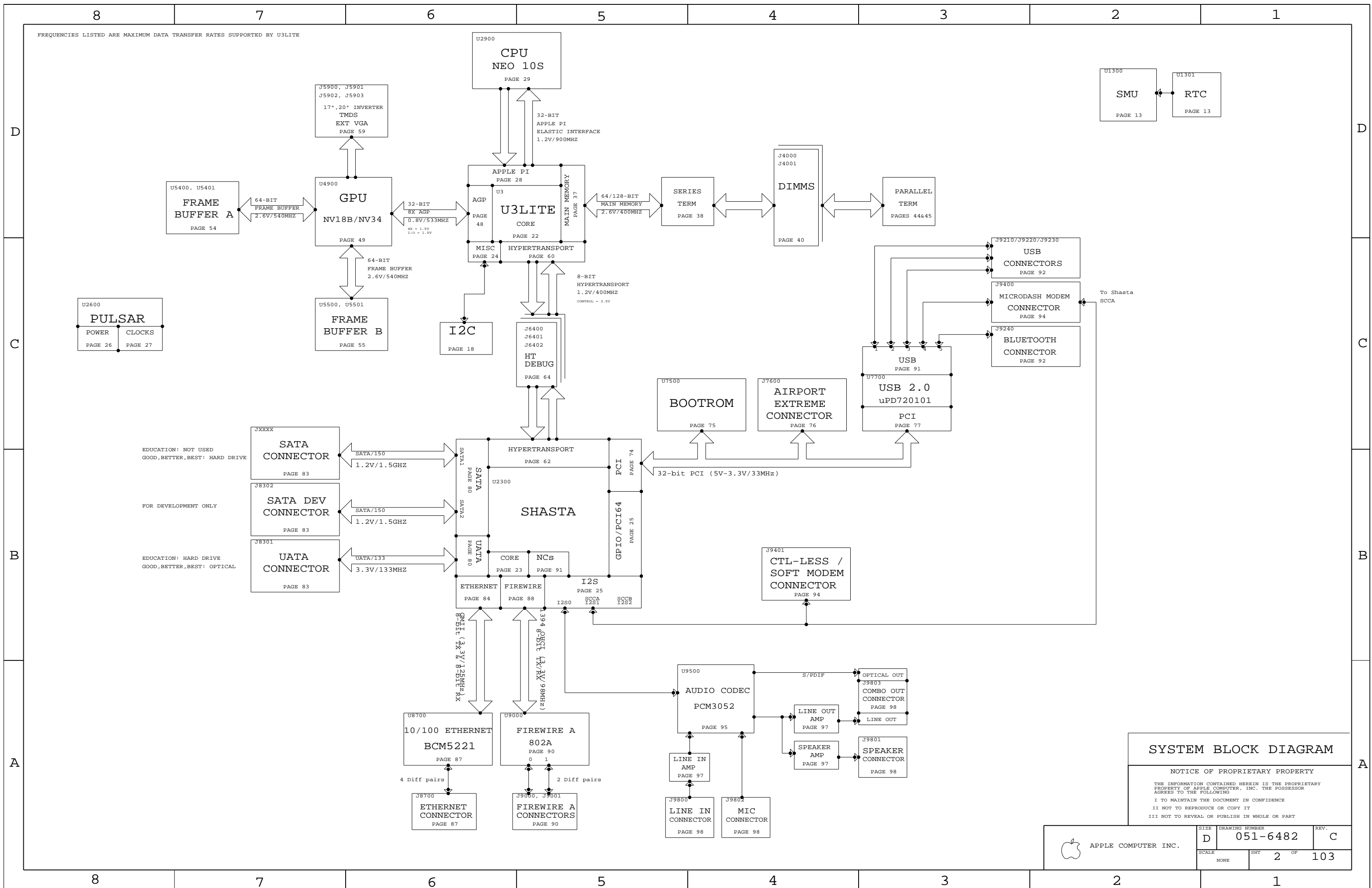
FIREWIRE

USB

MODEM

AUDIO

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
xx : _____	_____	DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
x.xx : _____	_____	ENG APPD	MFG APPD		
x.xxx : _____	_____	QA APPD	DESIGNER		
ANGLES : _____	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				051-6482	REV. C
				SHEET 1 OF 103	

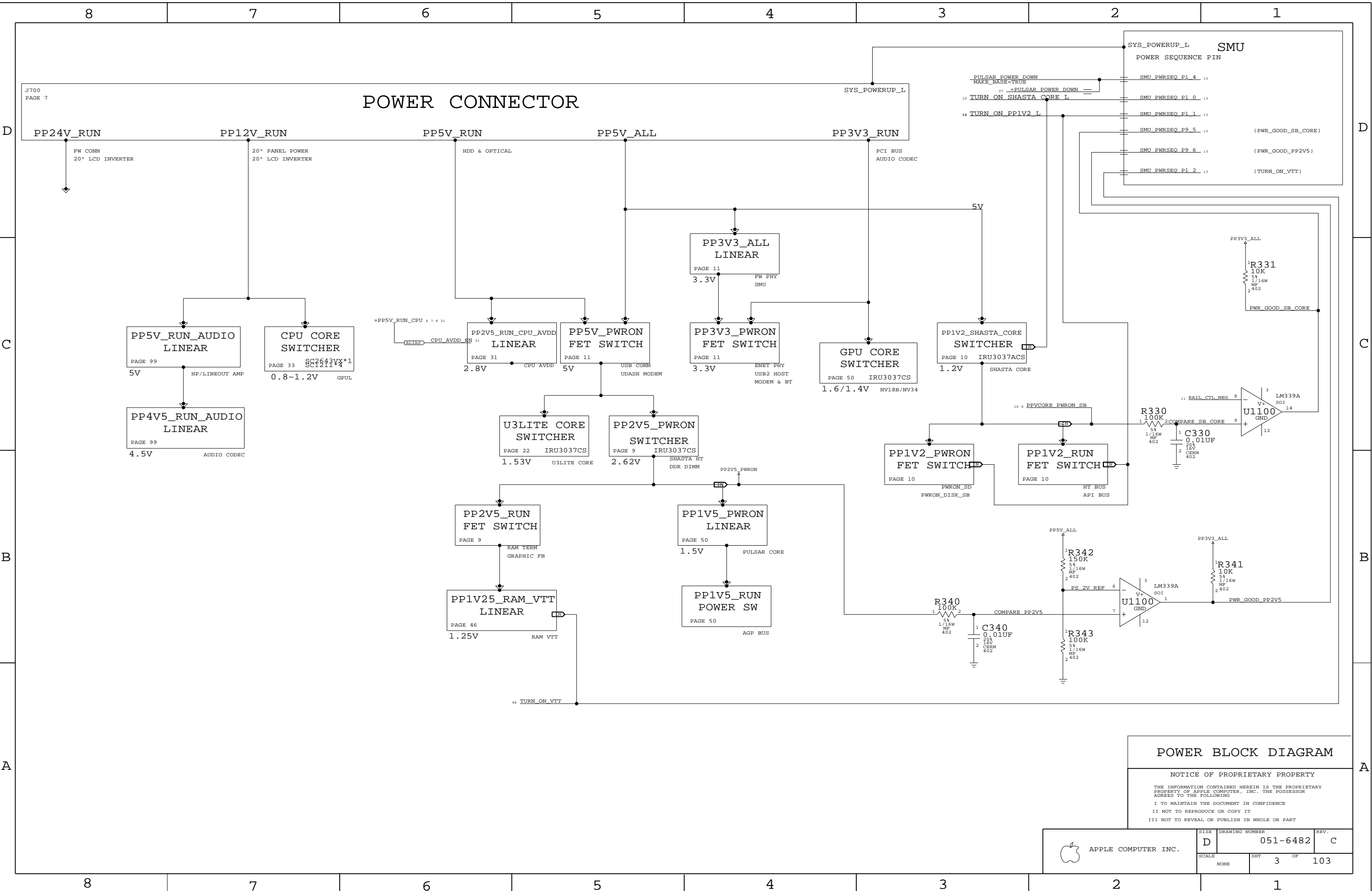


FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE

### SYSTEM BLOCK DIAGRAM

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**POWER BLOCK DIAGRAM**

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	SCALE NONE	SHEET 3	OF 103



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1

PROCESSORS

QUALIFIED

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2968	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD3,1.6G,85C,ARA	1.6GHZ	1.25V	45W	?	U2900	CPU_DD30_1_6GHZ
337S2969	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD3,1.8G,85C,BPA	1.8GHZ	1.20V	45W	?	U2900	CPU_DD30_1_8GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S2970	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BRA	1.25V

NOT QUALIFIED

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S2957	337S2786	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BNA	1.20V

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2865	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD2.11,1.8GHZ,85C	1.8GHZ	1.45V	45W	?	U2900	CPU_DD211_1_8GHZ
337S2866	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD2.11,2.0GHZ,85C	2.0GHZ	1.45V	45W	?	U2900	CPU_DD211_2_0GHZ
337S2787	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,REV3,2.0G,85C,CJA	2.0GHZ	1.25V	45W	?	U2900	CPU_DD30_2_0GHZ

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0284	1	IC,U3LITE,V1.1,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L,V1.1,200MM,PBGA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
820-1540	1	PCB,FAB,MLB	MLB1	
825-6447	1	BARCODE LABEL, MLB, Q45	LBL1	
051-6482	1	PCB,SCHEM,MLB	SCH1	
341T1366	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
341T1395	1	PURCH ASSY, SMU BIG	U1300	
CRITICAL 603-6015	1	HEAT SINK ASSEMBLY 17 IN	MECH17	17_INCH_LCD
CRITICAL 603-6016	1	HEAT SINK ASSEMBLY 20 IN	MECH20	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114	LED700	LED702	LED5900 KINGBRIGHT LED

TABLE ITEMS


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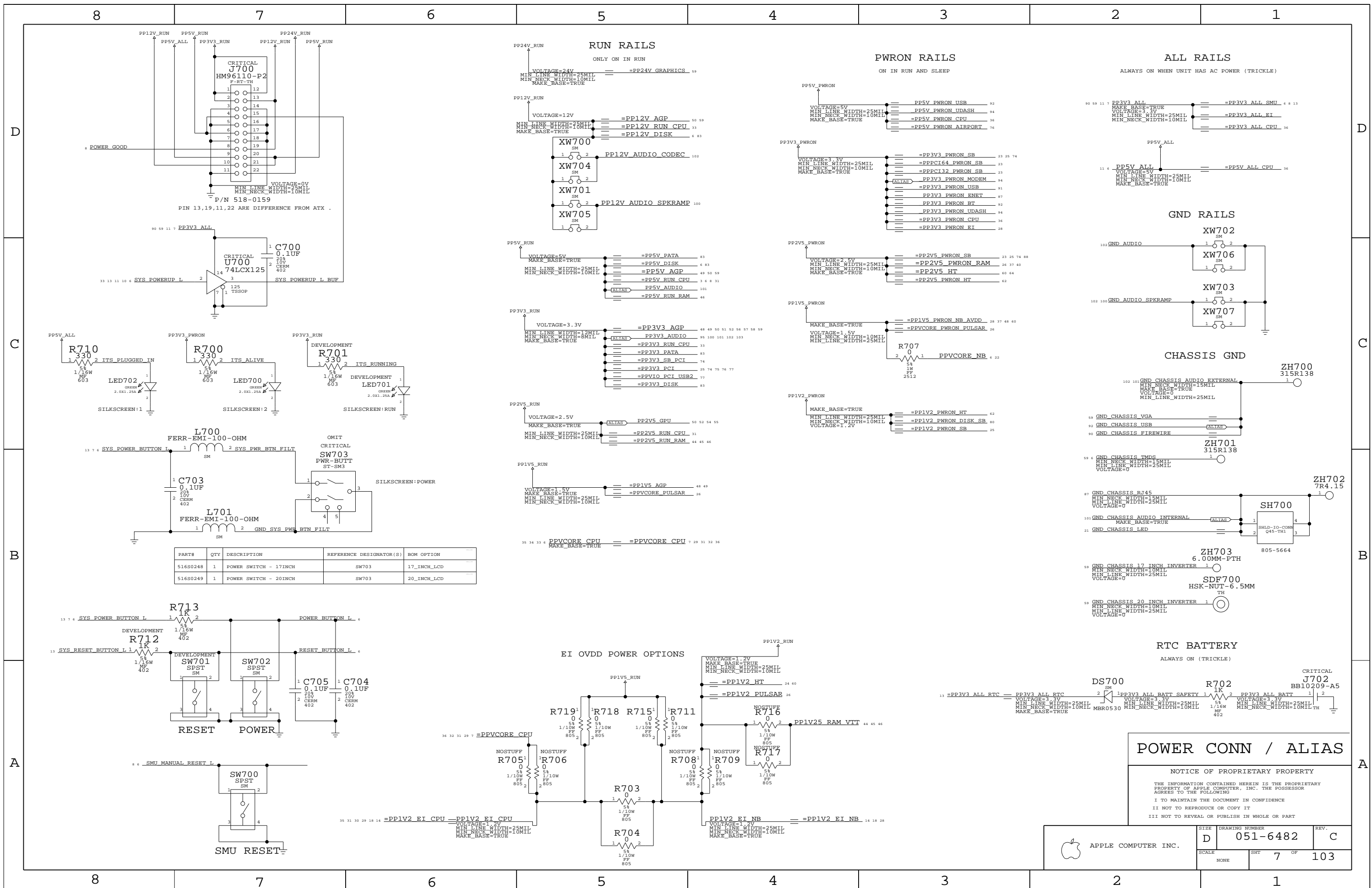
4

3

2

1





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
516S0248	1	POWER SWITCH - 17INCH	SW703	17_INCH_LCD
516S0249	1	POWER SWITCH - 20INCH	SW703	20_INCH_LCD

### POWER CONN / ALIAS

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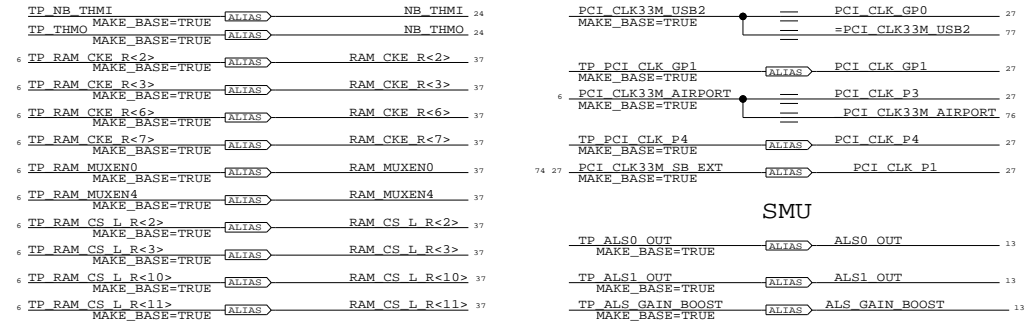
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II NOT TO REPRODUCE OR COPY IT

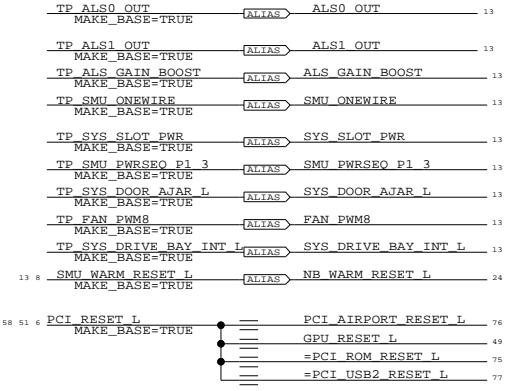
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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NONE			

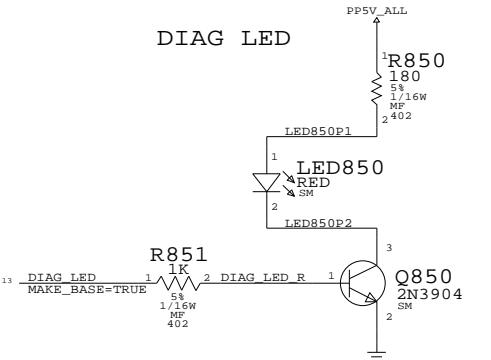
PCI CLOCKS



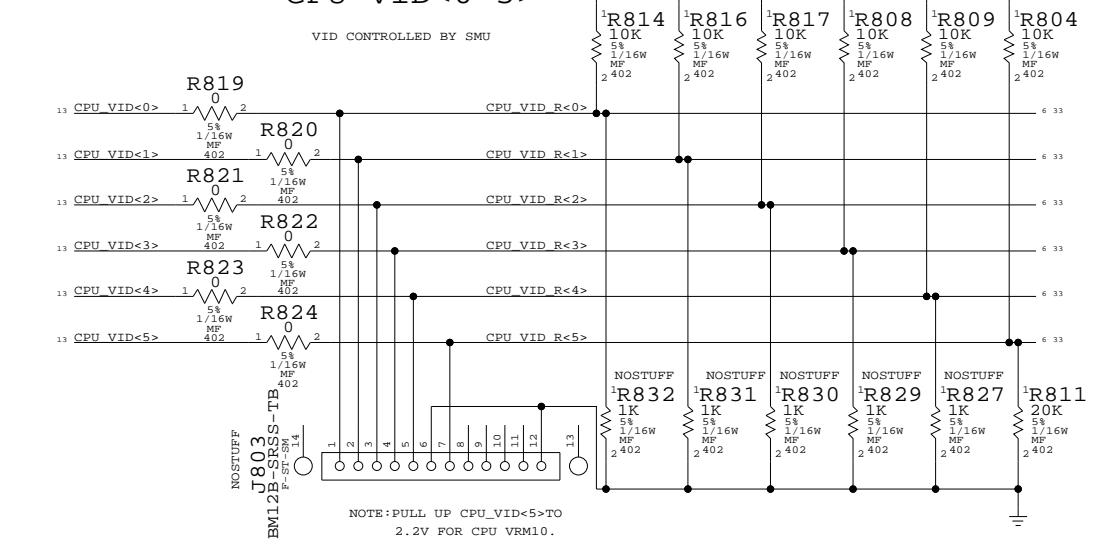
SMU



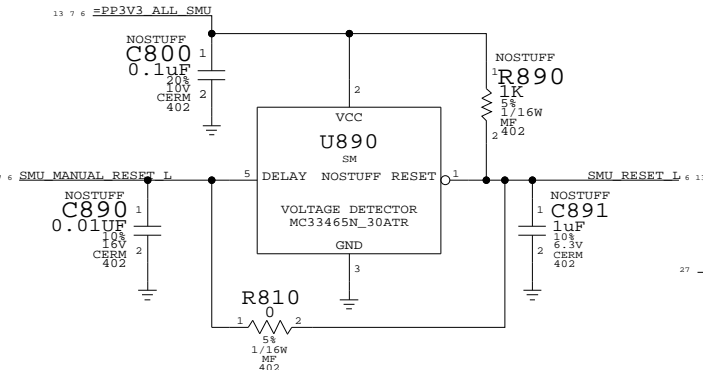
DIAG LED



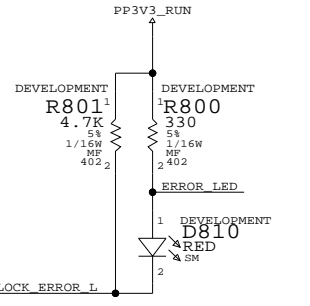
CPU VID<0:5>



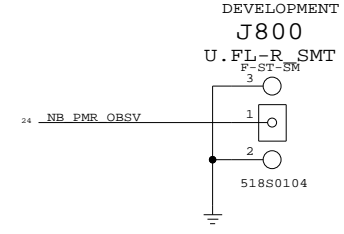
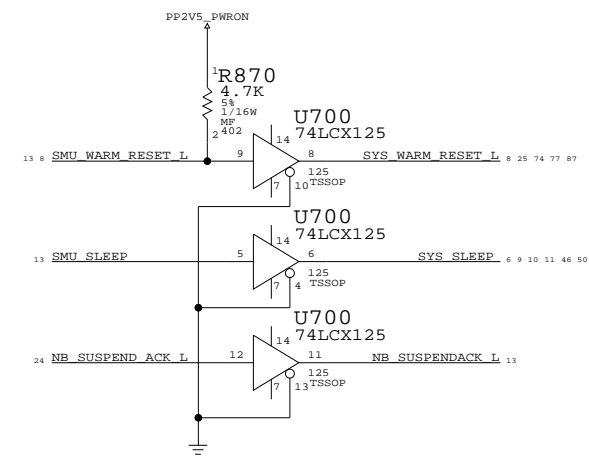
BACKUP SMU RESET CIRCUIT



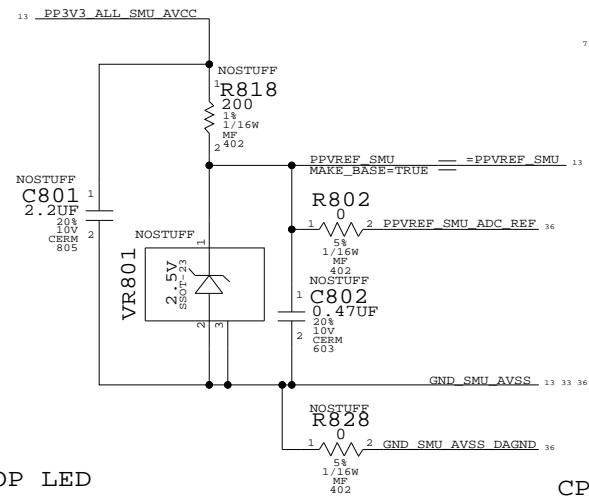
PULSAR ERROR\_L LED



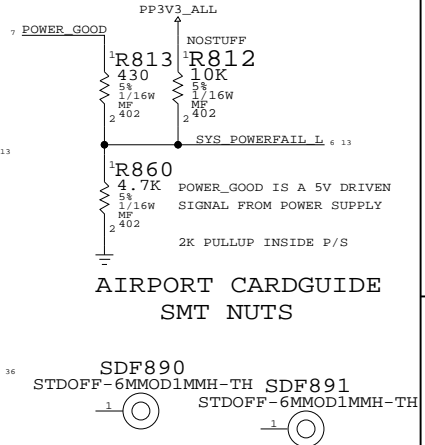
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_RESET	10 MIL SPACING	
SMU_RESET	10 MIL SPACING	



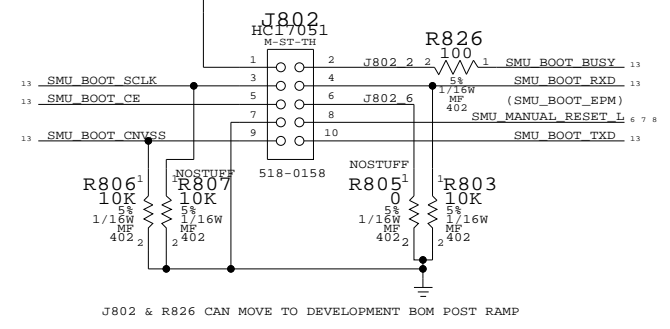
SMU ANALOG VREF



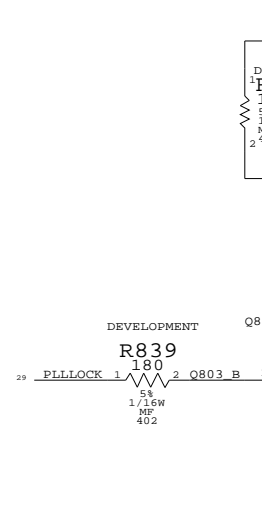
POWER\_FAIL\_L CONNECTION



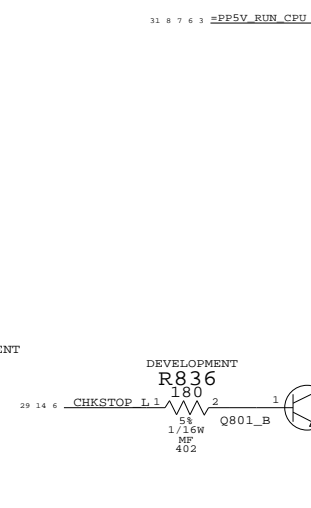
DOWNLOAD CONNECTOR



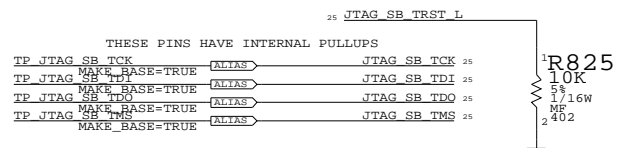
PLL LOCK LED



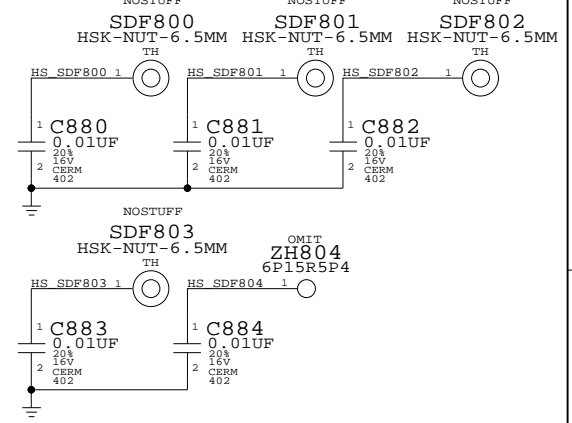
CHKSTOP LED



SHASTA JTAG PULL DOWN



CPU HEATSINK SMT NUTS



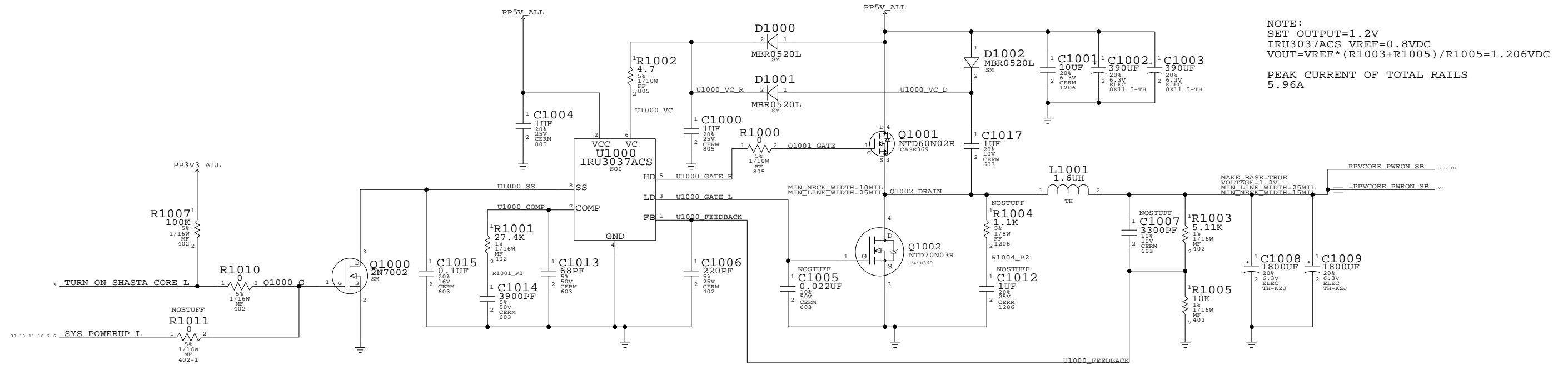
SIGNAL ALIAS

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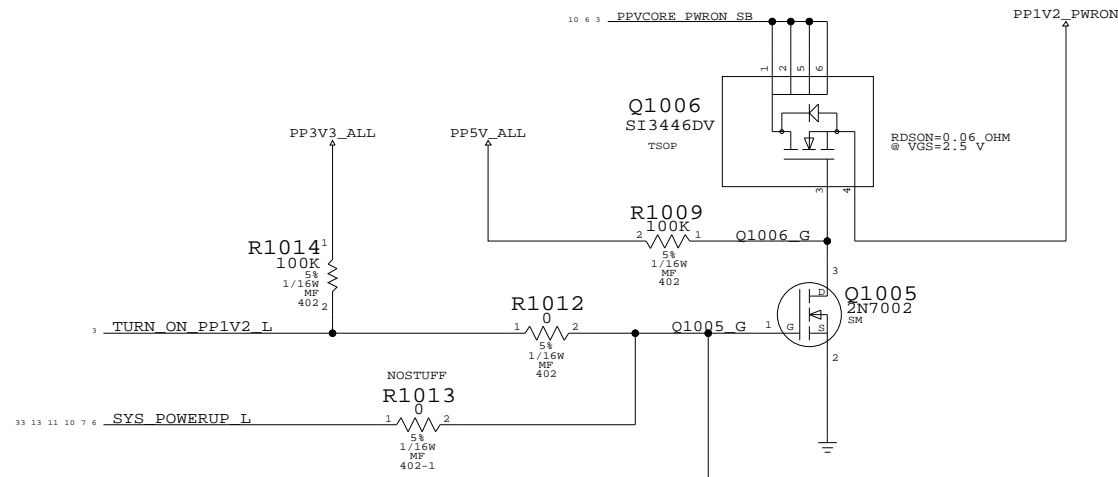


# SHASTA CORE VOLTAGE REGULATOR

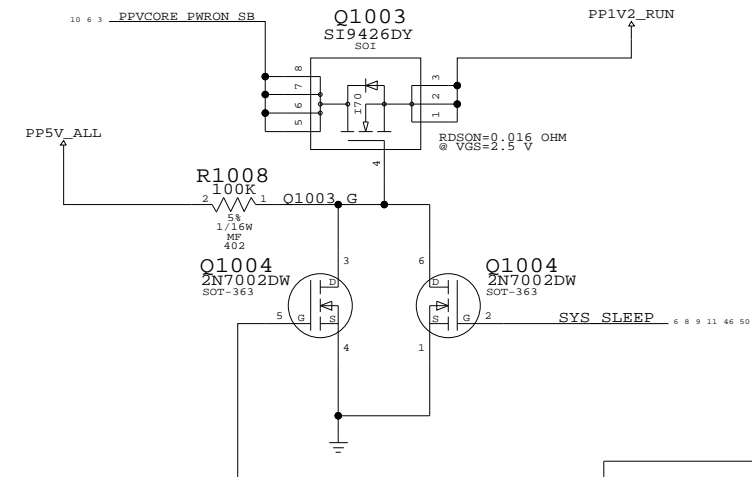


NOTE:  
 SET OUTPUT=1.2V  
 IRU3037ACS VREF=0.8VDC  
 $V_{OUT} = V_{REF} * (R_{1003} + R_{1005}) / R_{1005} = 1.206VDC$   
 PEAK CURRENT OF TOTAL RAILS  
 5.96A

PP1V2\_PWRON FET SWITCH  
 PEAK CURRENT 0.6A



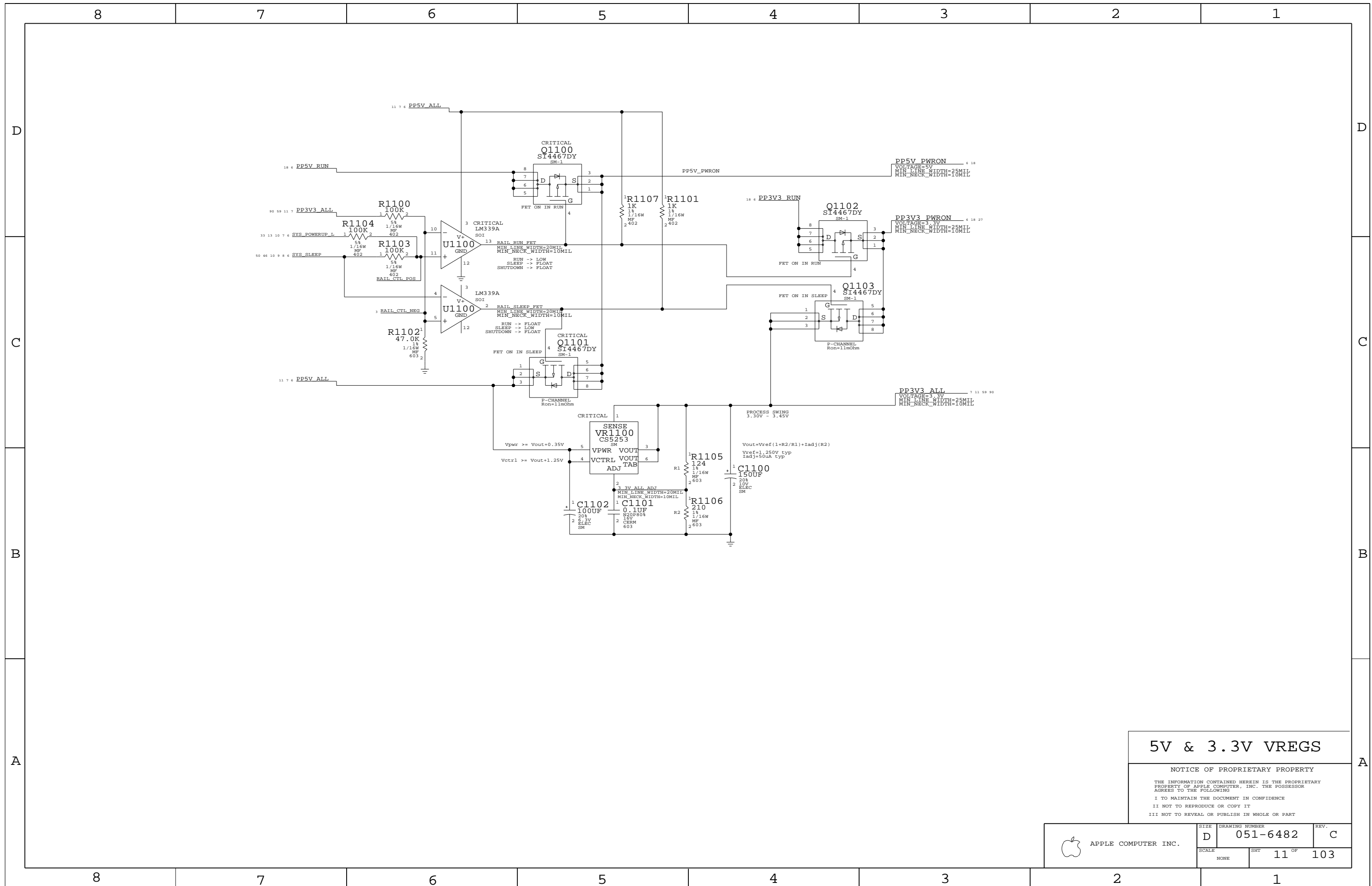
PP1V2\_RUN FET SWITCH  
 PEAK CURRENT 4.43A



## 1.2V VREG

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NONE			



# 5V & 3.3V VREGS

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SCALE	SHT	11 OF	103
NONE			

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	15 MIL SPACING	SMU_CLK10M_XIN
	15 MIL SPACING	SMU_CLK10M_XOUT
	15 MIL SPACING	SMU_CLK10M_XOUT_B
RTC_CLK32K_XTAL	15 MIL SPACING	RTC_CLK32K_X1
	15 MIL SPACING	RTC_CLK32K_X2

### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_ALL\_SMU  
 - \_PP3V3\_ALL\_RTC  
 - \_PP3V3\_PWRON\_SMU  
 - \_PPVREF\_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

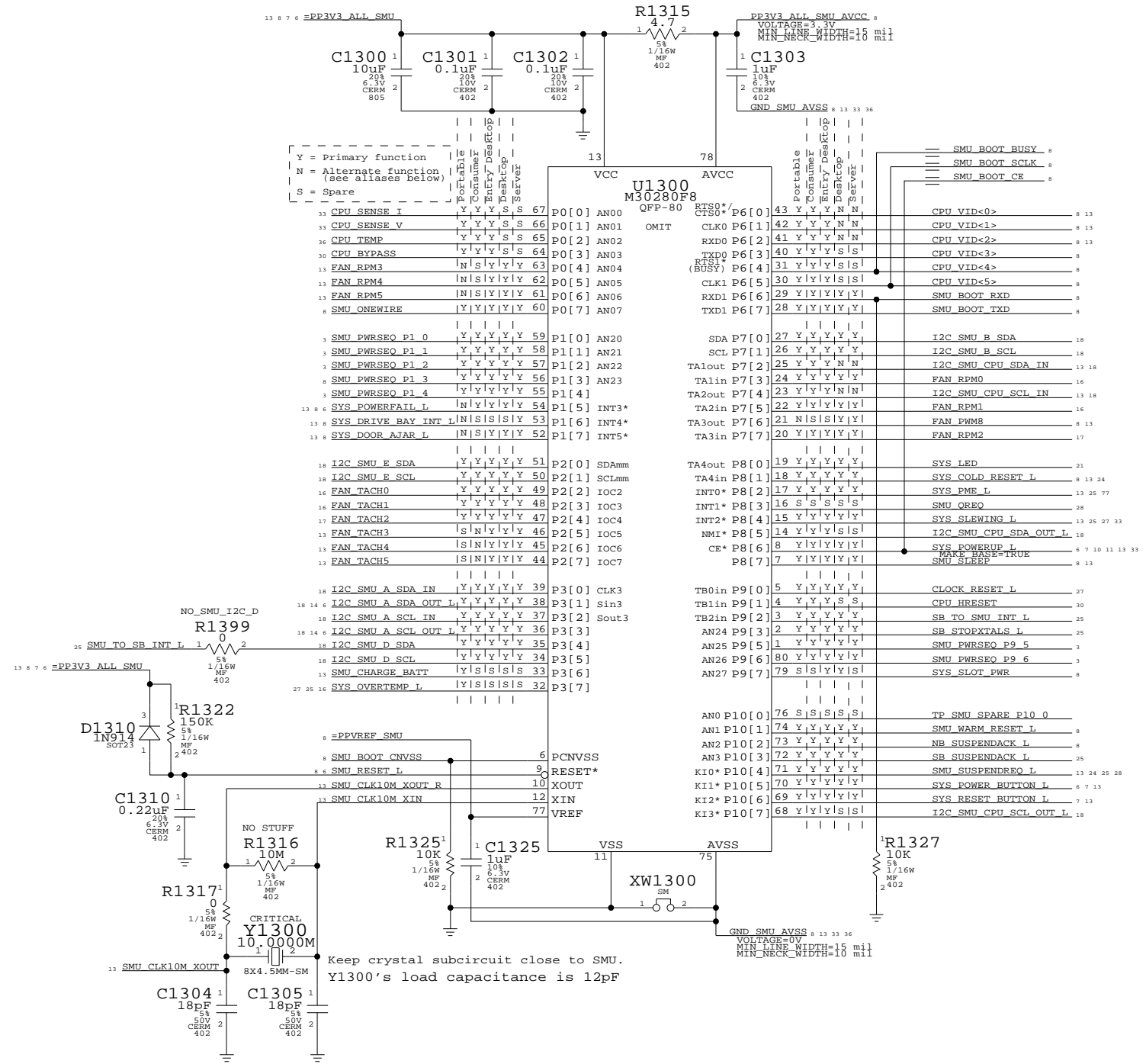
NOTE: CPU current/voltage monitoring (CPU\_SENSE\_I/CPU\_SENSE\_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND\_SMU\_AVSS. SMU\_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND\_SMU\_AVSS). None of those capacitors are provided on this page.

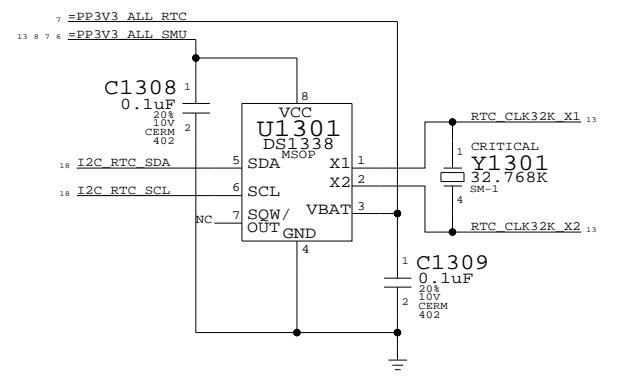
NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

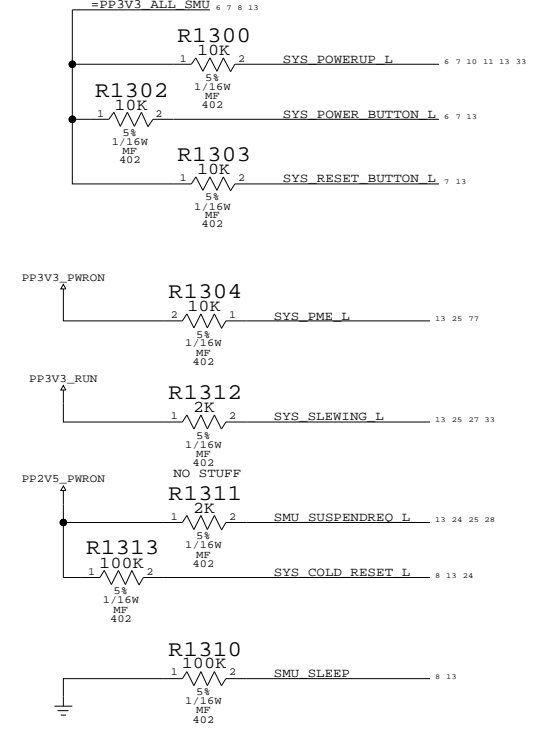
### System Management Unit



### Real Time Clock



### SMU Pull-ups / pull-down



### Alternate Functions

Portable		Consumer		Tower & Server	
Port		Port		Port	
13 FAN RPM3	0.4	13 FAN TACH3	2.5	13 CPU VID<0>	6.0
13 FAN RPM4	0.5	13 FAN TACH4	2.6	13 CPU VID<1>	6.1
13 FAN RPM5	0.6	13 FAN TACH5	2.7	13 CPU VID<2>	6.2
13 SYS_POWERFAIL_L	1.5	13 SMU CHARGE_BATT	3.6	13 I2C_SMU_CPU_SDA_IN	7.2
13 SYS_DRIVE_BAY_INT_L	1.6			13 I2C_SMU_CPU_SCL_IN	7.4
13 SYS_DOOR_AJAR_L	1.7				
13 FAN_PWM8	7.6				

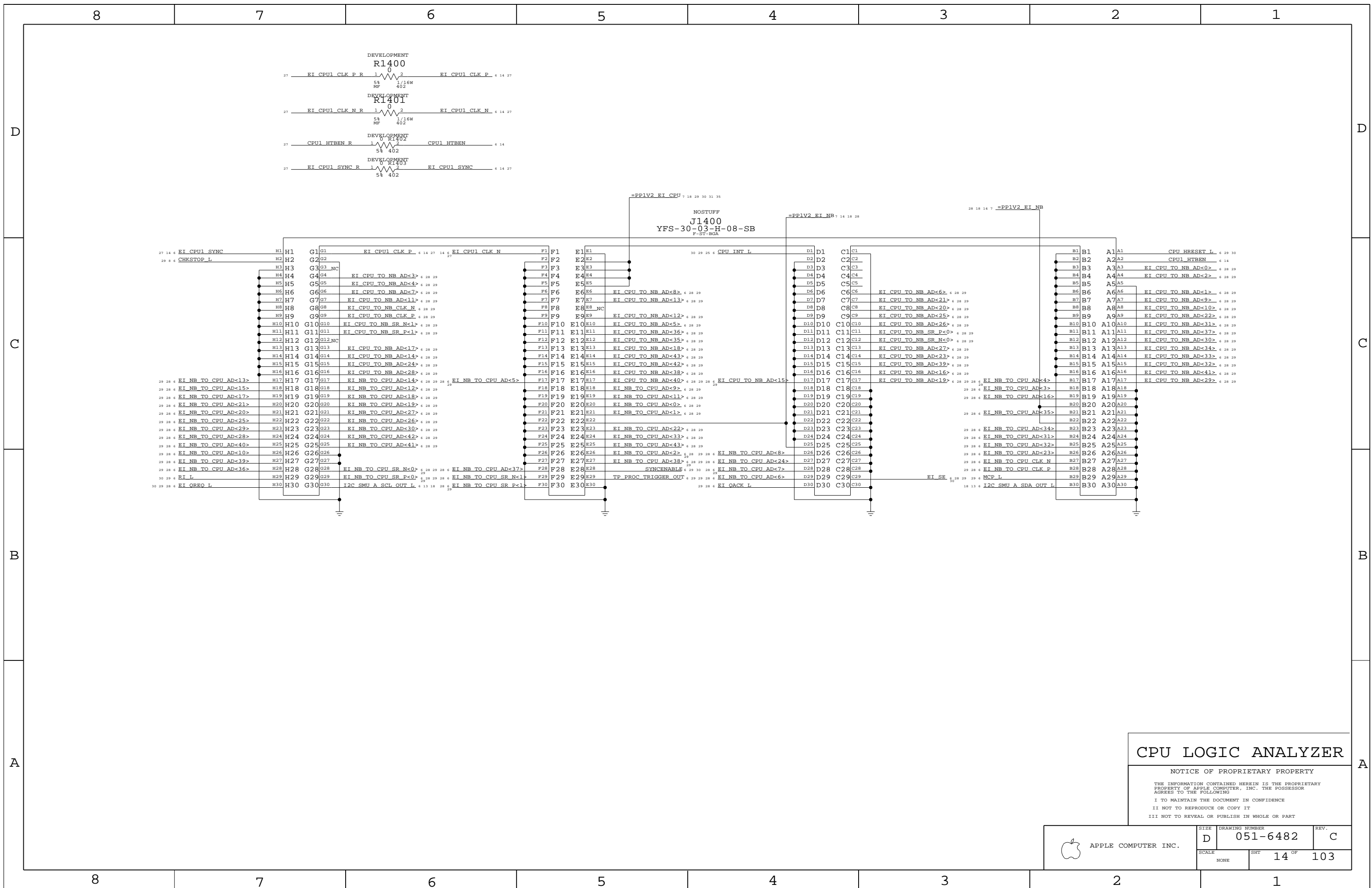
### System Management Unit

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		SHEET	13 OF 103



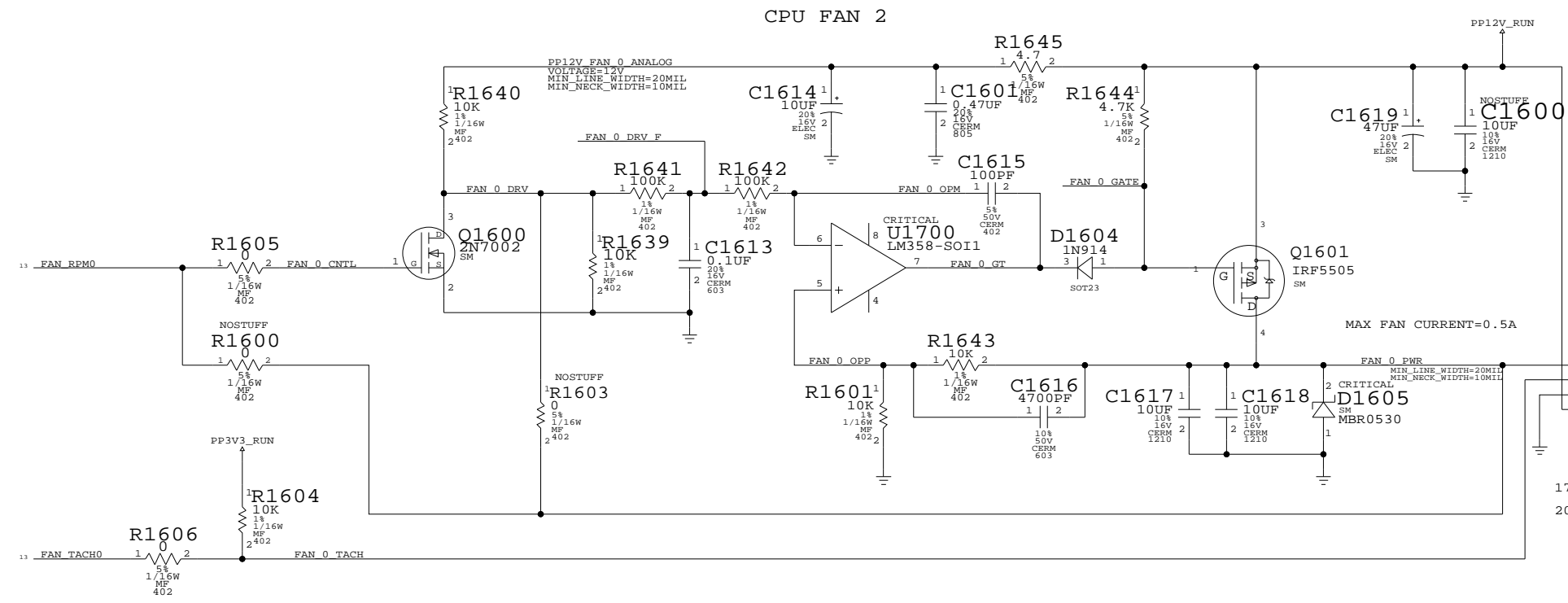
# CPU LOGIC ANALYZER

## NOTICE OF PROPRIETARY PROPERTY

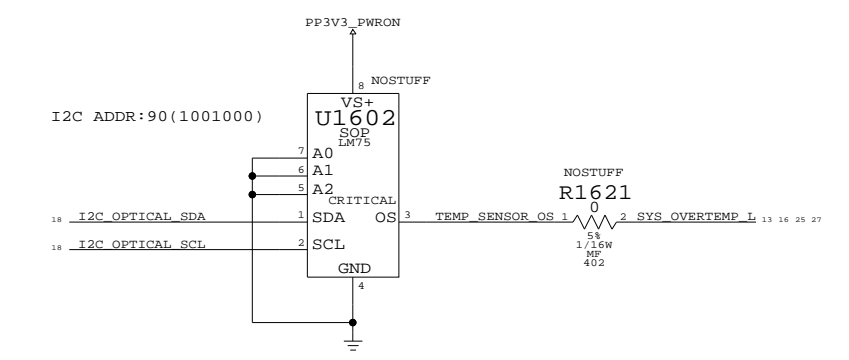
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	SCALE NONE	SHT 14 OF 103	

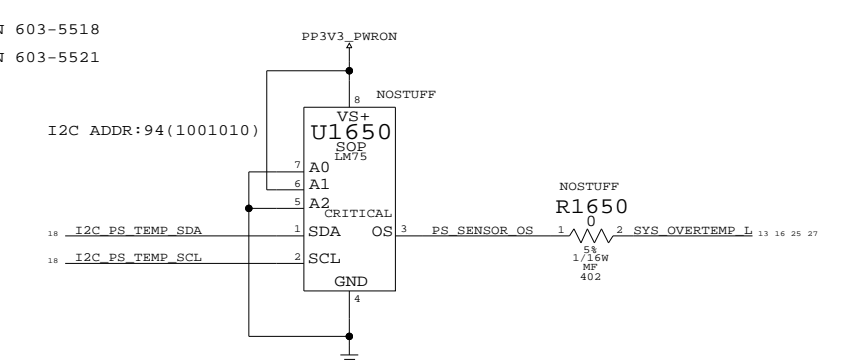
### FAN 1 - Q37 STYLE CPU FAN CONTROL CIRCUIT



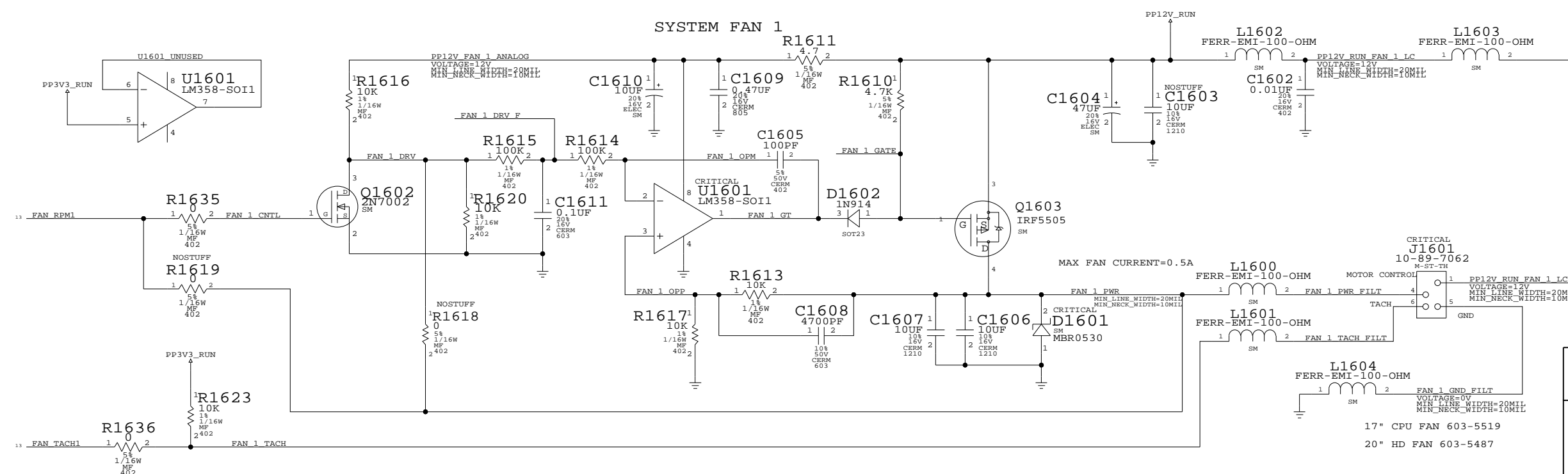
### OPTICAL TEMP SENSOR



### POWER SUPPLY TEMP SENSOR



### FAN 2 - Q37 STYLE CPU FAN CONTROL CIRCUIT



### FAN 1, 2 & SYSTEM TEMP

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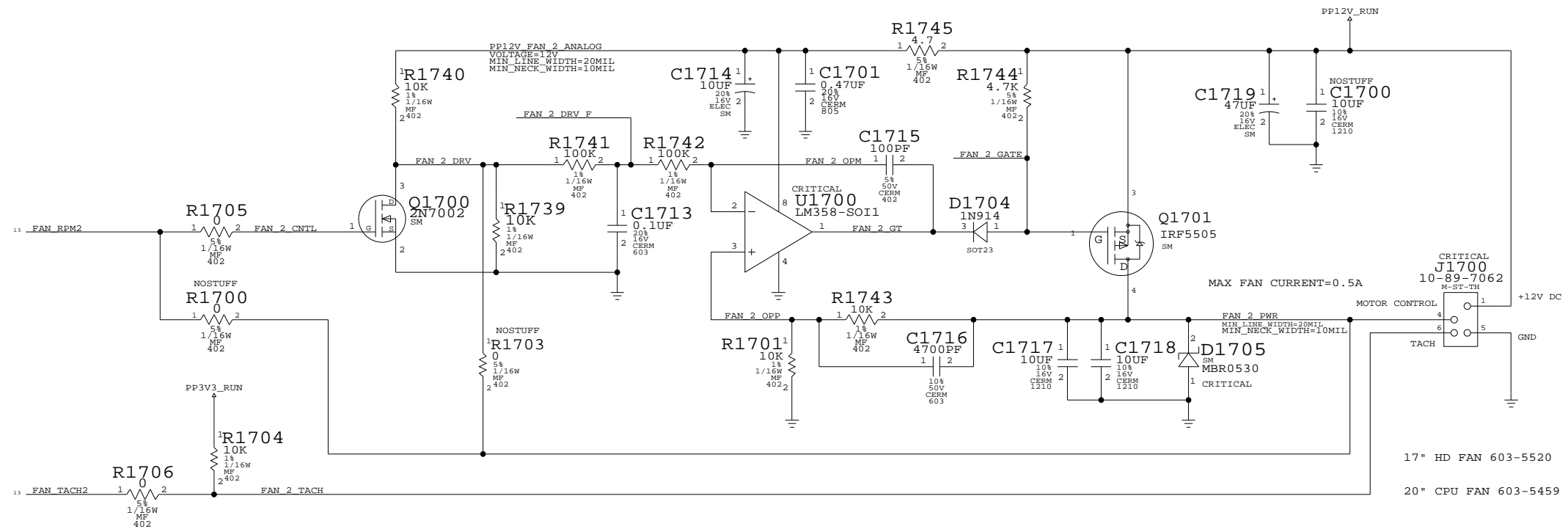
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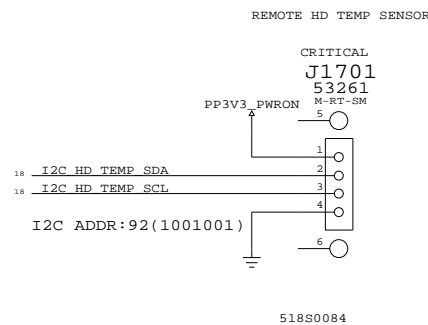
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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		16	103

# FAN 3 - Q37 STYLE SYSTEM FAN CONTROL CIRCUIT



17" HD FAN 603-5520  
20" CPU FAN 603-5459

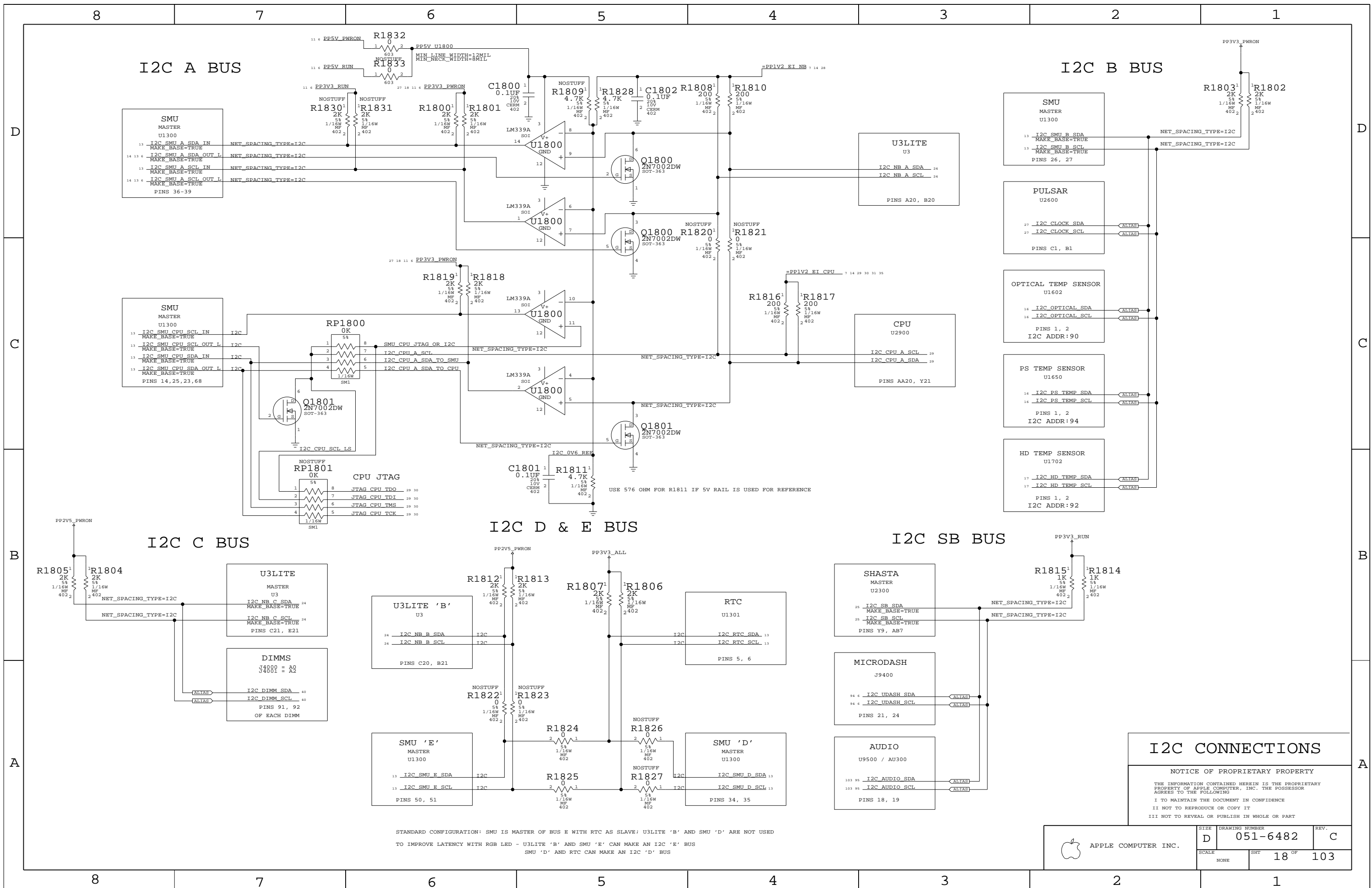
## REMOTE HARD DRIVE TEMP SENSOR



### FAN 3 & HD TEMP

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	D	051-6482	C
SCALE	SHT	17 OF	103
NONE			



I2C A BUS

I2C B BUS

I2C C BUS

I2C D & E BUS

I2C SB BUS

I2C CONNECTIONS

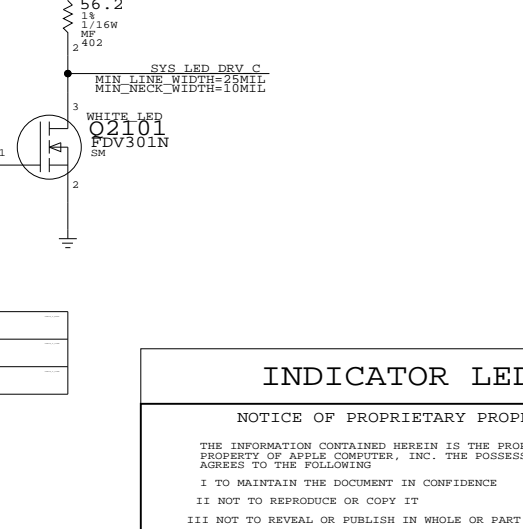
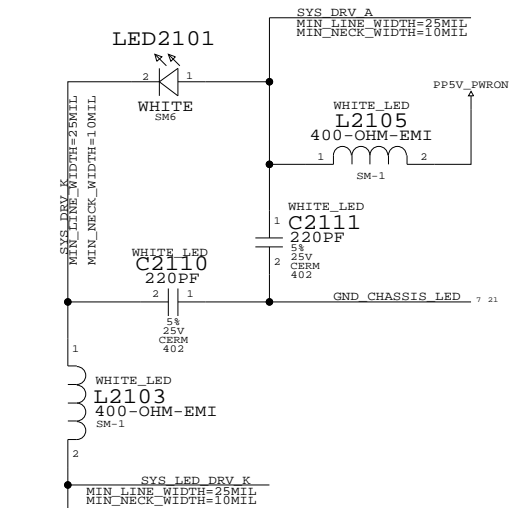
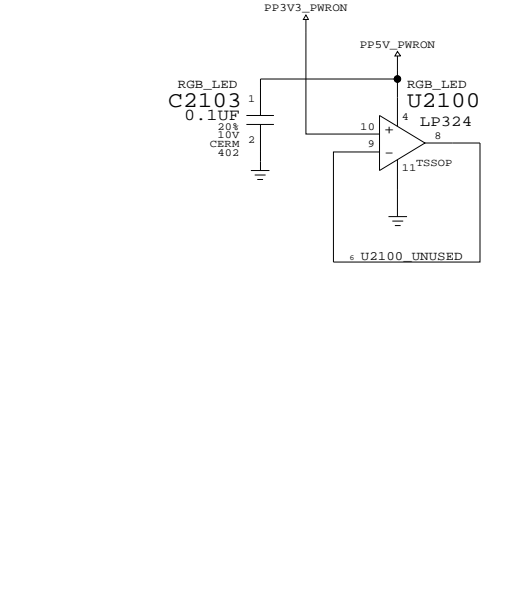
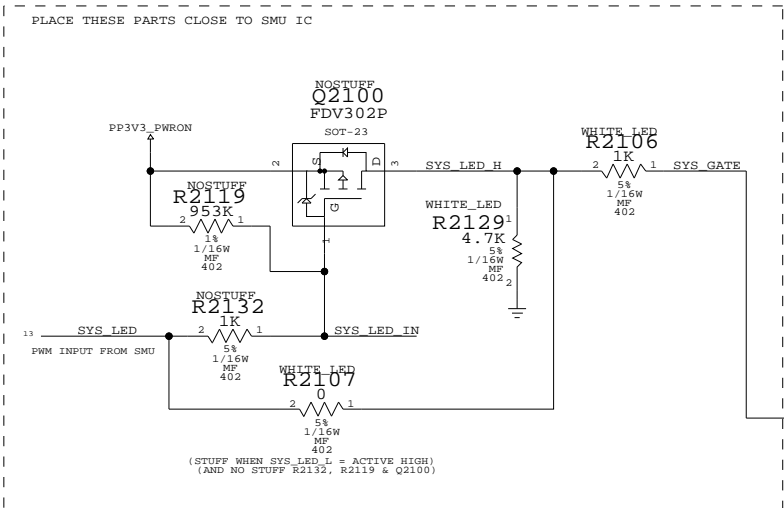
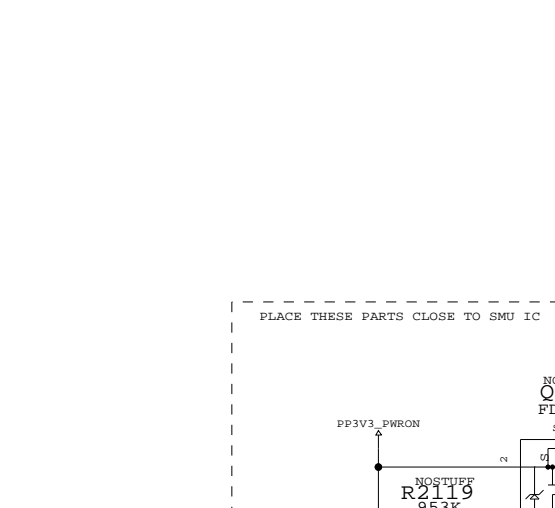
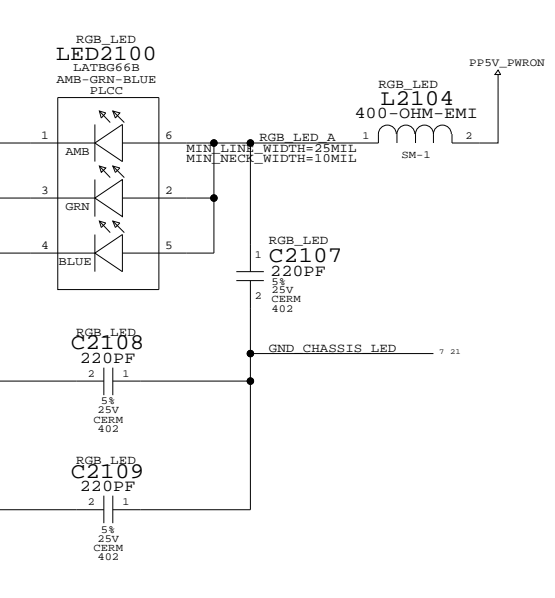
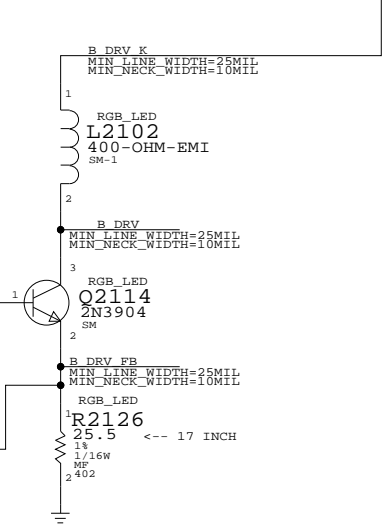
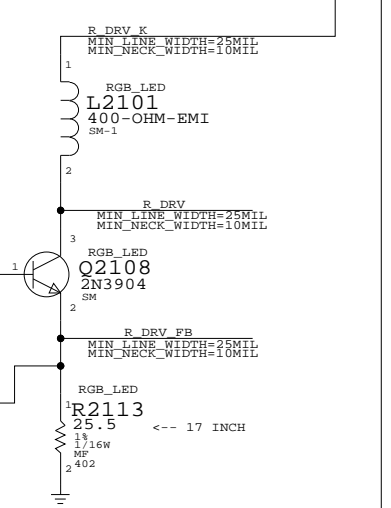
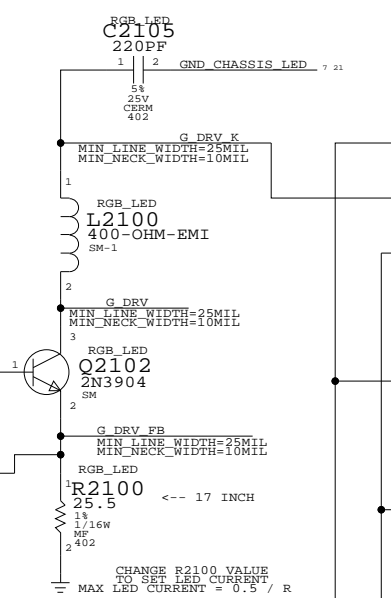
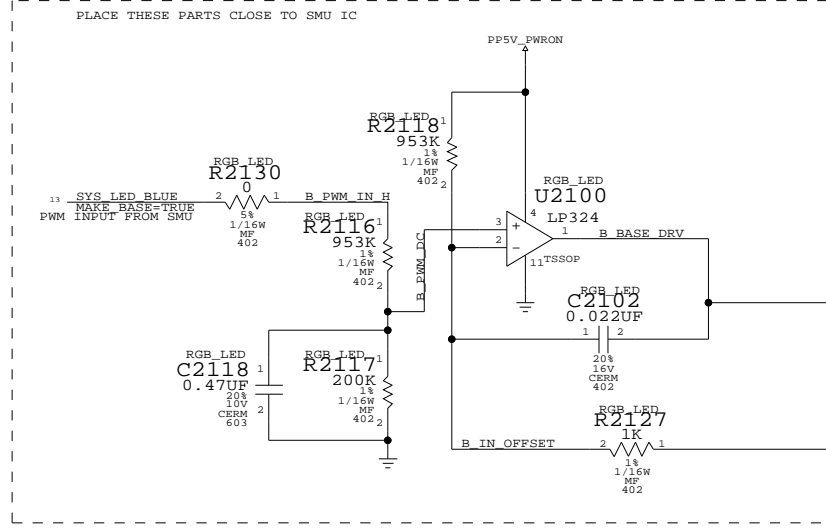
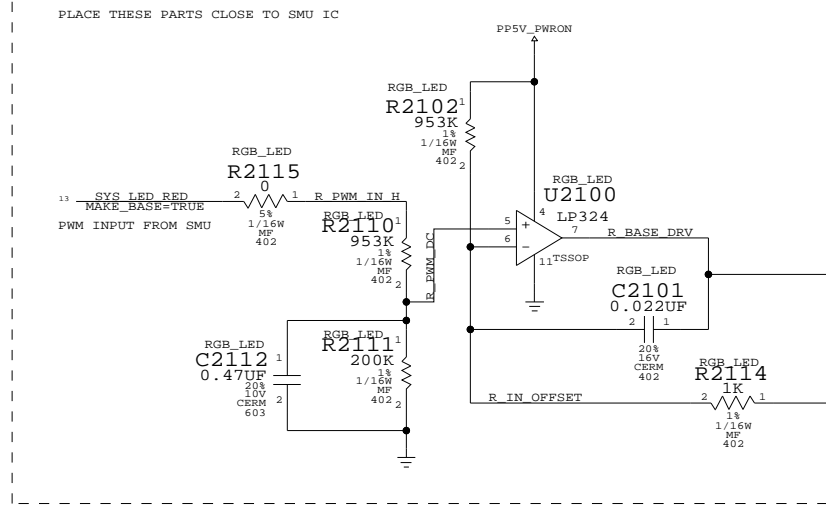
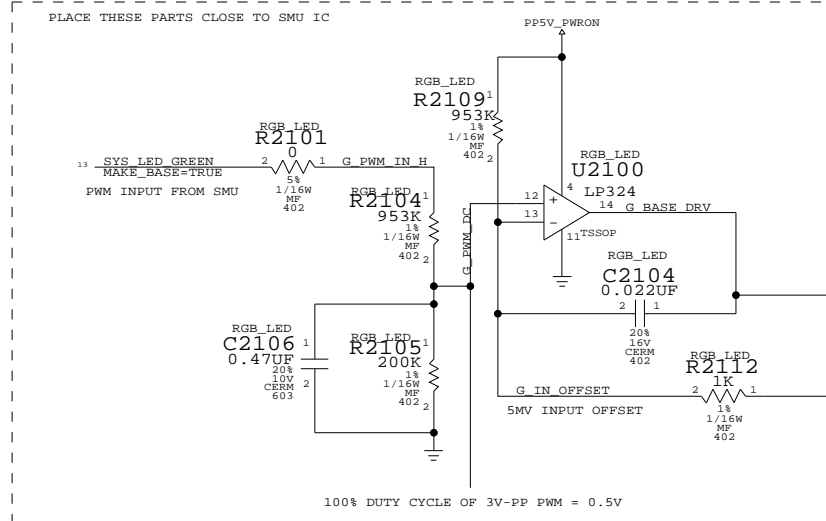
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STANDARD CONFIGURATION: SMU IS MASTER OF BUS E WITH RTC AS SLAVE; U3LITE 'B' AND SMU 'D' ARE NOT USED  
 TO IMPROVE LATENCY WITH RGB LED - U3LITE 'B' AND SMU 'E' CAN MAKE AN I2C 'E' BUS  
 SMU 'D' AND RTC CAN MAKE AN I2C 'D' BUS

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	18 OF	103
NONE			



TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11483921	1	RES, 39.2 OHM, 1%, 402	R2103	20_INCH_LCD
11481821	3	RES, 18.2 OHM, 1%, 402	R2100, R2113, R2126	NOSTUFF

**INDICATOR LED**

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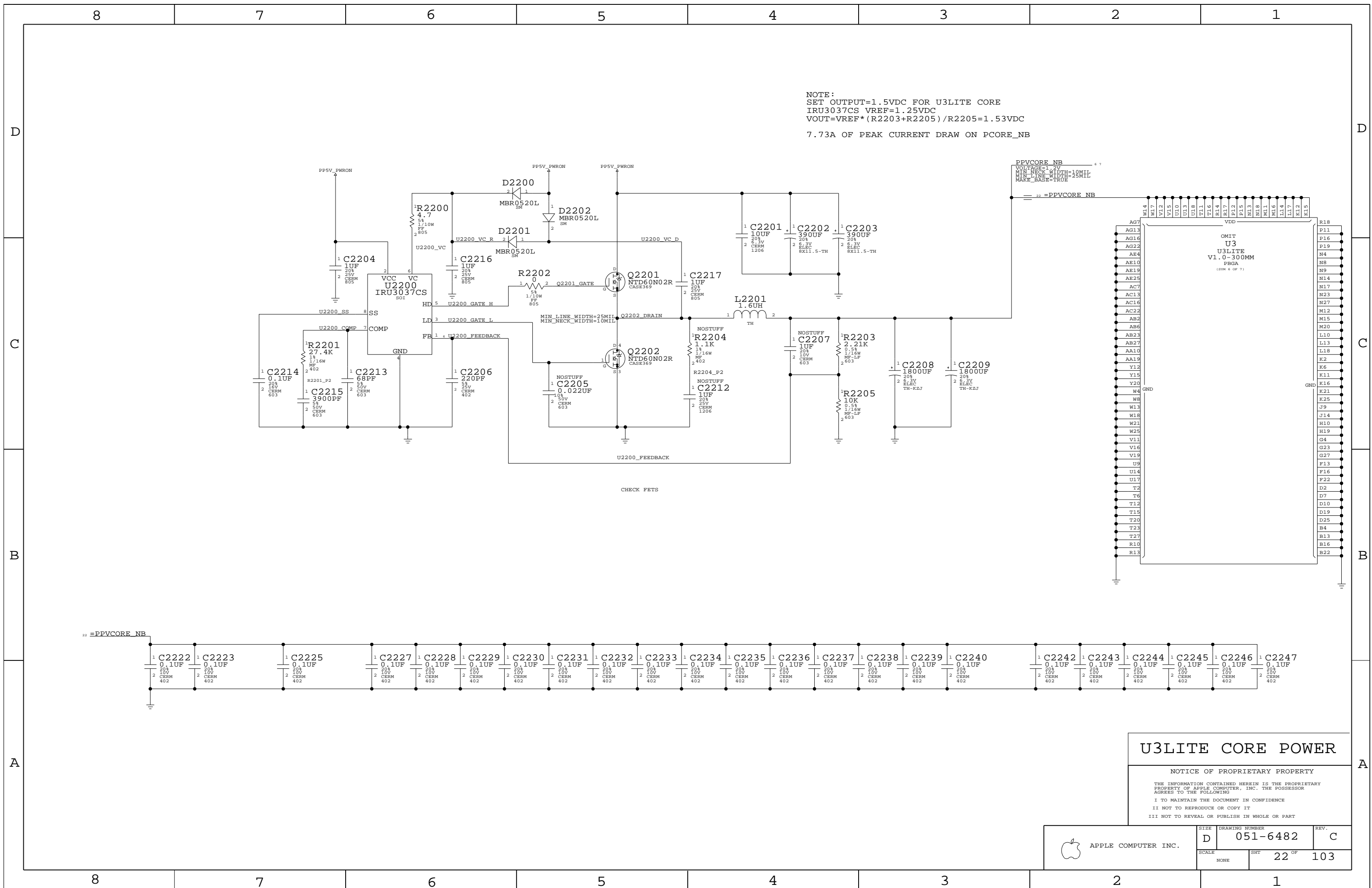
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APPLE COMPUTER INC.

SCALE	DRAWING NUMBER	REV.
NONE	D 051-6482	C
SHT	21 OF	103



NOTE:  
 SET OUTPUT=1.5VDC FOR U3LITE CORE  
 IRU3037CS VREF=1.25VDC  
 $V_{OUT} = V_{REF} * (R_{2203} + R_{2205}) / R_{2205} = 1.53VDC$   
 7.73A OF PEAK CURRENT DRAW ON PCORE\_NB

PPVCORE\_NB  
 VOLTAGE=1.2V  
 MIN\_PCK\_WIDTH=10MIL  
 MIN\_LINE\_WIDTH=25MIL  
 MAKE\_BASE=TRUE

CHECK FETS

### U3LITE CORE POWER

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	D	051-6482	C
SCALE	NONE	SHT	22 OF 103

# Page Notes

Power aliases required by this page:

- \_PPPCI64\_PWRON\_SB (to 5V or 3.3V)
- \_PPPCI32\_PWRON\_SB (to 5V or 3.3V)
- \_PP3V3\_PWRON\_SB
- \_PP2V5\_PWRON\_SB
- \_PPVCORE\_PWRON\_SB (1.2V)

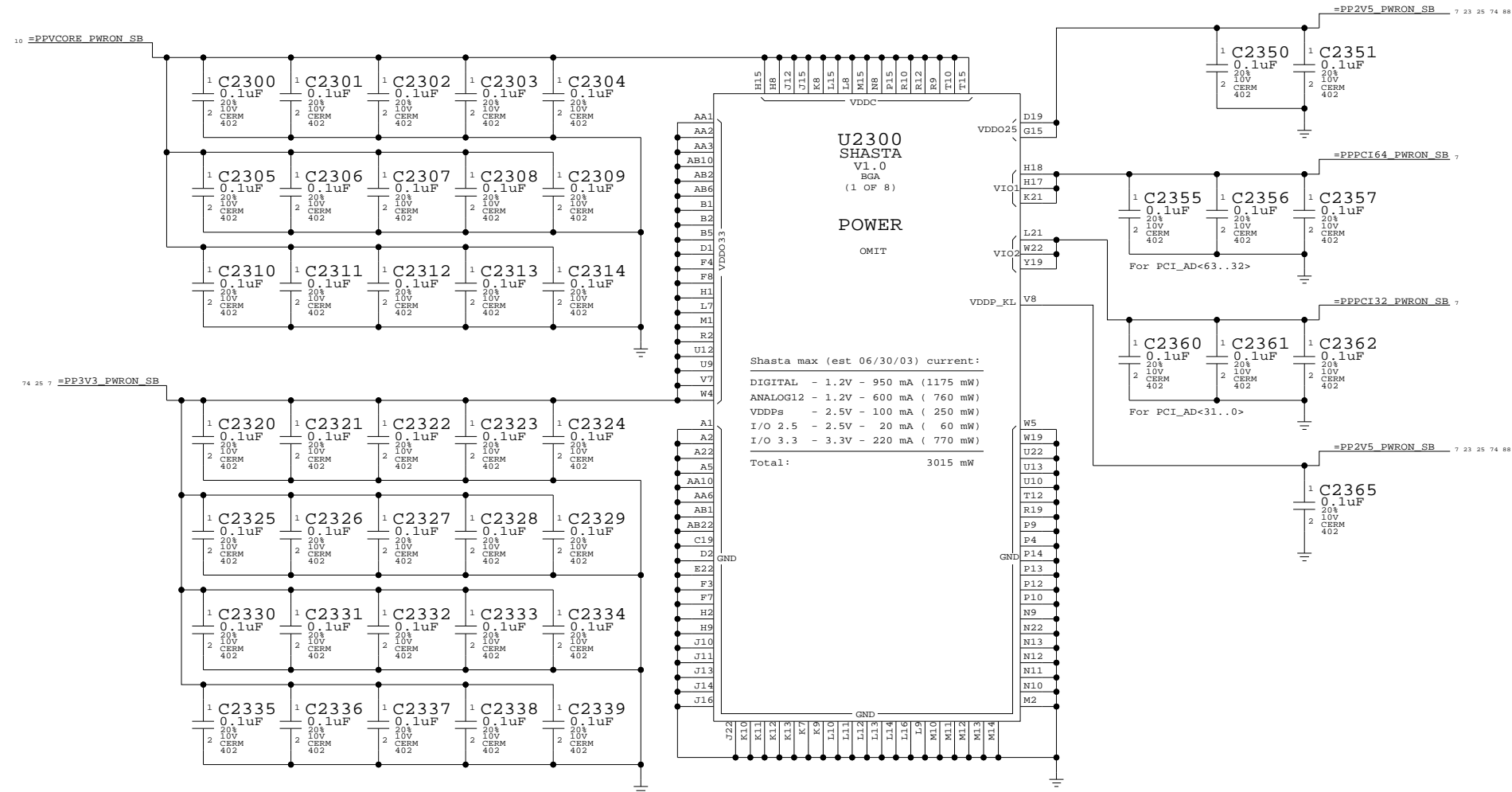
NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect \_PPPCI32\_PWRON\_SB to appropriate PCI bus voltage and \_PPPCI64\_PWRON\_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

**Power Sequencing:**

Must power Shasta VCore rail before any other Shasta supplies.



Master: Link

## Shasta Core Power

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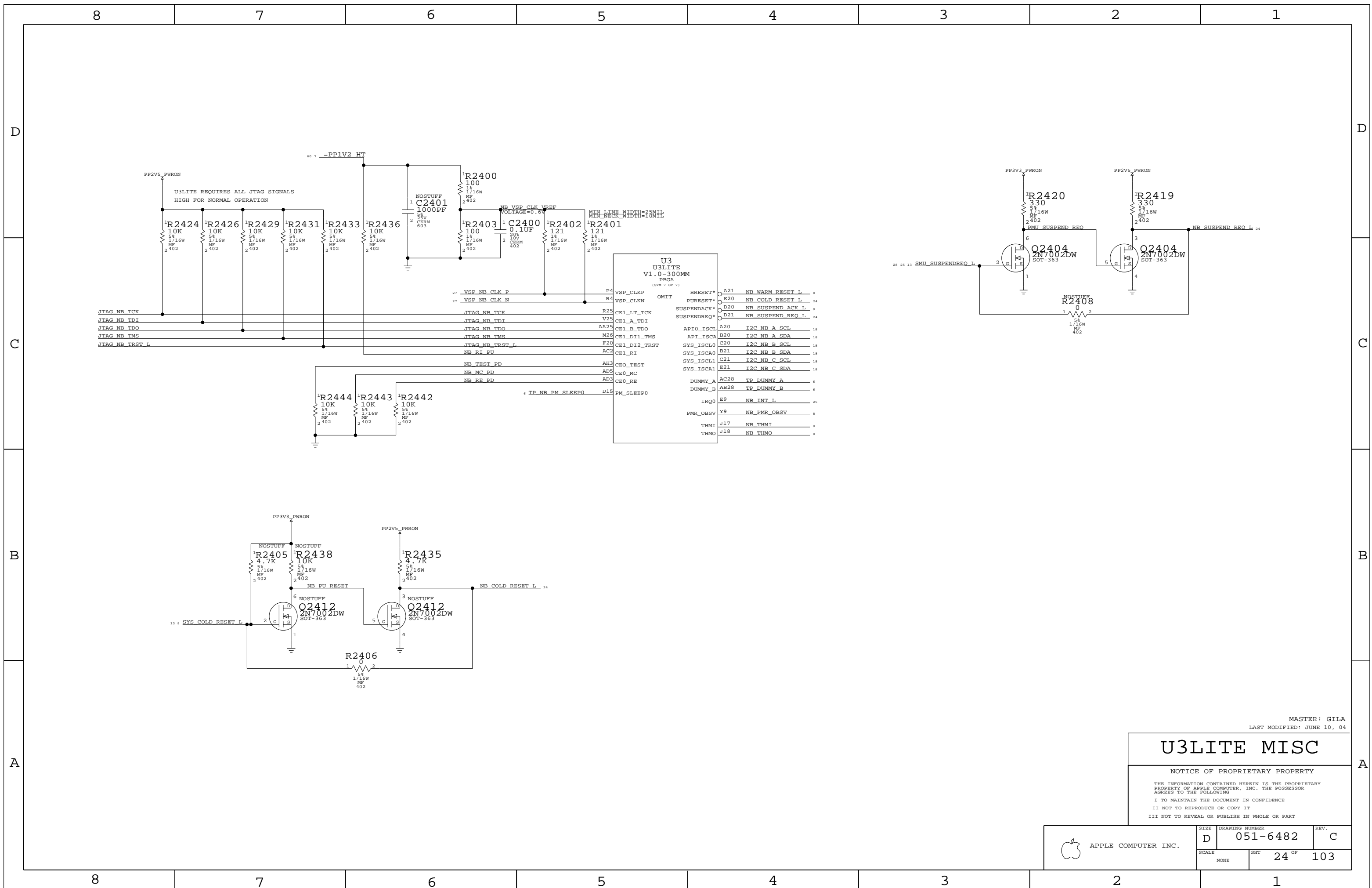
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D	051-6482	C
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NONE	23	103



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LAST MODIFIED: JUNE 10, 04

# U3LITE MISC

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	D	051-6482	C
SCALE	SHT	24 OF 103	
NONE			

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		I2S0_DEV_TO_SB DTI
I2S0_TO_DEV		I2S0_SB_TO_DEV DTO
I2S0_TO_DEV	AUDIO	I2S0_MCLK
I2S0_BIDIR		I2S0_BITCLK
I2S0_BIDIR		I2S0_SYNC
I2S1_TO_SB		I2S1_DEV_TO_SB DTI
I2S1_TO_DEV		I2S1_SB_TO_DEV DTO
I2S1_TO_DEV	10 MIL SPACING	I2S1_MCLK
I2S1_BIDIR		I2S1_BITCLK
I2S1_BIDIR		I2S1_SYNC
I2S2_TO_SB		I2S2_DEV_TO_SB DTI
I2S2_TO_DEV		I2S2_SB_TO_DEV DTO
I2S2_TO_DEV	10 MIL SPACING	I2S2_MCLK
I2S2_BIDIR		I2S2_BITCLK
I2S2_BIDIR		I2S2_SYNC
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALI
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALO
SB_CLK18M_XTAL	15 MIL SPACING	SB_CLK18M_XTALO_R
SB_CLK25M_ATA	15 MIL SPACING	SB_CLK25M_ATA

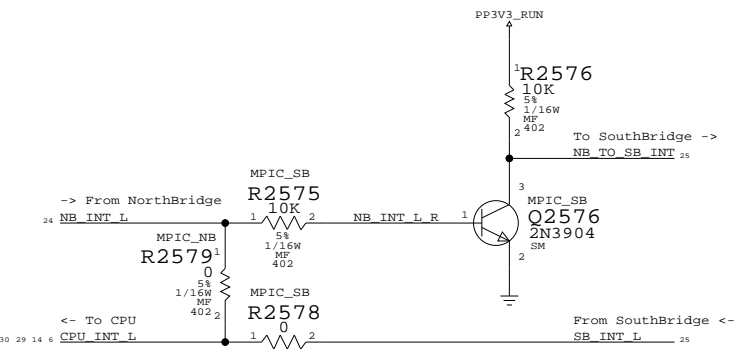
### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PCI  
 - \_PP3V3\_PWRON\_SB  
 - \_PP2V5\_PWRON\_SB  
 - \_PP1V2\_PWRON\_SB

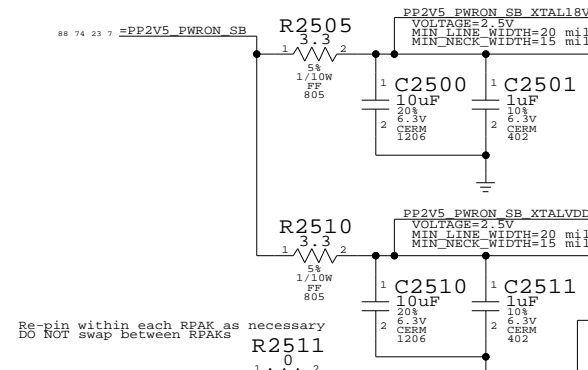
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - PCI\_64BIT  
 Configures Shasta for 64-bit PCI  
 NOTE: XGC required for Shasta GPIOs  
 - MPIC\_NB/MPIC\_SB  
 Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

### NorthBridge / SouthBridge MPIC Routing

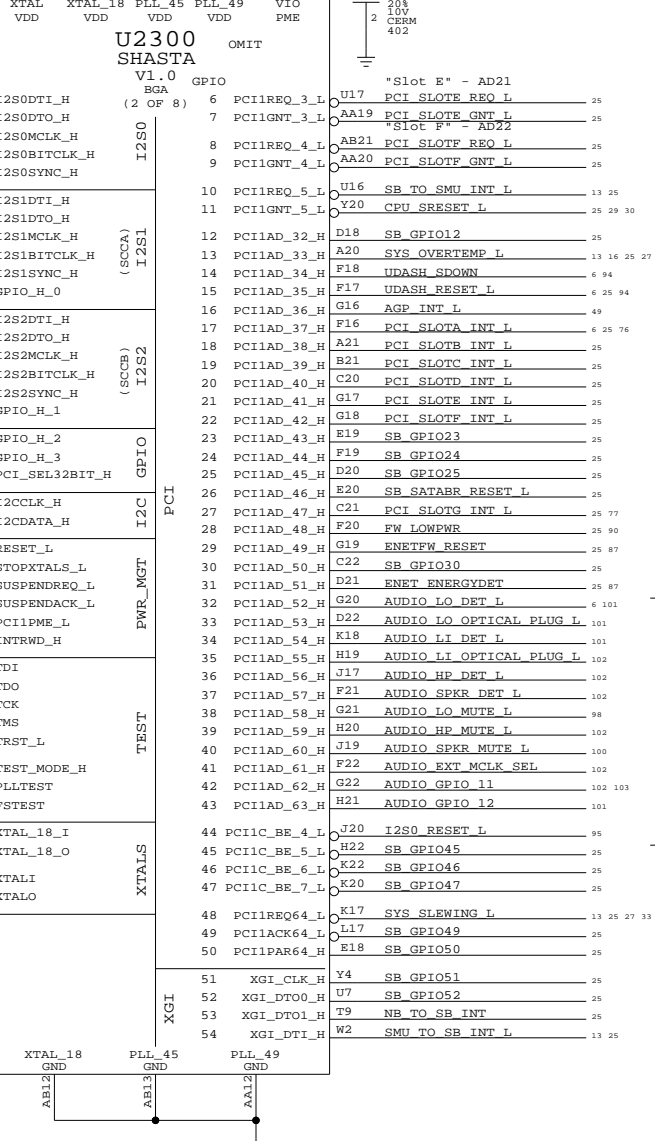
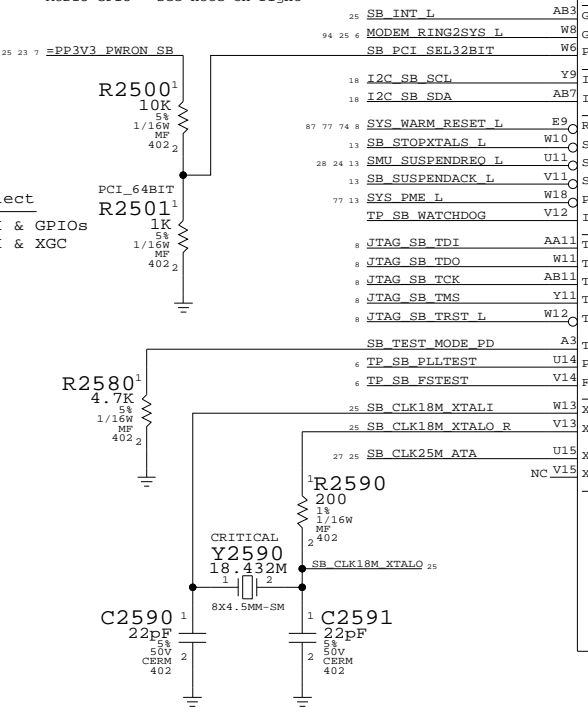


I2S1: Soft Modem  
 I2S2: S/P-D/F

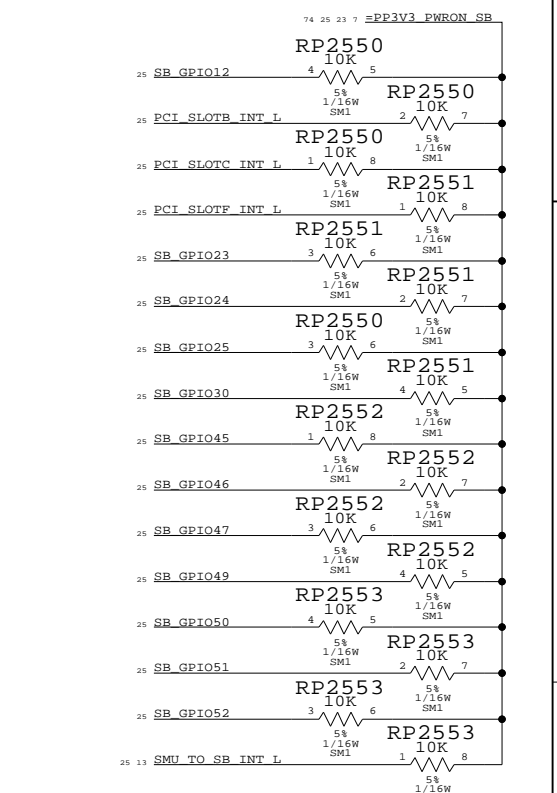
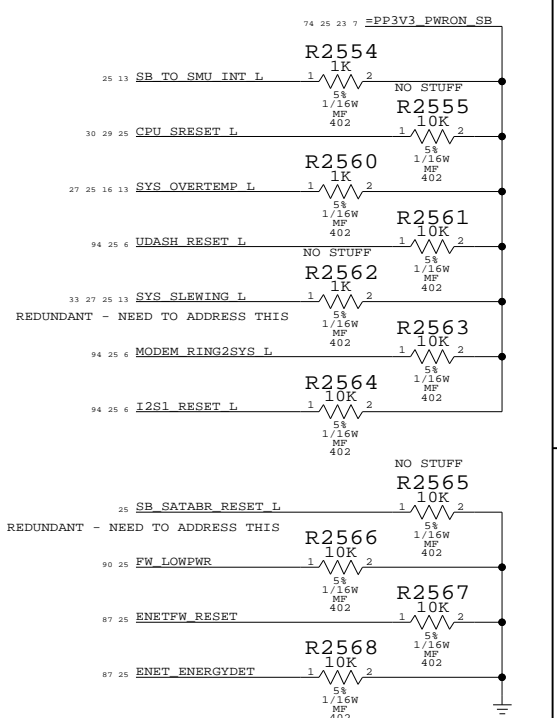
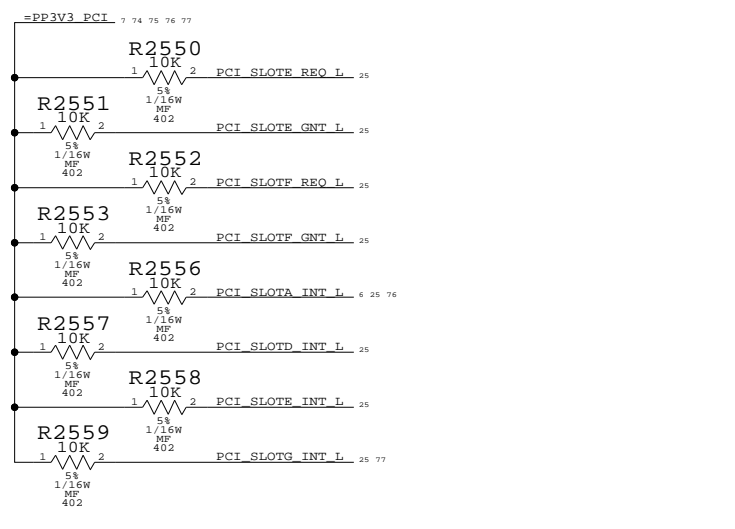


Re-pin with each RPAK as necessary  
 DO NOT swap between RPAKS

Pin	Signal	Component
95 25	I2S0_DEV_TO_SB DTI	RP2510
103 95 25	I2S0_SB_TO_DEV DTO	RP2510
102 25	I2S0_MCLK	RP2510
103 102 25	I2S0_BITCLK	RP2510
103 95 25	I2S0_SYNC	RP2510
94 76 25 6	I2S1_DEV_TO_SB DTI	RP2520
94 76 25 6	I2S1_SB_TO_DEV DTO	RP2520
94 76 25 6	I2S1_MCLK	RP2520
94 25 6	I2S1_BITCLK	RP2520
94 25 6	I2S1_SYNC	RP2520
94 25 6	I2S1_RESET L	RP2520
102 25	I2S2_DEV_TO_SB DTI	RP2530
102 25	I2S2_SB_TO_DEV DTO	RP2530
102 25	I2S2_MCLK	RP2530
102 25	I2S2_BITCLK	RP2530
102 25	I2S2_SYNC	RP2530
102	I2S2_RESET L	RP2530



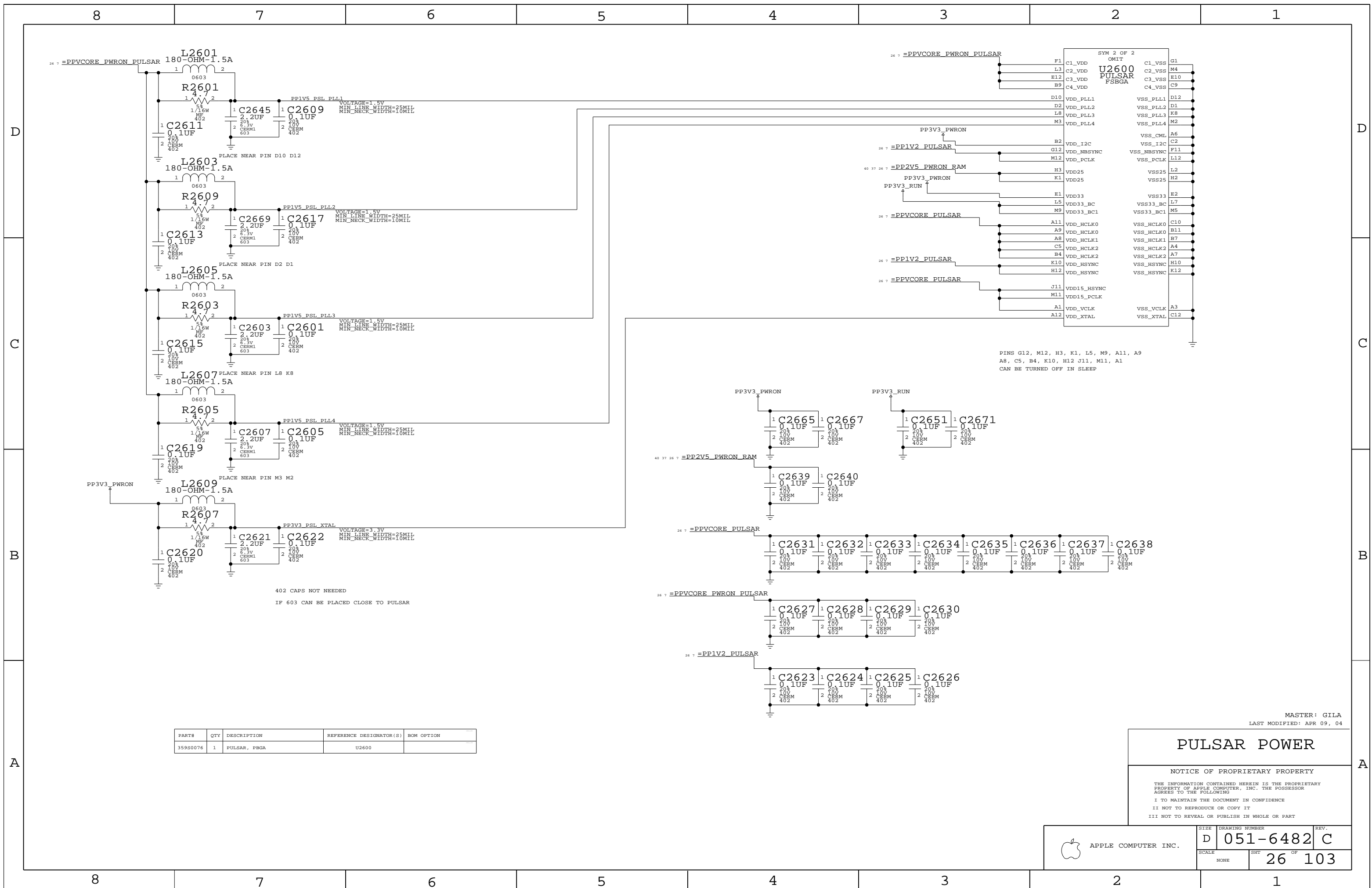
**AUDIO GPIOs**  
 NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.



Master: Link

### Shasta Serial / Misc

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PINS G12, M12, H3, K1, L5, M9, A11, A9, A8, C5, B4, K10, H12 J11, M11, A1 CAN BE TURNED OFF IN SLEEP

402 CAPS NOT NEEDED  
IF 603 CAN BE PLACED CLOSE TO PULSAR

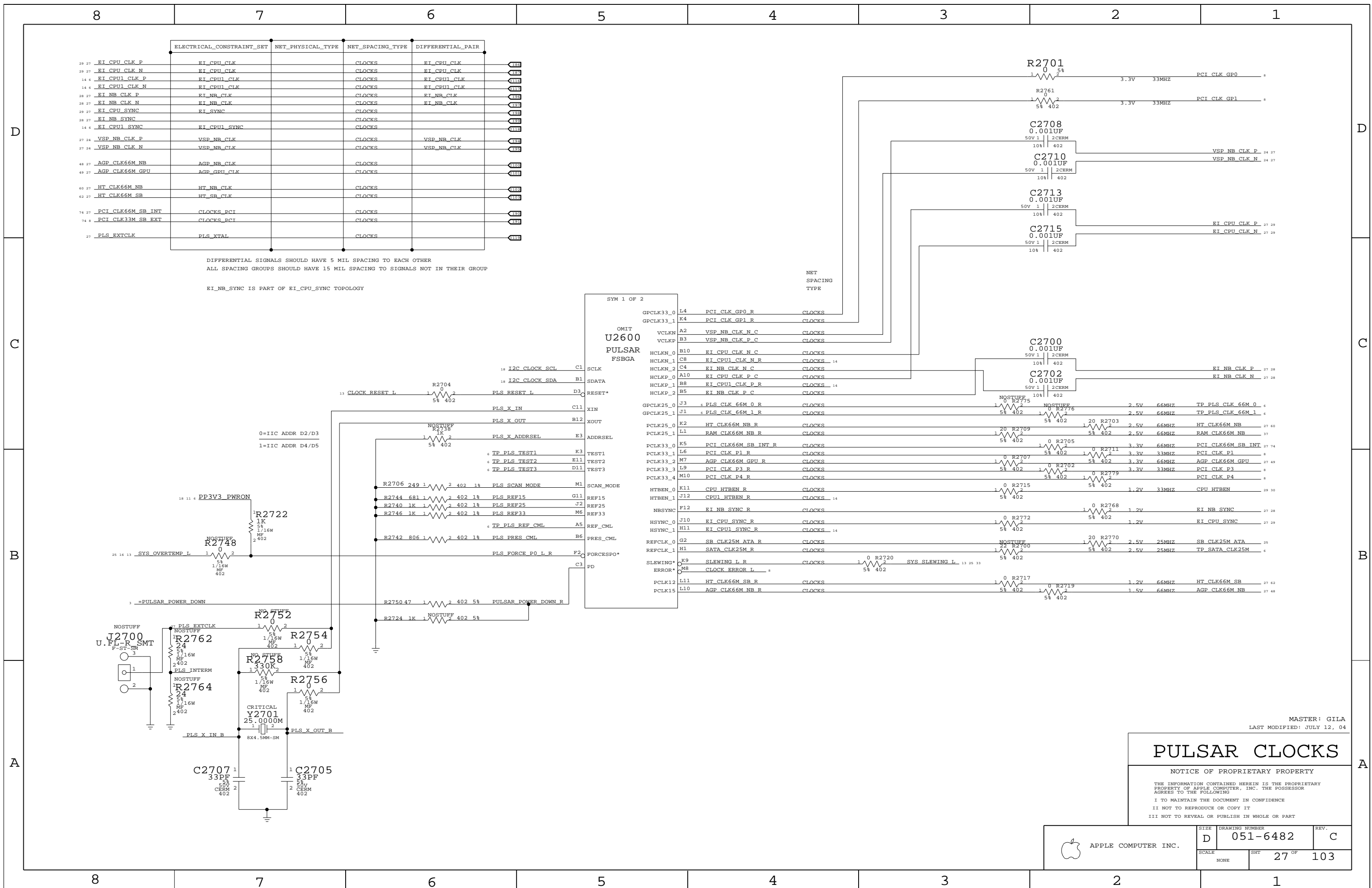
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, FBGA	U2600	

MASTER: GILA  
LAST MODIFIED: APR 09, 04

### PULSAR POWER

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	NONE	051-6482	C
SCALE		SHEET	
NONE		26 OF 103	



MASTER: GILA  
LAST MODIFIED: JULY 12, 04

# PULSAR CLOCKS

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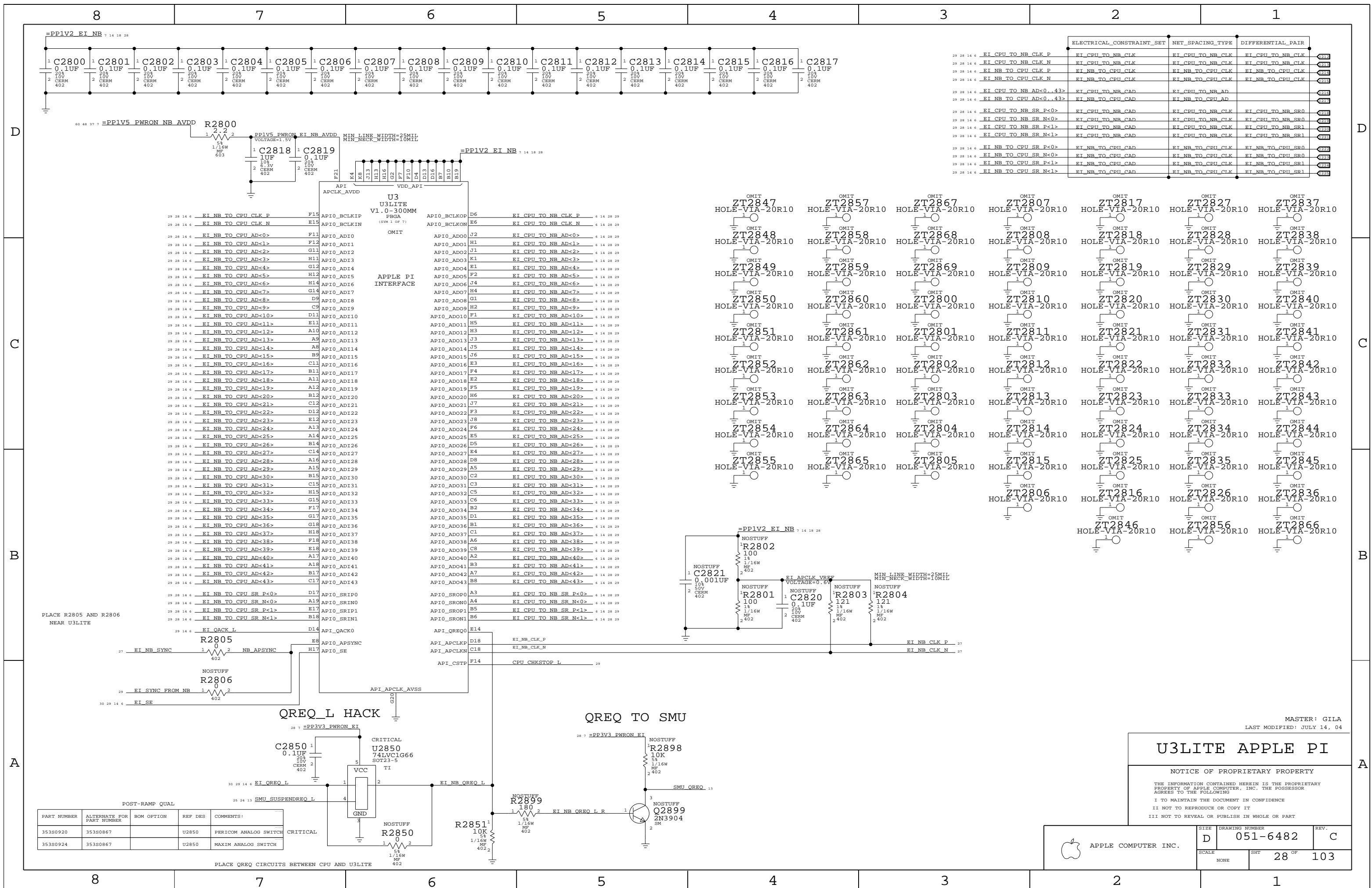
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	D	051-6482	C
SCALE	NONE	SHT	27 OF 103



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD
EI_CPU_TO_NB_SR<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR<N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_SR0
EI_CPU_TO_NB_SR<P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_SR1
EI_CPU_TO_NB_SR<N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_SR1
EI_NB_TO_CPU_SR<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR<N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR0
EI_NB_TO_CPU_SR<P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR1
EI_NB_TO_CPU_SR<N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_SR1

PLACE R2805 AND R2806 NEAR U3LITE

QREQ\_L HACK

QREQ TO SMU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35380920	35380867		U2850	PERICOM ANALOG SWITCH
35380924	35380867		U2850	MAXIM ANALOG SWITCH

PLACE QREQ CIRCUITS BETWEEN CPU AND U3LITE

MASTER: GILA  
LAST MODIFIED: JULY 14, 04

**U3LITE APPLE PI**

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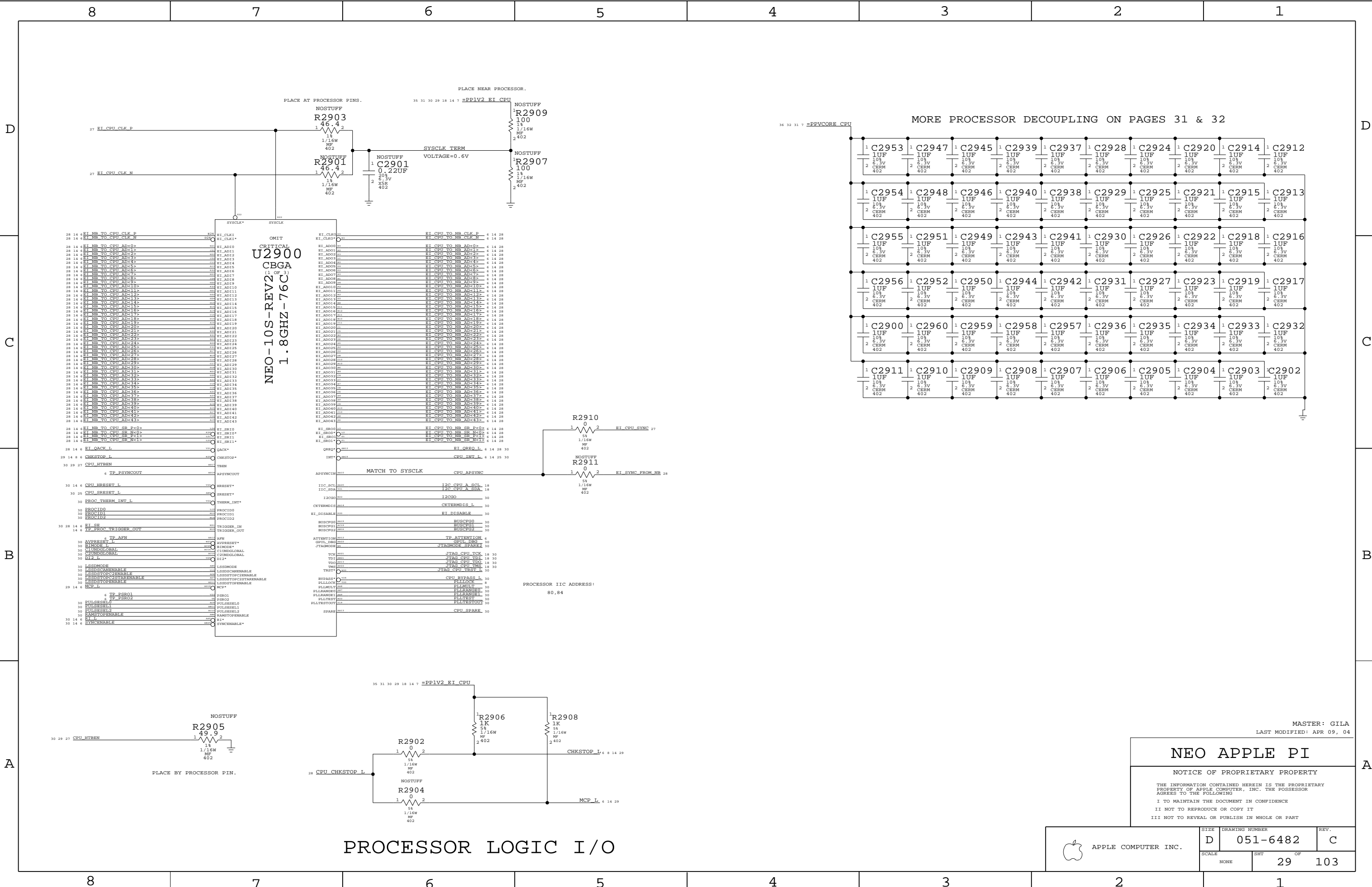
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	D	051-6482	C
SCALE	SHEET	28 OF 103	
NONE			





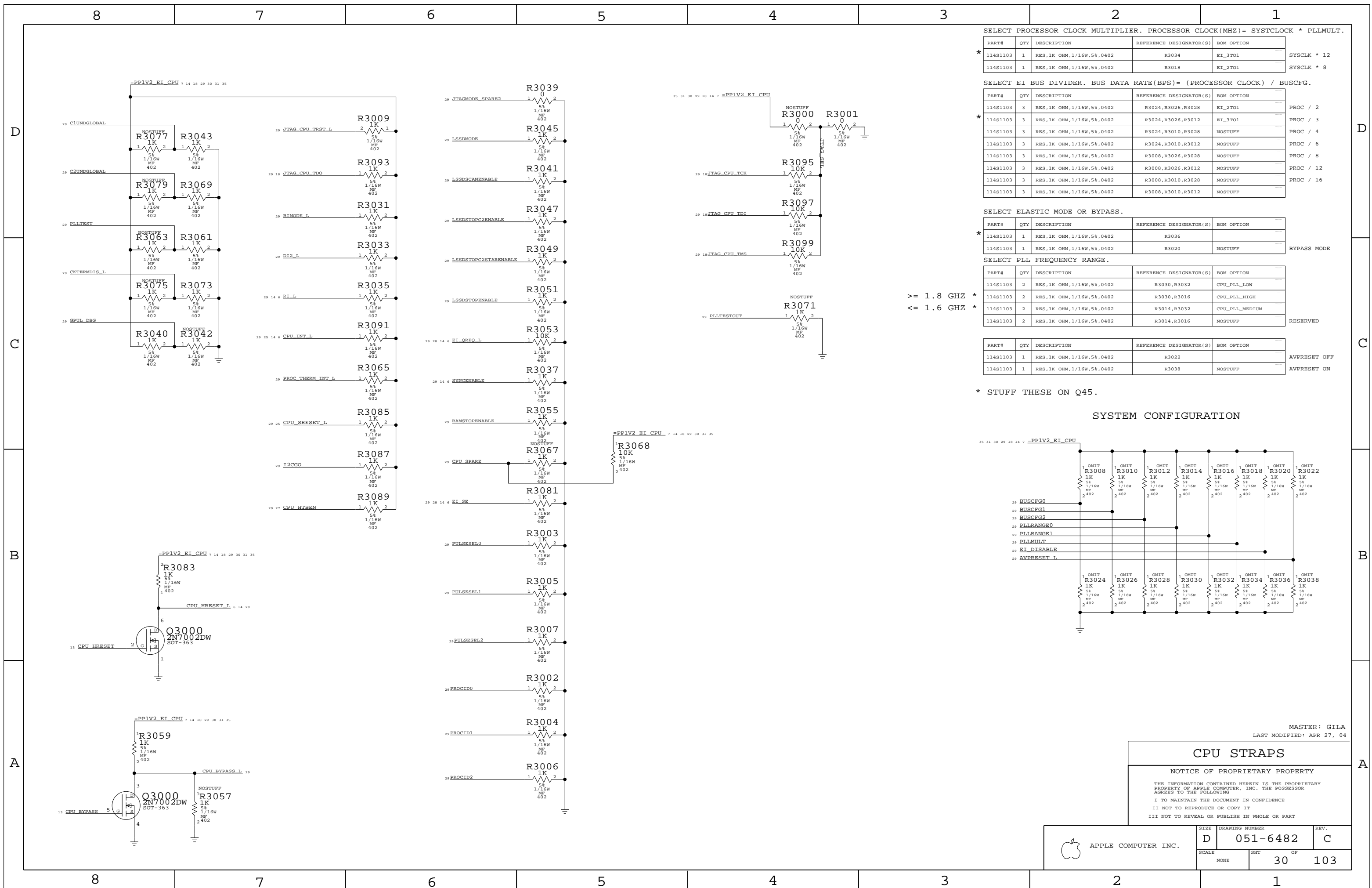
CRITICAL  
U2900  
(1 OF 1)  
CBGA  
NEO-10S-REV2  
1.8GHZ-76C

# PROCESSOR LOGIC I/O

MASTER: GILA  
LAST MODIFIED: APR 09, 04

NEO APPLE PI  
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6482	REV. C
	SCALE NONE	SHT 29 OF	103



SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK \* PLLMULT.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
* 114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3T01
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2T01

SYSCLK \* 12  
SYSCLK \* 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2T01
* 114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3T01
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF
114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF

PROC / 2  
PROC / 3  
PROC / 4  
PROC / 6  
PROC / 8  
PROC / 12  
PROC / 16

SELECT ELASTIC MODE OR BYPASS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
* 114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF

BYPASS MODE

SELECT PLL FREQUENCY RANGE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW
* 114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF

RESERVED

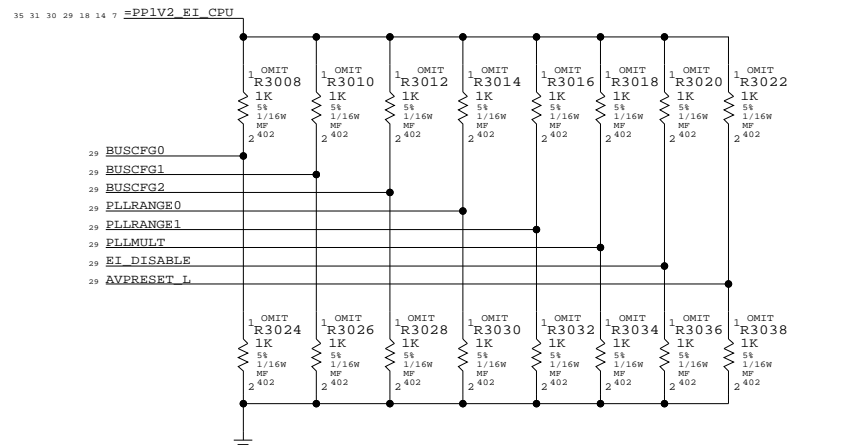
>= 1.8 GHZ \*  
<= 1.6 GHZ \*

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022	AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	AVPRESET ON

AVPRESET OFF  
AVPRESET ON

\* STUFF THESE ON Q45.

SYSTEM CONFIGURATION



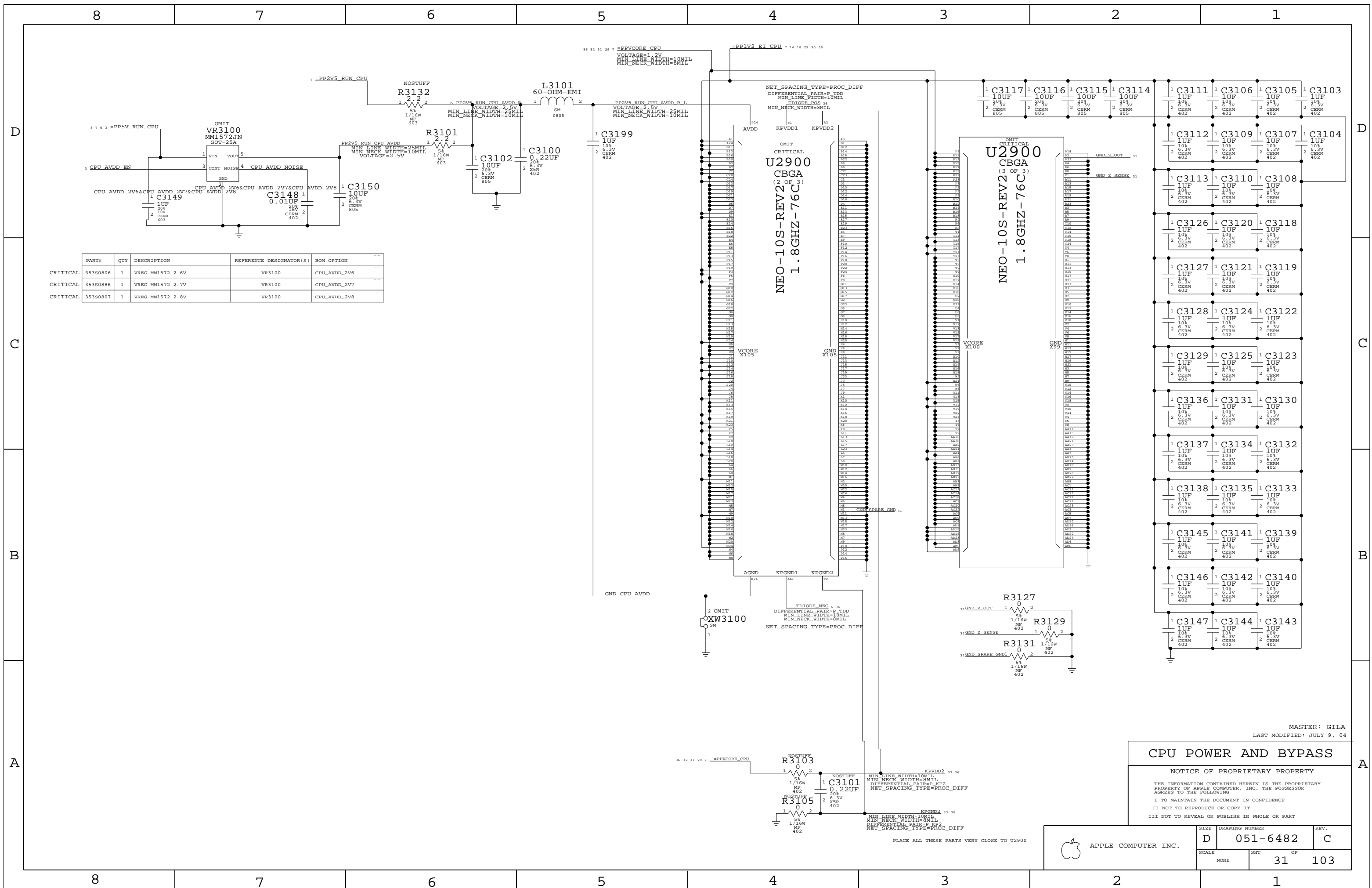
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CPU STRAPS

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	D	051-6482	C
SCALE	SHT	OF	
NONE	30	103	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL 353S0806	1	VREG MM1572 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL 353S0886	1	VREG MM1572 2.7V	VR3100	CPU_AVDD_2V7
CRITICAL 353S0807	1	VREG MM1572 2.8V	VR3100	CPU_AVDD_2V8

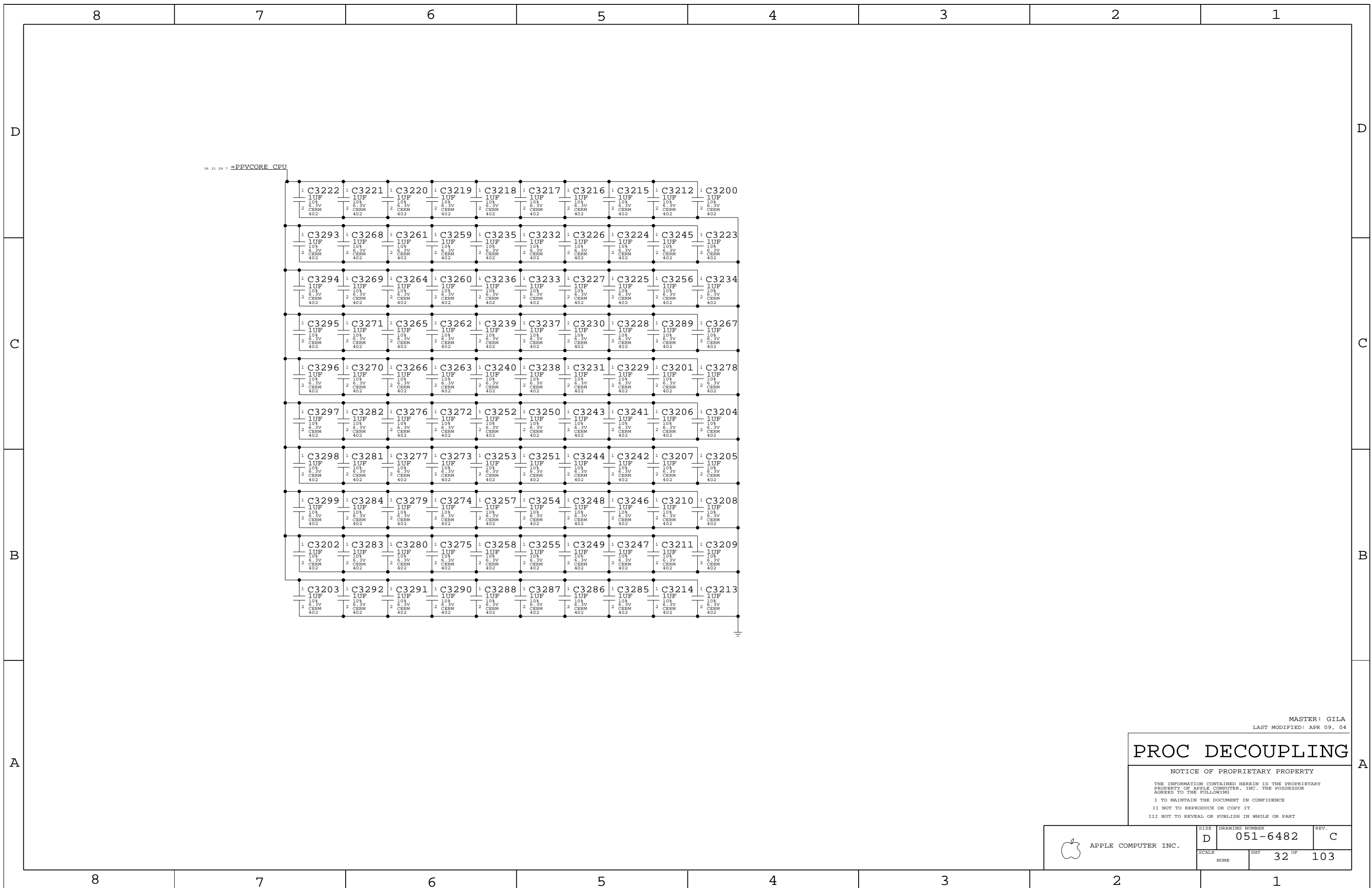
MASTER: GILA  
LAST MODIFIED: JULY 9, 04

### CPU POWER AND BYPASS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHEET		OF
NONE	31		103


PLACE ALL THESE PARTS VERY CLOSE TO U2900



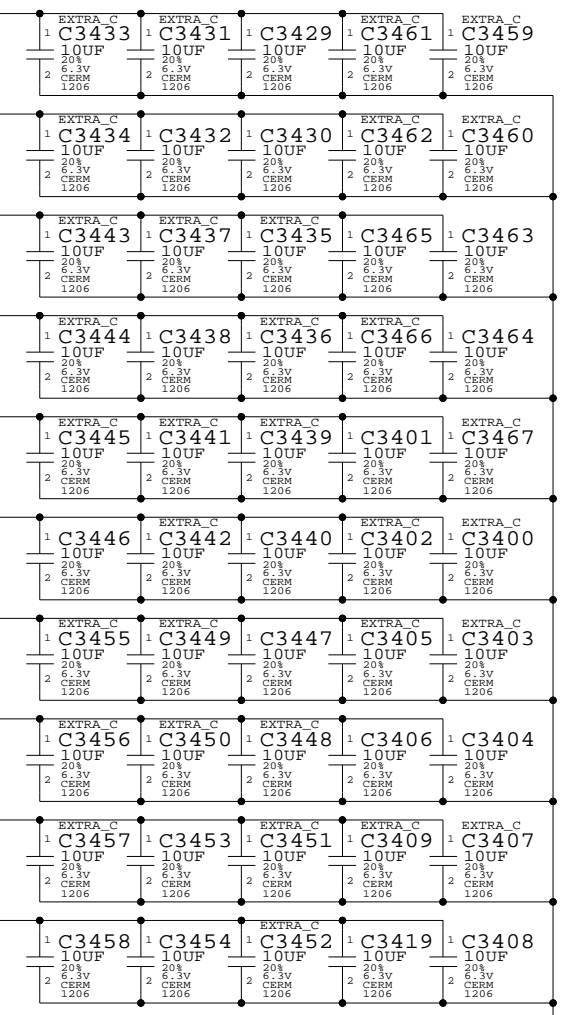
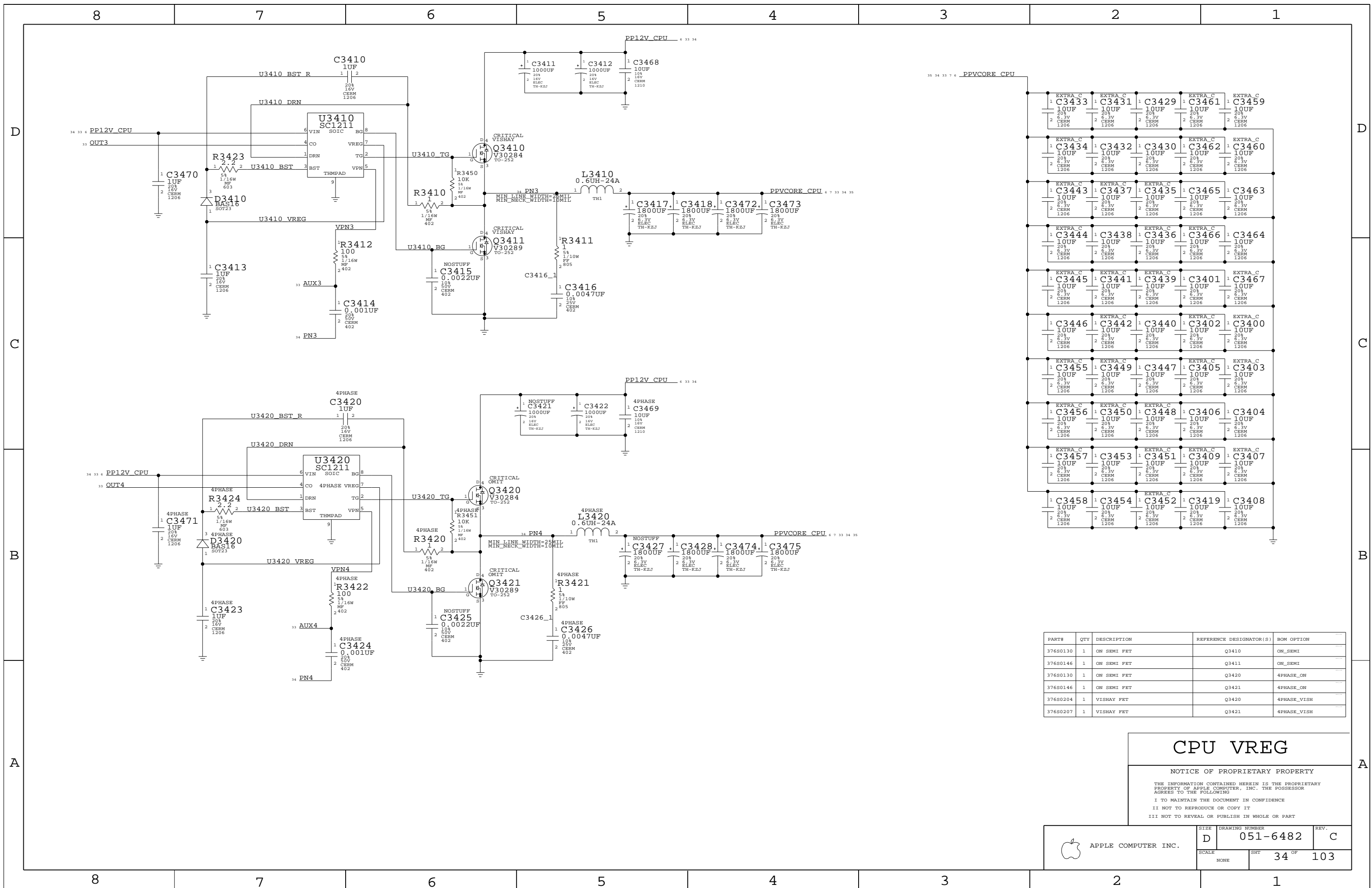
MASTER: GILA  
 LAST MODIFIED: APR 09, 04

# PROC DECOUPLING

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	OF	
NONE	32	103	





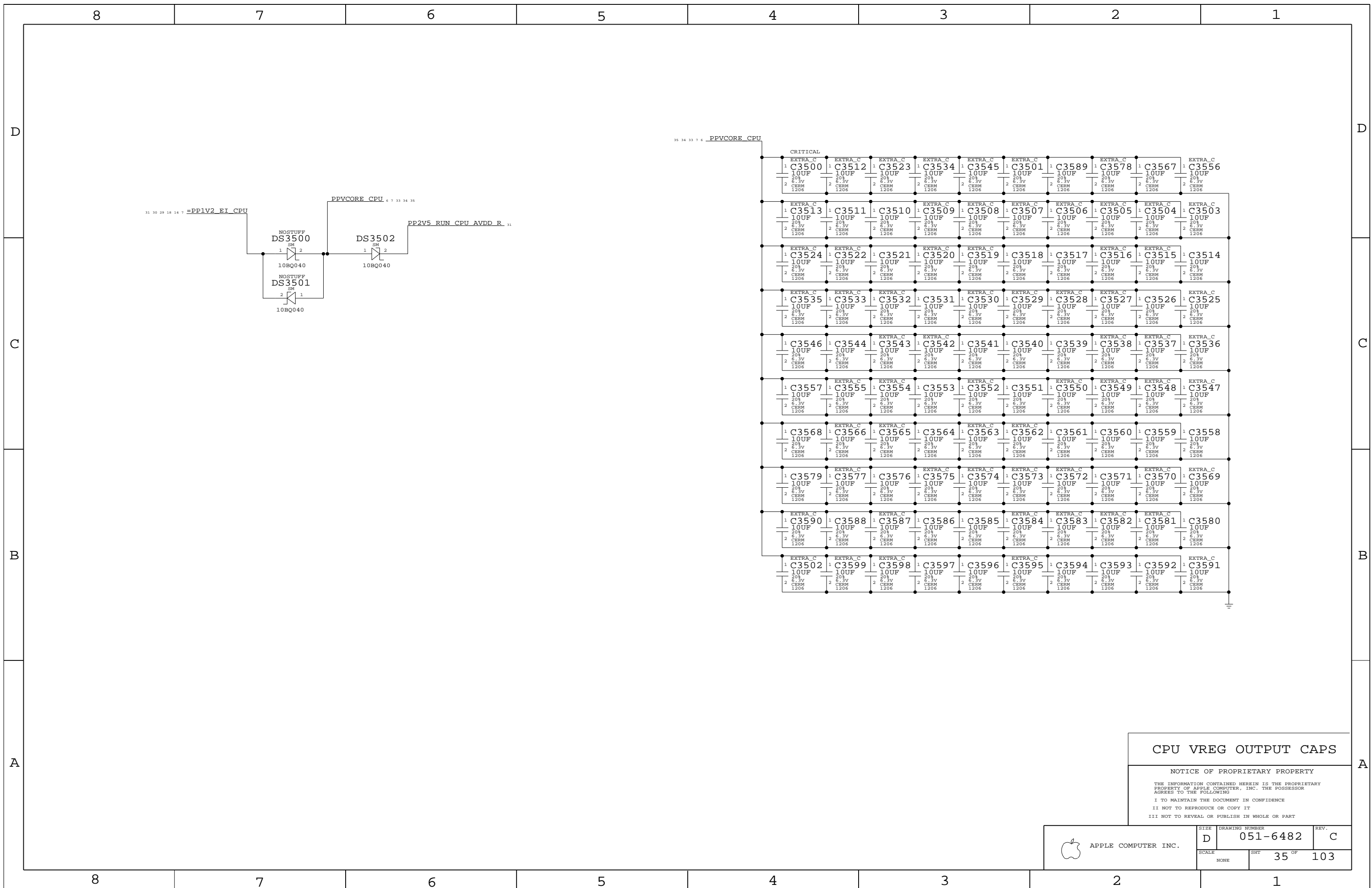
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376S0146	1	ON SEMI FET	Q3411	ON_SEMI
376S0130	1	ON SEMI FET	Q3420	4PHASE_ON
376S0146	1	ON SEMI FET	Q3421	4PHASE_ON
376S0204	1	VISHAY FET	Q3420	4PHASE_VISH
376S0207	1	VISHAY FET	Q3421	4PHASE_VISH

## CPU VREG

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	34 OF	103
NONE			



**CPU VREG OUTPUT CAPS**

**NOTICE OF PROPRIETARY PROPERTY**

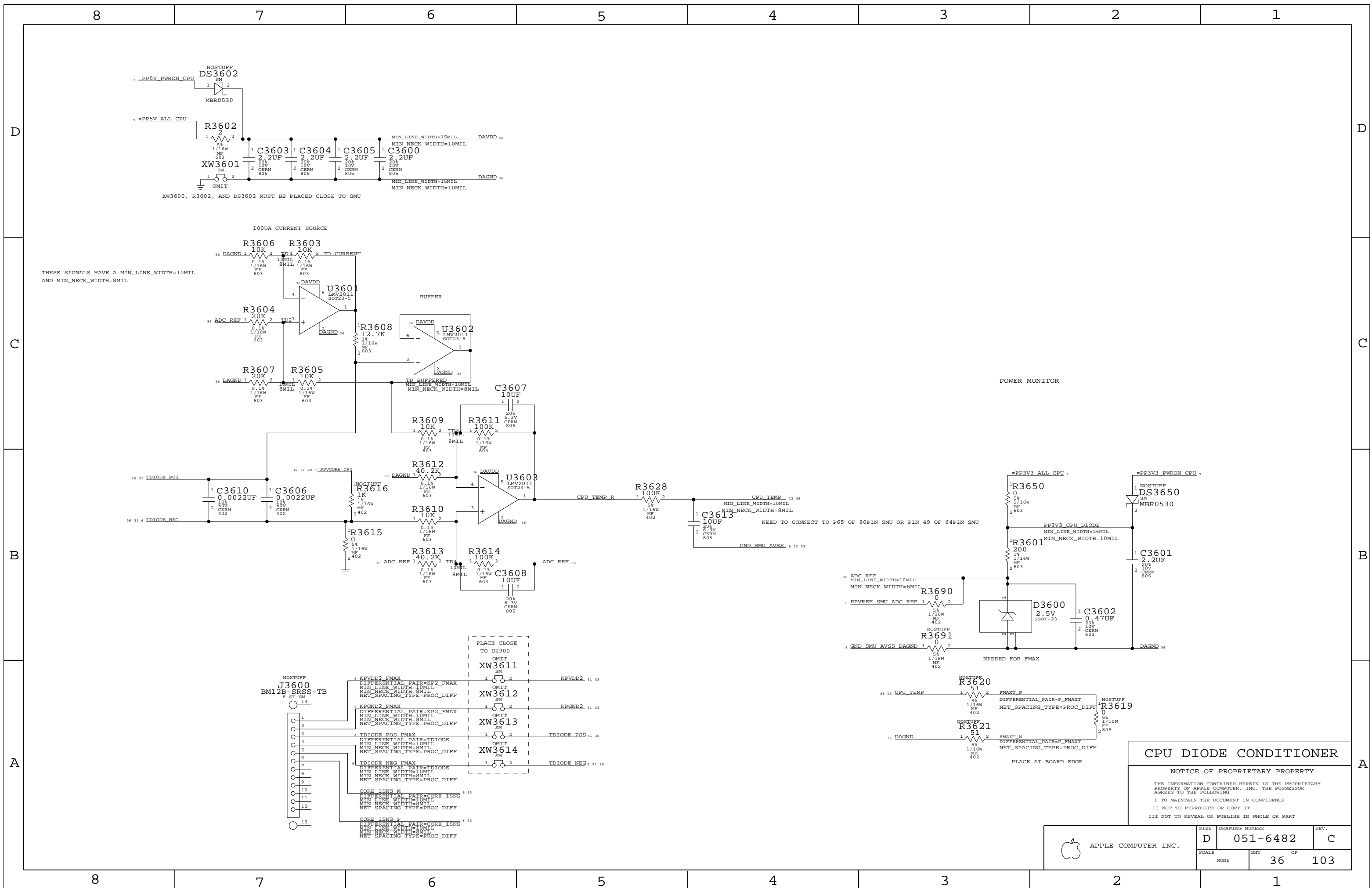
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	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	35 OF 103	
NONE			



THESE SIGNALS HAVE A MIN\_LINE\_WIDTH=10MIL AND MIN\_NECK\_WIDTH=8MIL

POWER MONITOR

PLACE CLOSE TO U2900

NEEDED FOR FMAX

PLACE AT BOARD EDGE

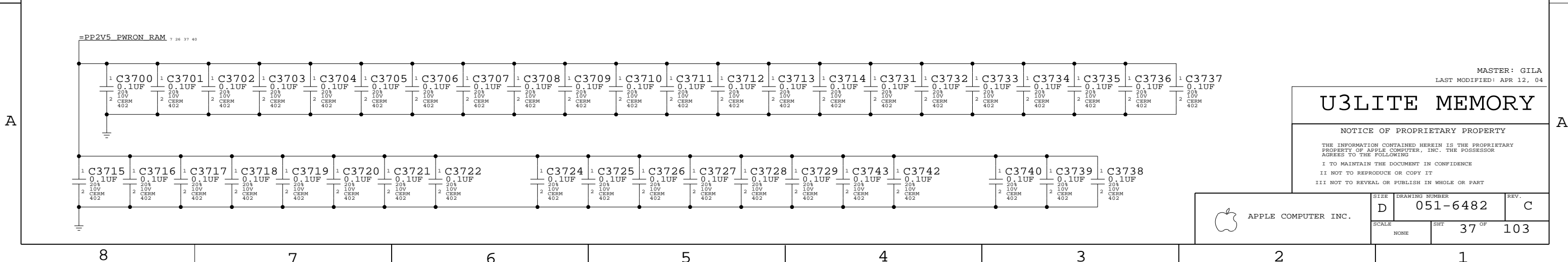
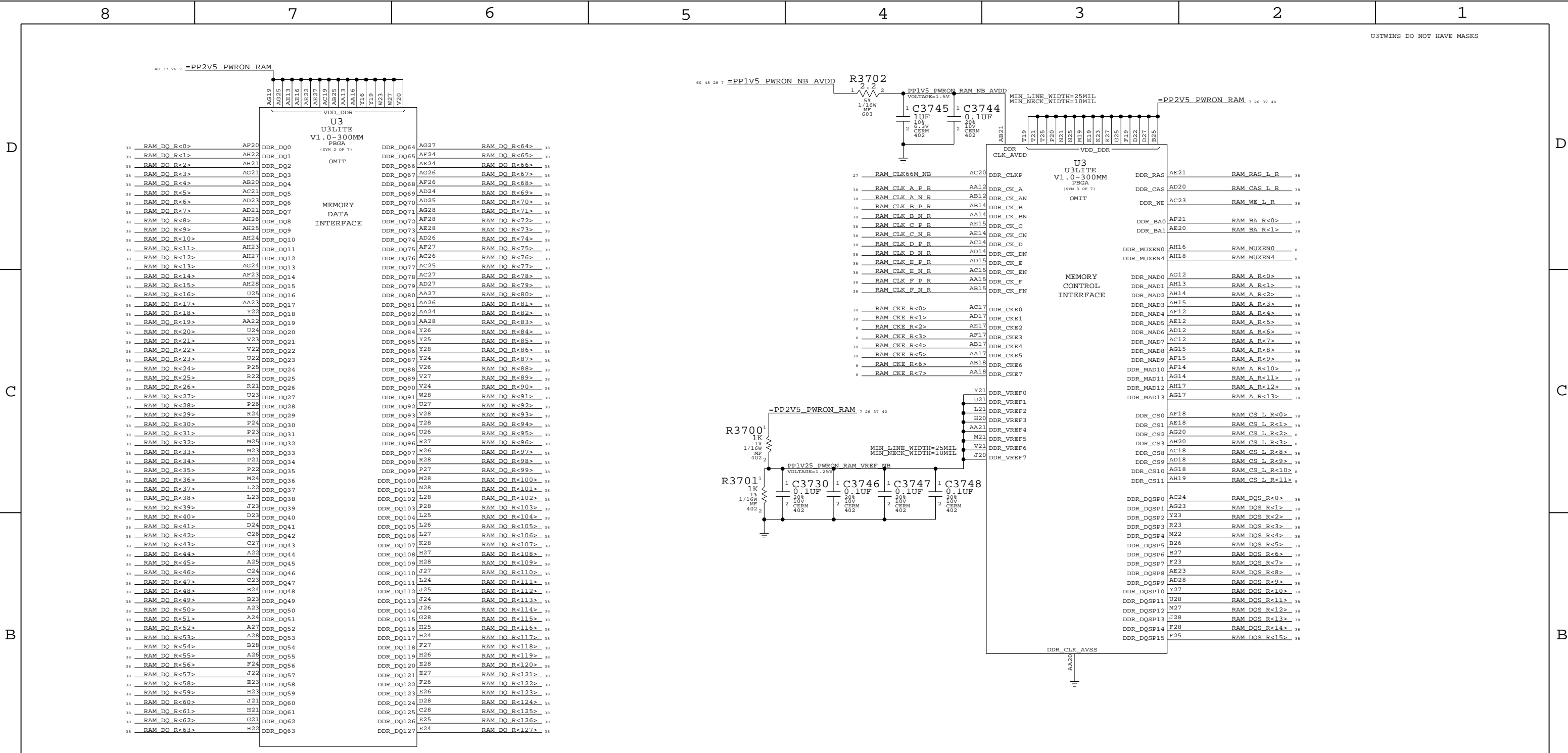
**CPU DIODE CONDITIONER**

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SCALE	SHT	OF	
NONE	36	103	





MASTER: GILA  
LAST MODIFIED: APR 12, 04

# U3LITE MEMORY

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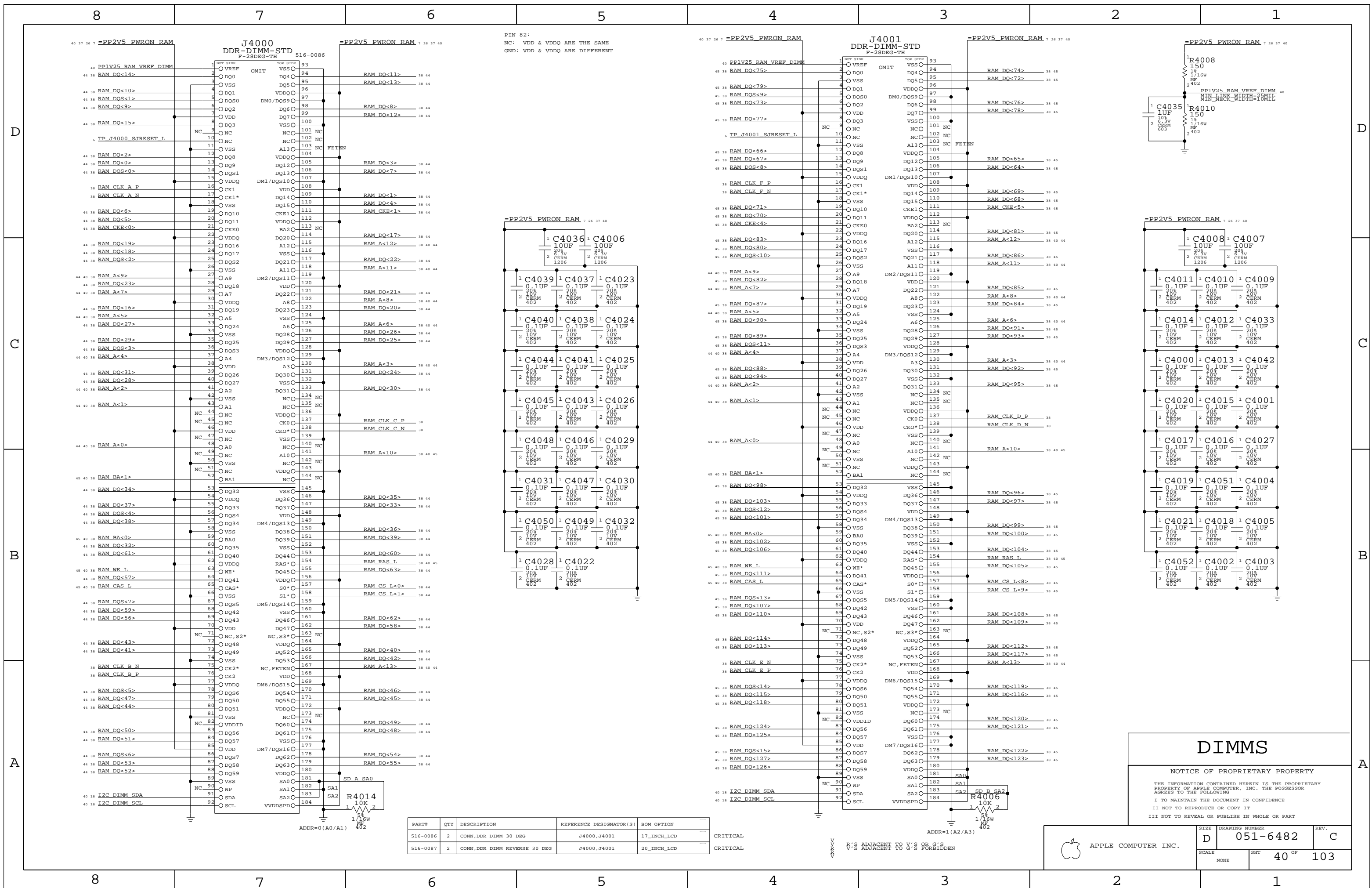
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	D	051-6482	C
SCALE	SHT	37 OF 103	
NONE			

ALL R PACKS ARE 1/16W 5%

ELECTRICAL\_CONSTRAINT\_SET NET\_PHYSICAL\_TYPE NET\_SPACING\_TYPE DIFFERENTIAL\_PAIR

38 37	RAM DO R<7>	RP3836	4	5	22	RAM DO<7>	38 40 44	38 37	RAM DO R<68>	RP3818	2	7	22	RAM DO<68>	38 40 45	38 37	RAM CLK A P R		RAM_CLK	RAM_CLK_A_R	0402
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38 37	RAM DO R<63>	RP3831																			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
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516-0087	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD

**DIMMS**

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-6482</b>	REV. <b>C</b>
	SCALE NONE	SHEET <b>40</b> OF <b>103</b>	

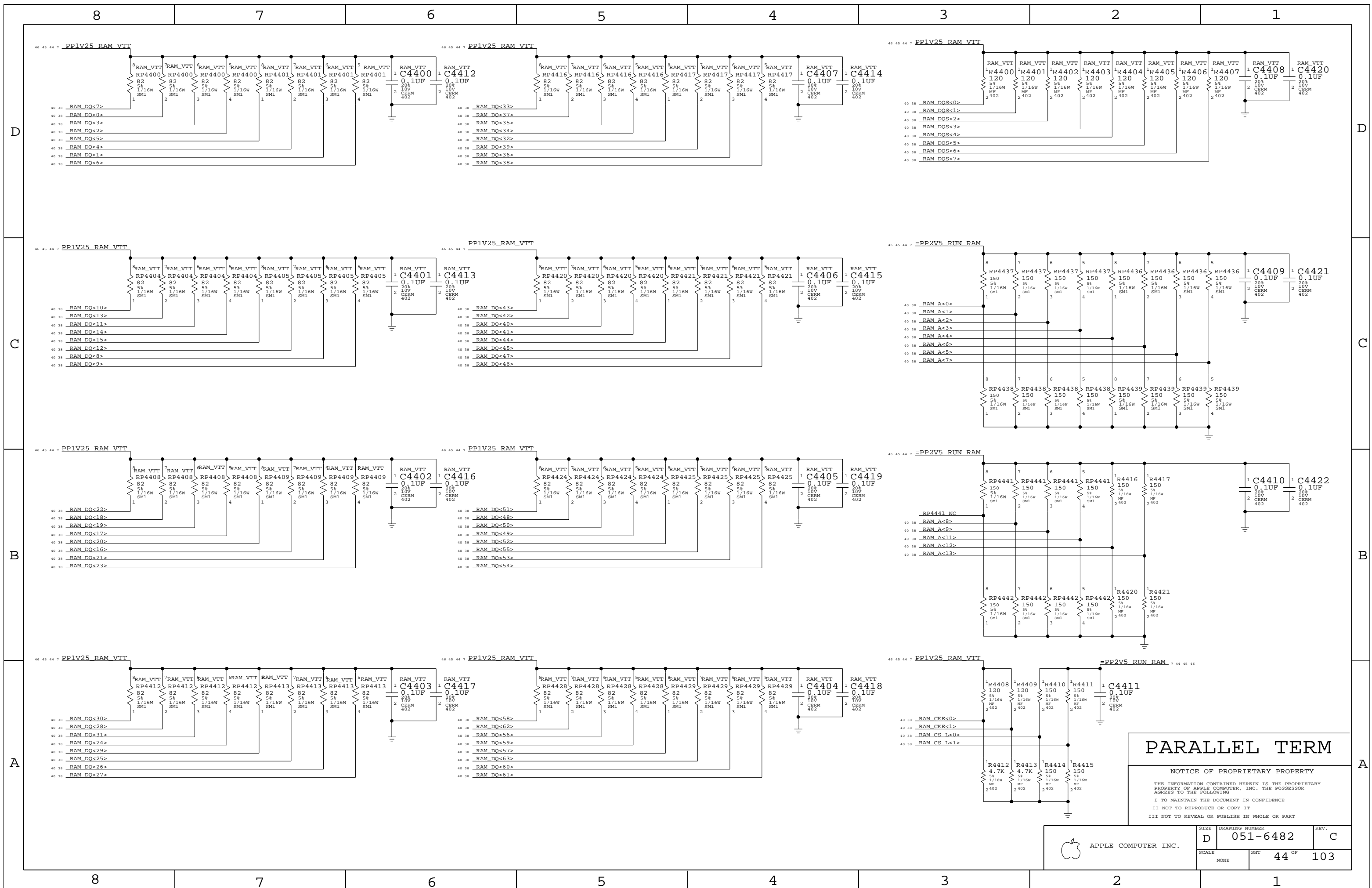
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CRITICAL

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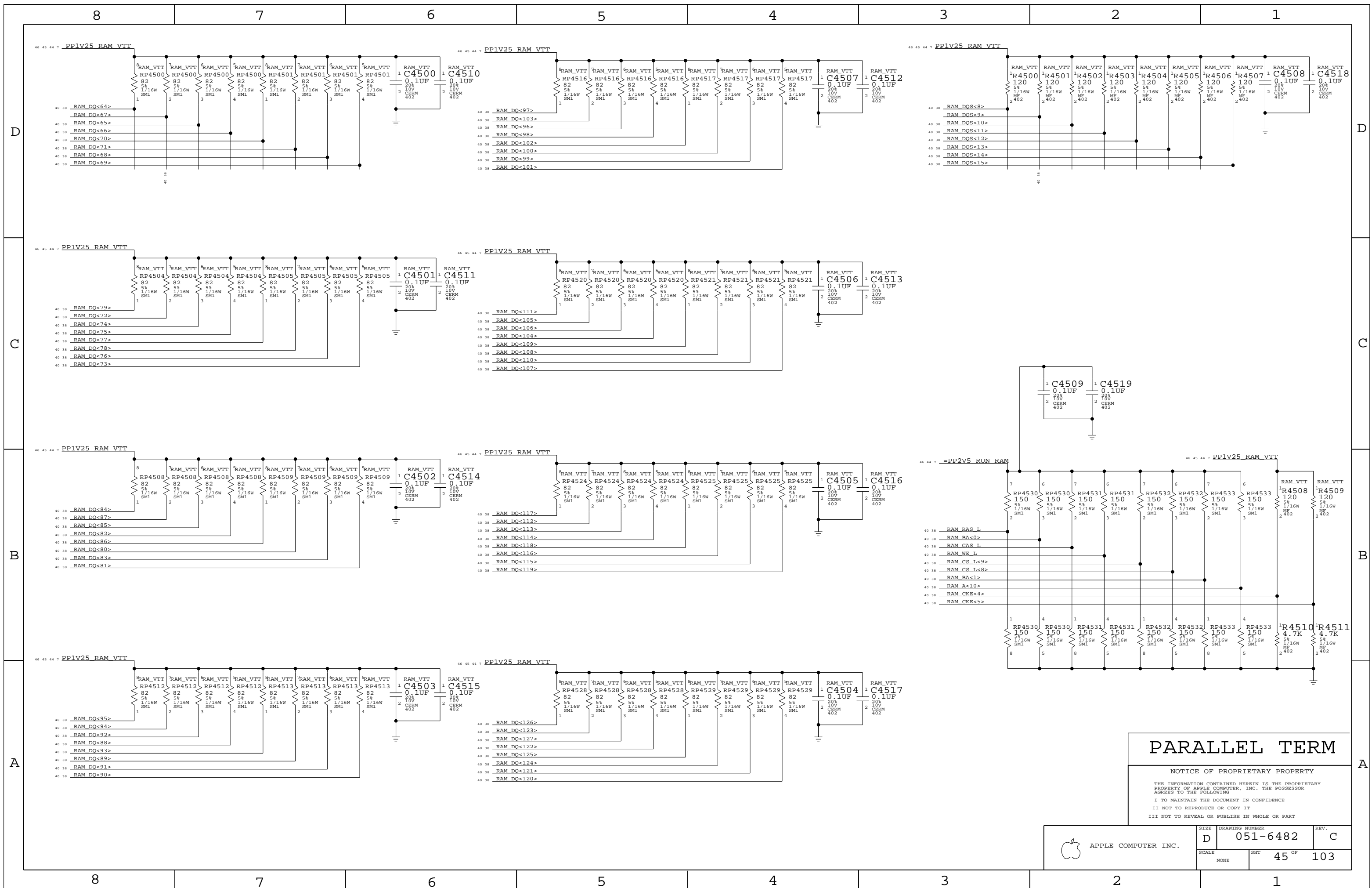
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 V'S ADJACENT TO V'S OR G'S  
 G'S ADJACENT TO G'S OR S'S  
 FORBIDDEN



**PARALLEL TERM**

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-6482</b>	REV. <b>C</b>
	SCALE NONE	SHEET <b>44</b> OF <b>103</b>	



# PARALLEL TERM


NOTICE OF PROPRIETARY PROPERTY

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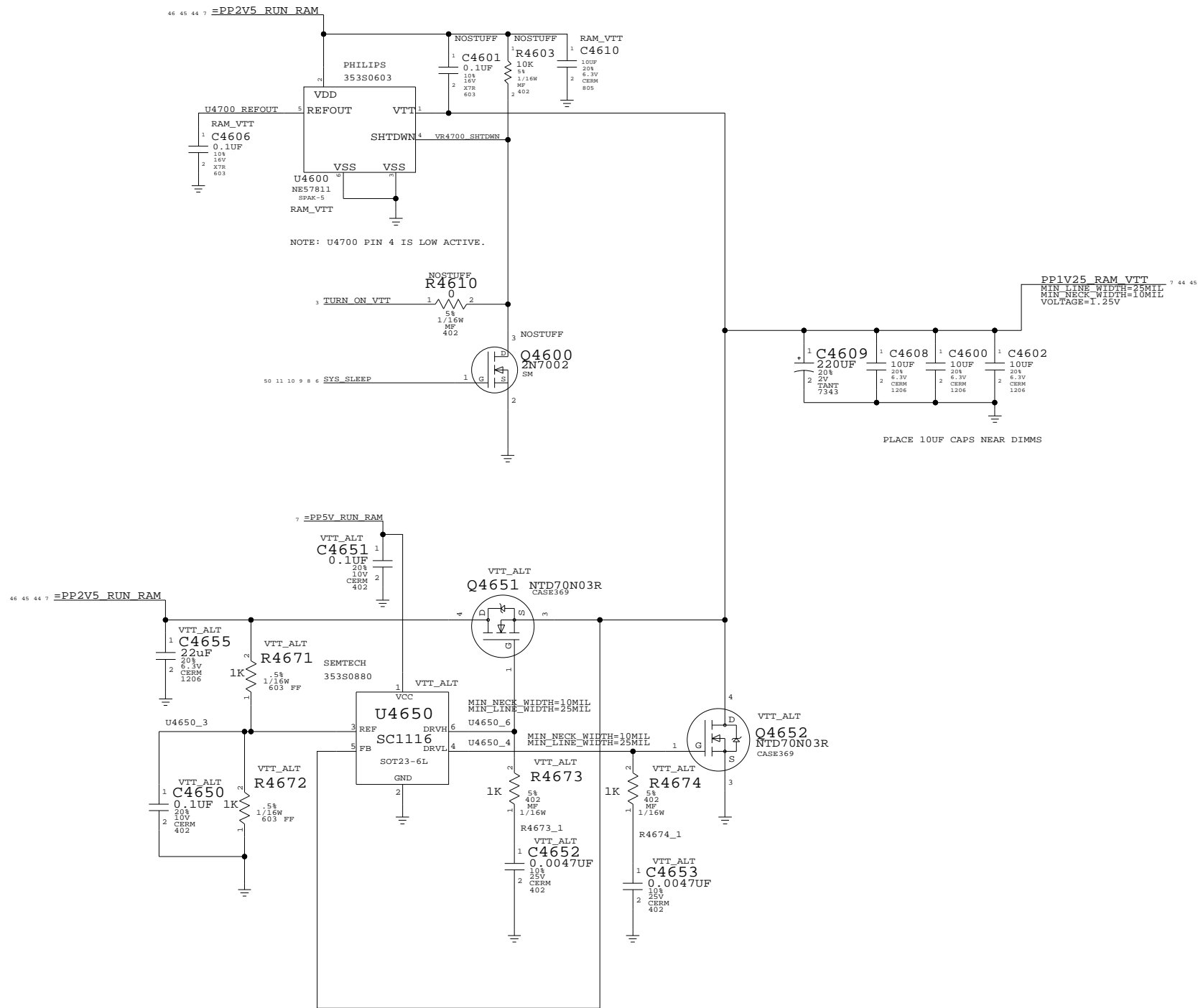
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	45 OF 103	
NONE			

ONLY STUFF ONE VTT VREG

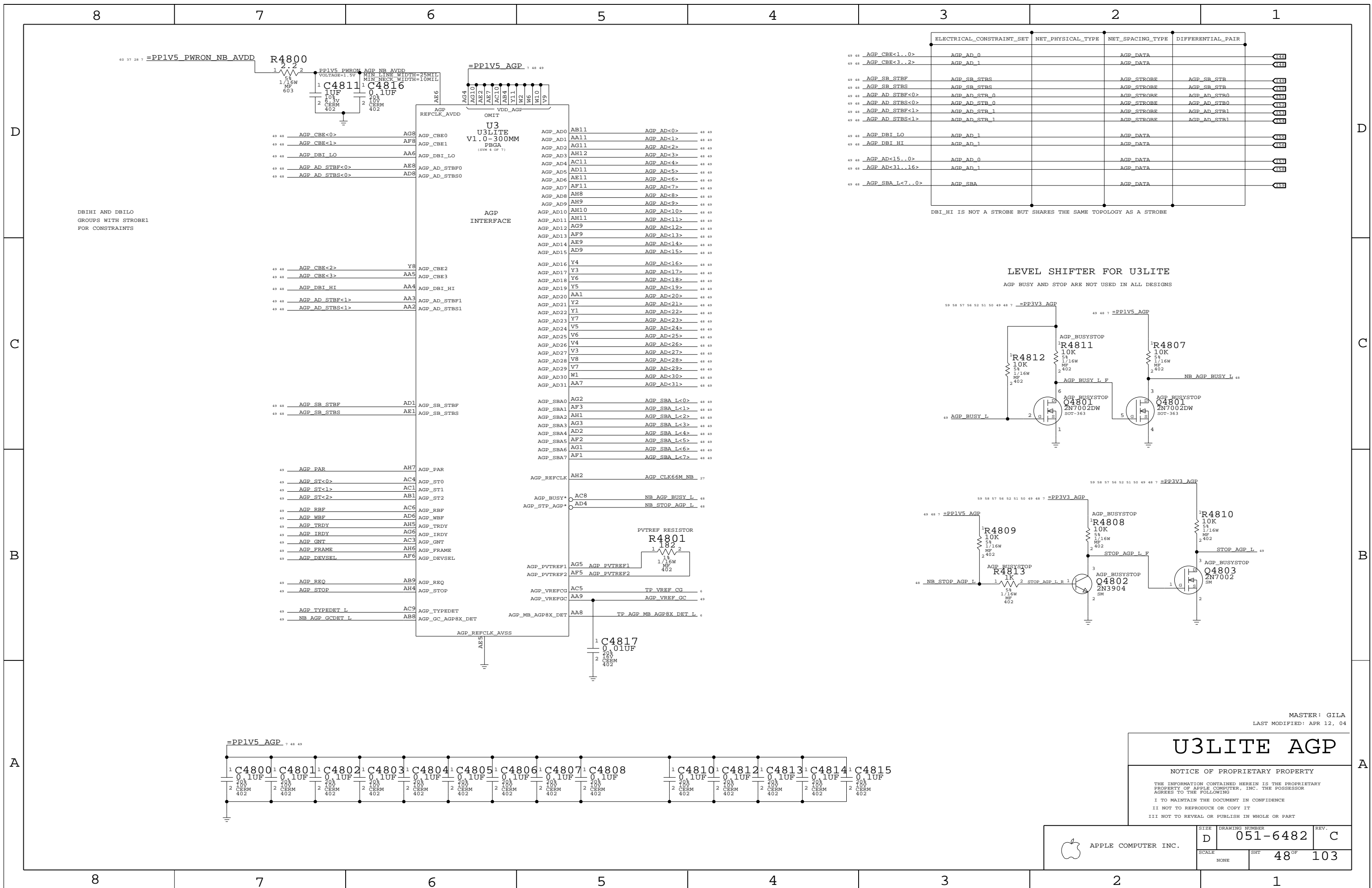


MEM TERM VREGS

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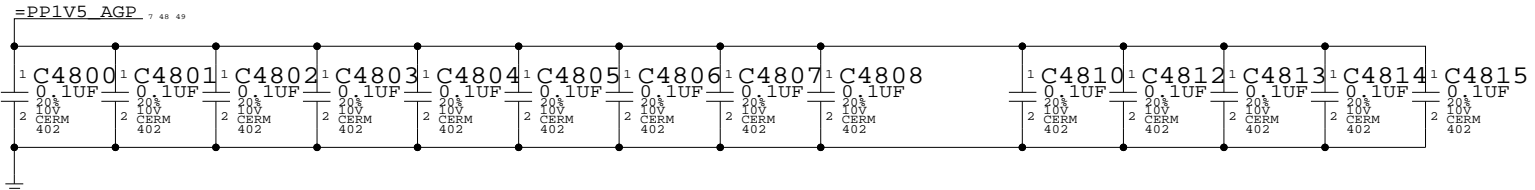
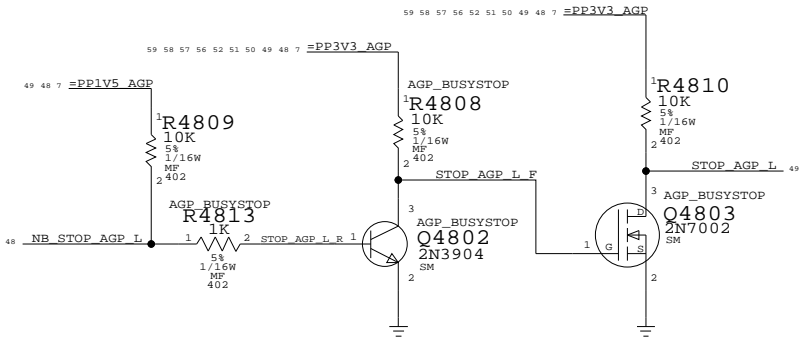
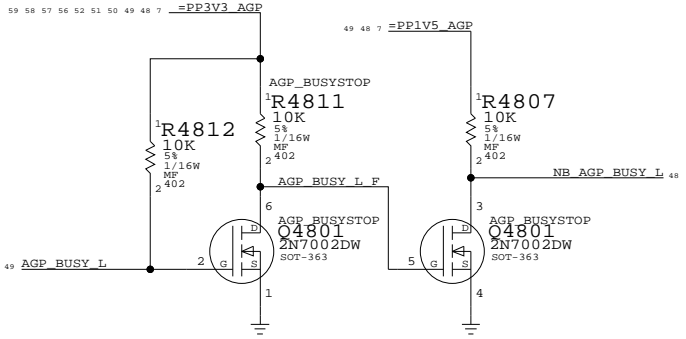
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	46 OF	103
NONE			



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
49 48	AGP_CBE<1..0>	AGP_AD_0	AGP_DATA		4848
49 48	AGP_CBE<3..2>	AGP_AD_1	AGP_DATA		4849
49 48	AGP_SB_STBF	AGP_SB_STBS	AGP_STROBE	AGP_SB_STR	4850
49 48	AGP_SB_STBS	AGP_SB_STBS	AGP_STROBE	AGP_SB_STR	4850
49 48	AGP_AD_STBF<0>	AGP_AD_STR_0	AGP_STROBE	AGP_AD_STR0	4851
49 48	AGP_AD_STBS<0>	AGP_AD_STR_0	AGP_STROBE	AGP_AD_STR0	4851
49 48	AGP_AD_STBF<1>	AGP_AD_STR_1	AGP_STROBE	AGP_AD_STR1	4852
49 48	AGP_AD_STBS<1>	AGP_AD_STR_1	AGP_STROBE	AGP_AD_STR1	4852
49 48	AGP_DBI_LO	AGP_AD_1	AGP_DATA		4855
49 48	AGP_DBI_HI	AGP_AD_1	AGP_DATA		4856
49 48	AGP_AD<15..0>	AGP_AD_0	AGP_DATA		4857
49 48	AGP_AD<31..16>	AGP_AD_1	AGP_DATA		4858
49 48	AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA		4859

DBI\_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE

**LEVEL SHIFTER FOR U3LITE**  
 AGP BUSY AND STOP ARE NOT USED IN ALL DESIGNS



MASTER: GILA  
 LAST MODIFIED: APR 12, 04

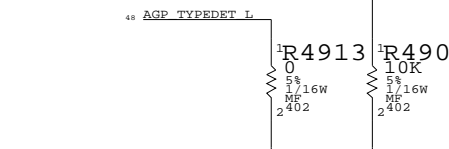
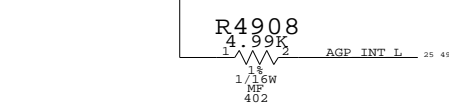
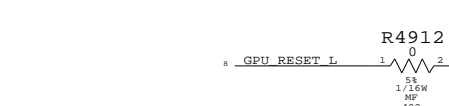
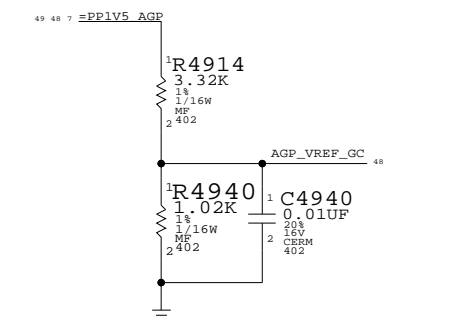
**U3LITE AGP**

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	D	051-6482	C
SCALE	SHT	48 OF 103	
NONE			

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0176	1	IC,NV18B,GRAPHIC CTRL,C1	U4900	NV18B
338S0175	1	IC,NV34,GRAPHIC CTRL,B1	U4900	NV34

**U3LITE AGP I/O REFERENCE**  
(PLACE CLOSE TO GPU AGP BALLS)



DOES HOOP UP AGP\_BUSY\_L & STOP\_AGP\_L TO 3.3V OR 1.5V?

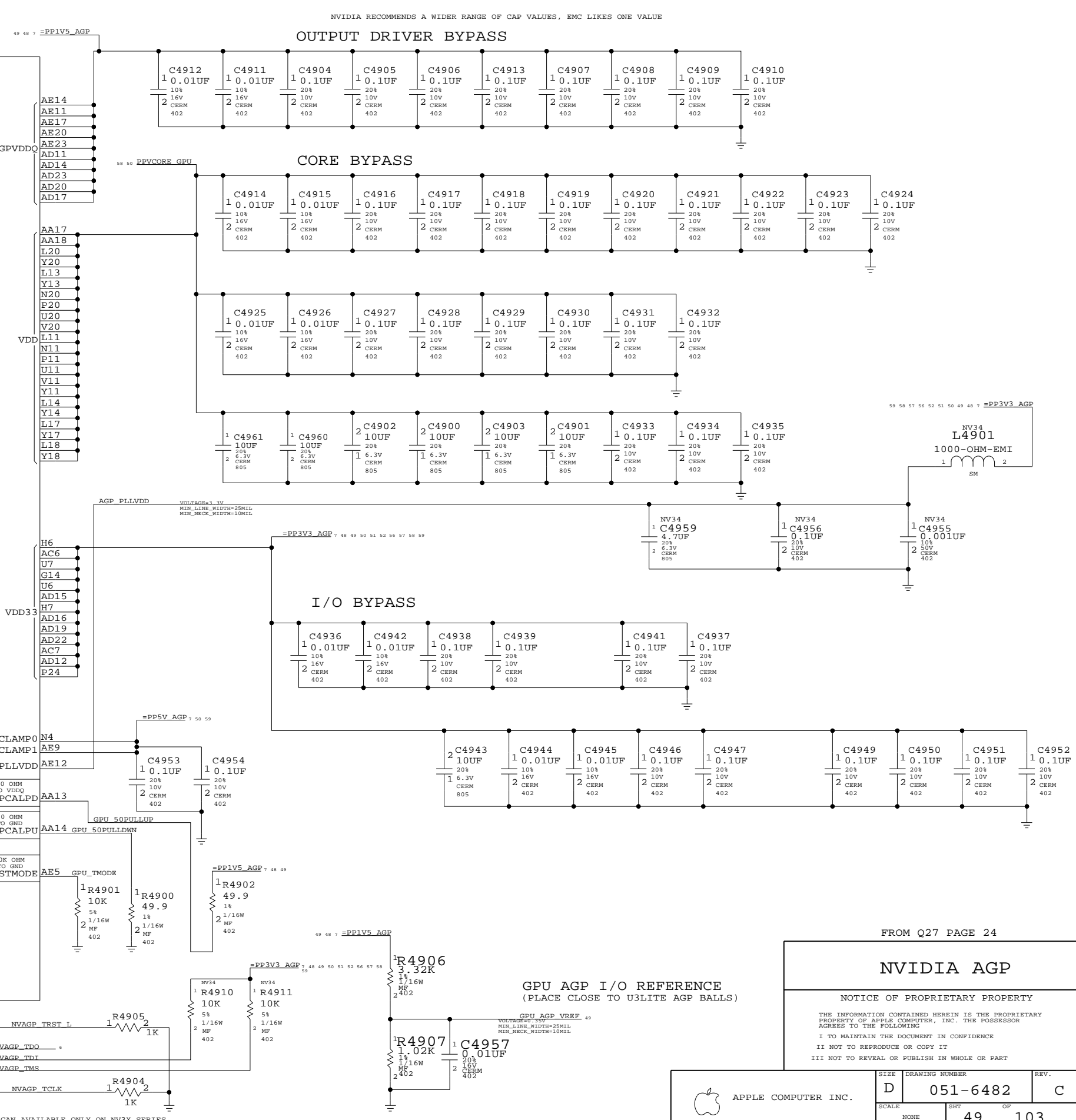
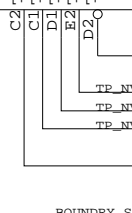
**AGP VERSION SELECT**  
(LOW = AGP V3.X)  
(HIGH = AGP V2.X)

48	AGP_AD<0>	AJ28	PCIAD0
48	AGP_AD<1>	AK28	PCIAD1
48	AGP_AD<2>	AH27	PCIAD2
48	AGP_AD<3>	AK27	PCIAD3
48	AGP_AD<4>	AJ27	PCIAD4
48	AGP_AD<5>	AH26	PCIAD5
48	AGP_AD<6>	AJ26	PCIAD6
48	AGP_AD<7>	AH25	PCIAD7
48	AGP_AD<8>	AH23	PCIAD8
48	AGP_AD<9>	AJ23	PCIAD9
48	AGP_AD<10>	AH22	PCIAD10
48	AGP_AD<11>	AJ22	PCIAD11
48	AGP_AD<12>	AJ21	PCIAD12
48	AGP_AD<13>	AK21	PCIAD13
48	AGP_AD<14>	AH20	PCIAD14
48	AGP_AD<15>	AJ20	PCIAD15
48	AGP_AD<16>	AG26	PCIAD16
48	AGP_AD<17>	AE24	PCIAD17
48	AGP_AD<18>	AG25	PCIAD18
48	AGP_AD<19>	AG24	PCIAD19
48	AGP_AD<20>	AF24	PCIAD20
48	AGP_AD<21>	AG23	PCIAD21
48	AGP_AD<22>	AE22	PCIAD22
48	AGP_AD<23>	AF22	PCIAD23
48	AGP_AD<24>	AE21	PCIAD24
48	AGP_AD<25>	AG20	PCIAD25
48	AGP_AD<26>	AG19	PCIAD26
48	AGP_AD<27>	AF19	PCIAD27
48	AGP_AD<28>	AE19	PCIAD28
48	AGP_AD<29>	AF18	PCIAD29
48	AGP_AD<30>	AG18	PCIAD30
48	AGP_AD<31>	AE18	PCIAD31
48	AGP_CBE<0>	AJ24	PCIC0/BE0*
48	AGP_CBE<1>	AH19	PCIC1/BE1*
48	AGP_CBE<2>	AF25	PCIC2/BE2*
48	AGP_CBE<3>	AG22	PCIC3/BE3*
27	AGP_CLK66M GPU	AG12	PCICLK : CLK
	NV_PCIRST L	AF15	PCIRST* : RST*
48	AGP_GNT	AE15	PCIGNT* : GNT
48	AGP_REQ	AF13	PCIREQ* : REQ
48	AGP_FRAME	AK16	PCIFRAME* : FRAME
48	AGP_IRDY	AG16	PCIIRDY* : IRDY
48	AGP_TRDY	AJ17	PCITRDY* : TRDY
48	AGP_DEVSEL	AJ16	PCIDEVSEL* : DEVSEL
48	AGP_STOP	AH17	PCISTOP* : STOP
48	AGP_PAR	AK18	PCIPAR : PAR
25	AGP_INT L	AG15	PCIINTA* : INTA
6	TP_GPU_INTB L	AE10	NC_PCIINTB* : INTB
48	AGP_RBF	AG14	AGPRBF* : RBF
48	AGP_WBF	AG17	AGPWBF* : WBF
48	AGP_DBI_HI	AJ18	AGPDBI* : DBI_HI
48	AGP_DBI_LO	AJ19	<RESRVD> : DBI_LO
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48	AGP_ST<1>	AE16	AGPST1 : ST1
48	AGP_ST<2>	AE13	AGPST2 : ST2
48	AGP_AD_STBF<0>	AK24	AGPADSTBF0 : ADSTBF0
48	AGP_AD_STBS<0>	AJ25	AGPADSTBS0* : ADSTBS0
48	AGP_AD_STBF<1>	AG21	AGPADSTBF1 : ADSTBF1
48	AGP_AD_STBS<1>	AF21	AGPADSTBS1* : ADSTBS1
48	AGP_SB_STBF	AK13	AGPSBSTBF : SBSTBF
48	AGP_SB_STBS	AJ13	AGPSBSTBS* : SBSTBS
48	AGP_SBA_L<0>	AJ11	AGPSBA0 : SBA0*
48	AGP_SBA_L<1>	AH11	AGPSBA1 : SBA1*
48	AGP_SBA_L<2>	AJ12	AGPSBA2 : SBA2*
48	AGP_SBA_L<3>	AH12	AGPSBA3 : SBA3*
48	AGP_SBA_L<4>	AJ14	AGPSBA4 : SBA4*
48	AGP_SBA_L<5>	AH14	AGPSBA5 : SBA5*
48	AGP_SBA_L<6>	AJ15	AGPSBA6 : SBA6*
48	AGP_SBA_L<7>	AH15	AGPSBA7 : SBA7*
48	<RESRVD>	AF16	GPU_MBDT L : MBDT*
48	AGP_BUSY L	AF12	AGPBUSY* : BUSY*
48	STOP_AGP L	AG11	AGPSTOP* : STOP*
48	GPU_AGP_VREF	AK29	AGPVREF : AGPVREF

AGP 2X, 4X : AGP 8X

PCIC0/BE0\* : C0\*/BE0  
PCIC1/BE1\* : C1\*/BE1  
PCIC2/BE2\* : C2\*/BE2  
PCIC3/BE3\* : C3\*/BE3

AGPADSTBF0 : ADSTBF0  
AGPADSTBS0\* : ADSTBS0  
AGPADSTBF1 : ADSTBF1  
AGPADSTBS1\* : ADSTBS1  
AGPSBSTBF : SBSTBF  
AGPSBSTBS\* : SBSTBS  
AGPSBA0 : SBA0\*  
AGPSBA1 : SBA1\*  
AGPSBA2 : SBA2\*  
AGPSBA3 : SBA3\*  
AGPSBA4 : SBA4\*  
AGPSBA5 : SBA5\*  
AGPSBA6 : SBA6\*  
AGPSBA7 : SBA7\*  
<RESRVD> : MBDT\*  
AGPBUSY\* : BUSY\*  
AGPSTOP\* : STOP\*  
AGPVREF : AGPVREF



**OUTPUT DRIVER BYPASS**

**CORE BYPASS**

**I/O BYPASS**

**GPU AGP I/O REFERENCE**  
(PLACE CLOSE TO U3LITE AGP BALLS)

FROM Q27 PAGE 24

**NVIDIA AGP**

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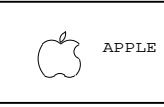
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SCALE	SHT	OF
NONE	49	103

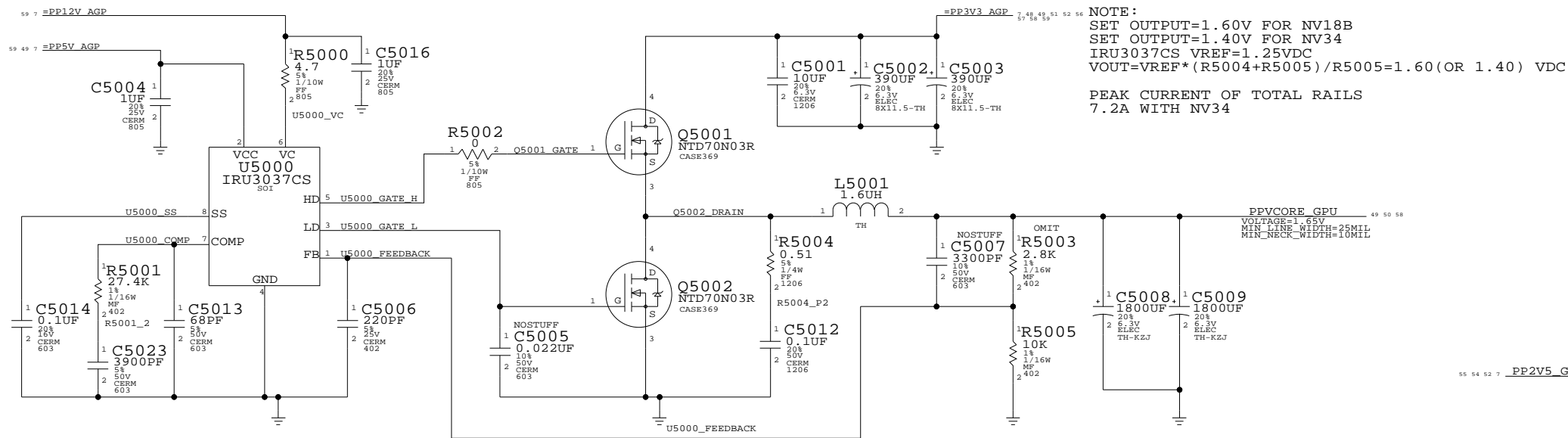


BOUNDARY SCAN AVAILABLE ONLY ON NV3X SERIES



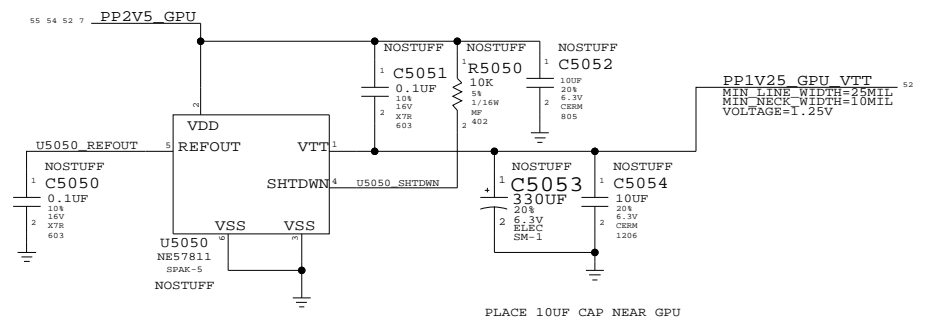
# GPU VCORE VREG

PPVCORE_GPU	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
1.60VDC	114S2803	1	RES,2.8K OHM,1/16W,1%,0402	R5003	NV18B
1.40VDC	114S1213	1	RES,1.21K OHM,1/16W,1%,0402	R5003	NV34

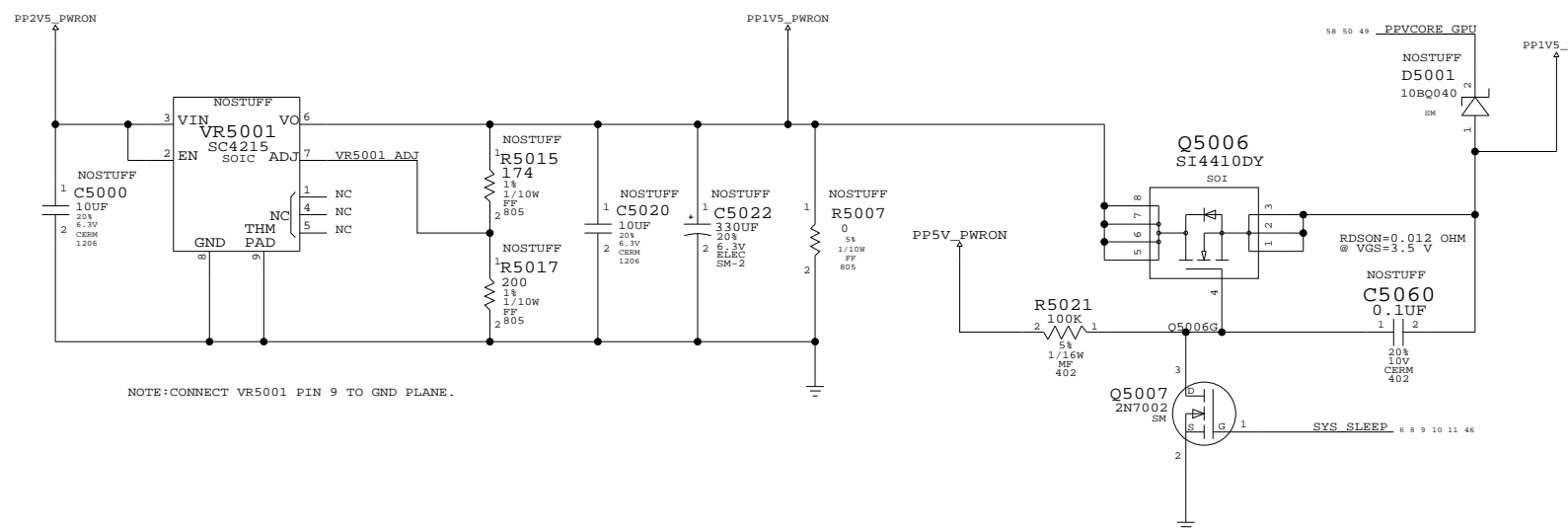


NOTE:  
 SET OUTPUT=1.60V FOR NV18B  
 SET OUTPUT=1.40V FOR NV34  
 IRU3037CS VREF=1.25VDC  
 $VOUT=VREF*(R5004+R5005)/R5005=1.60(OR\ 1.40)\ VDC$   
 PEAK CURRENT OF TOTAL RAILS  
 7.2A WITH NV34

# GPU VTT VREG



# AGP 1.5V VREG



NOTE:  
 SET OUTPUT=1.5V  
 SC4215 VREF=0.8VDC  
 $VOUT=VREF*(R5015+R5017)/R5017=1.5\ VDC$   
 PEAK CURRENT OF TOTAL RAILS  
 0.95A

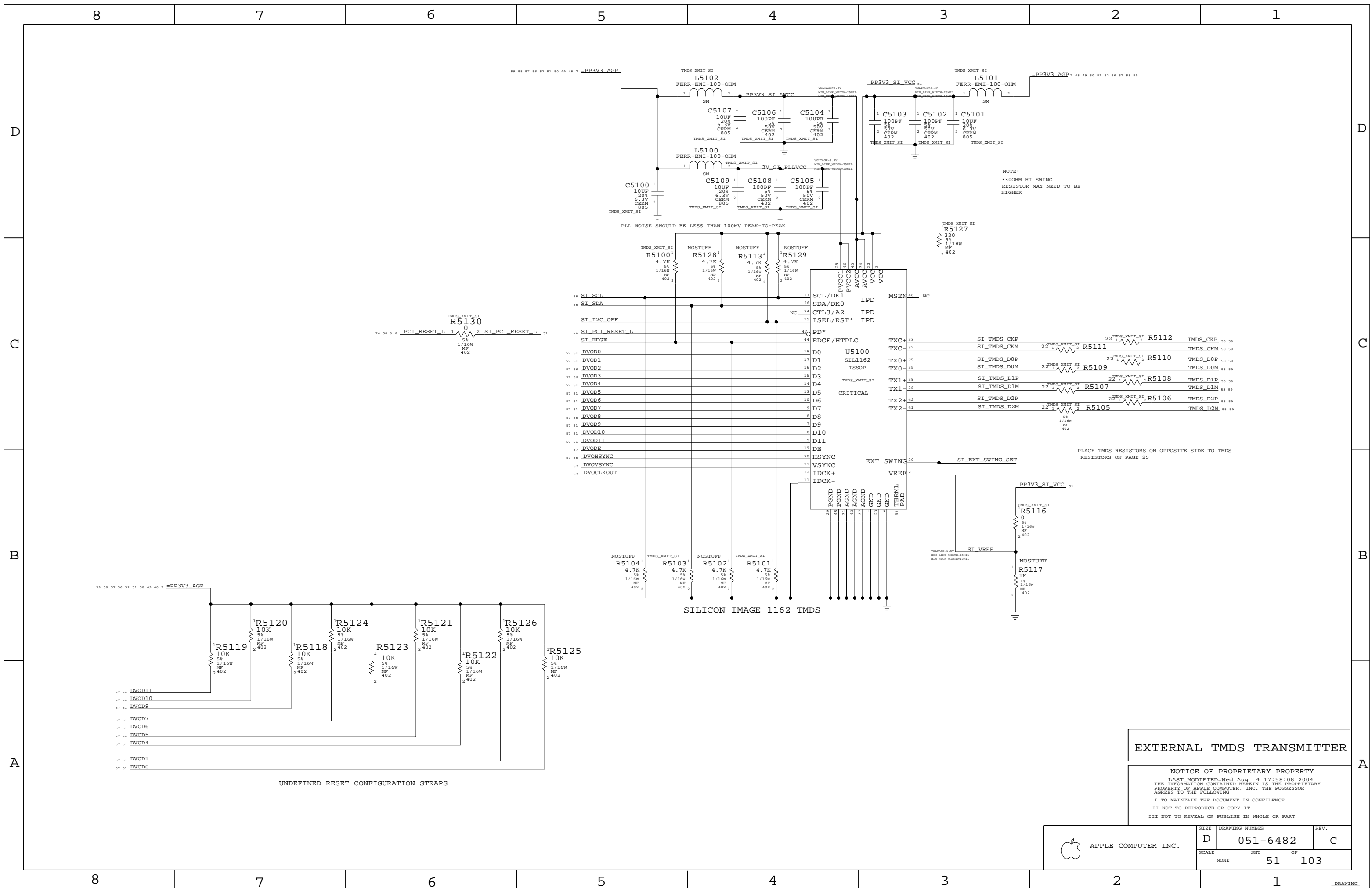
NOTE:CONNECT VR5001 PIN 9 TO GND PLANE.

## GRAPHICS VREGS

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	D	051-6482	C
SCALE	NONE	SHT	OF
		50	103



NOTE:  
330OHM HI SWING  
RESISTOR MAY NEED TO BE  
HIGHER

PLL NOISE SHOULD BE LESS THAN 100MV PEAK-TO-PEAK

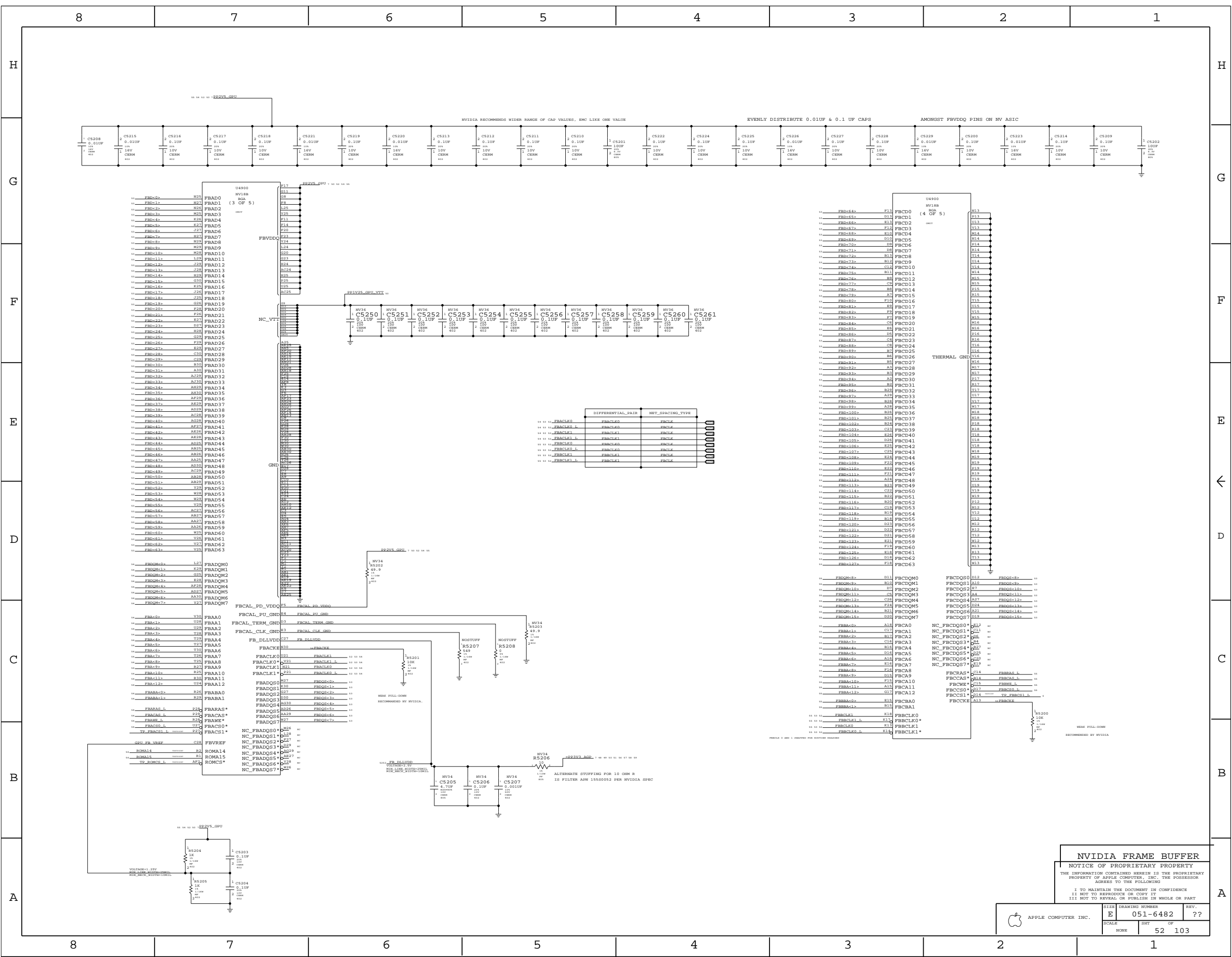
PLACE TMSD RESISTORS ON OPPOSITE SIDE TO TMSD  
RESISTORS ON PAGE 25

UNDEFINED RESET CONFIGURATION STRAPS

**EXTERNAL TMSD TRANSMITTER**

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SCALE	NONE	SHT	OF
		51	103



**NVIDIA FRAME BUFFER**  
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	E	051-6482	??
	SCALE	SHT	OF
		52	103

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8 7 6 5 4 3 2 1

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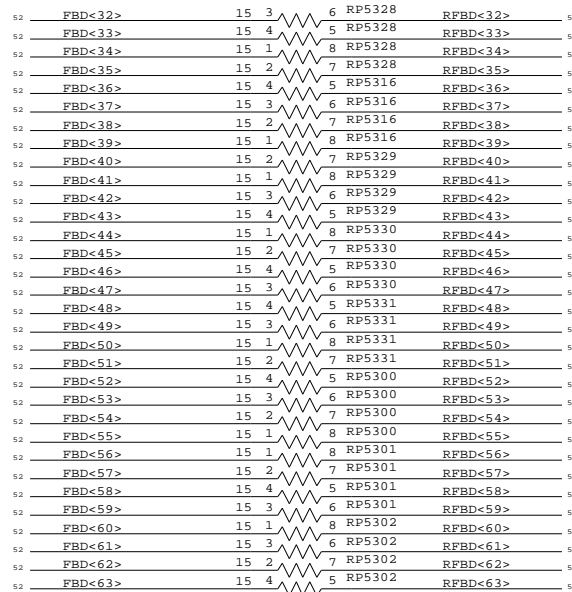
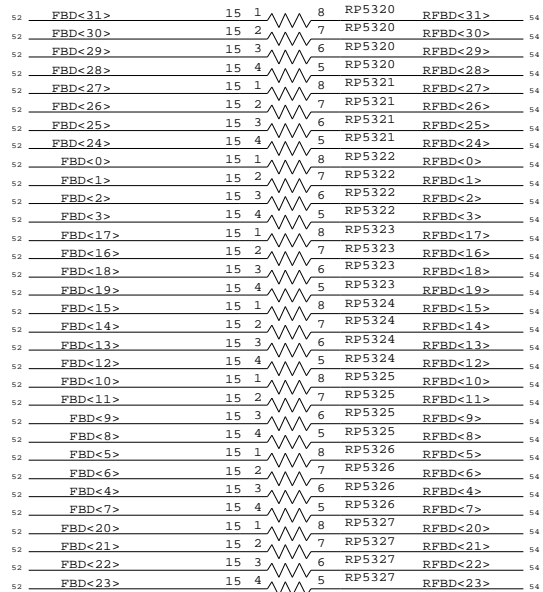
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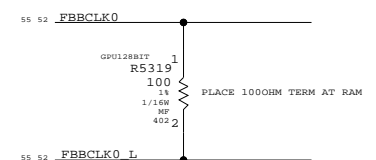
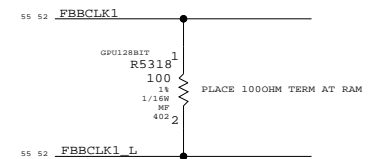
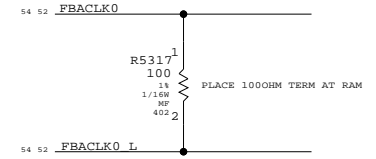
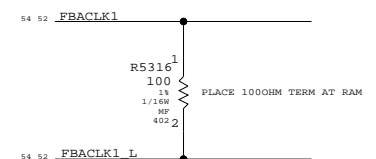
2

1

PLACE R'S CLOSE TO MEMORY



PLACE R'S CLOSE TO GPU



D

D

C

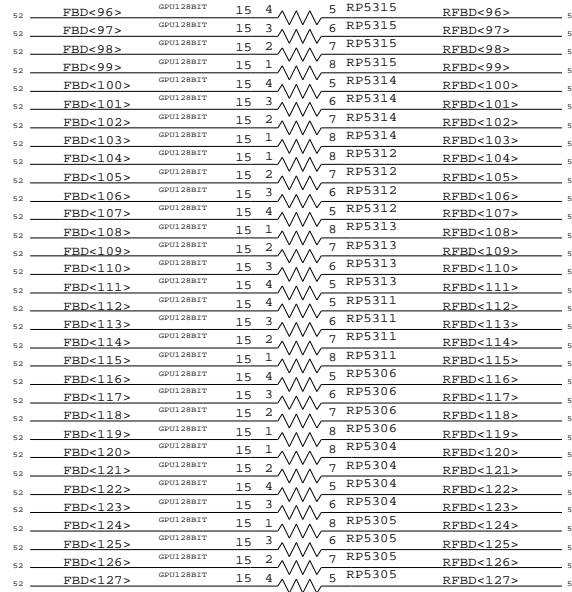
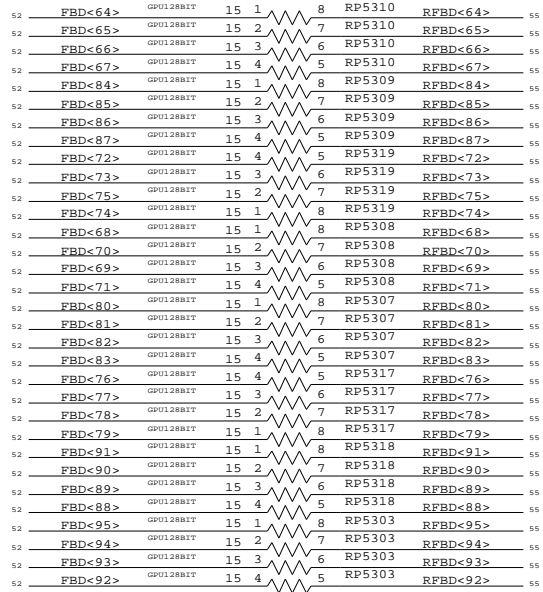
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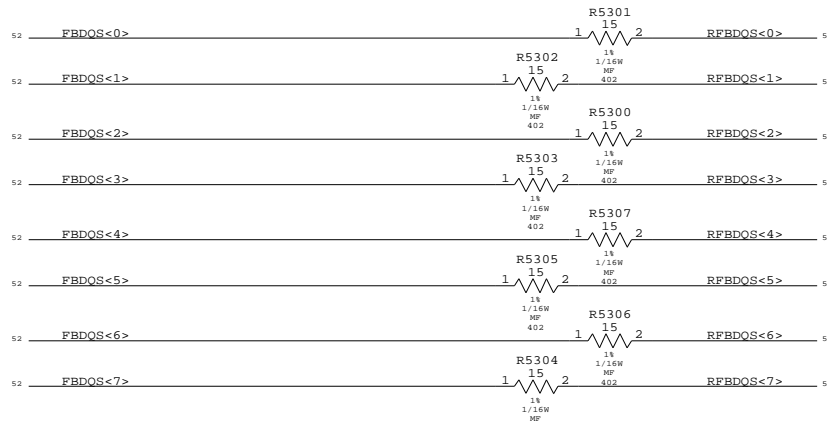
B

A

A



PLACE THESE R CLOSE TO SGRAM



PLACE THESE R CLOSE TO SGRAM



FROM Q27 PAGE 26

### FB TERMINATION

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	D	051-6482	C
SCALE	NONE	SHT OF	53 103

8

7

6

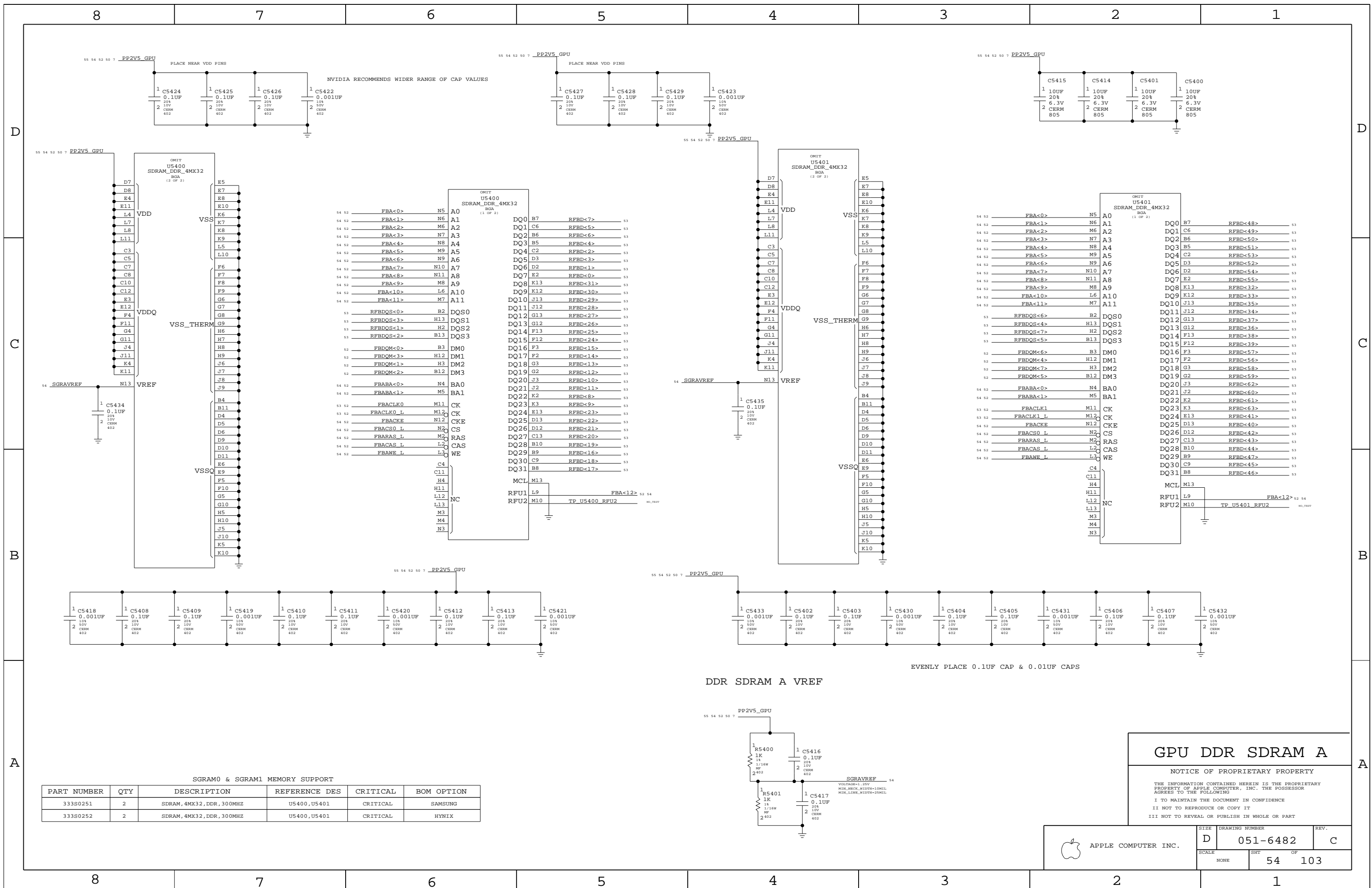
5

4

3

2

1



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U5400, U5401	CRITICAL	SAMSUNG
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U5400, U5401	CRITICAL	HYNIX

**GPU DDR SDRAM A**

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SCALE: NONE

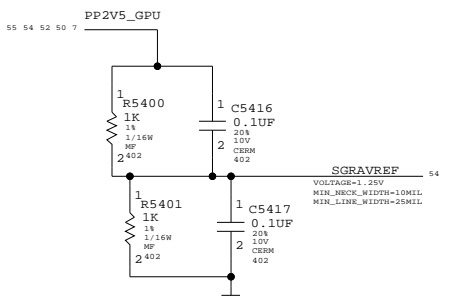
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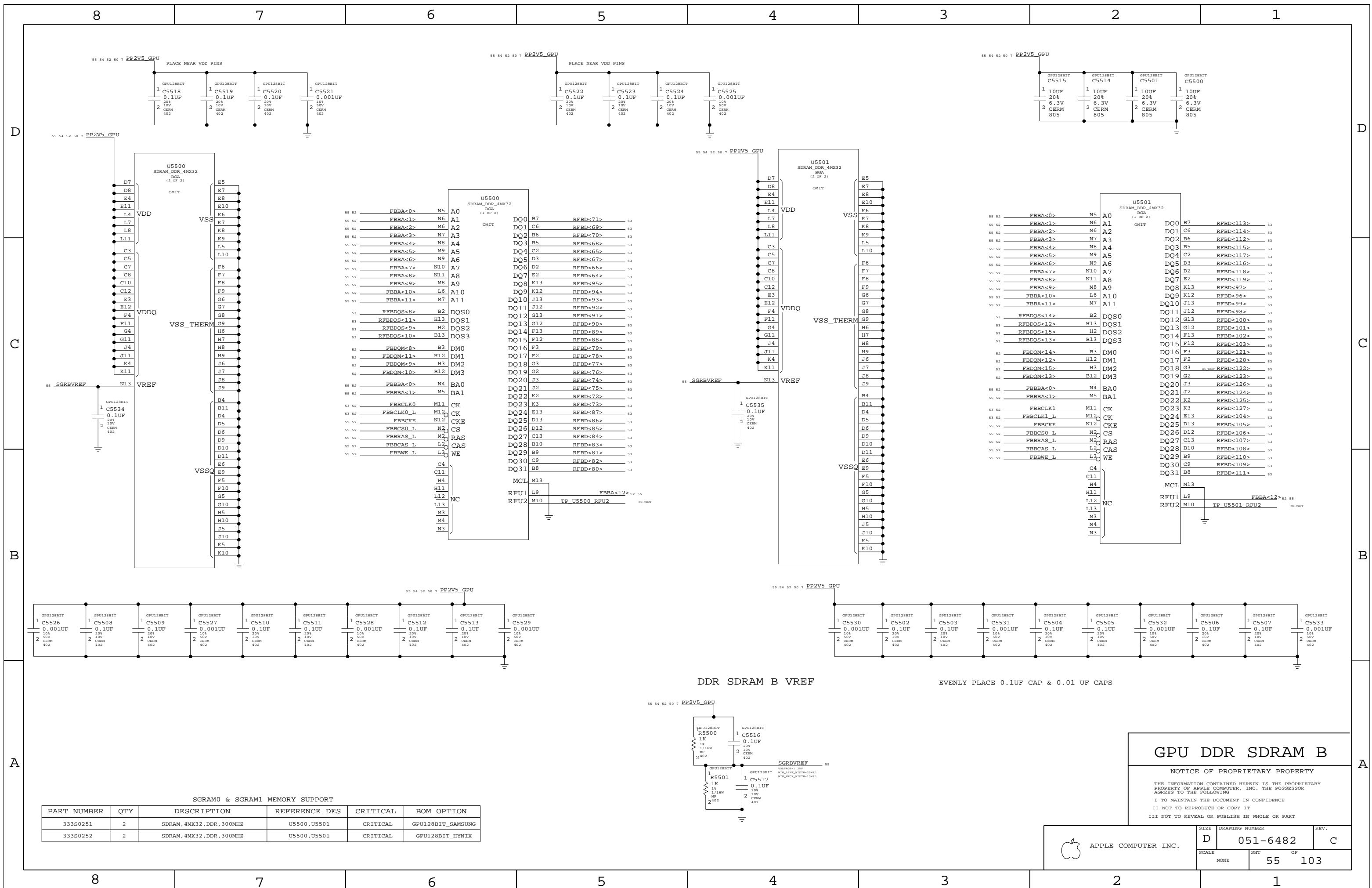
SHEET: 54 OF 103

REV: C

EVENLY PLACE 0.1UF CAP & 0.01UF CAPS

DDR SDRAM A VREF





D

C

B

A

D

C

B

A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

U5500 SDRAM\_DDR\_4MX32 BGA (1 OF 2)

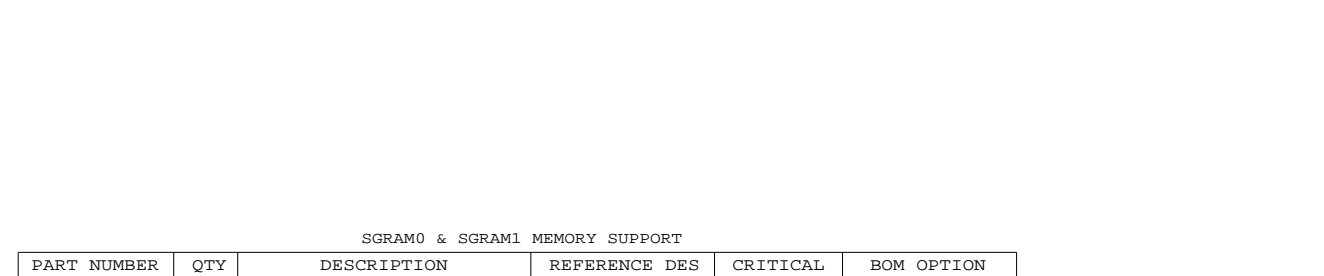
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		C11					
		H4					
		H11					
		L12					
		L13					
		M3					
		M4					
		N3					
		NC					
		RFU1	L9	FBBA<12>	52	55	
		RFU2	M10	TP U5500_RFU2			ML_TEST

U5501 SDRAM\_DDR\_4MX32 BGA (1 OF 2)

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55 52	FBBA<1>	N6	A1	DQ1	C6	RFBD<114>	53
55 52	FBBA<2>	M6	A2	DQ2	B6	RFBD<112>	53
55 52	FBBA<3>	N7	A3	DQ3	B5	RFBD<115>	53
55 52	FBBA<4>	N8	A4	DQ4	C2	RFBD<117>	53
55 52	FBBA<5>	M9	A5	DQ5	D3	RFBD<116>	53
55 52	FBBA<6>	N9	A6	DQ6	D2	RFBD<118>	53
55 52	FBBA<7>	N10	A7	DQ7	E2	RFBD<119>	53
55 52	FBBA<8>	M11	A8	DQ8	K13	RFBD<97>	53
55 52	FBBA<9>	M8	A9	DQ9	K12	RFBD<96>	53
55 52	FBBA<10>	L6	A10	DQ10	J13	RFBD<99>	53
55 52	FBBA<11>	M7	A11	DQ11	J12	RFBD<98>	53
53	RFBDQS<14>	B2	DQS0	DQ12	G13	RFBD<100>	53
53	RFBDQS<12>	H13	DQS1	DQ13	G12	RFBD<101>	53
53	RFBDQS<15>	H2	DQS2	DQ14	F13	RFBD<102>	53
53	RFBDQS<13>	B13	DQS3	DQ15	F12	RFBD<103>	53
52	FBDQM<14>	B3	DM0	DQ16	F3	RFBD<121>	53
52	FBDQM<12>	H12	DM1	DQ17	F2	RFBD<120>	53
52	FBDQM<15>	H3	DM2	DQ18	G3	RFBD<122>	53
52	FBDQM<13>	B12	DM3	DQ19	G2	RFBD<123>	53
55 52	FBBA<0>	N4	BA0	DQ20	J3	RFBD<126>	53
55 52	FBBA<1>	M5	BA1	DQ21	J2	RFBD<124>	53
55 52	FBBA<2>	K2	RFBD<125>	DQ22	K2	RFBD<125>	53
55 52	FBBA<3>	M11	CK	DQ23	K3	RFBD<127>	53
55 52	FBBA<4>	L	M12	DQ24	E13	RFBD<104>	53
55 52	FBBA<5>	N12	CK	DQ25	D13	RFBD<105>	53
55 52	FBBA<6>	N2	CSE	DQ26	D12	RFBD<106>	53
55 52	FBBA<7>	M2	RAS	DQ27	C13	RFBD<107>	53
55 52	FBBA<8>	L2	CAS	DQ28	B10	RFBD<108>	53
55 52	FBBA<9>	L3	CAS	DQ29	B9	RFBD<110>	53
55 52	FBBA<10>	L3	WE	DQ30	C9	RFBD<109>	53
55 52	FBBA<11>	L3	WE	DQ31	B8	RFBD<111>	53
		C4					
		C11					
		H4					
		H11					
		L12					
		L13					
		M3					
		M4					
		N3					
		NC					
		RFU1	L9	FBBA<12>	52	55	
		RFU2	M10	TP U5501_RFU2			ML_TEST



DDR SDRAM B VREF EVENLY PLACE 0.1UF CAP & 0.01 UF CAPS



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33380251	2	SDRAM, 4MX32, DDR, 300MHZ	U5500, U5501	CRITICAL	GPU128BIT_SAMSUNG
33380252	2	SDRAM, 4MX32, DDR, 300MHZ	U5500, U5501	CRITICAL	GPU128BIT_HYNIX

**GPU DDR SDRAM B**

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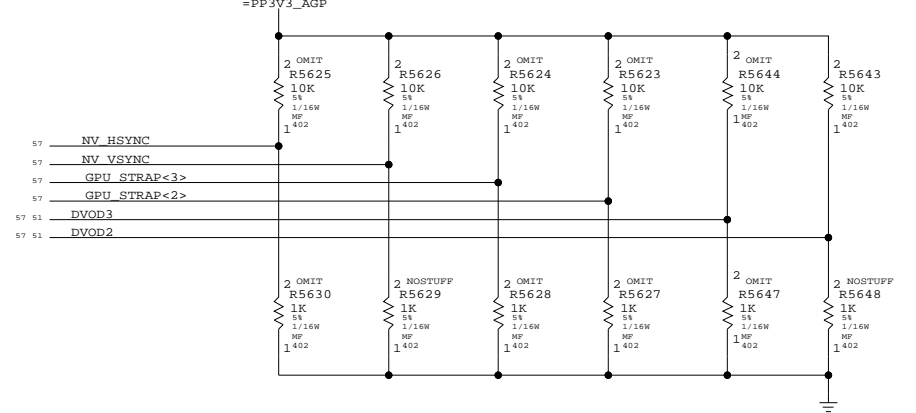
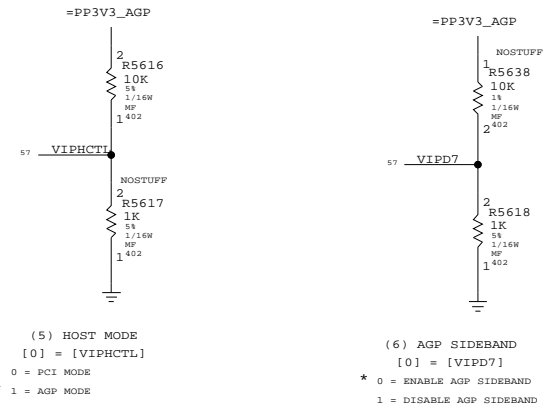
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	NONE	D 051-6482	C
SHEET		OF	
55		103	

D

D

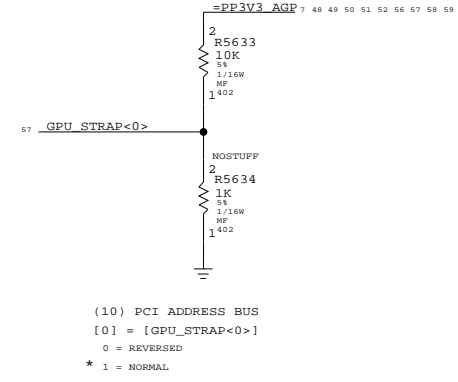
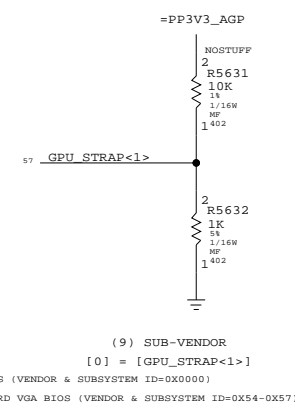
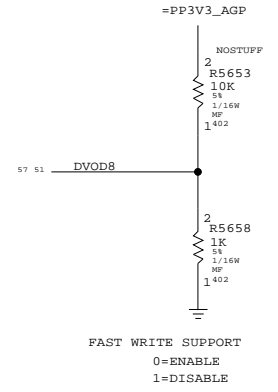
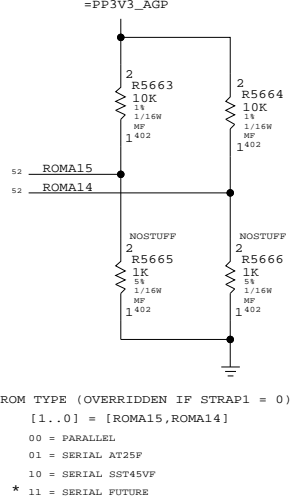


(8) FRAME BUFFER MEMORY SPEED  
[5..0] = [NV11\_HSYNC, NV11\_VSYNC, GPU\_STRAP<3>, GPU\_STRAP<2>, DVOD3, DVOD2]

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
<b>110111 = 270MHZ SAMSUNG (NV18B)</b>					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5623		270MHZ_SAM_18
116S1104	1	RES,10K-OHM,1/16W,5%	R5644		270MHZ_SAM_18
116S1103	1	RES,1K-OHM,1/16W,5%	R5628		270MHZ_SAM_18
<b>110011 = 270MHZ HYNIX (NV18B)</b>					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5644		270MHZ_HYN_18
116S1103	2	RES,1K-OHM,1/16W,5%	R5628,R5627		270MHZ_HYN_18
<b>111101 = 270MHZ SAMSUNG (NV34)</b>					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5624		270MHZ_SAM_34
116S1104	1	RES,10K-OHM,1/16W,5%	R5623		270MHZ_SAM_34
116S1103	1	RES,1K-OHM,1/16W,5%	R5647		270MHZ_SAM_34
<b>111100 = 270MHZ HYNIX (NV34)</b>					
116S1104	2	RES,10K-OHM,1/16W,5%	R5624,R5623		270MHZ_HYN_34
116S1103	2	RES,1K-OHM,1/16W,5%	R5630,R5647		270MHZ_HYN_34

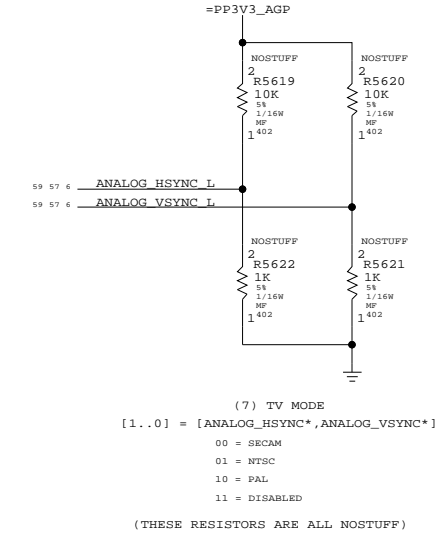
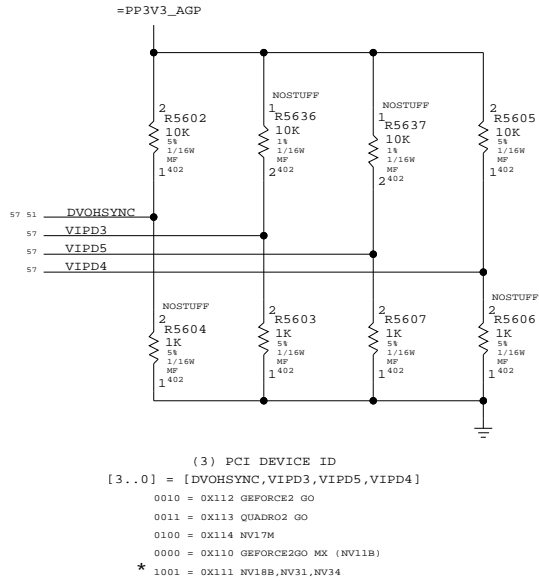
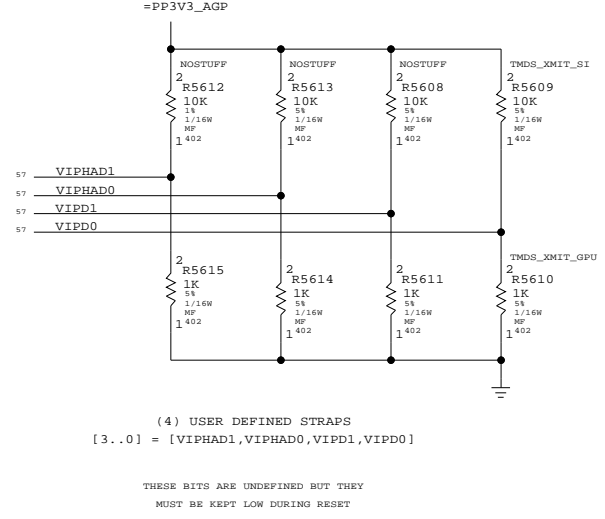
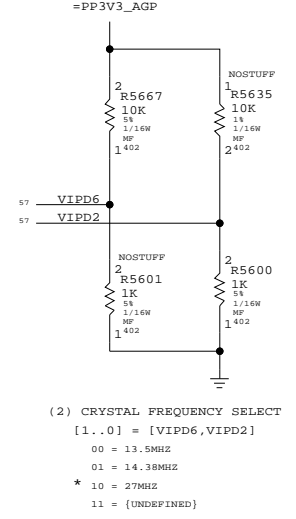
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**NVIDIA STRAPS**

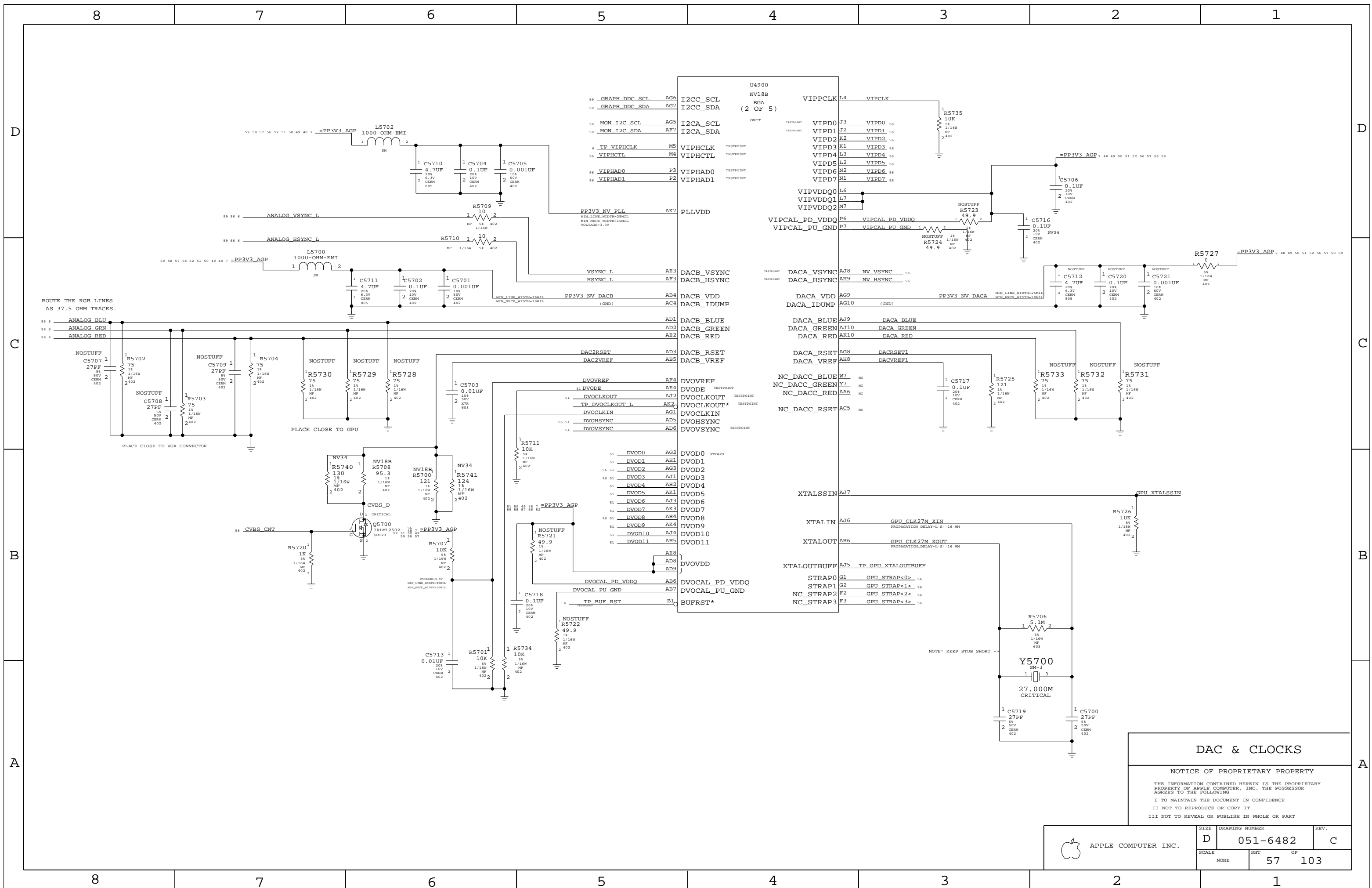
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**DAC & CLOCKS**

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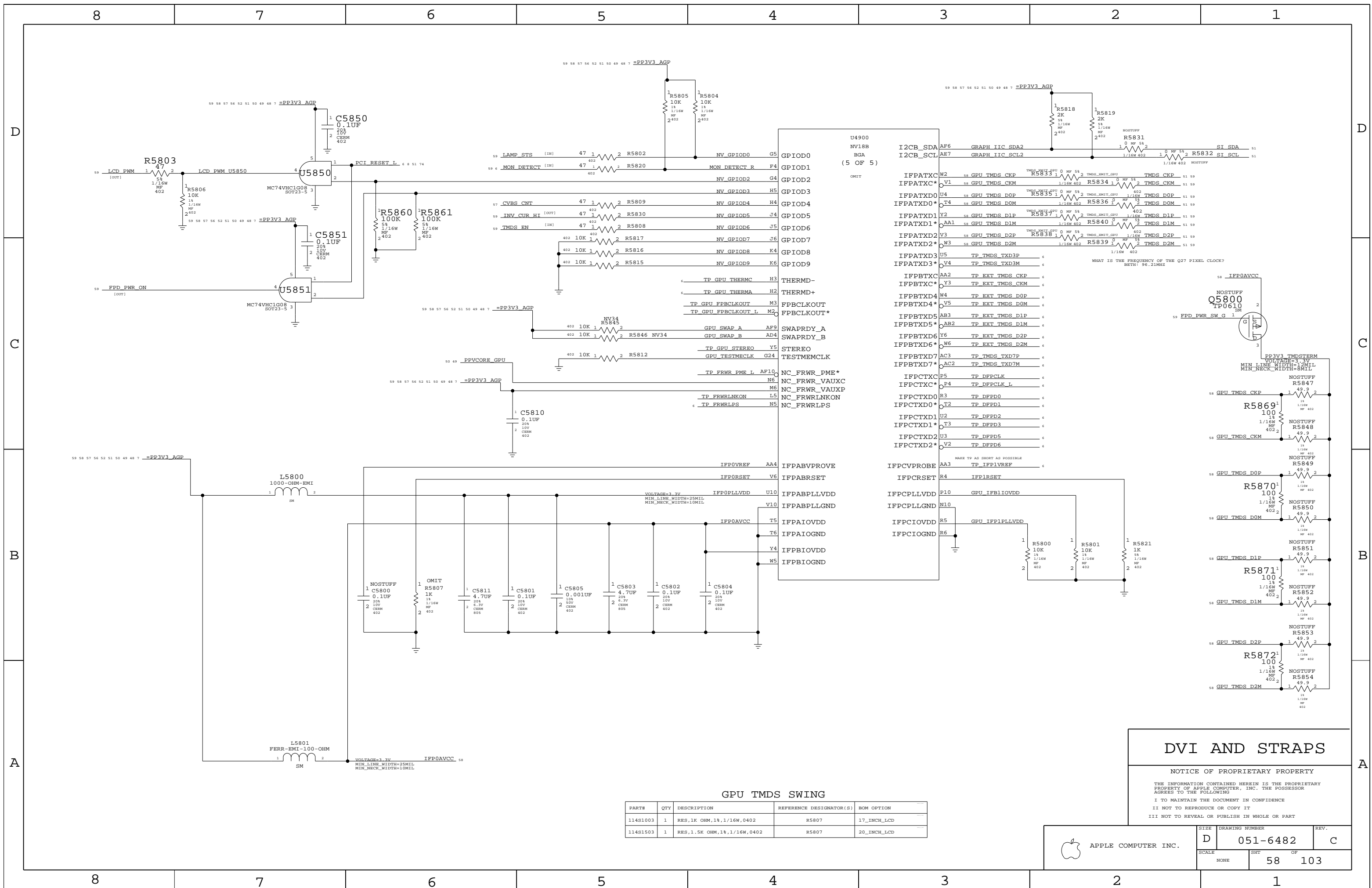
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SCALE NONE	SHEET 57	OF 103	





**DVI AND STRAPS**

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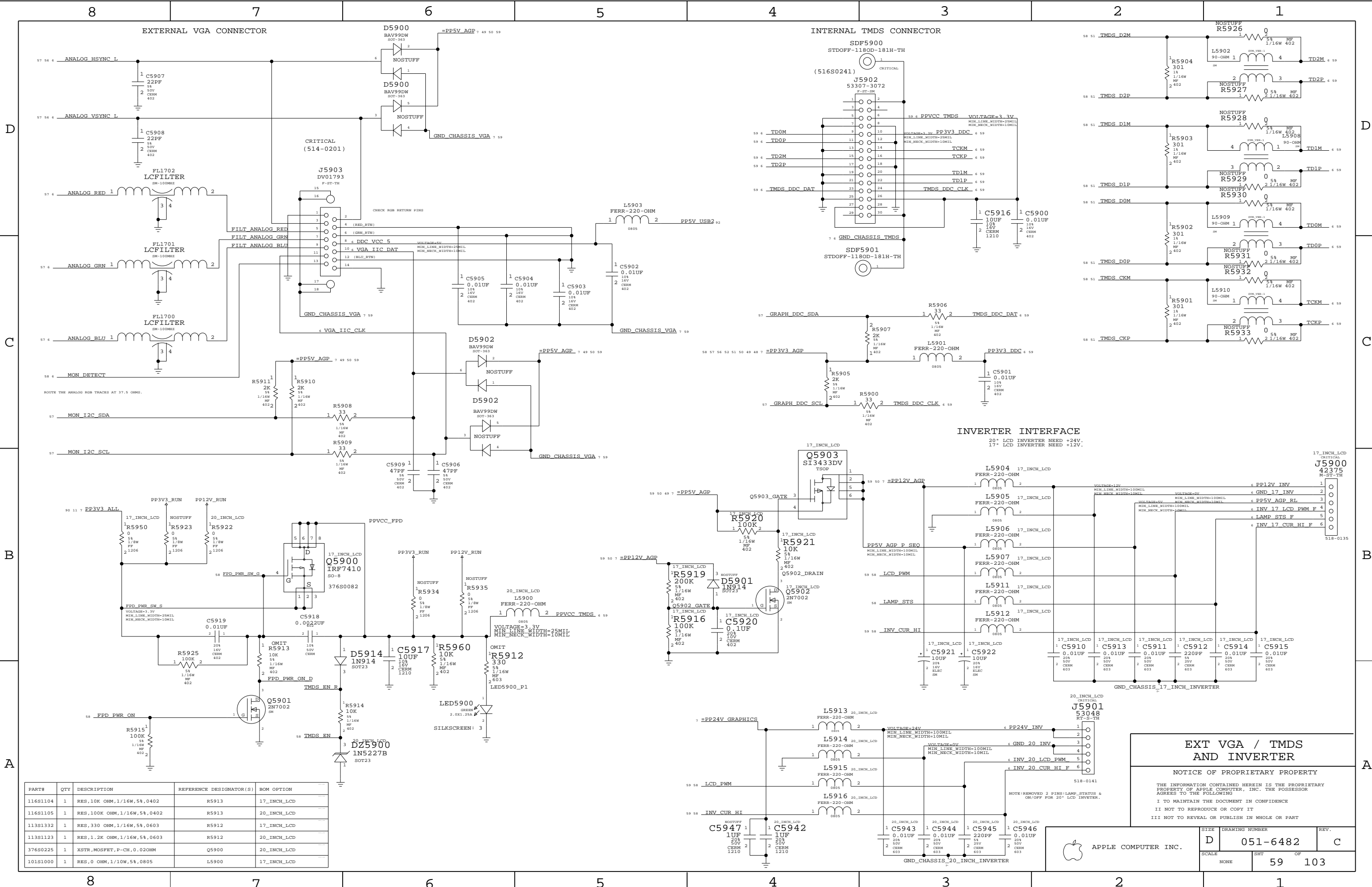
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	D	051-6482	C
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,10K OHM,1/16W,5%,0402	R5913	17_INCH_LCD
116S1105	1	RES,100K OHM,1/16W,5%,0402	R5913	20_INCH_LCD
113S1332	1	RES,330 OHM,1/16W,5%,0603	R5912	17_INCH_LCD
113S1123	1	RES,1.2K OHM,1/16W,5%,0603	R5912	20_INCH_LCD
376S0225	1	XSTR.MOSFET,P-CH,0.020OHM	Q5900	20_INCH_LCD
101S1000	1	RES,0 OHM,1/10W,5%,0805	L5900	17_INCH_LCD

**EXT VGA / TMD5 AND INVERTER**

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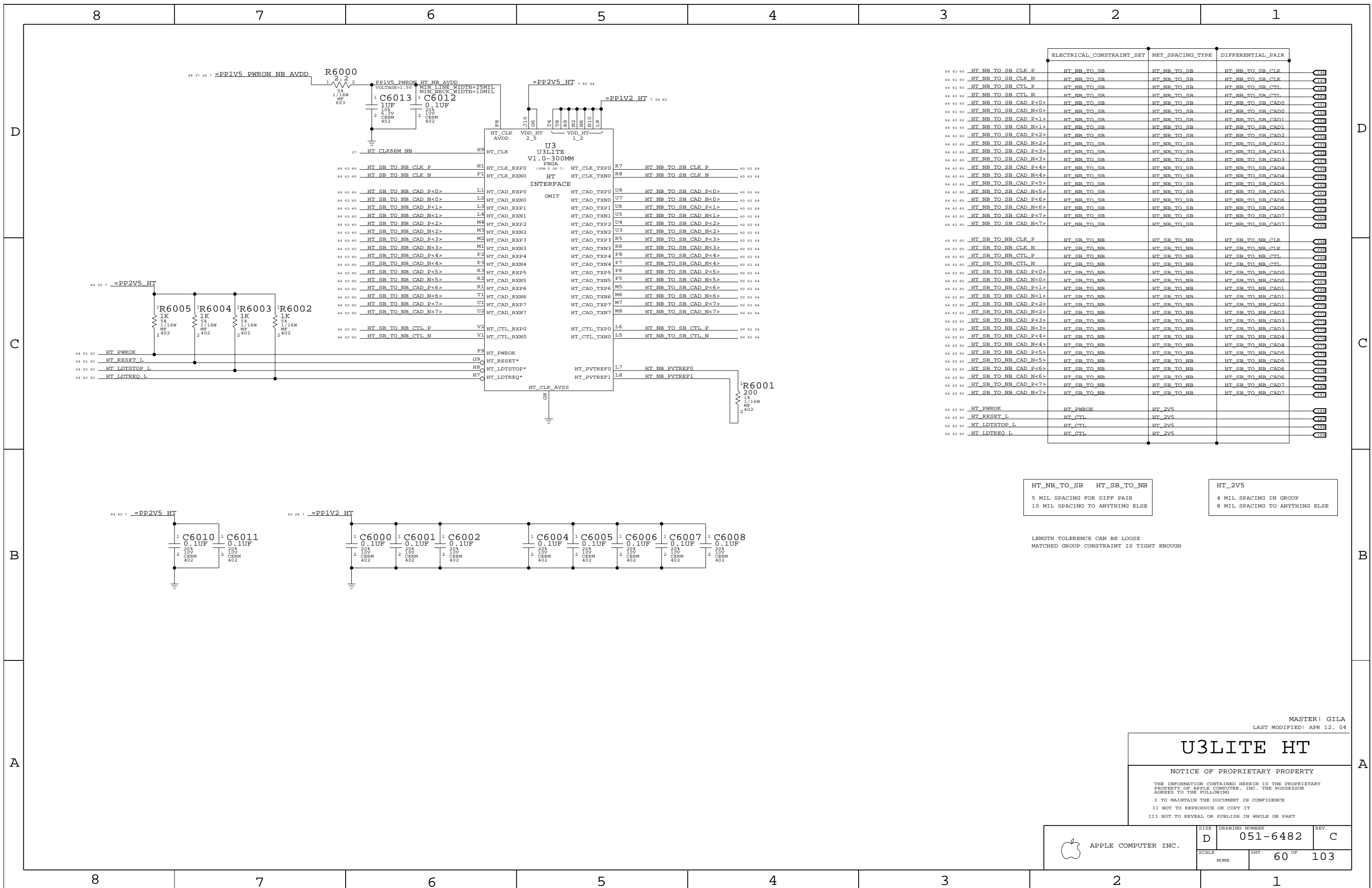
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		D	051-6482	C
SCALE	NONE	SHEET	59	OF 103



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_NB_TO_SB_CLK
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_NB_TO_SB_CLK
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_NB_TO_SB_CTL
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_NB_TO_SB_CTL
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_NB_TO_SB_CAD0
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_NB_TO_SB_CAD0
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_NB_TO_SB_CAD1
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_NB_TO_SB_CAD1
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_NB_TO_SB_CAD2
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_NB_TO_SB_CAD2
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_NB_TO_SB_CAD3
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_NB_TO_SB_CAD3
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_NB_TO_SB_CAD4
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_NB_TO_SB_CAD4
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_NB_TO_SB_CAD5
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_NB_TO_SB_CAD5
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_NB_TO_SB_CAD6
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_NB_TO_SB_CAD6
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_NB_TO_SB_CAD7
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_NB_TO_SB_CAD7
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_SB_TO_NB_CLK
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_SB_TO_NB_CLK
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_SB_TO_NB_CTL
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HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_SB_TO_NB_CAD1
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_SB_TO_NB_CAD1
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_SB_TO_NB_CAD2
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_SB_TO_NB_CAD2
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_SB_TO_NB_CAD3
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_SB_TO_NB_CAD3
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_SB_TO_NB_CAD4
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_SB_TO_NB_CAD4
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_SB_TO_NB_CAD5
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_SB_TO_NB_CAD5
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_SB_TO_NB_CAD6
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_SB_TO_NB_CAD6
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_SB_TO_NB_CAD7
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_SB_TO_NB_CAD7
HT_PWROK	HT_PWROK	HT_2V5
HT_RESET_L	HT_CTL	HT_2V5
HT_LDTSTOP_L	HT_CTL	HT_2V5
HT_LDTREQ_L	HT_CTL	HT_2V5

HT\_NB\_TO\_SB HT\_SB\_TO\_NB  
 5 MIL SPACING FOR DIFF PAIR  
 10 MIL SPACING TO ANYTHING ELSE

HT\_2V5  
 4 MIL SPACING IN GROUP  
 8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERANCE CAN BE LOOSE  
 MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: GILA  
 LAST MODIFIED: APR 12, 04

# U3LITE HT

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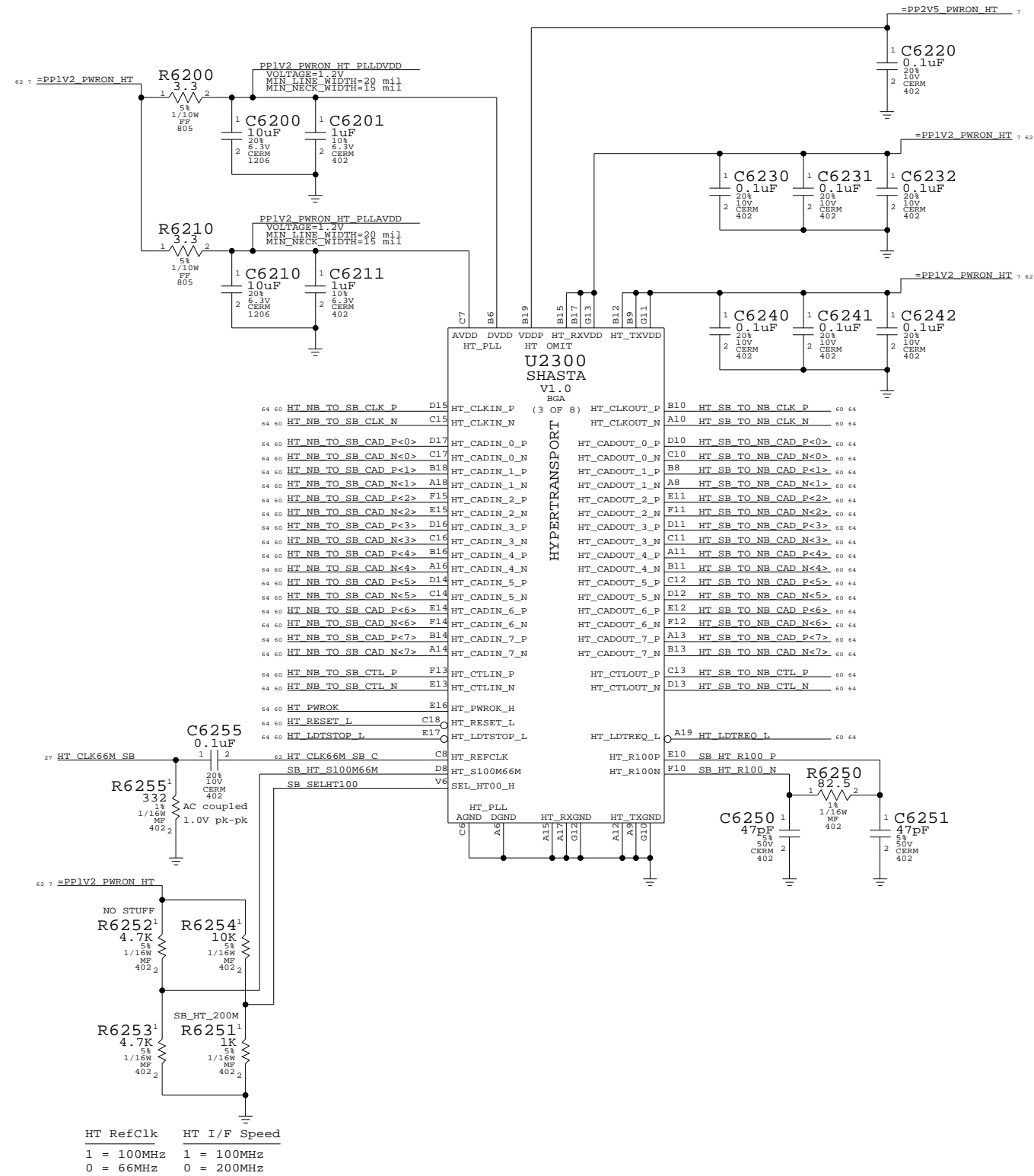
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	60 OF	103
NONE			

# Page Notes

Power aliases required by this page:  
 - \_PP2V5\_PWRON\_HT  
 - \_PP1V2\_PWRON\_HT

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - SB\_HT\_200M  
 Stuffs resistor to select 200MHz HT I/F.



Master: Link

## Shasta HyperTransport

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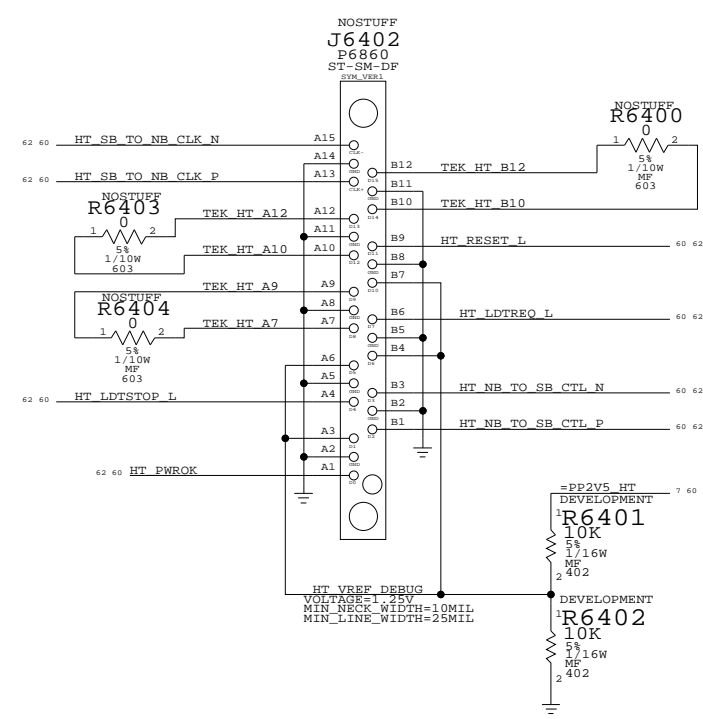
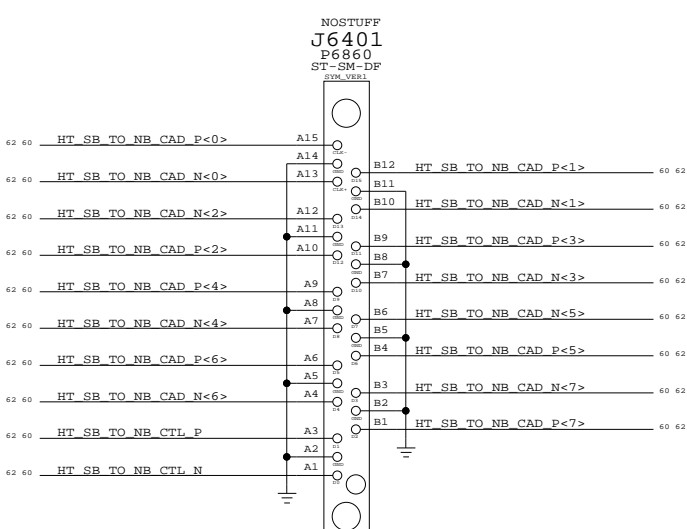
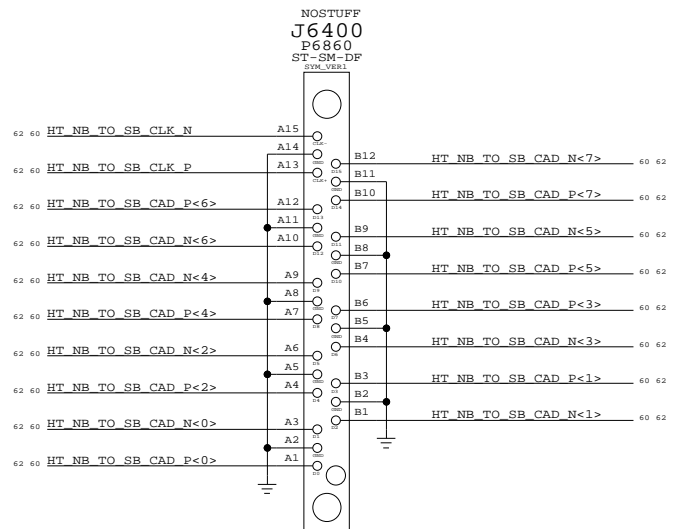
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SAME CONNECTORS & PINOUT AS  
Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2



MASTER: GILA  
LAST MODIFIED: APR 12, 04

## HT DEBUG CONN

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	SCALE NONE	SHT 64 OF	103

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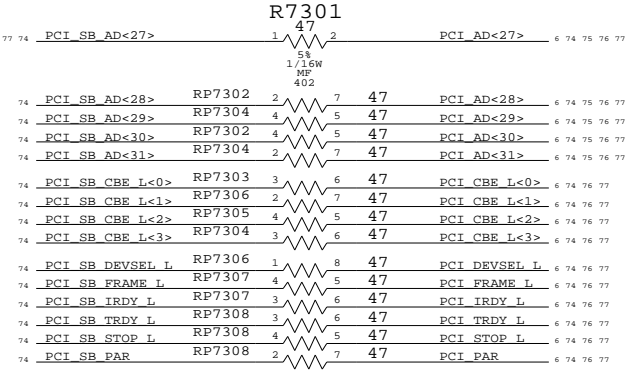
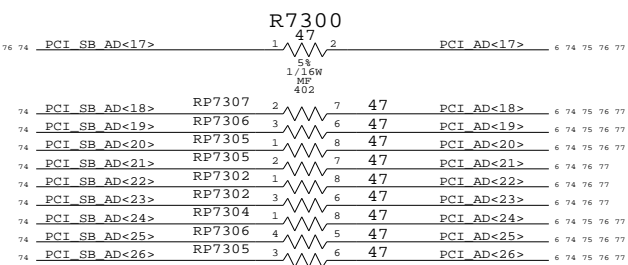
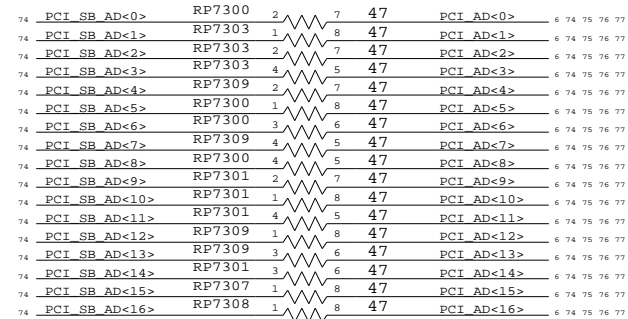
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ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)



PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT  
AD<27> IS IDSEL FOR USB

### PCI SERIES TERMINATION


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	D	051-6482	C
SCALE	SHT	73 OF 103	
NONE			

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_AD		
PCI_AD27		
PCI_AD		
PCI_AD23		
PCI_AD22		
PCI_AD21		
PCI_AD20		
PCI_AD		
PCI_AD17		
PCI_AD		
PCI		
PCI		
PCI_CTT1		
PCI_CTT1		
PCI_CTT1		
PCI_CTT1		
PCI_CTT1		

PCI_AD<31..28>	6 73 75 76 77
PCI_AD<27>	6 73 75 76 77
PCI_AD<26..24>	6 73 75 76 77
PCI_AD<23>	6 73 76 77
PCI_AD<22>	6 73 76 77
PCI_AD<21>	6 73 76 77
PCI_AD<20>	6 73 75 76 77
PCI_AD<19..18>	6 73 75 76 77
PCI_AD<17>	6 73 75 76 77
PCI_AD<16..0>	6 73 75 76 77
PCI_CBE L<3..0>	6 73 76 77
PCI_PAR	6 73 76 77
PCI_DEVSEL L	6 73 74 76 77
PCI_FRAME L	6 73 74 76 77
PCI_IRDY L	6 73 74 76 77
PCI_TRDY L	6 73 74 76 77
PCI_STOP L	6 73 74 76 77

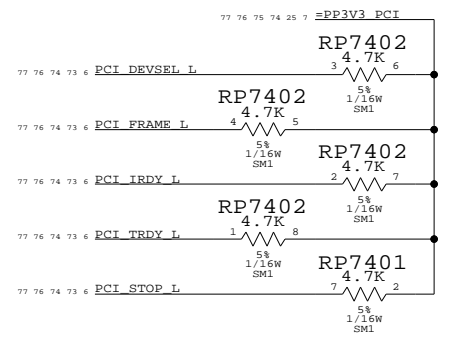
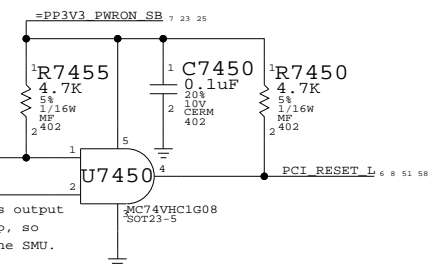
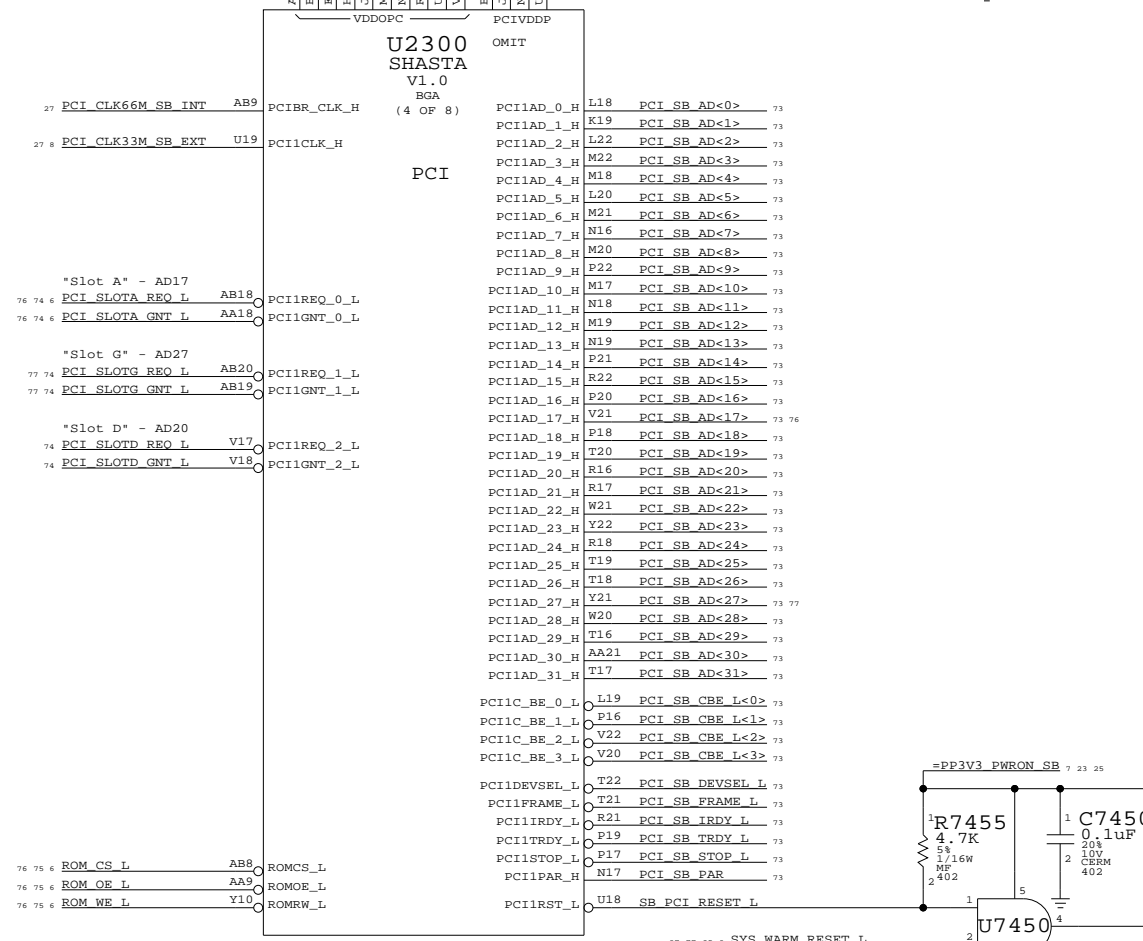
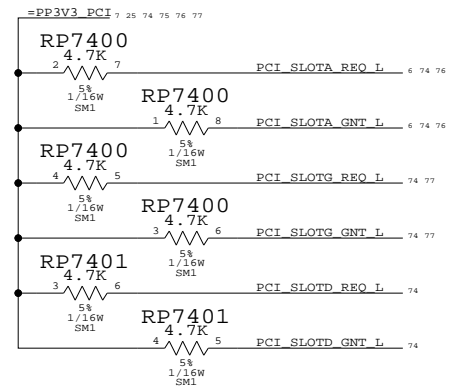
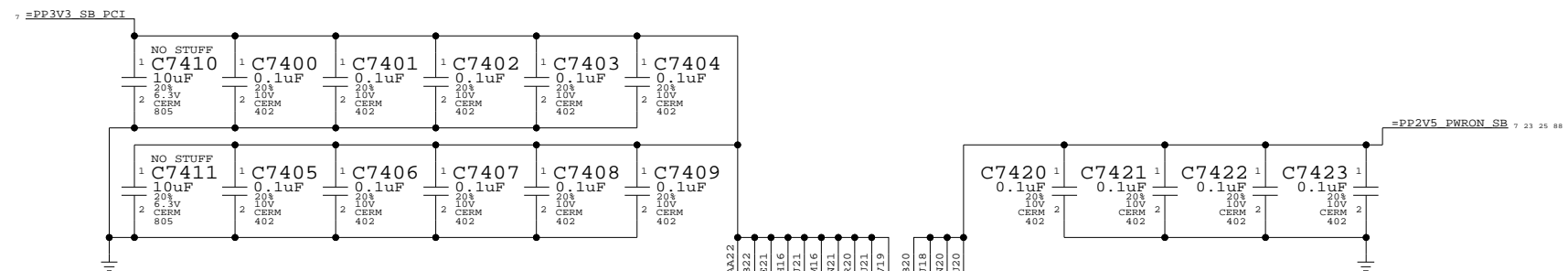
### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PCI  
 - \_PP3V3\_SB\_PCI (can be \_PP3V3\_PCI)  
 - \_PP3V3\_PWRON\_SB  
 - \_PP2V5\_PWRON\_SB

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

PCI Devices implemented on this page:  
 AD11 - PCI0 (0x106B/0x0053)  
 AD11 - PCI1 (0x106B/0x0054)  
 AD11 - PCI2 (0x106B/0x0055)  
 AD23 - KeyLargo (0x106B/0x004F, PCI1)  
 AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)  
 AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)  
 AD30 - FireWire (0x106B/0x0052, PCI0 or 2)  
 AD31 - Ethernet (0x106B/0x0051, PCI0)



## Shasta PCI Interface

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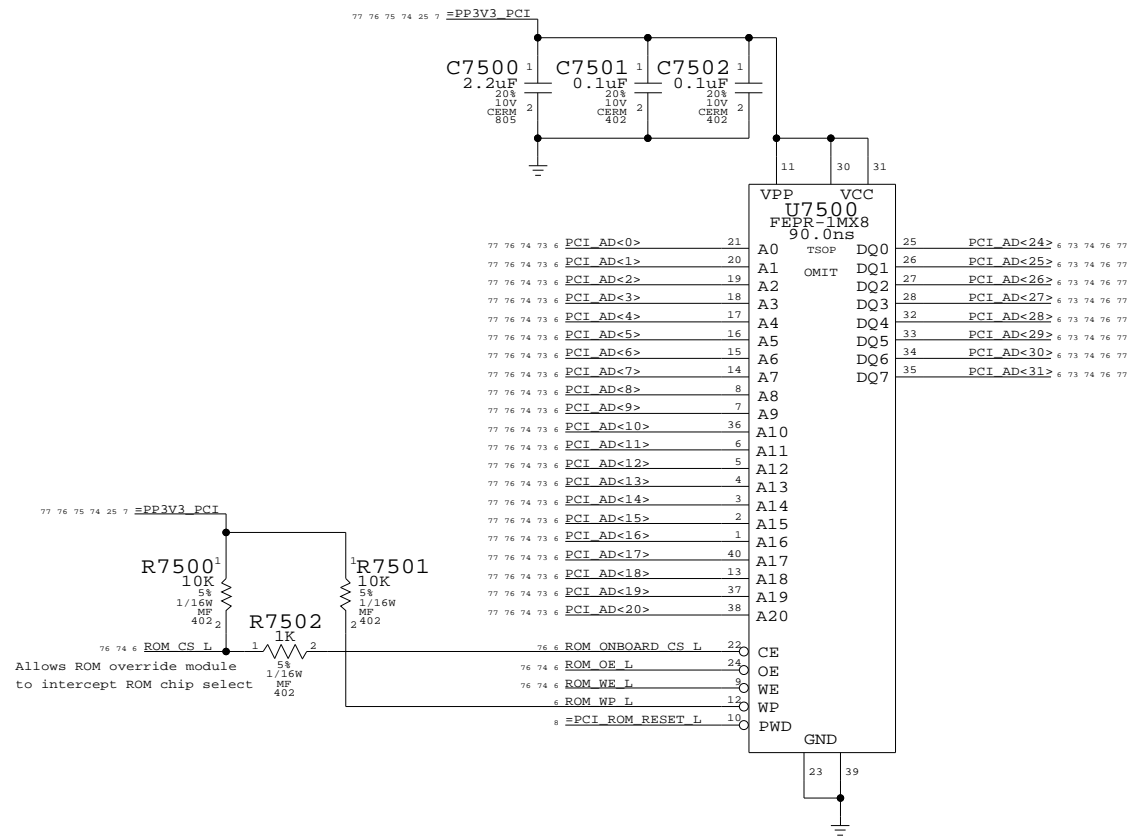
# Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PCI

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE\_x\_ITEM symbol to declare U7500 part number.



Master: Link

## BootROM

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\_DRAWING  
 TITLE=FIZZY  
 ABBREV=DRAWING  
 LAST\_MODIFIED=Wed Aug 4 17:58:24 2004

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	OF	
NONE	75	103	



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	PCI_CLK33M_AIRPORT

# Page Notes

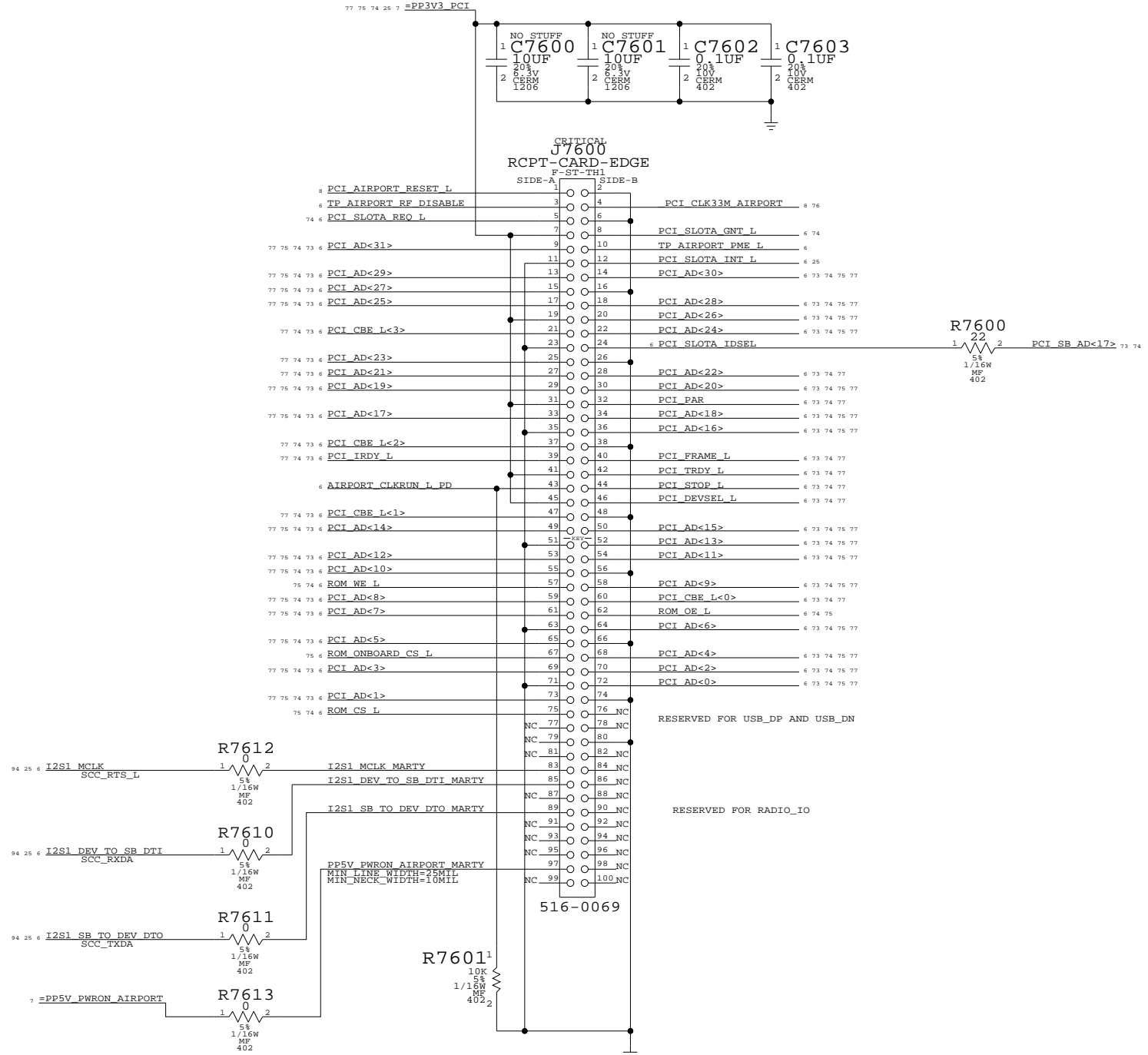
Power aliases required by this page:  
 - \_PP3V3\_PCI

Signal aliases required by this page:  
 - \_PCI\_CLK33M\_AIRPORT (33MHz PCI clock)

BOM options provided by this page:  
 (NONE)

PCI Devices implemented on this page:  
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



**AirPort Extreme**

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	D	051-6482	C
SCALE	SHT	OF	
NONE	76	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	=PCI_CLK33M_USB2

# Page Notes

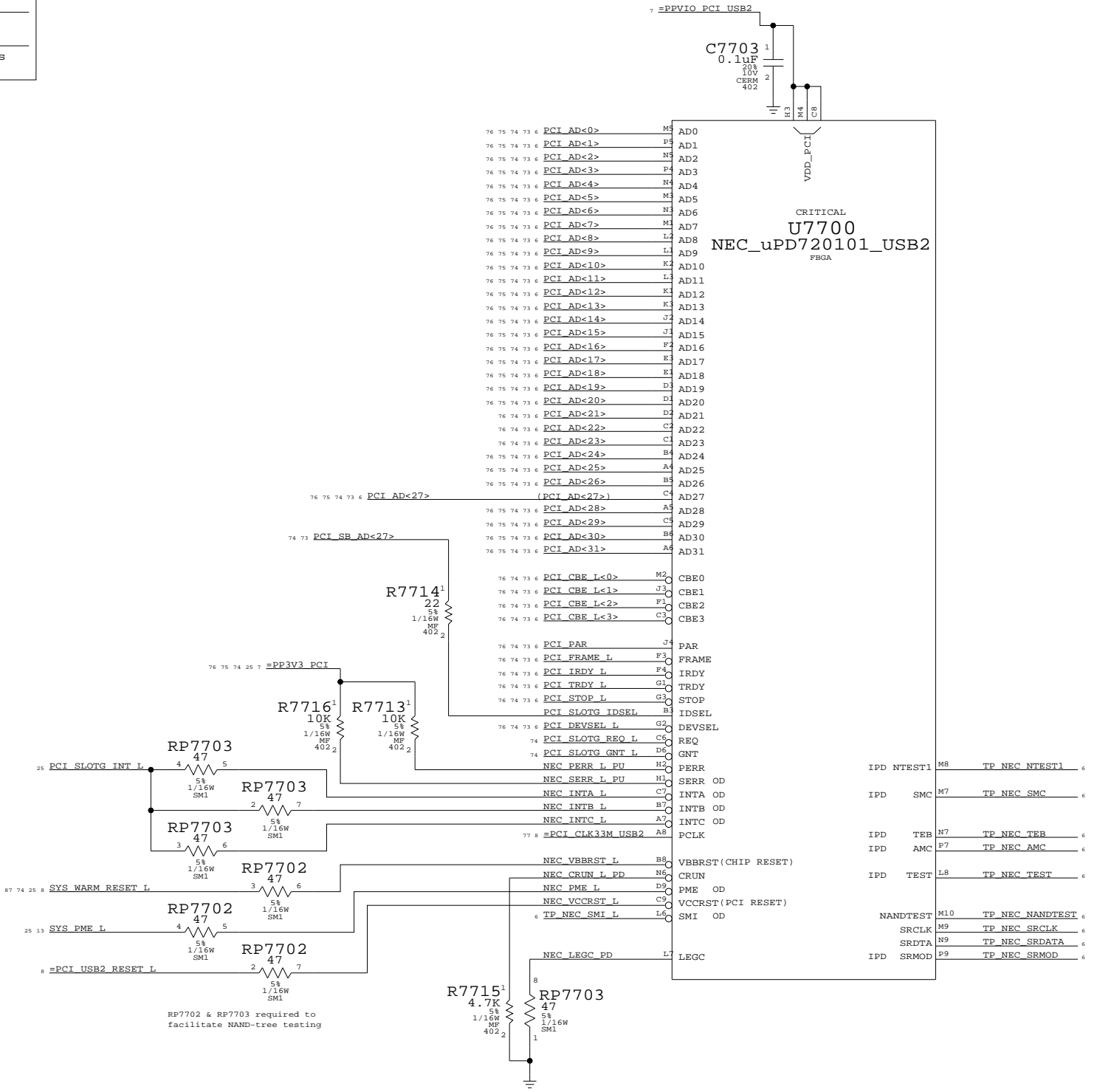
Power aliases required by this page:  
 - \_PPVIO\_PCI (to 3.3V or 5V)

Signal aliases required by this page:  
 - \_PCI\_CLK33M\_USB2 (33MHz PCI clock)

BOM options provided by this page:  
 (NONE)

PCI Devices implemented on this page:  
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



Master: Link

## USB 2.0 PCI Interface

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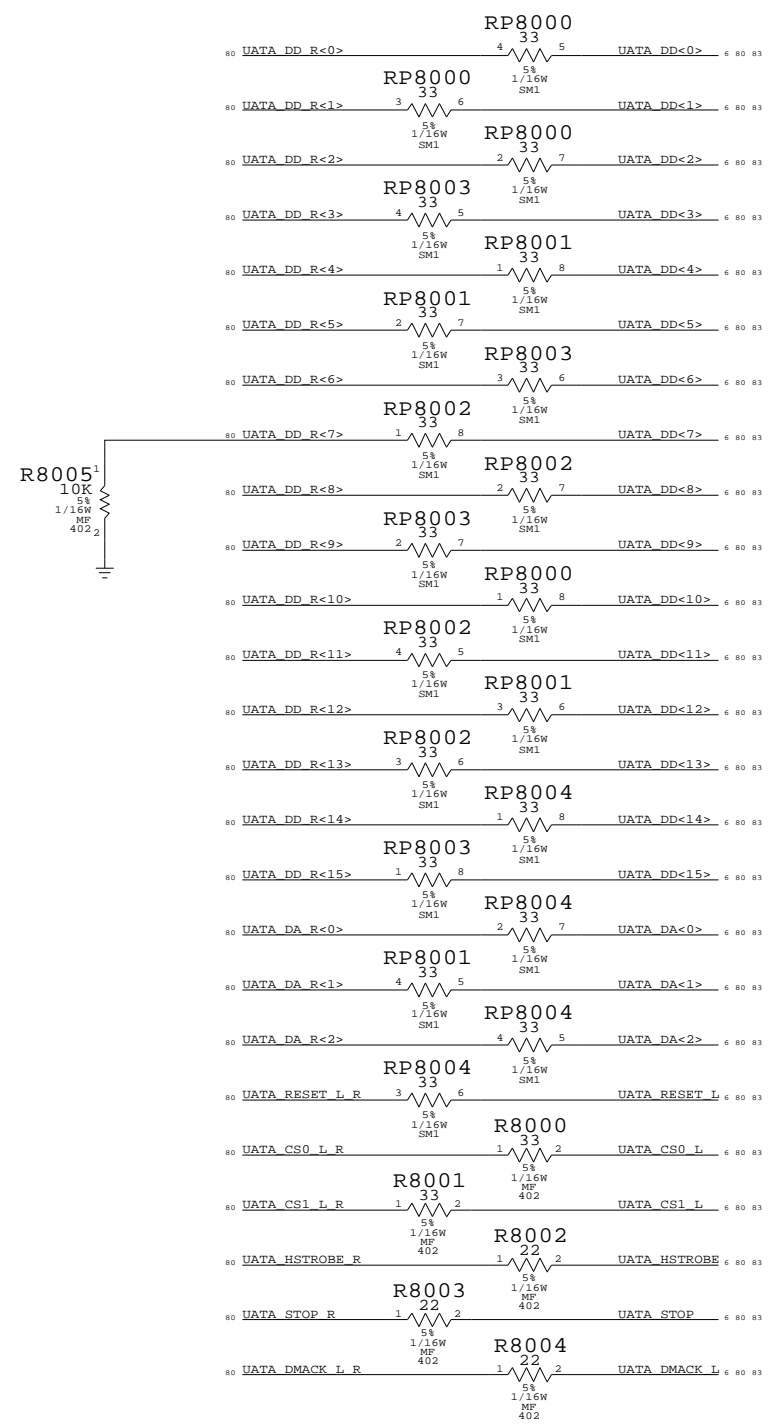
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	D	051-6482	C
SCALE	SHT	OF	
NONE	77	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD			UATA_DD<15..8>
UATA_DD7			UATA_DD<7>
UATA_DD			UATA_DD<6..0>
UATA_HOST			UATA_DA<2..0>
UATA_HOST			UATA_CS0_L
UATA_HOST			UATA_CS1_L
UATA_HOST			UATA_HSTROBE
UATA_HOST			UATA_STOP
UATA_HOST_R			UATA_DMACK_L
UATA_HOST_R			UATA_RESET_L
UATA_DEV_R_C			UATA_DSTROBE
UATA_DEV_R			UATA_DMARQ
UATA_DEV_R			UATA_INTRO

### UATA Termination



### Page Notes

Power aliases required by this page:  
 - \_PP1V2\_PWRON\_DISK

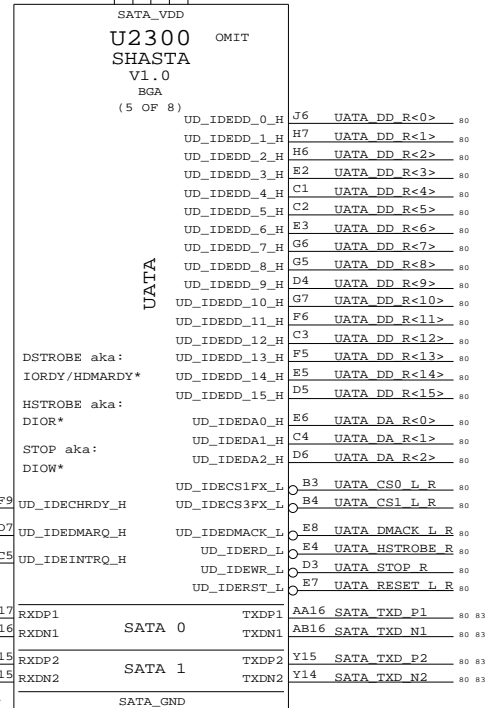
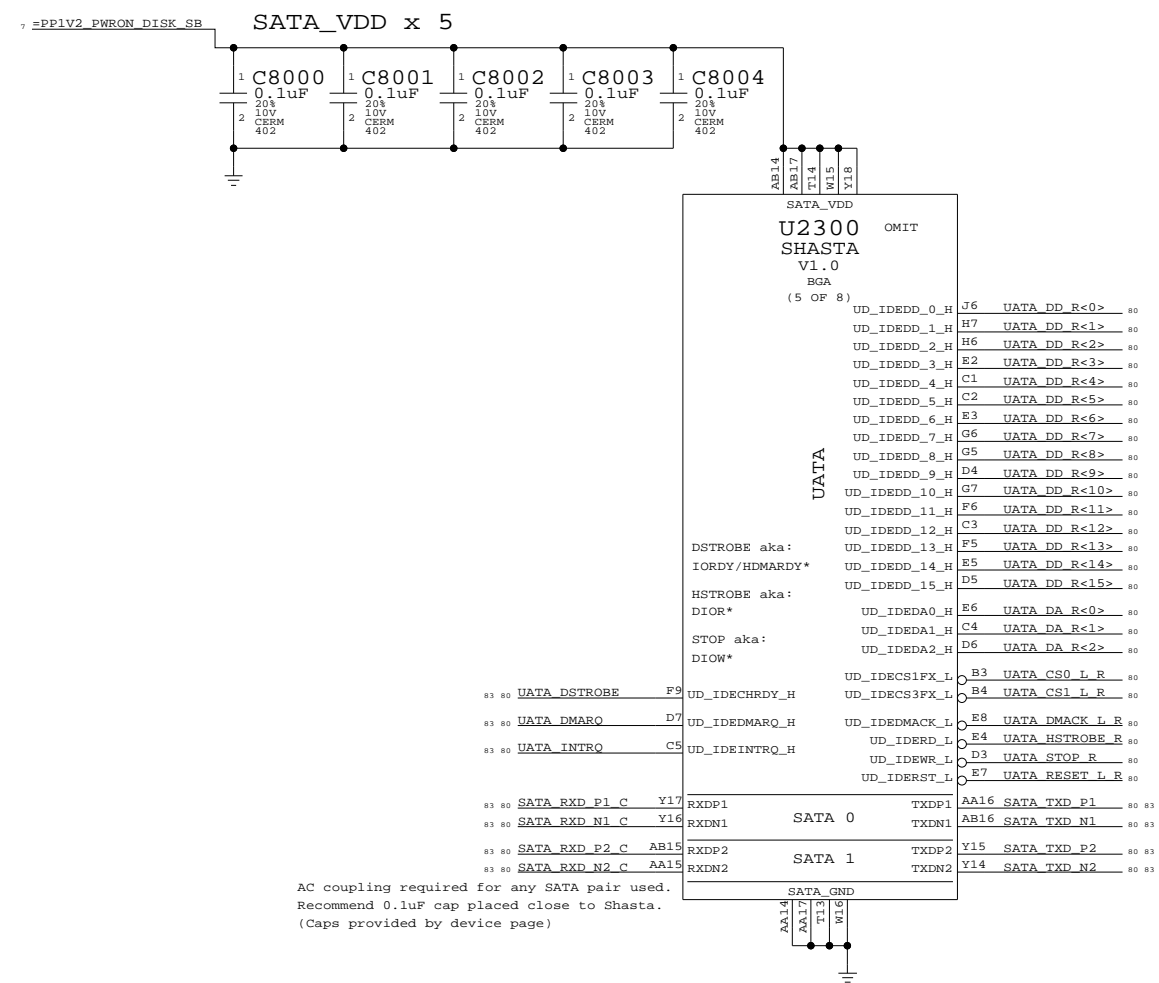
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

**Net Spacing Type: SATA**

Line To Line: 15 mils  
 Length Tolerance: 50 mils  
 Primary Max Sep: 10 mils outer  
 Primary Max Sep: 9 mils inner  
 Secondary Max Sep: 100 mils  
 Secondary Length: 500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.



AC coupling required for any SATA pair used.  
 Recommend 0.1uF cap placed close to Shasta.  
 (Caps provided by device page)

Master: Link

### Shasta Disk

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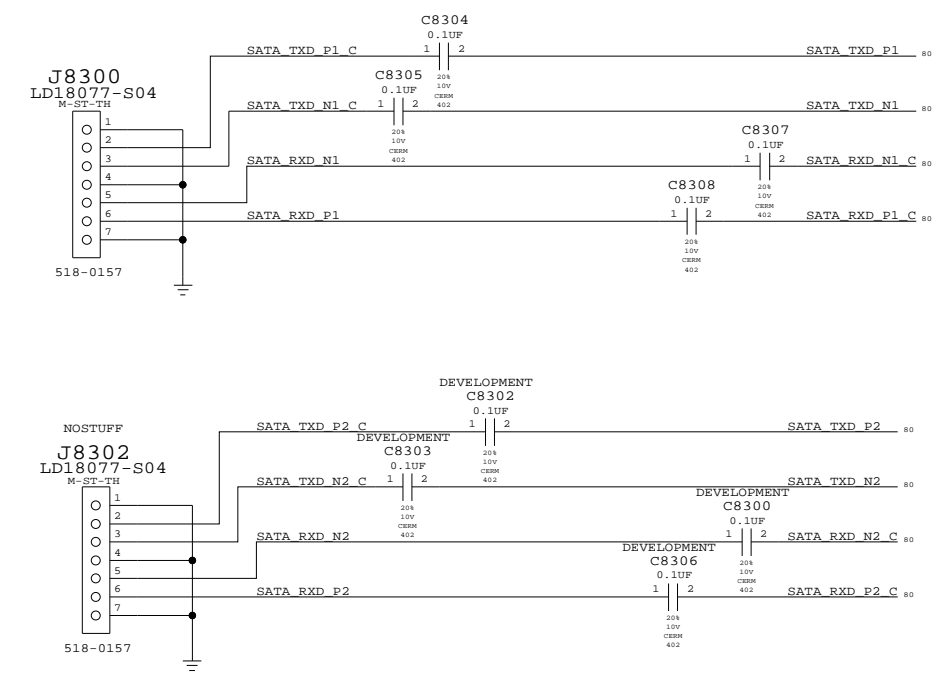
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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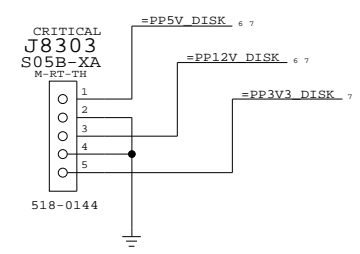
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	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
83 80 6 UATA_DD<15..8>		UATA_DD		
83 80 6 UATA_DD<7>		UATA_DD7		
83 80 6 UATA_DD<6..0>		UATA_DD		
83 80 6 UATA_DA<2..0>		UATA_HOST		
83 80 6 UATA_CS0_L		UATA_HOST		
83 80 6 UATA_CS1_L		UATA_HOST		
83 80 6 UATA_HSTROBE		UATA_HOST		
83 80 6 UATA_STOP		UATA_HOST		
83 80 6 UATA_DMACK_L		UATA_HOST_R		
83 80 6 UATA_RESET_L		UATA_HOST_R		
83 80 6 UATA_DSTROBE		UATA_DEV_R_C		
83 80 6 UATA_DMARQ		UATA_DEV_R		
83 80 6 UATA_INTRO		UATA_DEV_R		

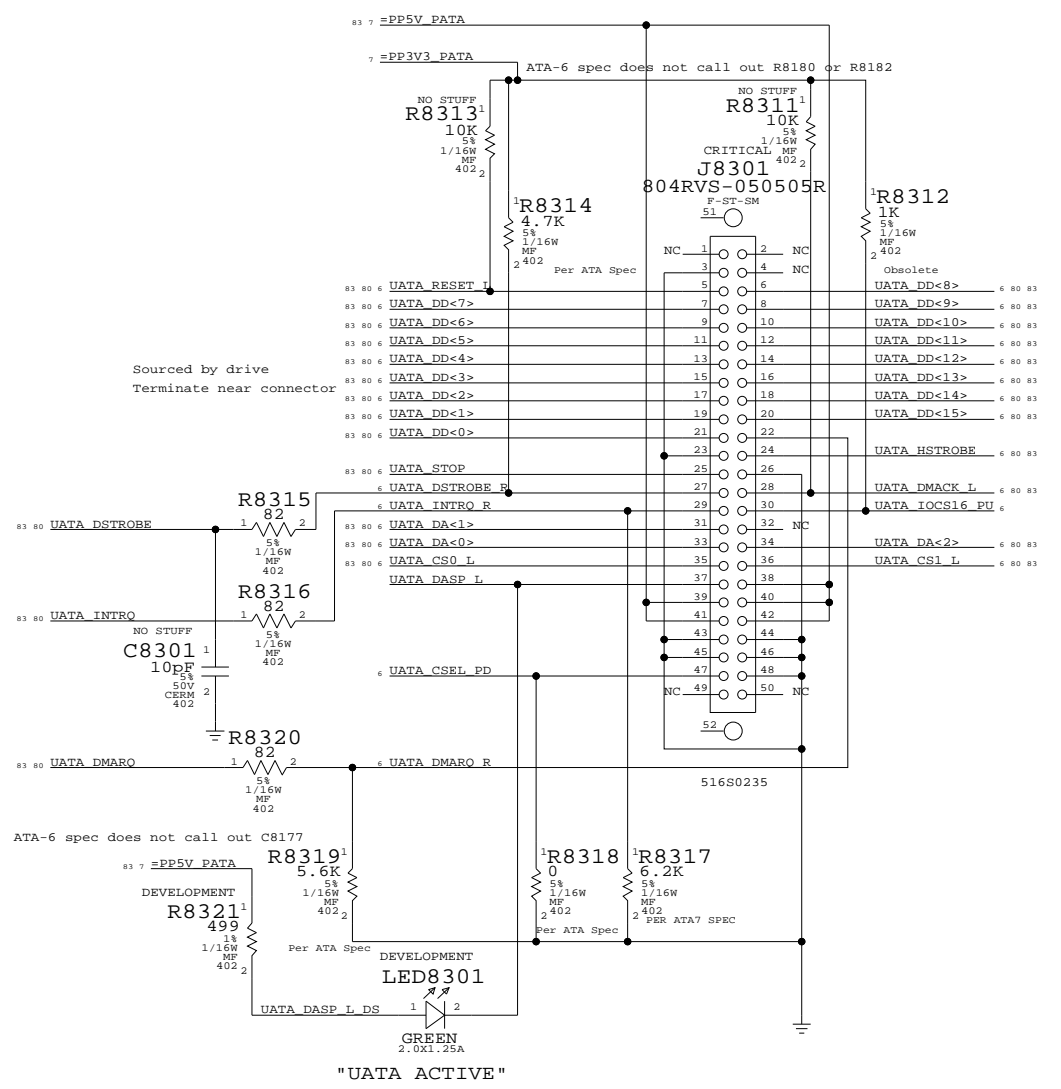
SATA CONNECTORS



HD POWER



PATA CONNECTOR



DISK CONNECTORS

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	D	051-6482	C
SCALE	NONE	SHT OF	83 OF 103

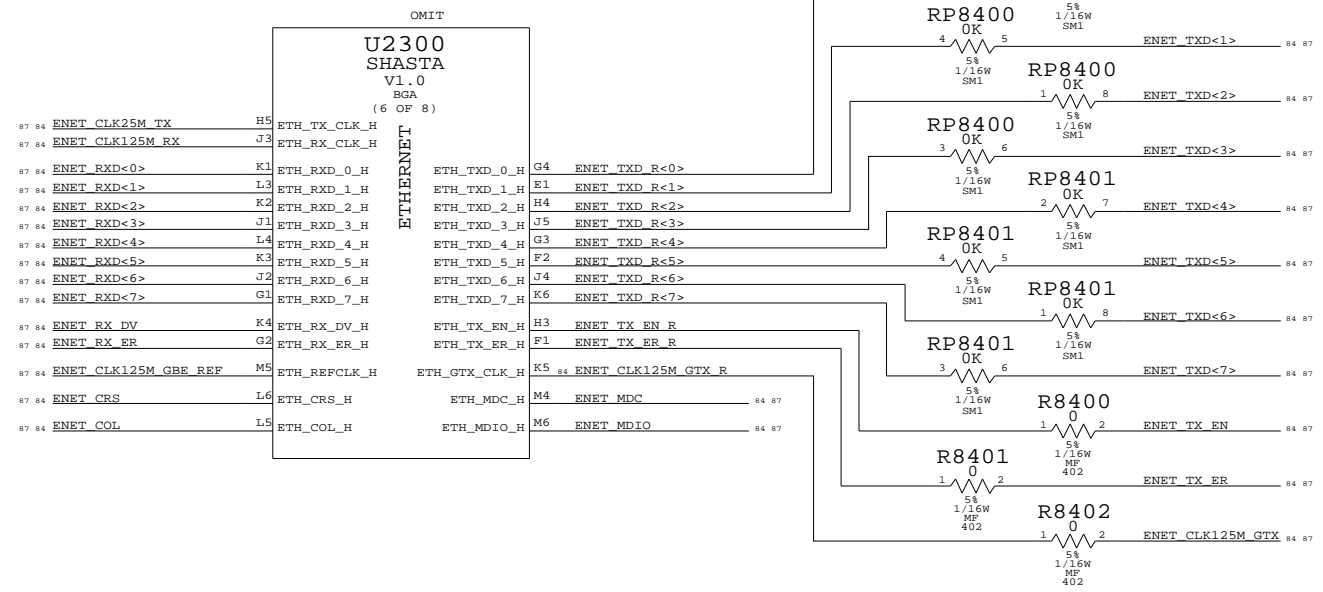
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_RX_CLK	ENET	10 MIL	ENET_CLK25M_TX
ENET_RX_CLK	ENET	10 MIL	ENET_CLK125M_RX
ENET_GBE_REF	ENET	15 MIL SPACING	ENET_CLK125M_GBE_REF
ENET_TX_CLK	ENET	15 MIL SPACING	ENET_CLK125M_GTX
	ENET	15 MIL SPACING	ENET_CLK125M_GTX_R
ENET_RX	ENET		ENET_RXD<7..0>
ENET_RX_CTL	ENET		ENET_RX_DV
ENET_RX_CTL	ENET		ENET_RX_ER
ENET_TX	ENET		ENET_TXD<7..0>
ENET_TX_CTL	ENET		ENET_TX_EN
ENET_TX_CTL	ENET		ENET_TX_ER
ENET_RX_CTL	ENET		ENET_CR_S
ENET_RX_CTL	ENET		ENET_COL
ENET_MDC	ENET		ENET_MDC
ENET_MDIO	ENET		ENET_MDIO

### Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



Master: Link

### Shasta Ethernet

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	SHT	REV.	
NONE	84	103	

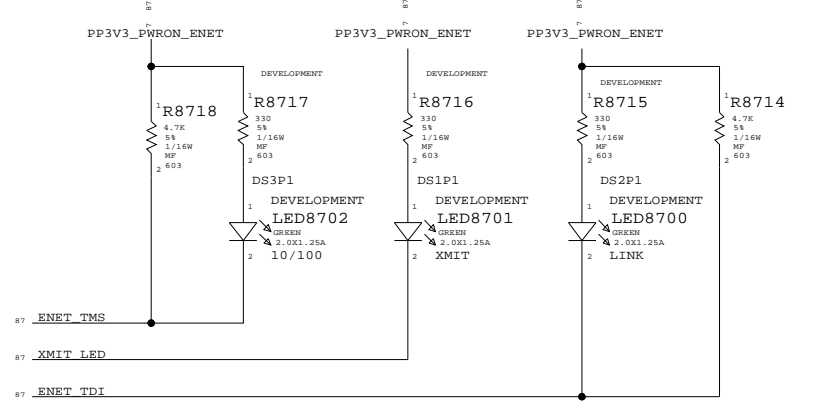
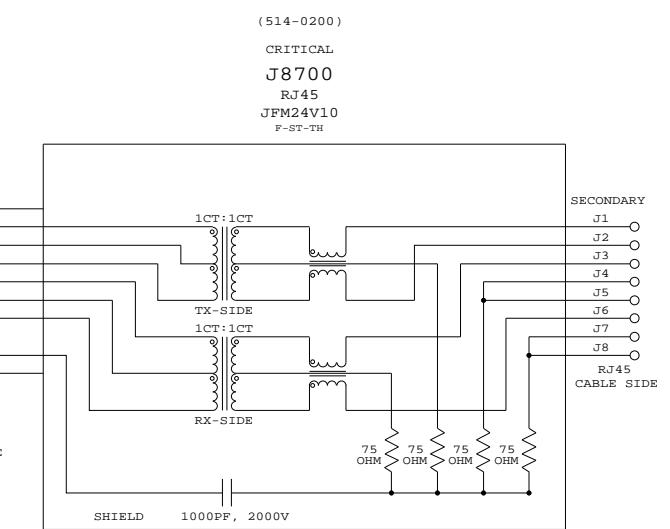
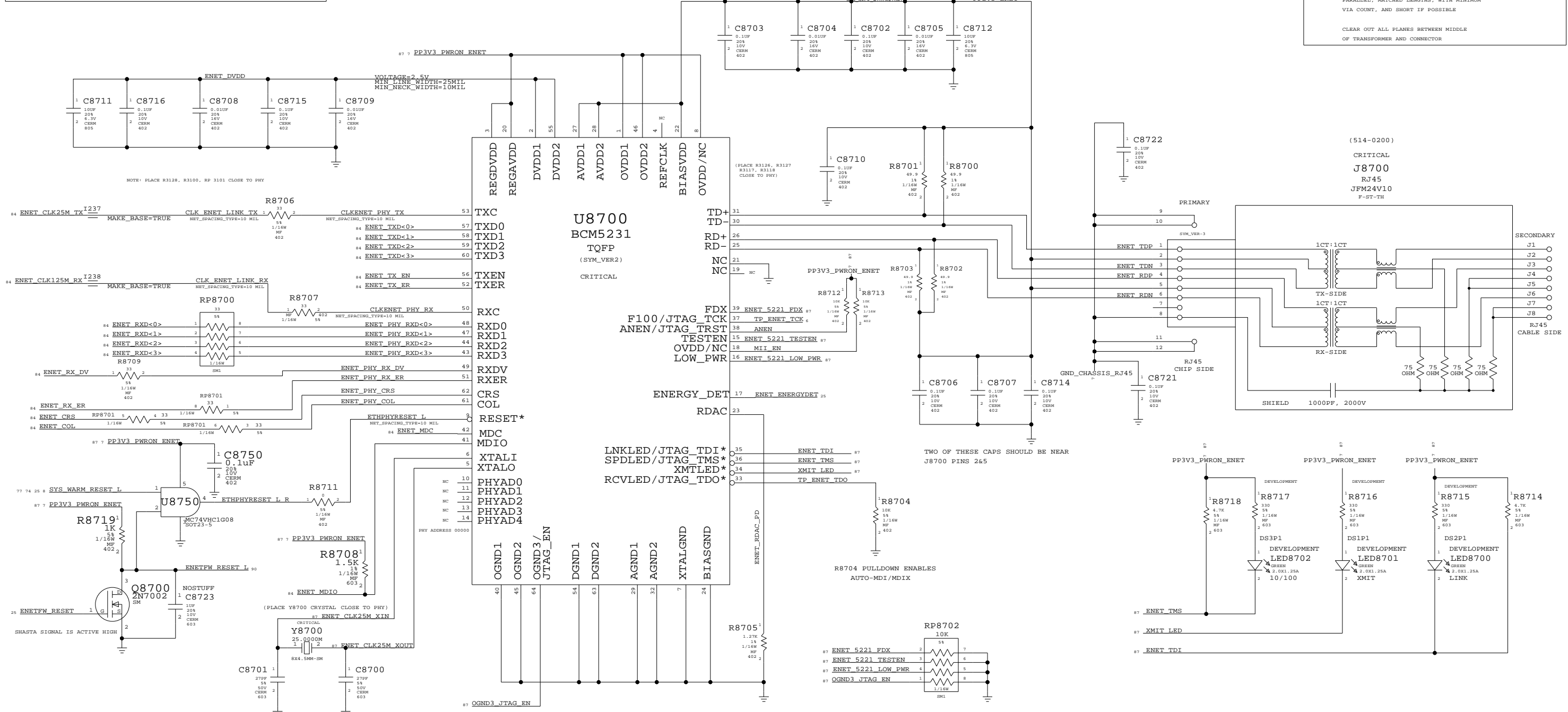
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDP 87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDP 87
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDN 87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDN 87
ENET_XTAL	15 MIL SPACING	ENET_CLK25M_XIN	ENET_CLK25M_XIN 87
	15 MIL SPACING	ENET_CLK25M_XOUT	ENET_CLK25M_XOUT 87

ETHERNET ROUTING PRIORITY:  
 1. DECOUPLING CAPS  
 2. TX TERMINATION - LOCATE NEAR PHY  
 3. RX TERMINATION - LOCATE NEAR PHY

ROUTE TD OVER 2.5V PLANE (BOTTOM LAYER) ONLY  
 ROUTE RD OVER GROUND PLANE (TOP LAYER) ONLY

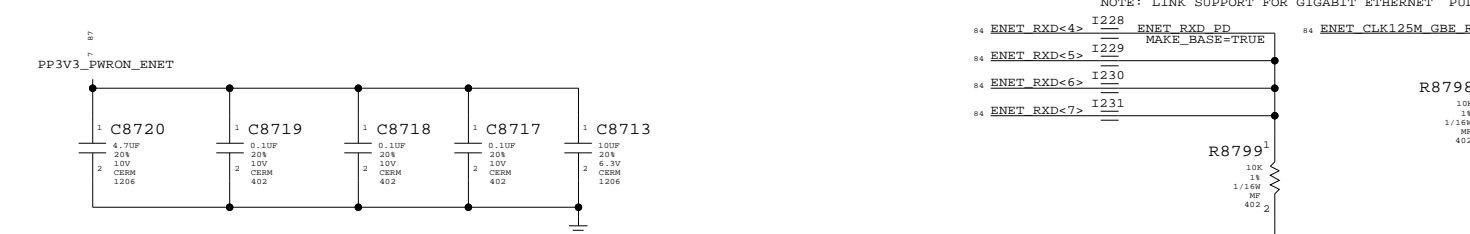
ALL DIFFERENTIAL SIGNALS SHOULD BE CLOSE, PARALLEL, MATCHED LENGTHS, WITH MINIMUM VIA COUNT, AND SHORT IF POSSIBLE

CLEAR OUT ALL PLANES BETWEEN MIDDLE OF TRANSFORMER AND CONNECTOR



**ETHERNET PHY**

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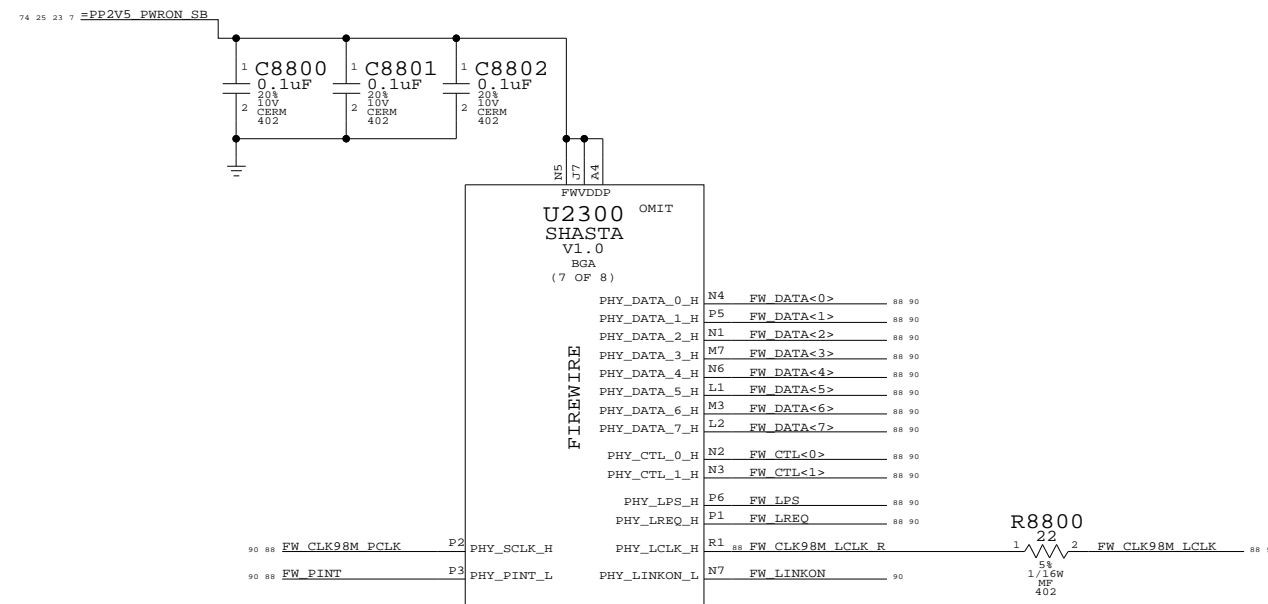
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW	FW		FW_DATA<7..0>
FW	FW		FW_CTL<1..0>
FW_LPS	FW		FW LPS
FW_LREQ	FW		FW LREQ
FW_PINT	FW		FW PINT
FW_LCLK	FW	15 MIL SPACING	FW CLK98M LCLK
FW_PCLK	FW	15 MIL SPACING	FW CLK98M PCLK
		15 MIL SPACING	FW CLK98M LCLK R

## Page Notes

Power aliases required by this page:  
- \_PP2V5\_PWRON\_SB

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



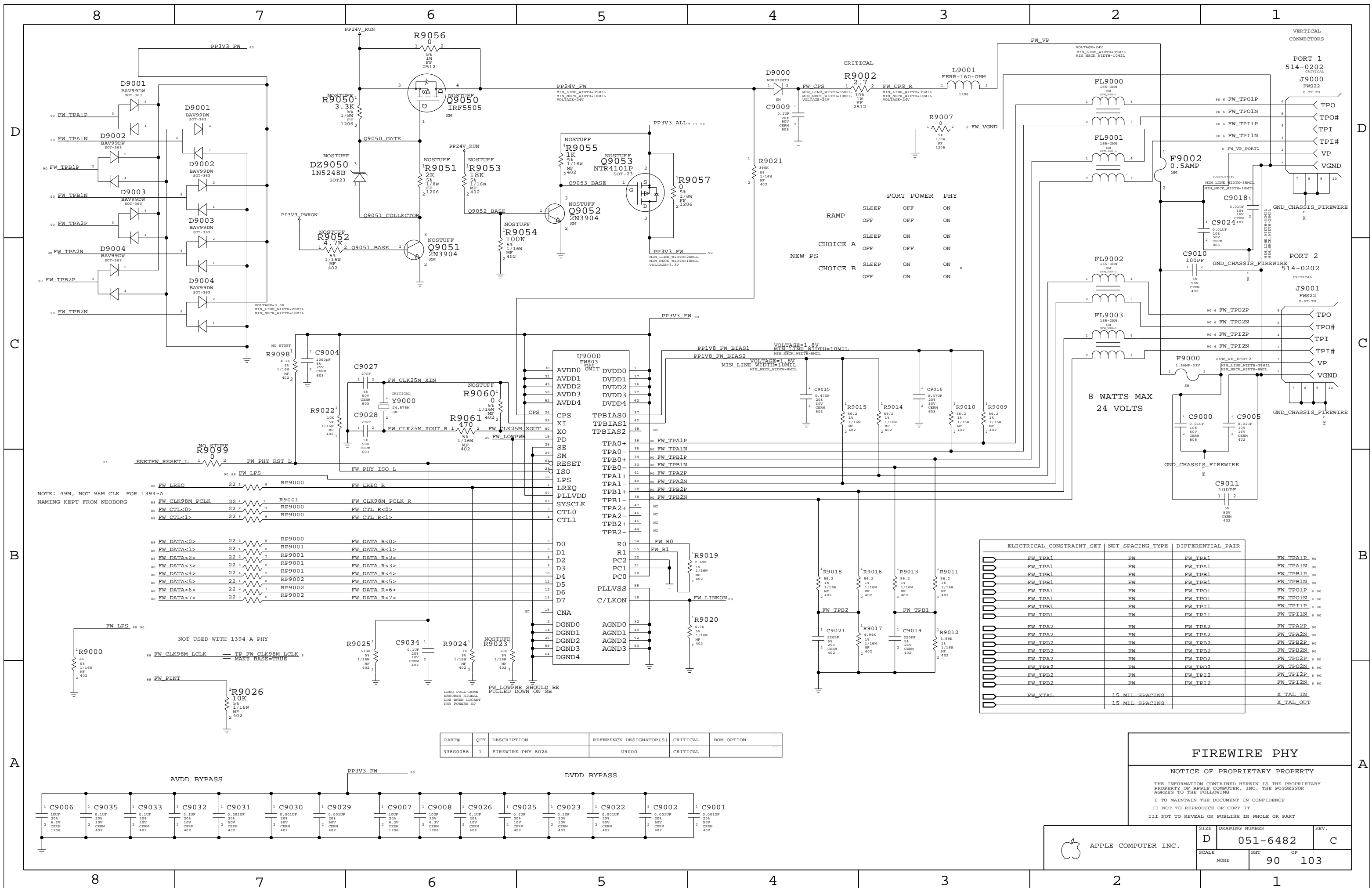
Master: Link

### Shasta FireWire

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NOTE: 49M, NOT 98M CLK FOR 1394-A NAMING KEPT FROM NEOBORG

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	FW	FW_TPA1	FW_TPA1P_90
	FW	FW_TPA1	FW_TPA1N_90
	FW	FW_TPB1	FW_TPB1P_90
	FW	FW_TPB1	FW_TPB1N_90
	FW	FW_TPA1	FW_TPA1P_90
	FW	FW_TPA1	FW_TPA1N_90
	FW	FW_TPB1	FW_TPB1P_90
	FW	FW_TPB1	FW_TPB1N_90
	FW	FW_TPA2	FW_TPA2P_90
	FW	FW_TPA2	FW_TPA2N_90
	FW	FW_TPB2	FW_TPB2P_90
	FW	FW_TPB2	FW_TPB2N_90
	FW	FW_TPA2	FW_TPA2P_90
	FW	FW_TPA2	FW_TPA2N_90
	FW	FW_TPB2	FW_TPB2P_90
	FW	FW_TPB2	FW_TPB2N_90
	FW	FW_TPI2	FW_TPI2P_90
	FW	FW_TPI2	FW_TPI2N_90
	15 MIL SPACING		X TAL IN
	15 MIL SPACING		X TAL OUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0088	1	FIREWIRE PHY 802A	U9000	CRITICAL	

**FIREWIRE PHY**

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APPLE COMPUTER INC.	SCALE	SHEET	OF	REV.
	NONE	90	103	C

AVDD BYPASS				DVDD BYPASS			
1	C9006	100P	20K	1	C9001	0.0010P	20K
2	C9035	0.10P	20K	2	C9002	0.0010P	20K
3	C9033	0.10P	20K	3	C9007	100P	20K
4	C9032	0.10P	20K	4	C9008	100P	20K
5	C9031	0.0010P	20K	5	C9026	0.10P	20K
6	C9030	0.0010P	20K	6	C9025	0.10P	20K
7	C9029	0.0010P	20K	7	C9023	0.10P	20K
8	C9007	100P	20K	8	C9022	0.0010P	20K



ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2 P<0>
USB2_0	USB2	USB2	USB2_0	USB2 N<0>
USB2_1	USB2	USB2	USB2_1	USB2 P<1>
USB2_1	USB2	USB2	USB2_1	USB2 N<1>
USB2_2	USB2	USB2	USB2_2	USB2 P<2>
USB2_2	USB2	USB2	USB2_2	USB2 N<2>
USB2_3	USB2	USB2	USB2_3	USB2 P<3>
USB2_3	USB2	USB2	USB2_3	USB2 N<3>
USB2_4	USB2	USB2	USB2_4	USB2 P<4>
USB2_4	USB2	USB2	USB2_4	USB2 N<4>
USB2_NEC_XTAL		15 MIL SPACING	NEC_CLK30M_XT1	
		15 MIL SPACING	NEC_CLK30M_XT2	
		15 MIL SPACING	NEC_CLK30M_XT2_R	

### Page Notes

Power aliases required by this page:  
 - \_PP3V3\_PWRON\_USB

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

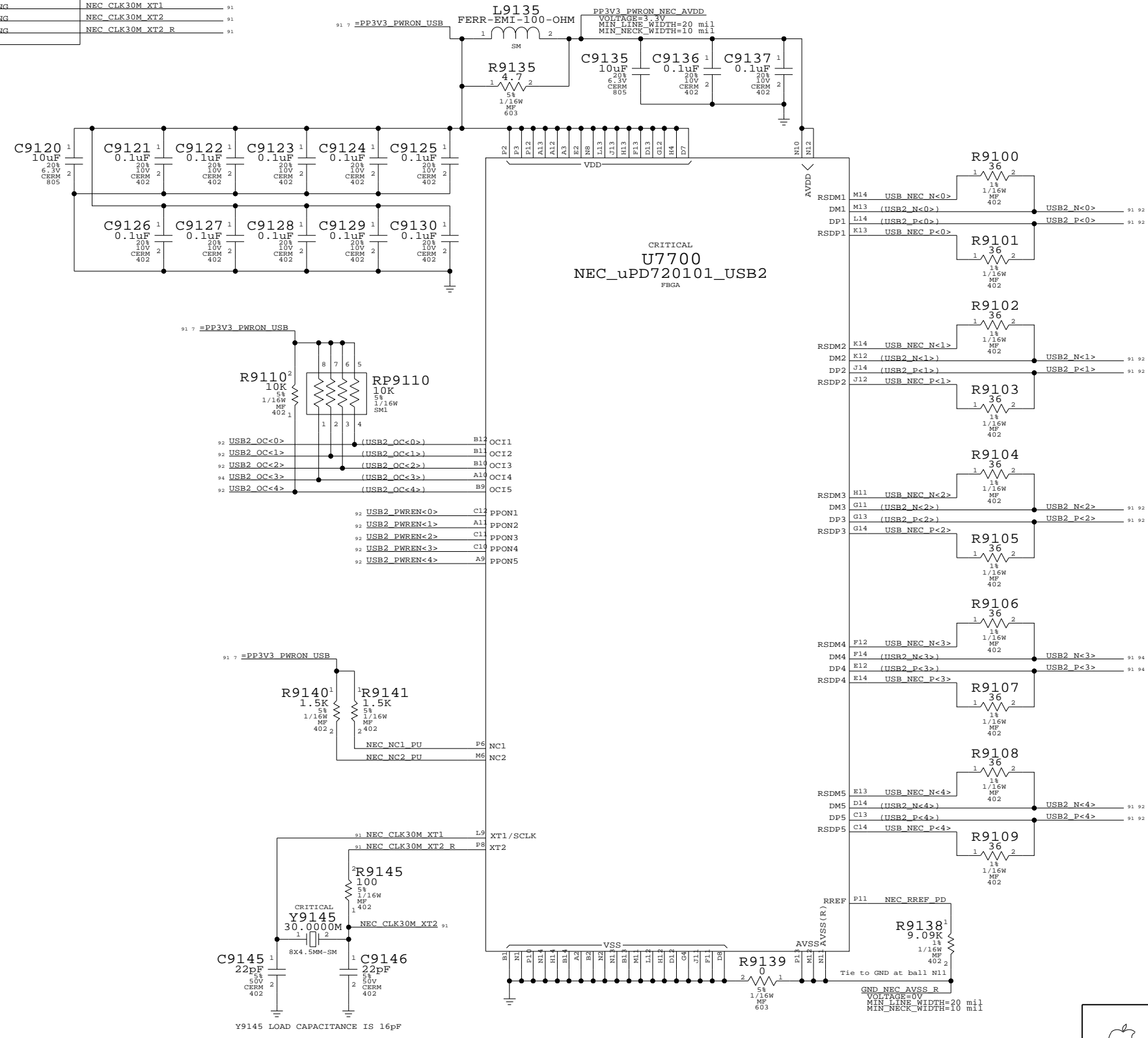
**Net Spacing Type: USB2**

Line To Line: 19.5 mils  
 Length Tolerance: 50 mils  
 Primary Max Sep: 7.5 mils  
 Secondary Max Sep: 100 mils  
 Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

### U2300 SHASTA V1.0 BGA (8 OF 8) OMIT

- NC0 P7 TP\_SB\_NC\_P7
- NC1 P8 TP\_SB\_NC\_P8
- NC2 R3 TP\_SB\_NC\_R3
- NC3 R4 TP\_SB\_NC\_R4
- NC4 R5 TP\_SB\_NC\_R5
- NC5 R6 TP\_SB\_NC\_R6
- NC6 R7 TP\_SB\_NC\_R7
- NC7 R8 TP\_SB\_NC\_R8
- NC8 T1 TP\_SB\_NC\_T1
- NC9 T2 TP\_SB\_NC\_T2
- NC10 T3 TP\_SB\_NC\_T3
- NC11 T4 TP\_SB\_NC\_T4
- NC12 T5 TP\_SB\_NC\_T5
- NC13 T6 TP\_SB\_NC\_T6
- NC14 T7 TP\_SB\_NC\_T7
- NC15 T8 TP\_SB\_NC\_T8
- NC16 U1 TP\_SB\_NC\_U1
- NC17 U2 TP\_SB\_NC\_U2
- NC18 U3 TP\_SB\_NC\_U3
- NC19 U4 TP\_SB\_NC\_U4
- NC20 U5 TP\_SB\_NC\_U5
- NC21 U6 TP\_SB\_NC\_U6
- NC22 V1 TP\_SB\_NC\_V1
- NC23 V2 TP\_SB\_NC\_V2
- NC24 V3 TP\_SB\_NC\_V3
- NC25 V4 TP\_SB\_NC\_V4
- NC26 W1 TP\_SB\_NC\_W1
- NC27 W3 TP\_SB\_NC\_W3
- NC28 Y1 TP\_SB\_NC\_Y1
- NC29 Y3 TP\_SB\_NC\_Y3



## Master: Fizzy

### USB Host Interfaces

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	D	051-6482	C
SCALE	SHT	OF	
NONE	91	103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PROVIDED	USB2	USB2_PORT1_F USB2_PORT1_P_F
BY	USB2	USB2_PORT1_F USB2_PORT1_N_F
USB	USB2	USB2_PORT2_F USB2_PORT2_P_F
CONTROLLER	USB2	USB2_PORT2_F USB2_PORT2_N_F
	USB2	USB2_PORT3_F USB2_PORT3_P_F
	USB2	USB2_PORT3_F USB2_PORT3_N_F

### External USB Ports

## Page Notes

Power aliases required by this page:  
 - \_PP5V\_PWRON\_USB  
 - \_PP5V\_PWRON\_UDASH  
 - \_PP3V3\_PWRON\_UDASH  
 - \_PP3V3\_PWRON\_BT

Signal aliases required by this page:  
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:  
 (NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

## neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

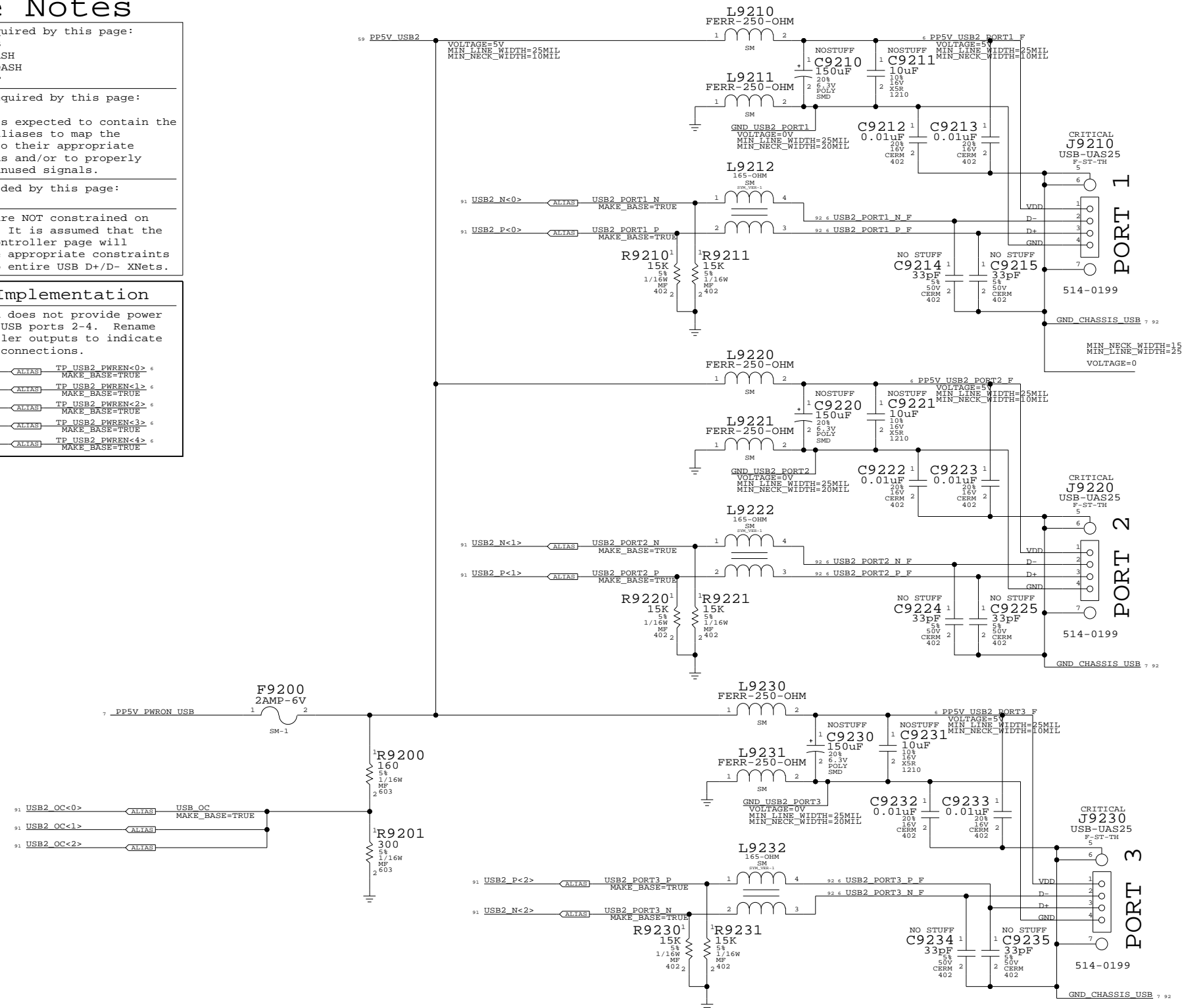
91 USB2\_PWREN<0> <ALIAS> TP\_USB2\_PWREN<0> MAKE\_BASE=TRUE

91 USB2\_PWREN<1> <ALIAS> TP\_USB2\_PWREN<1> MAKE\_BASE=TRUE

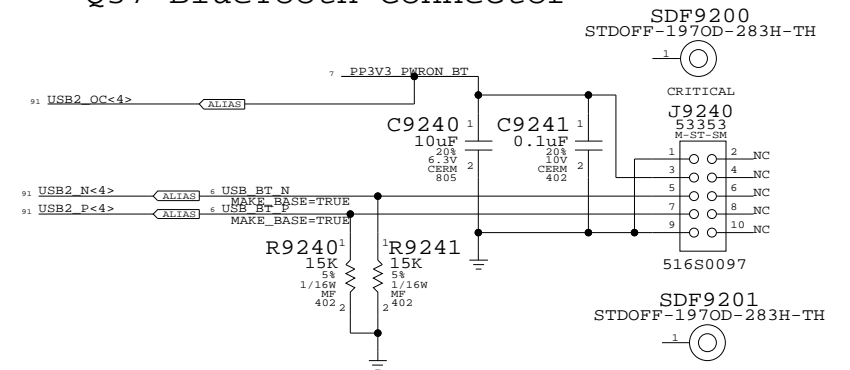
91 USB2\_PWREN<2> <ALIAS> TP\_USB2\_PWREN<2> MAKE\_BASE=TRUE

91 USB2\_PWREN<3> <ALIAS> TP\_USB2\_PWREN<3> MAKE\_BASE=TRUE

91 USB2\_PWREN<4> <ALIAS> TP\_USB2\_PWREN<4> MAKE\_BASE=TRUE



## Q37 BlueTooth Connector



## USB Device Interfaces

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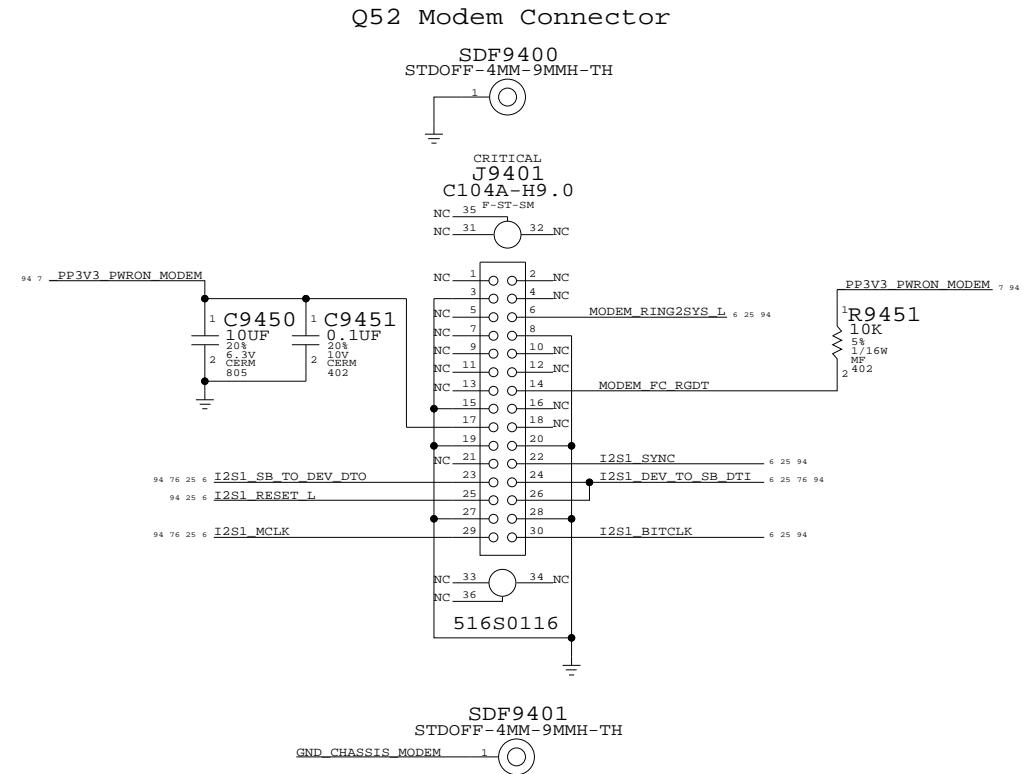
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	NONE	SHT	OF
		92	103

# Page Notes

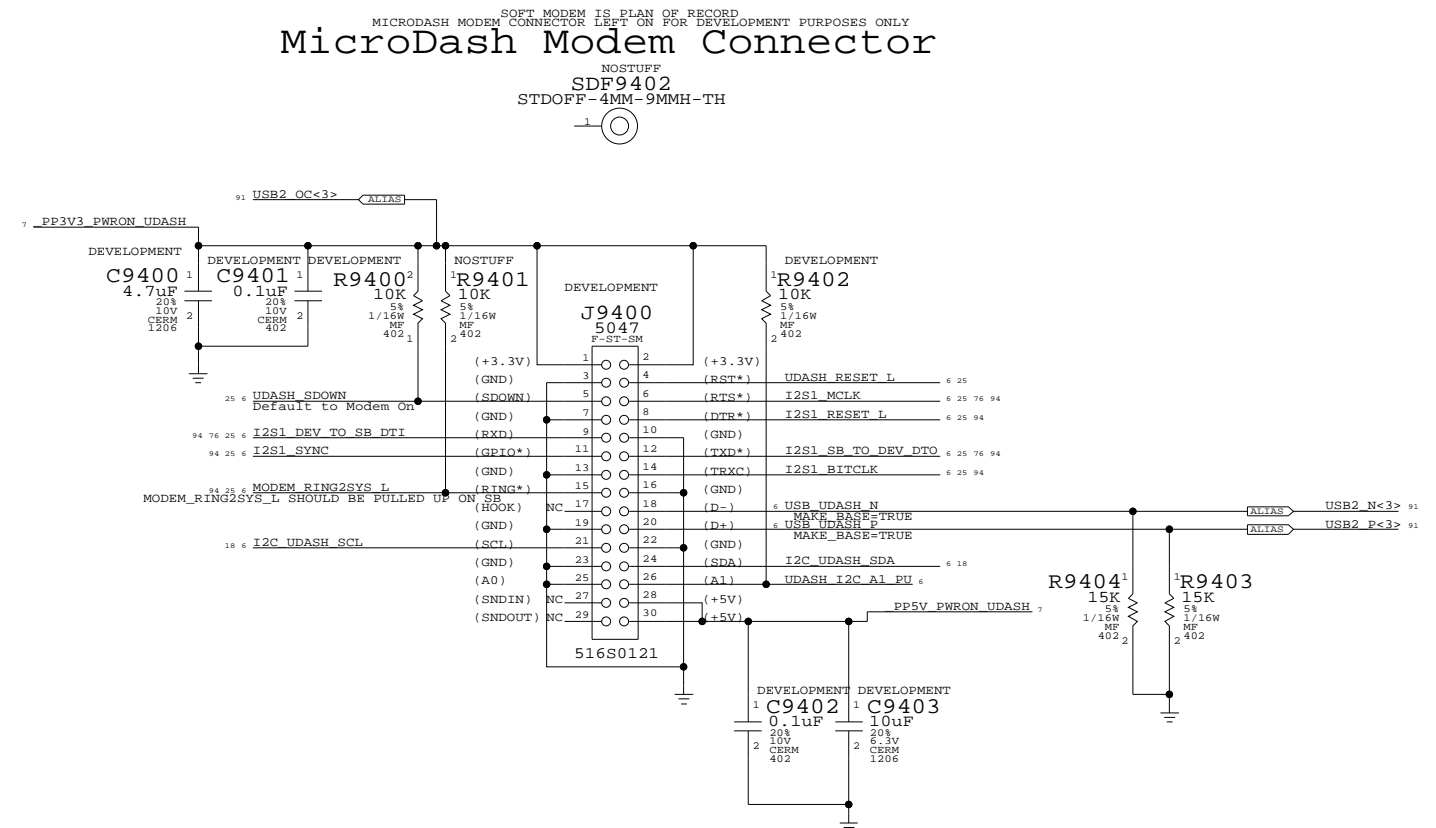
Power aliases required by this page:  
 - \_PP3V3\_PWRON\_MODEM  
 Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:  
 (NONE)

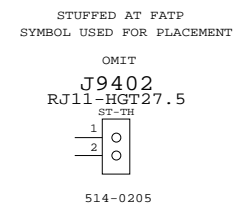
BOM options provided by this page:  
 (NONE)



# MicroDash Modem Connector



# RJ11 CONNECTOR



- From Intel Mobile Audio/Modem Daughter Card Specification Rev 1.0, February 22, 1999
- |                      |                     |
|----------------------|---------------------|
| 1 - MONO_OUT/PC_BEEP | 2 - AUDIO_PWRON     |
| 3 - GND              | 4 - MONO_PHONE      |
| 5 - AUX_A_RIGHT      | 6 - RESERVED        |
| 7 - AUX_A_LEFT       | 8 - GND             |
| 9 - CD_GND           | 10 - 5Vmain         |
| 11 - CD_RIGHT        | 12 - RESERVED       |
| 13 - CD_LEFT         | 14 - RESERVED       |
| 15 - GND             | 16 - PRIMARY_DN     |
| 17 - 3.3Vaux         | 18 - 5Vd            |
| 19 - GND             | 20 - GND            |
| 21 - 3.3Vmain        | 22 - AC97_SYNC      |
| 23 - AC97_SDATA_OUT  | 24 - AC97_SDATA_INB |
| 25 - AC97_RESET#     | 26 - AC97_SDATA_INA |
| 27 - GND             | 28 - GND            |
| 29 - AC97_MSTRCLK    | 30 - AC97_BITCLK    |

# Modem Interface

NOTICE OF PROPRIETARY PROPERTY

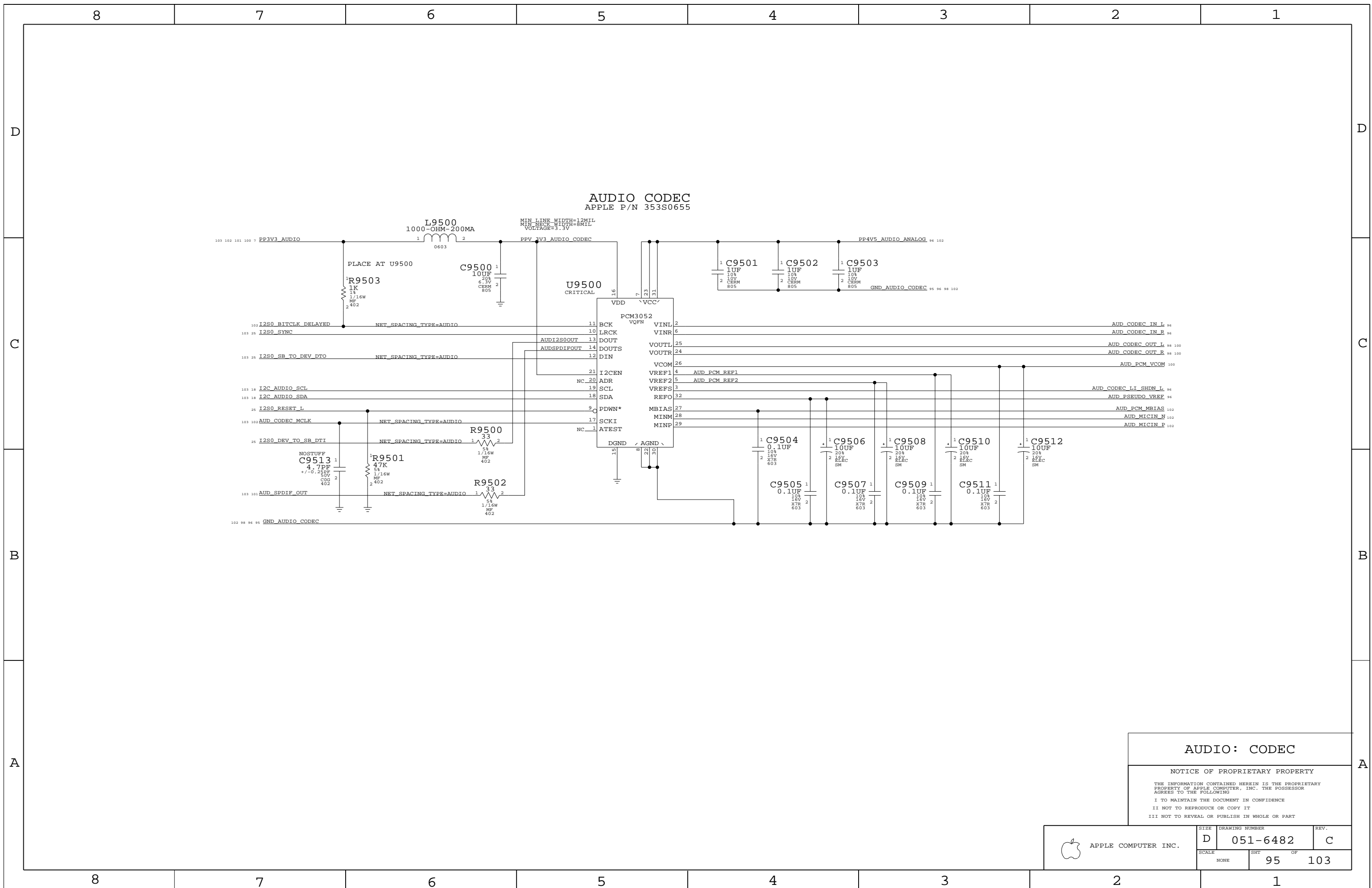
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	D	051-6482	C
SCALE	SHT OF		
NONE	94		103



**AUDIO: CODEC**

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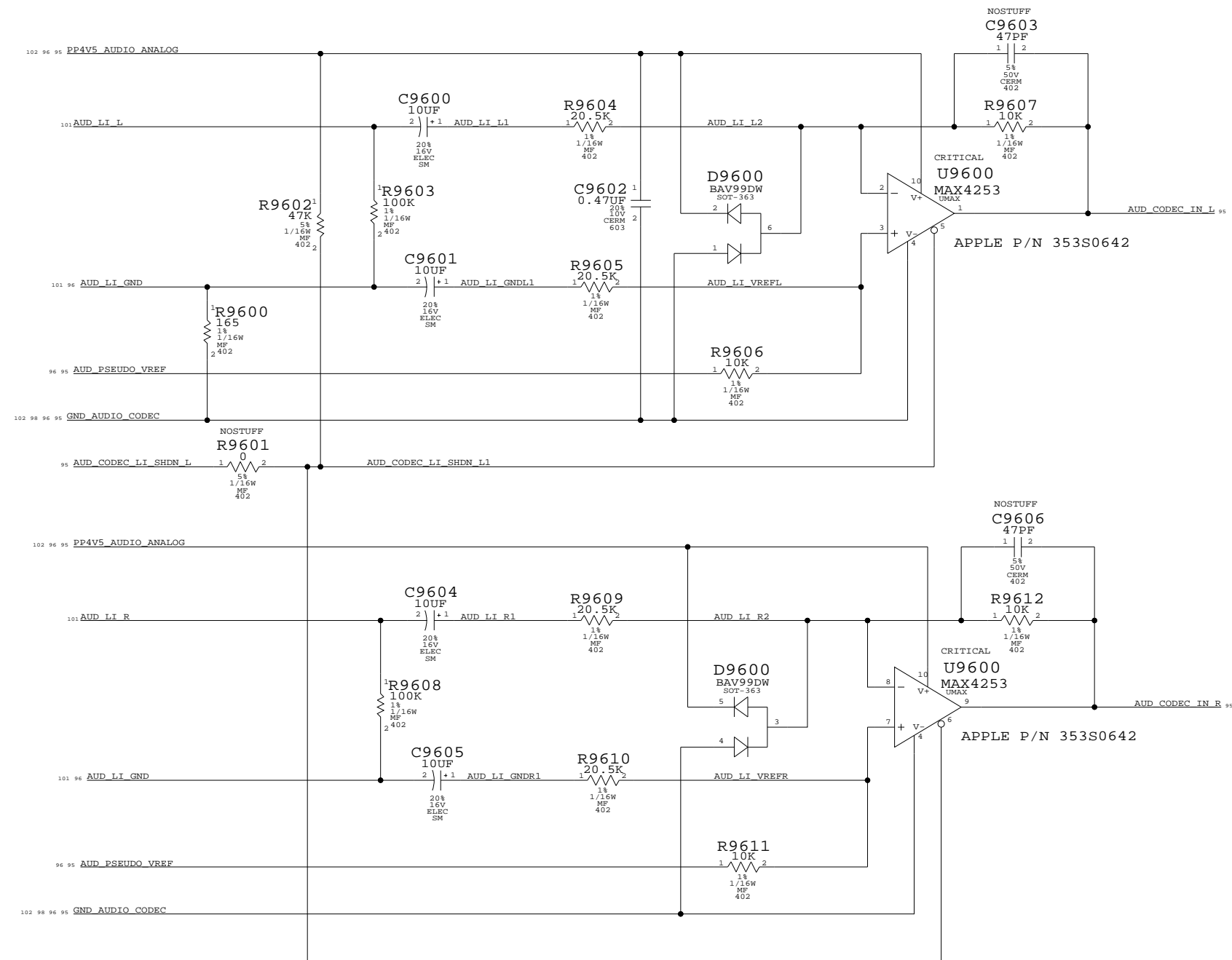
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	SCALE NONE	SHT <b>95</b>	OF <b>103</b>

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

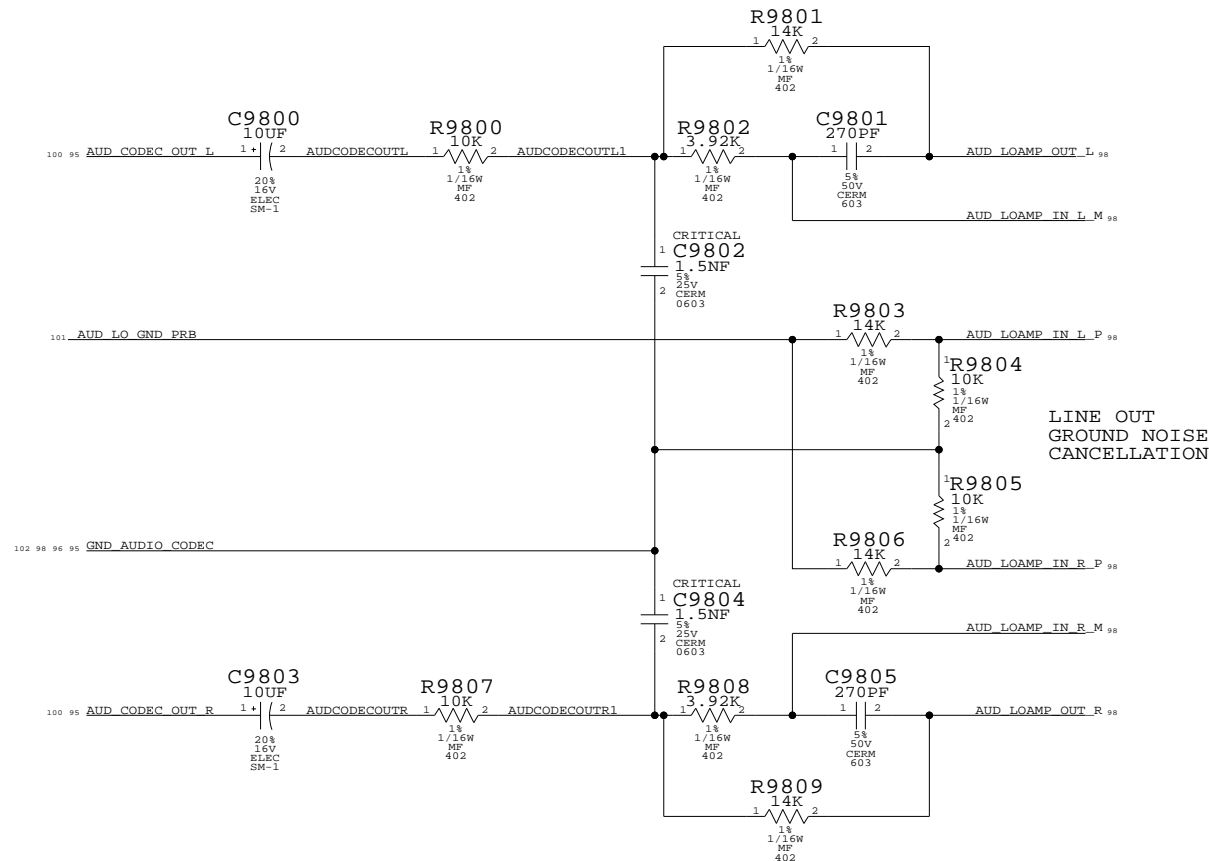
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	D	051-6482	C
SCALE	NONE	SHT	OF
		96	103

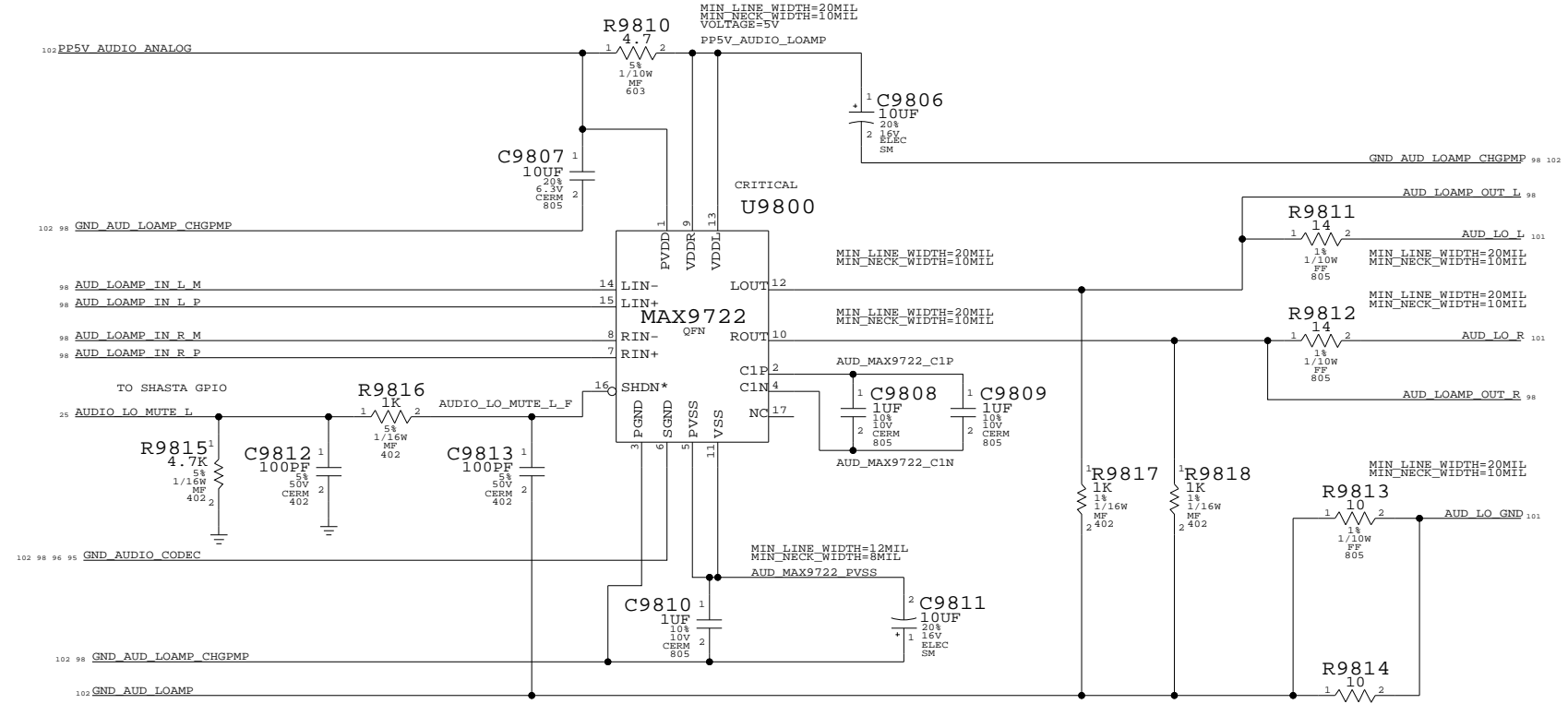
### LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



### LINE OUT AMP

APPLE P/N 353S0687



### AUDIO: LINE OUT AMP

NOTICE OF PROPRIETARY PROPERTY

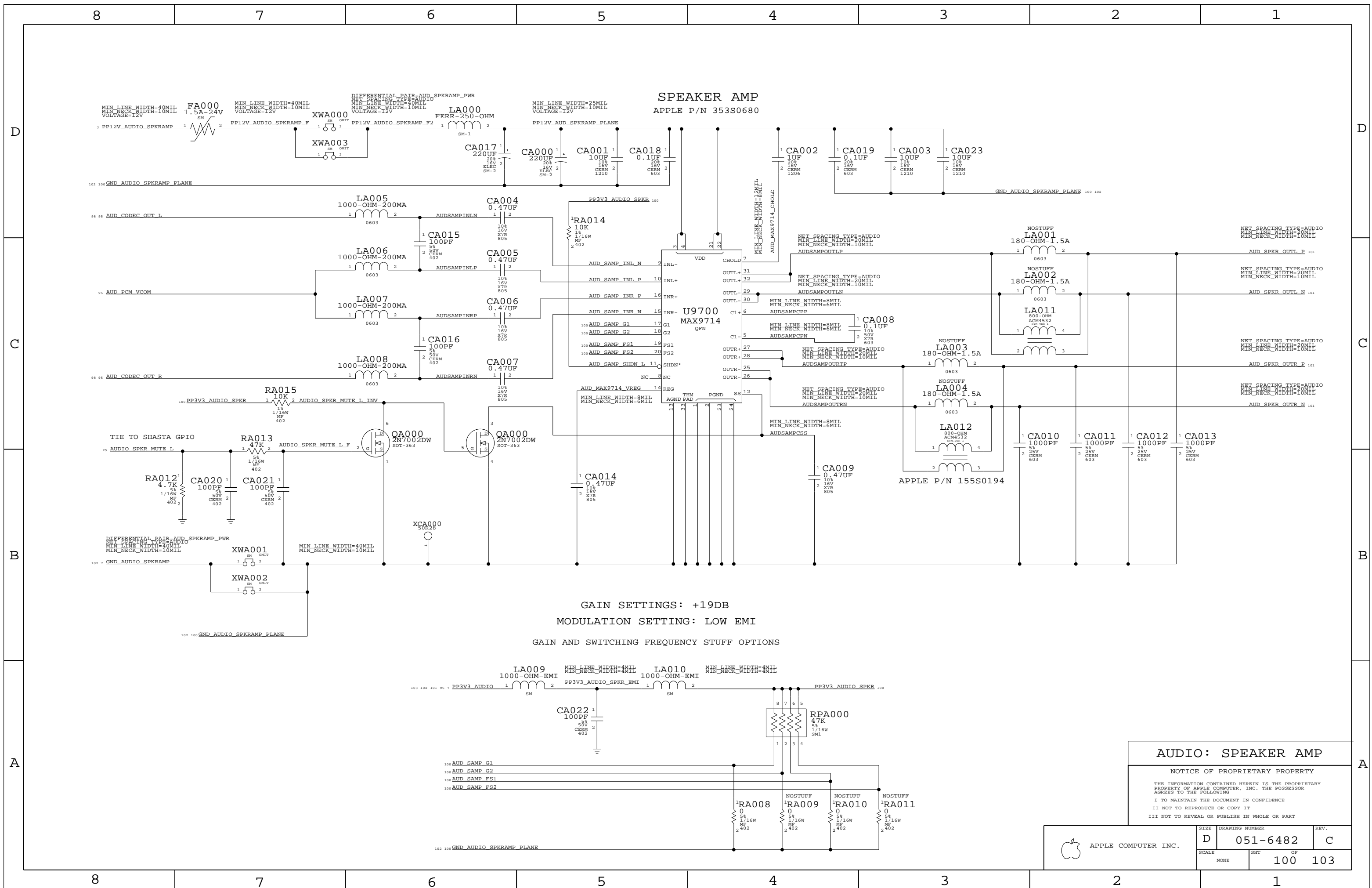
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	D	051-6482	C
SCALE	SHT	OF	
NONE	98	103	



GAIN SETTINGS: +19DB  
 MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

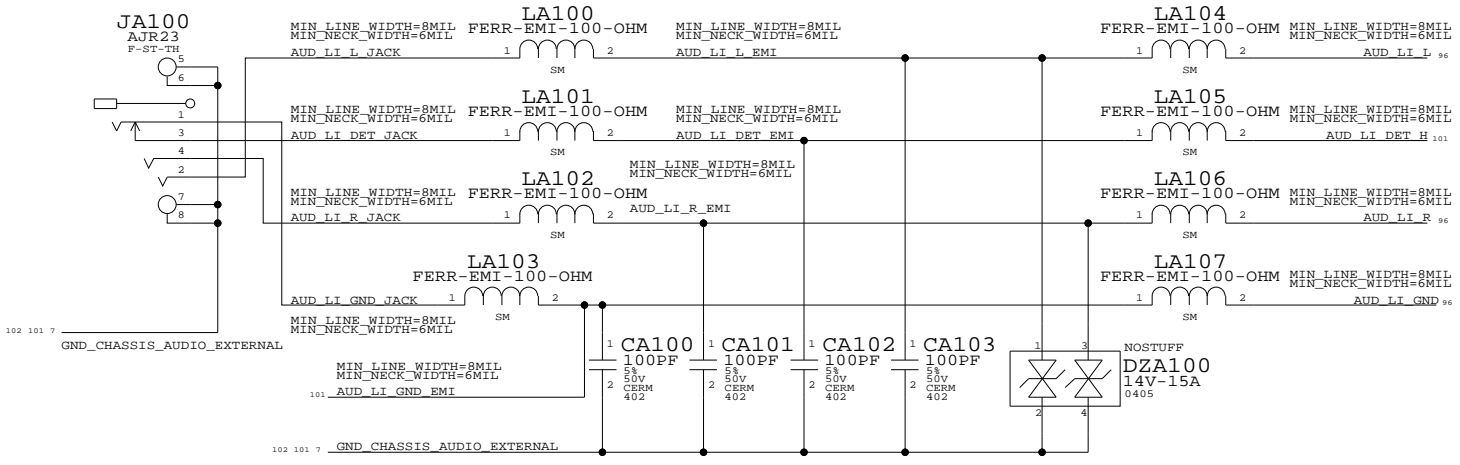
**AUDIO: SPEAKER AMP**

**NOTICE OF PROPRIETARY PROPERTY**

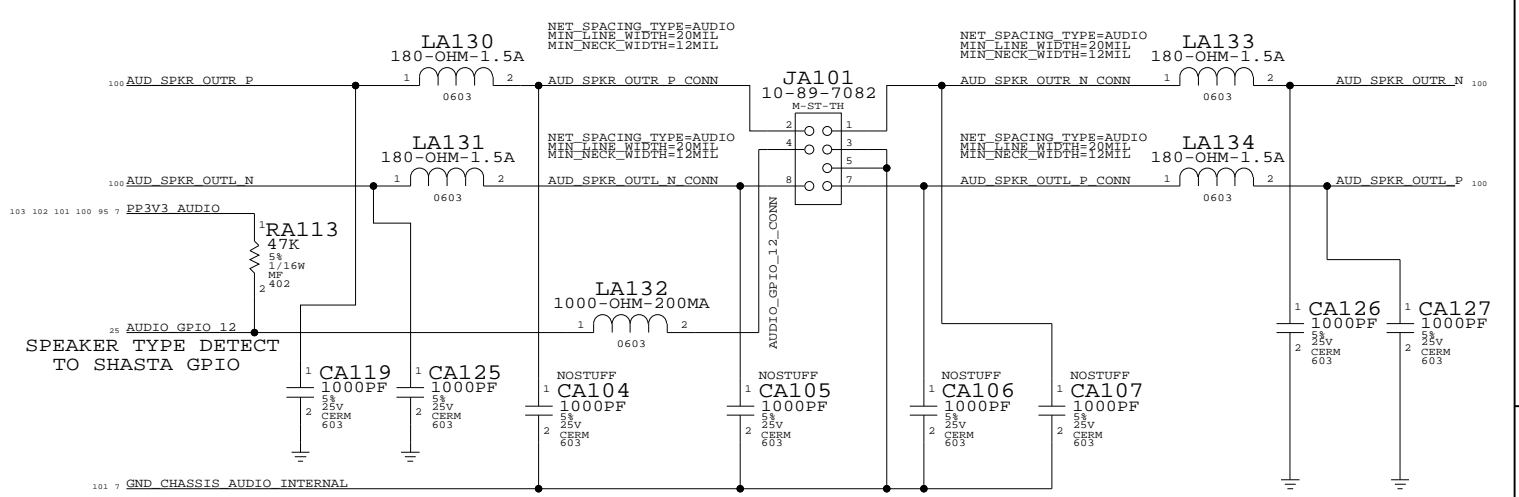
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	D	051-6482	C
SCALE	NONE	SHT OF	100 103

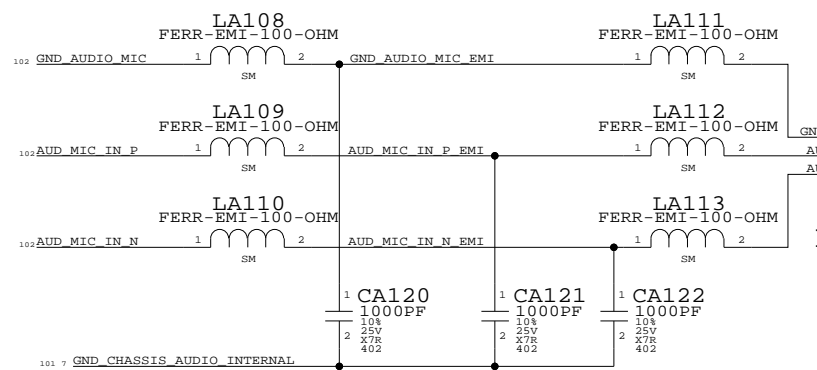
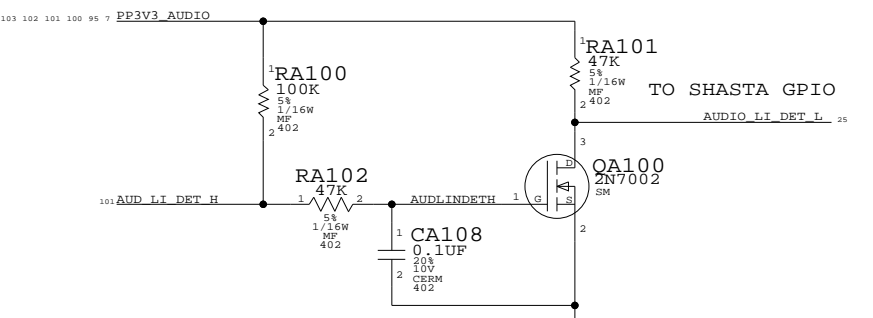
**LINE IN JACK**  
APPLE P/N 514-0203



**SPEAKER CABLE CONNECTOR**  
APPLE P/N 518-0138

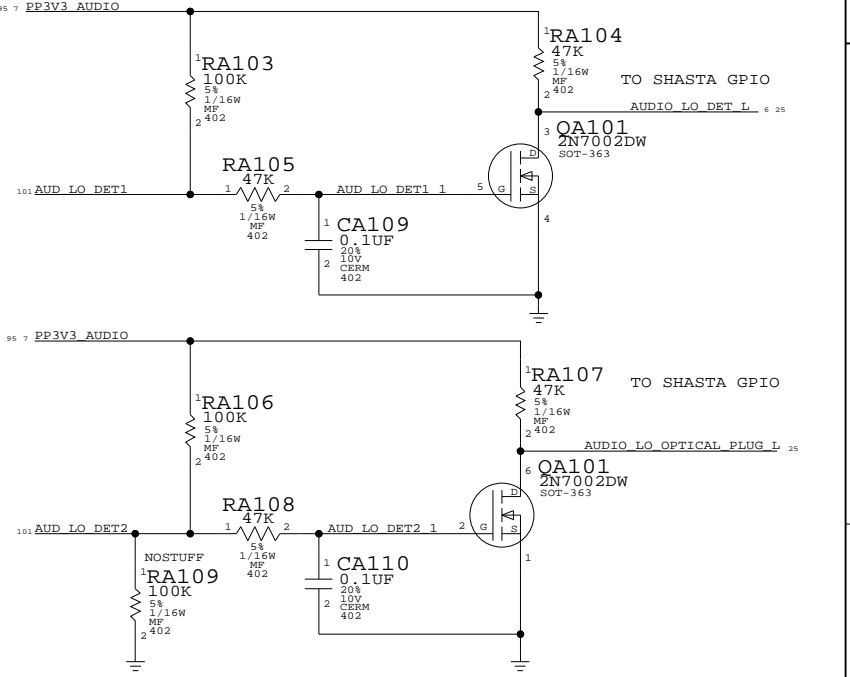


**LINE IN PLUG DETECT**  
AUDIO\_IN\_DET0\_L = LOW: PLUG INSERTED  
AUDIO\_IN\_DET0\_L = HIGH: PLUG NOT INSERTED

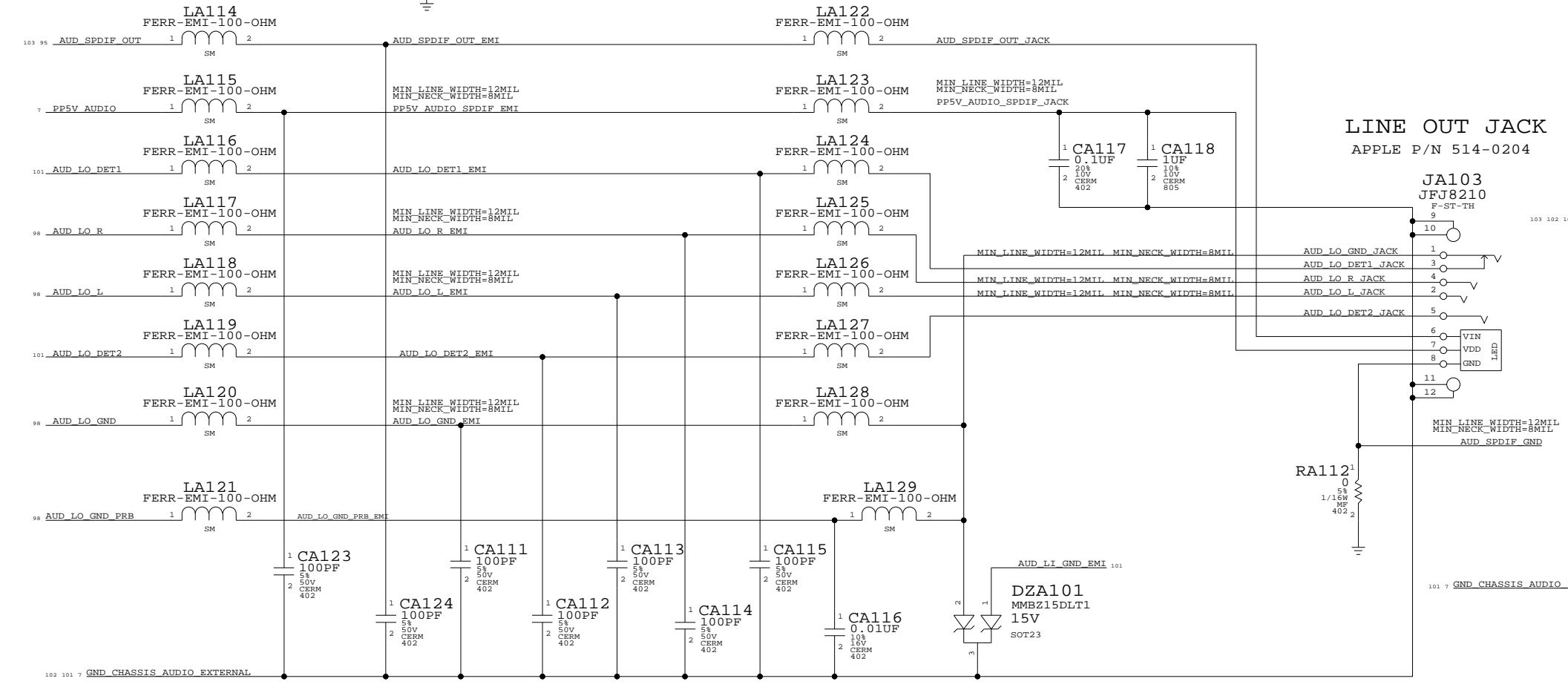


**MIC CABLE CONNECTOR**  
APPLE P/N 518-0034

**LINE OUT PLUG DETECTS**  
AUDIO\_LO\_DET\_L = LOW: PLUG INSERTED  
AUDIO\_LO\_DET\_L = HIGH: PLUG NOT INSERTED  
AUDIO\_LO\_OPTICAL\_PLUG\_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED  
AUDIO\_LO\_OPTICAL\_PLUG\_L = HIGH: ANALOG AUDIO PLUG INSERTED



**LINE OUT JACK**  
APPLE P/N 514-0204



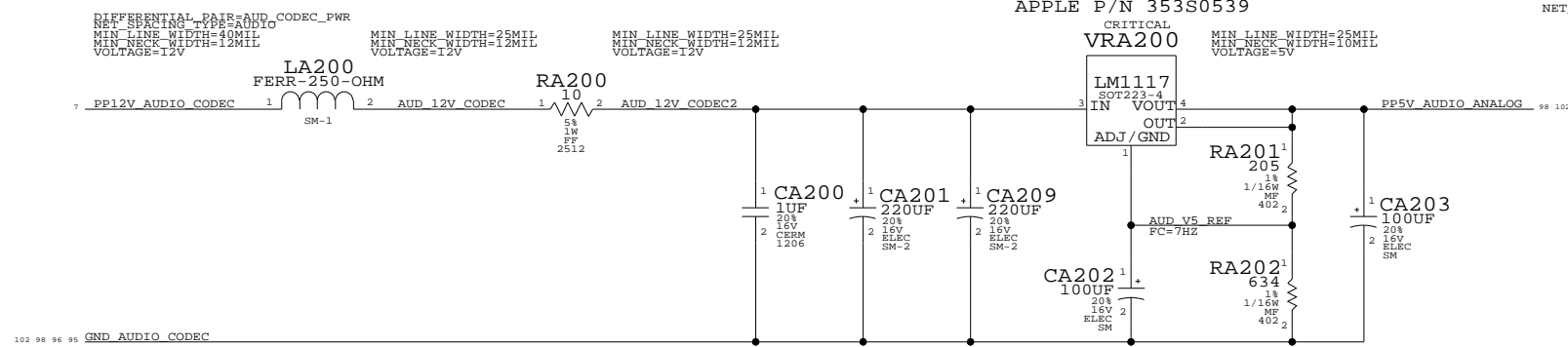
**AUDIO: Q45 CONNECTORS**

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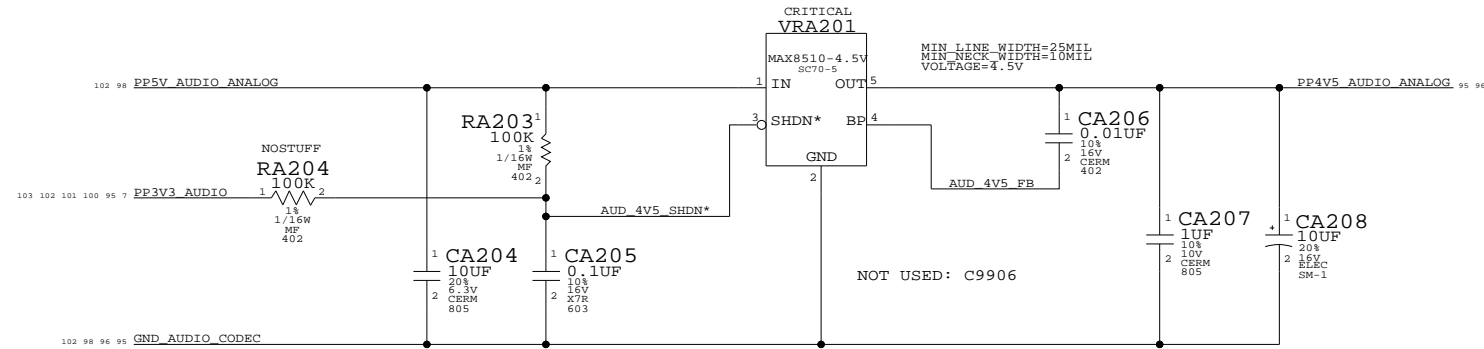
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	101	103
NONE			



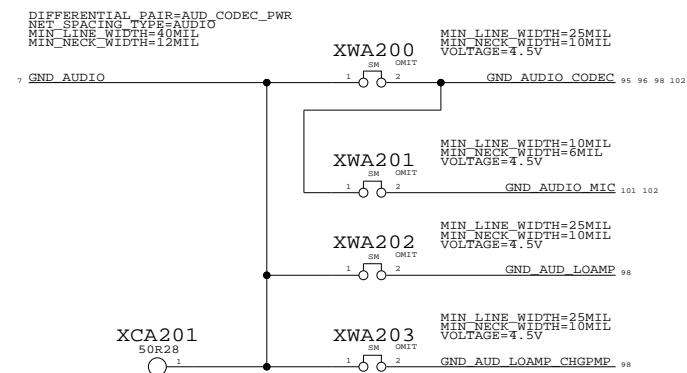
### 5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP



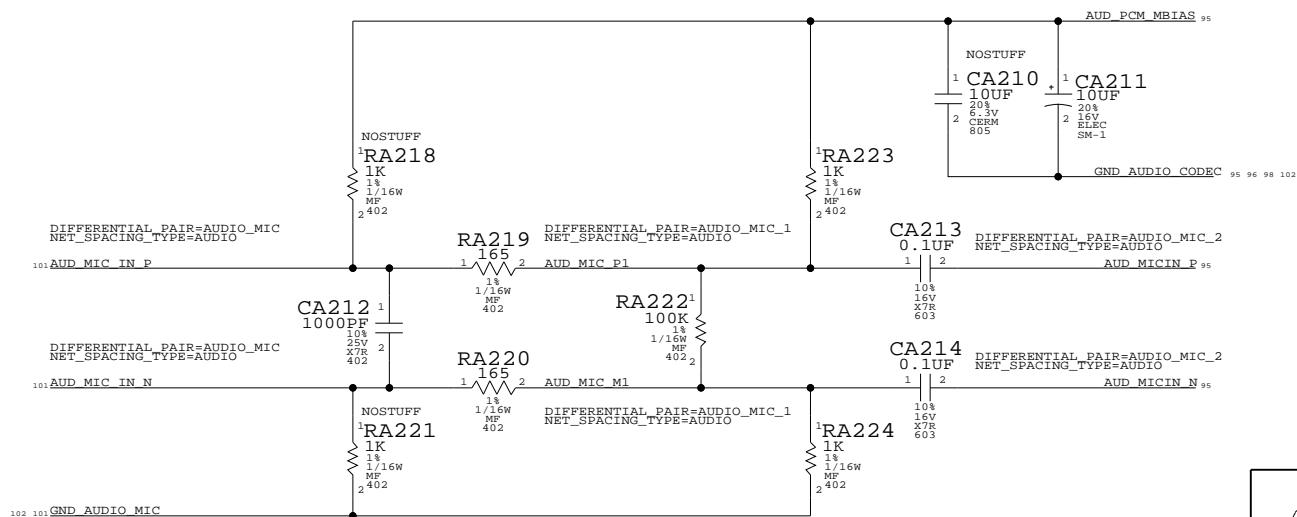
### 4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP



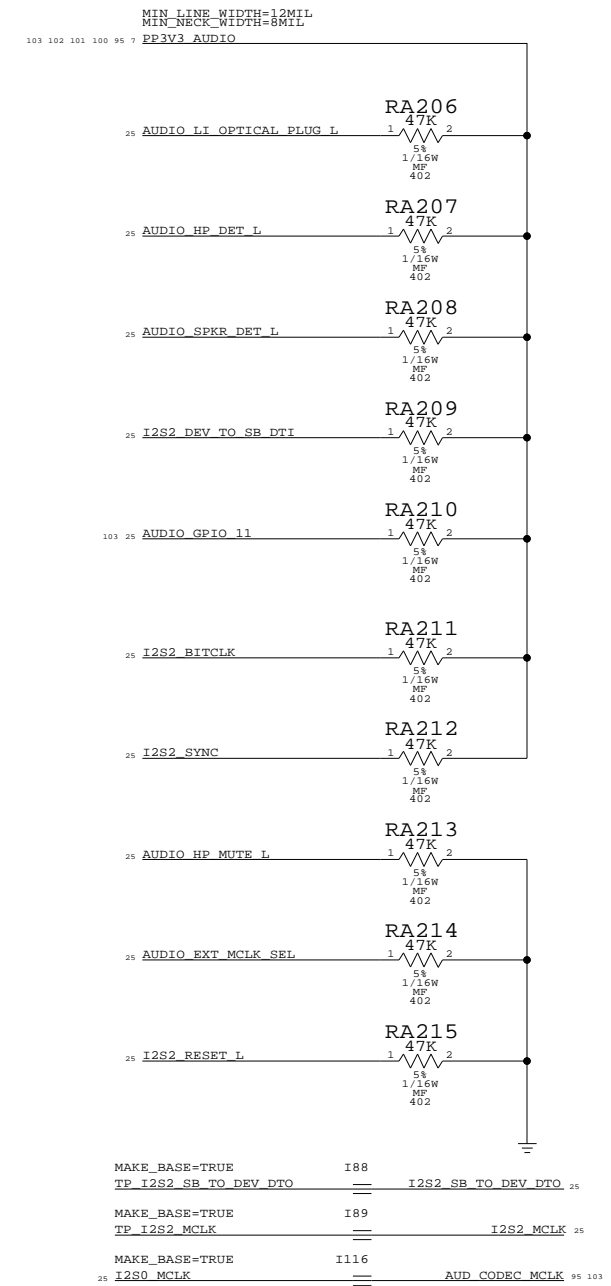
### AUDIO GROUND RETURNS



### MICROPHONE IMPEDANCE MATCHING CIRCUIT



### UNUSED GPIO TERMINATIONS



### AUDIO: Q45 POWER SUPPLIES

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6482	C
SCALE	NONE	SHT OF	102 OF 103

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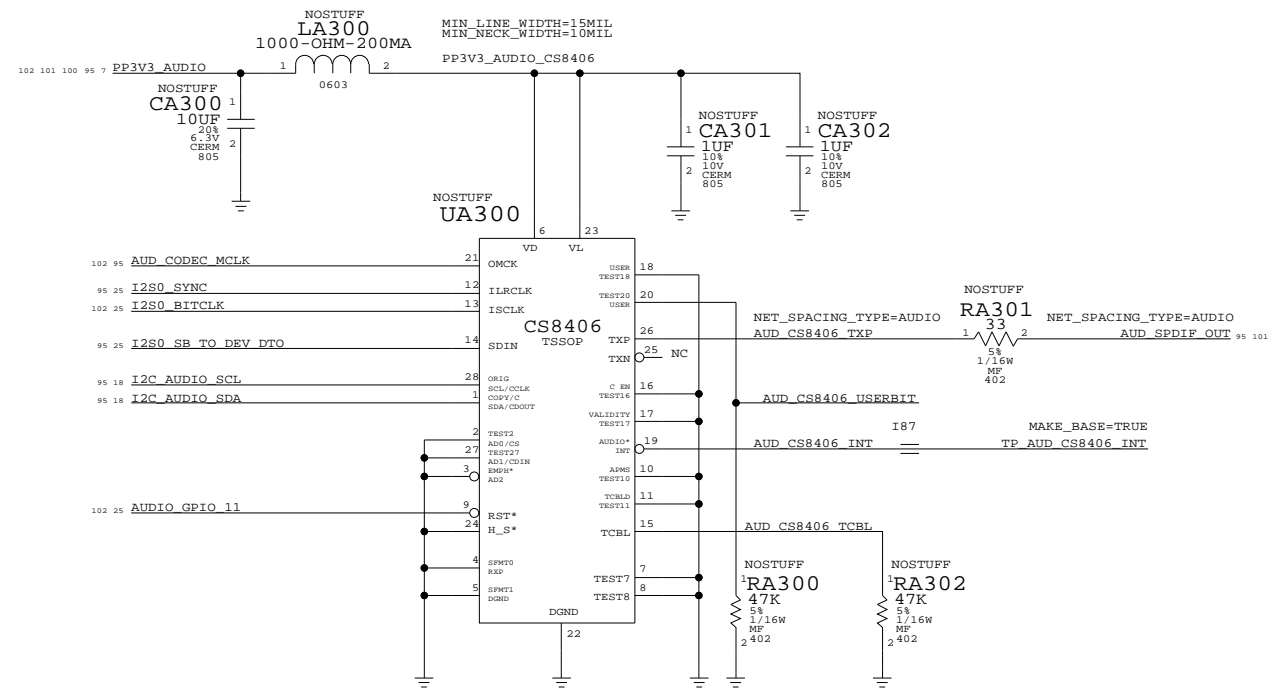
B

B

A

A

S/PDIF TRANSMITTER  
 I2C ADDRESS = 0010 000X  
 APPLE P/N 353S0597



AUDIO: S/PDIF XMITTER

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	D	051-6482	C
SCALE	NONE	SHT OF	103 OF 103

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