P-TSLP-2-1 / P-TSLP-3-1

Recommendations for the Board Assembly

Target

The target of this document is to provide guidelines for our customers to successfully introduce Infineon's leadless packages P-TSLP2-1 / P-TSLP-3-1 into production. This includes recommendations for board pad design, stencil layout, component placement, and soldering process. Generally standard SMT equipment and processes are suitable for the board assembly of all P-TSLP packages.

The Packages P-TSLP-2-1 and -3-1

The Plastic-ThinSmallLeadlessPackage is one of the smallest packages for diodes and transistors available today.

A comparison with the SOT23 (see Figure 1) shows its space-saving capabilities for all space and height critical board assembly applications.

The P-TSLP-2-1 is a diode package with two terminals, which are of the same size. The P-TSLP-3-1 is a transistor package with three terminals.

The P-TSLP is a GREEN PACKAGE, that means it contains no halogenides and no lead. It is compatible with all Pb-free and Pb containing solder pastes.

For further information about the package dimensions, the marking, the packing and other general information, please observe our package information book or the information about packages on our homepage (www.infineon.com).

Figure 1
Comparison between P-TSLP-2-1/P-TSLP-3-1 and a SOT23 package

Board Pad Design

The solder pads have to be designed in a way to ensure optimum manufacturability and reliability. Generally two basic types of solder pads are commonly used for area array packages:

- "Solder mask defined" (SMD) pad: The copper pad is larger than the solder mask opening above this pad. Thus the land area is defined by the opening in the solder mask.
- "Non solder mask defined" (NSMD) pad: Around each copper pad there is solder mask clearance.

Because solder mask between the pads of the P-TSLP-2-1 and -3-1 can cause tilted devices, the solder mask opening should be larger than the outline of the device (opening = outline + clearance). Therefore SMD pads are not useable. NSMD pads generally provide more space for routing and result in a higher solder joint reliability (also the side walls of the lands can be wetted by the solder, which results in less stress concentration).

Therefore this type is recommended for the P-TSLP-2-1 and -3-1.

The copper pad dimensions which have been tested up to now are shown in Figure 2.

The solder pads must have good wettability to eutectic solder. Electroless NiAu plating is a common surface finish and proven to be suitable for P-TSLP assembly.

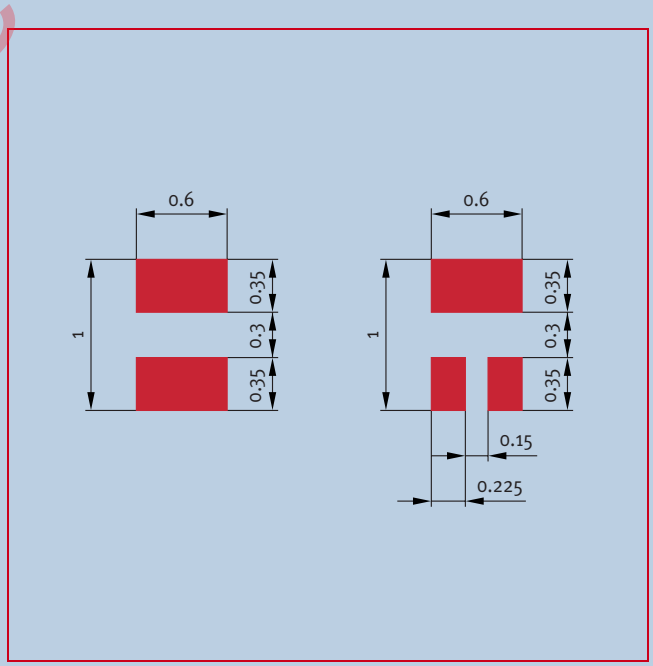

Figure 2
Recommendation for optimum pad design (non solder mask defined pad)

Solder Paste Printing Process

The solder paste deposited on the printed circuit board by stencil printing has to be of eutectic or near eutectic composition (e.g. 63Sn37Pb, 62Sn36Pb2Ag or lead free 95.5Sn3.8Ago.7Cu). A no clean solder paste is preferred, because cleaning under the soldered P-TSLP-2-1/P-TSLP-3-1 may be difficult. The paste must have the printing capability for the pitch 0.8 mm, or pitch 0.65 mm, respectively (typically type 3 paste; to ensure a uniform deposition of the solder paste a type 4 paste is not a disadvantage).

A stencil thickness between 120 µm and 100 µm is recommended, to ensure a uniform and high solder paste transfer to the PCB.

Typical dimensions of the stencil apertures are shown in Figure 3.

For applications with a large displacement between stencil and PCB (e.g. FR4, ceramic) of more than ca. 100 µm, this process may not be reliable for the P-TSLP- 3-1. In this case the solder deposition should be carried out for example by a solder dispenser.

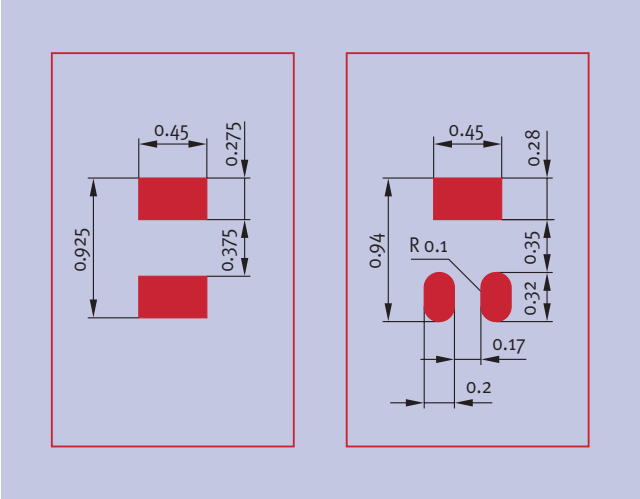

Figure 3
Recommendation for the stencil layouts. The rounded holes in the case of the two small pads of the P-TSLP-3-1 are used in order to have a better solder transfer

Placement of Components

Generally the P-TSLP can be placed with a wide range of placement systems.
The following remarks are important:

- On large boards especially, local fiducials, close to the device, can compensate tolerances of PCB (e.g. FR4, ceramic).
- Vision systems with pad recognition and alignment with regard to the pad locations (in contrast to outline centering) are typical for the placement of such packages.

Reflow Soldering Process

Generally all standard reflow soldering processes (vapour phase, convection, infrared) and typical temperature profiles used for fine pitch devices are suitable for board assembly of the P-TSLP. Wave soldering is not possible. At the reflow process each solder joint has to be exposed to temperatures above solder liquidus for a sufficient time to attain the optimum solder joint quality, whereas overheating the board with its components has to be avoided. Using infrared ovens without convection special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB (especially on large, complex boards with different thermal masses of the components) including those under the P-TSLP. The most recommended types are therefore forced convection or vapour phase reflow. Nitrogen atmosphere can generally improve solder joint quality as for soldering of leaded SMD devices, but is normally not necessary for the P-TSLP.

Figure 4 shows a typical forced convection reflow profile, which is suitable for soldering the P-TSLP-2-1 and -3-1. The temperature profile also has to be within the specification of the used solder paste, and depends on the board and the oven.

For typical Pb-free reflow soldering (e.g. with SnAgCu) peak temperatures up to 260°C are used. Figure 5 shows a corresponding reflow profile.

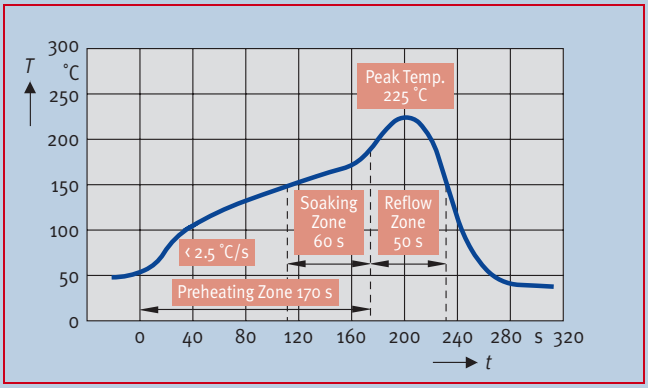

Figure 4
Typical forced convection reflow profile suitable for P-TSLP-2-1/ P-TSLP-3-1. (example for solder paste Litton Kester R256)

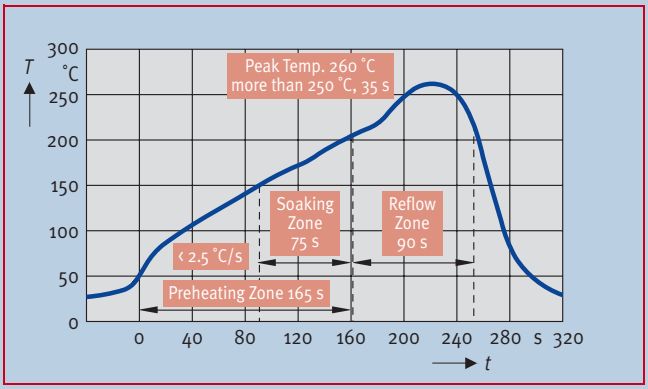

Figure 5
Typical forced convection reflow profile suitable for P-TSLP's lead free soldering

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