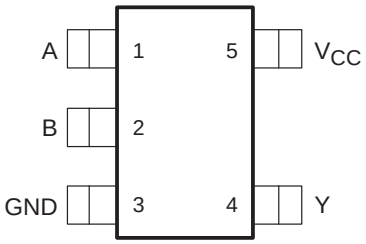
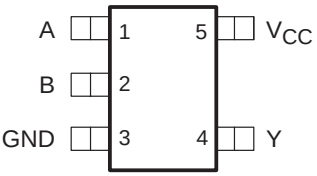
- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 3.6 ns at 3.3 V**
- **Low Power Consumption, 10-μA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

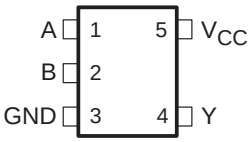
DBV PACKAGE
(TOP VIEW)



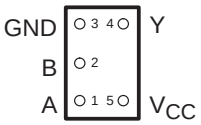
DCK PACKAGE
(TOP VIEW)



DRL PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

description/ordering information

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G32 performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.17-mm Small Bump − YEA	Reel of 3000	SN74LVC1G32YEAR	_ _ _CG_
	NanoFree™ − WCSP (DSBGA) 0.17-mm Small Bump − YZA (Pb-free)		SN74LVC1G32YZAR	
	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP		SN74LVC1G32YEPR	
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)		SN74LVC1G32YZPR	
	SOT (SOT-23) − DBV	Reel of 3000	SN74LVC1G32DBVR	C32_
		Reel of 250	SN74LVC1G32DBVT	
	SOT (SC-70) − DCK	Reel of 3000	SN74LVC1G32DCKR	CG_
		Reel of 250	SN74LVC1G32DCKT	
	SOT (SOT-553) − DRL	Reel of 4000	SN74LVC1G32DRLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package	206°C/W
DCK package	252°C/W
DRL package	142°C/W
YEA/YZA package	154°C/W
YEP/YZP package	132°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = −100 μA	1.65 V to 5.5 V	V_{CC} − 0.1			V
		I_{OH} = −4 mA	1.65 V	1.2			
		I_{OH} = −8 mA	2.3 V	1.9			
		I_{OH} = −16 mA	3 V	2.4			
		I_{OH} = −24 mA		2.3			
		I_{OH} = −32 mA	4.5 V	3.8			
V_{OL}		I_{OL} = 100 μA	1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 8 mA	2.3 V			0.3	
		I_{OL} = 16 mA	3 V			0.4	
		I_{OL} = 24 mA				0.55	
		I_{OL} = 32 mA	4.5 V			0.55	
I_I	A or B inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5	μA
I_{off}		V_I or V_O = 5.5 V	0			±10	μA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	μA
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	μA
C_i		V_I = V_{CC} or GND	3.3 V		4		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	1.9	7.2	0.8	4.4	0.9	3.6	0.8	3.4	ns

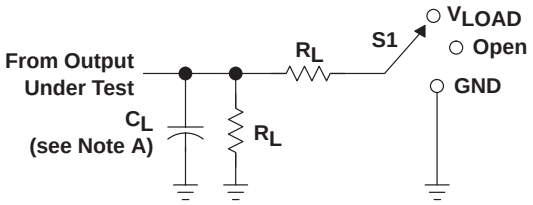
switching characteristics over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2.8	8	1.2	5.5	1.1	4.5	1	4	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	20	20	21	22	pF

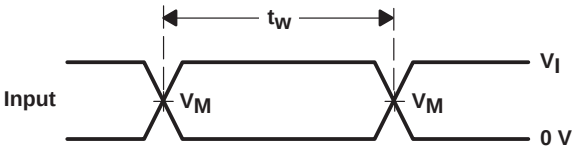
PARAMETER MEASUREMENT INFORMATION



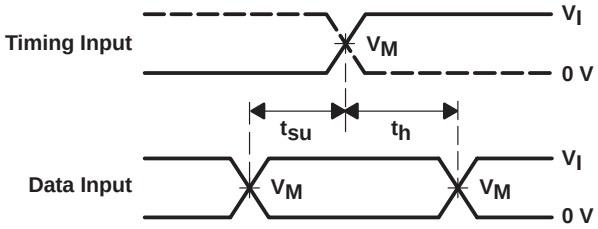
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

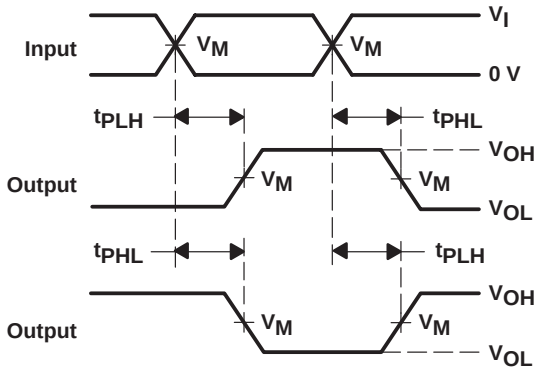
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.3 V



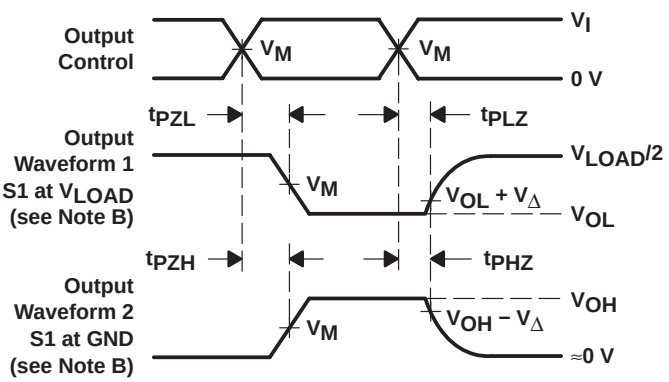
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

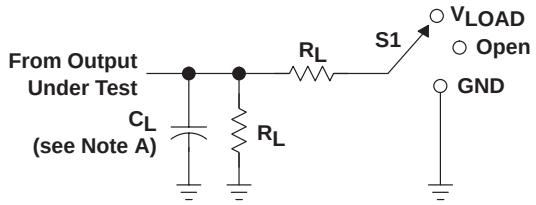


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

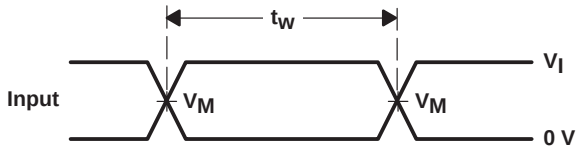
PARAMETER MEASUREMENT INFORMATION



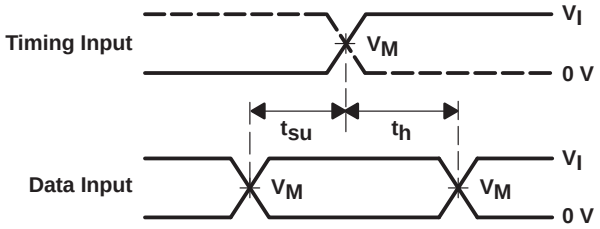
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

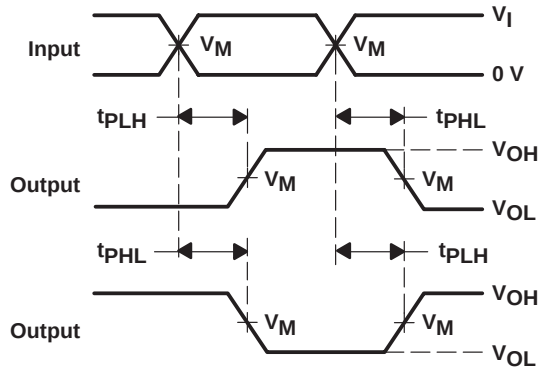
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



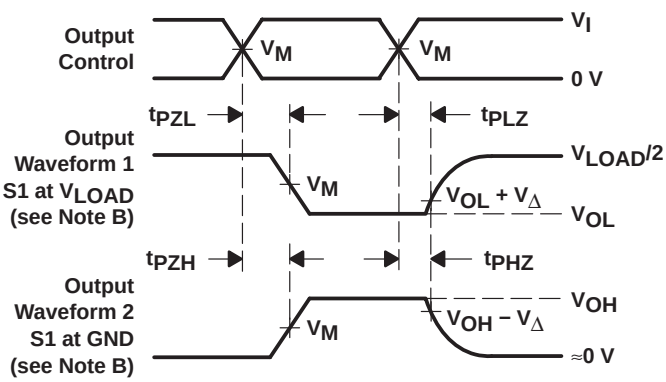
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LVC1G32DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DRLRG4	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32YEAR	ACTIVE	WCSP	YEA	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G32YEPR	ACTIVE	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G32YZAR	ACTIVE	WCSP	YZA	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74LVC1G32YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

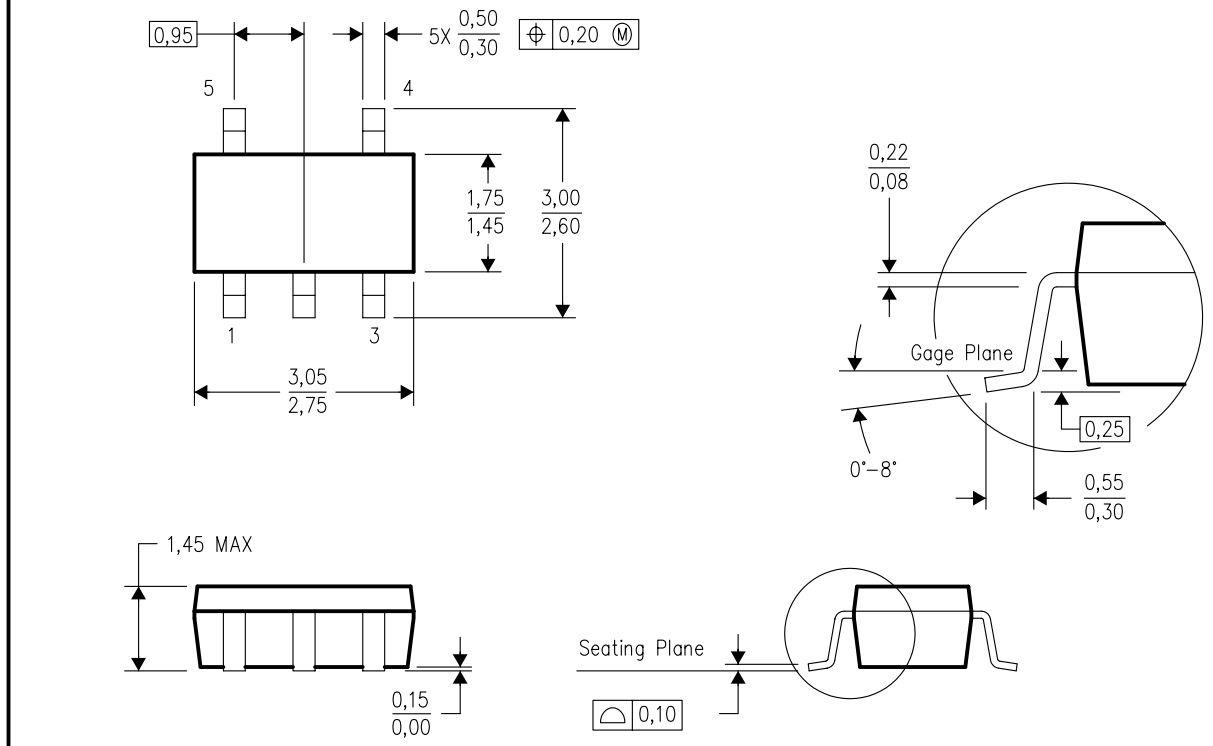
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

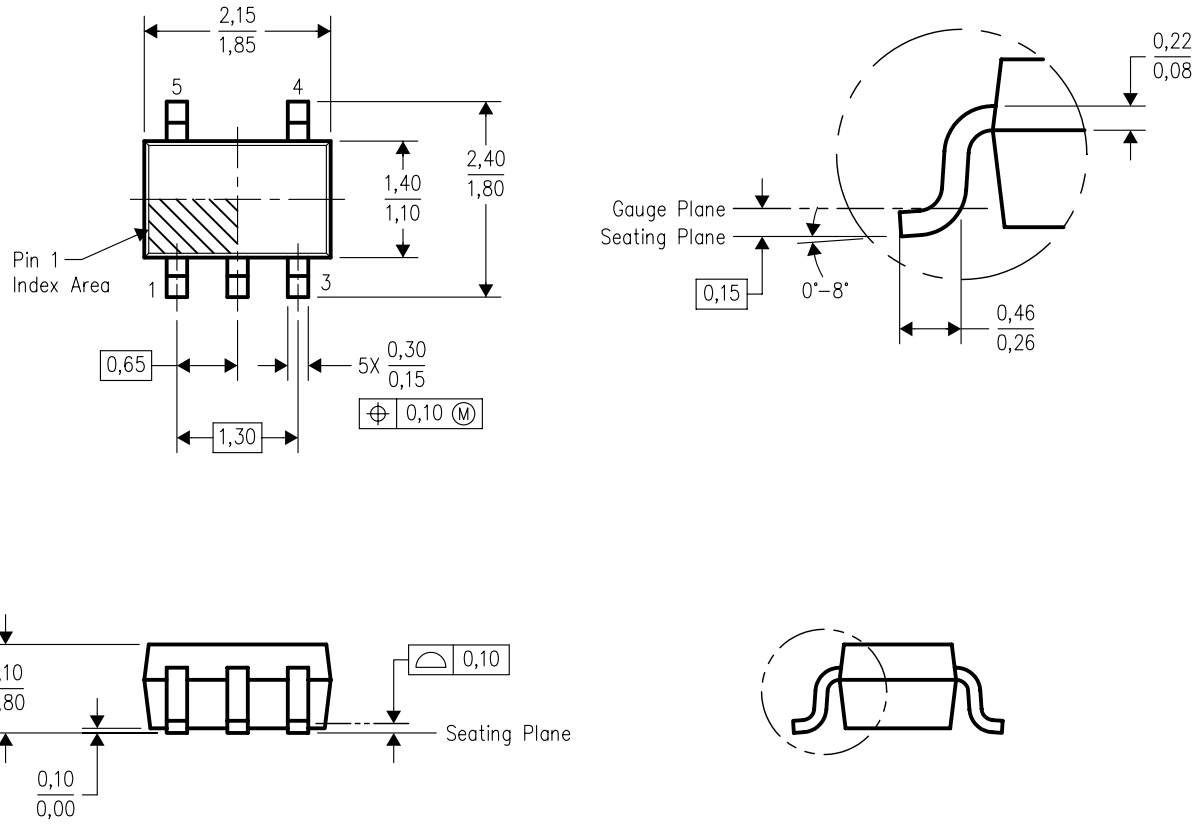
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/J 10/2005

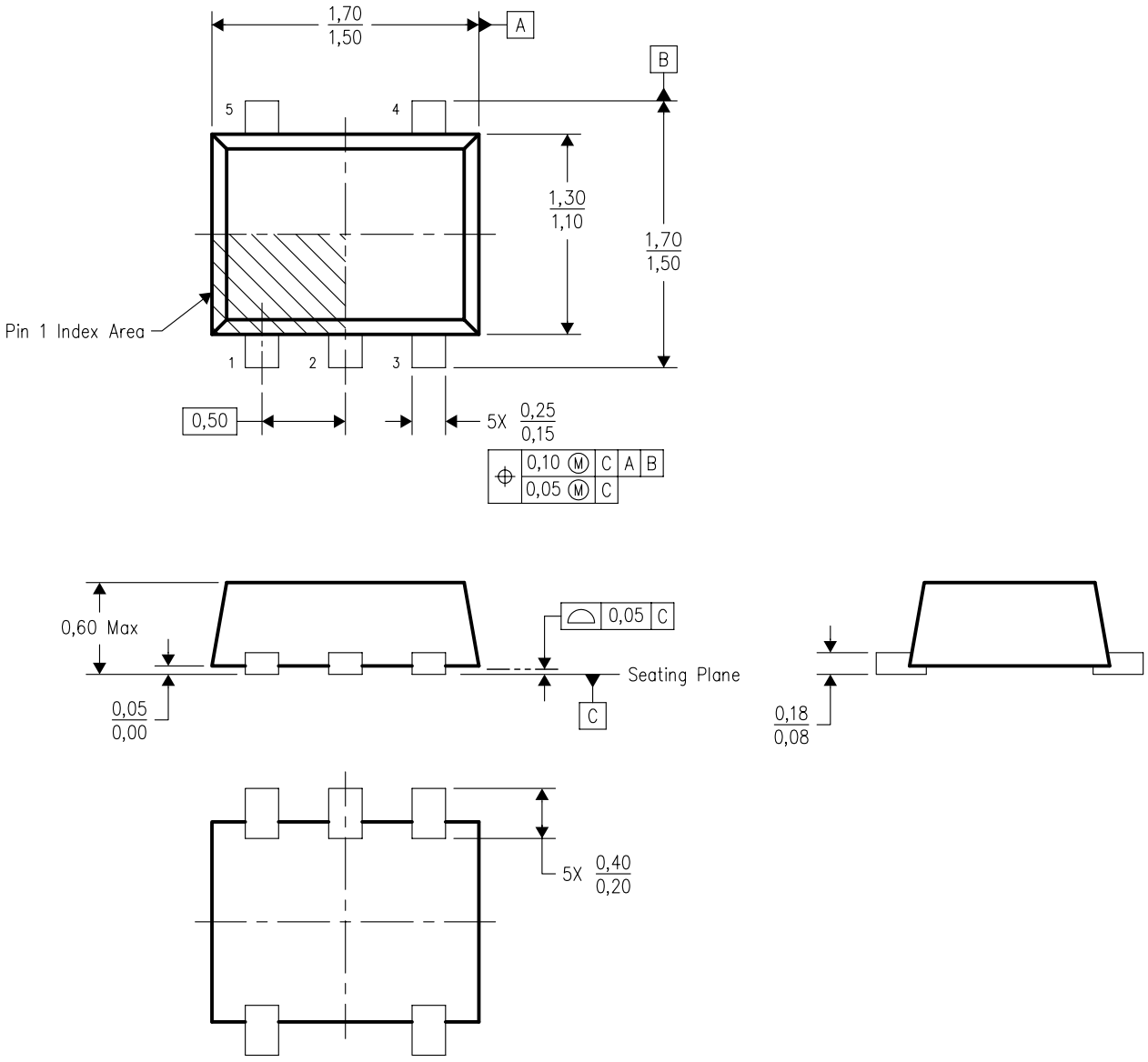
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



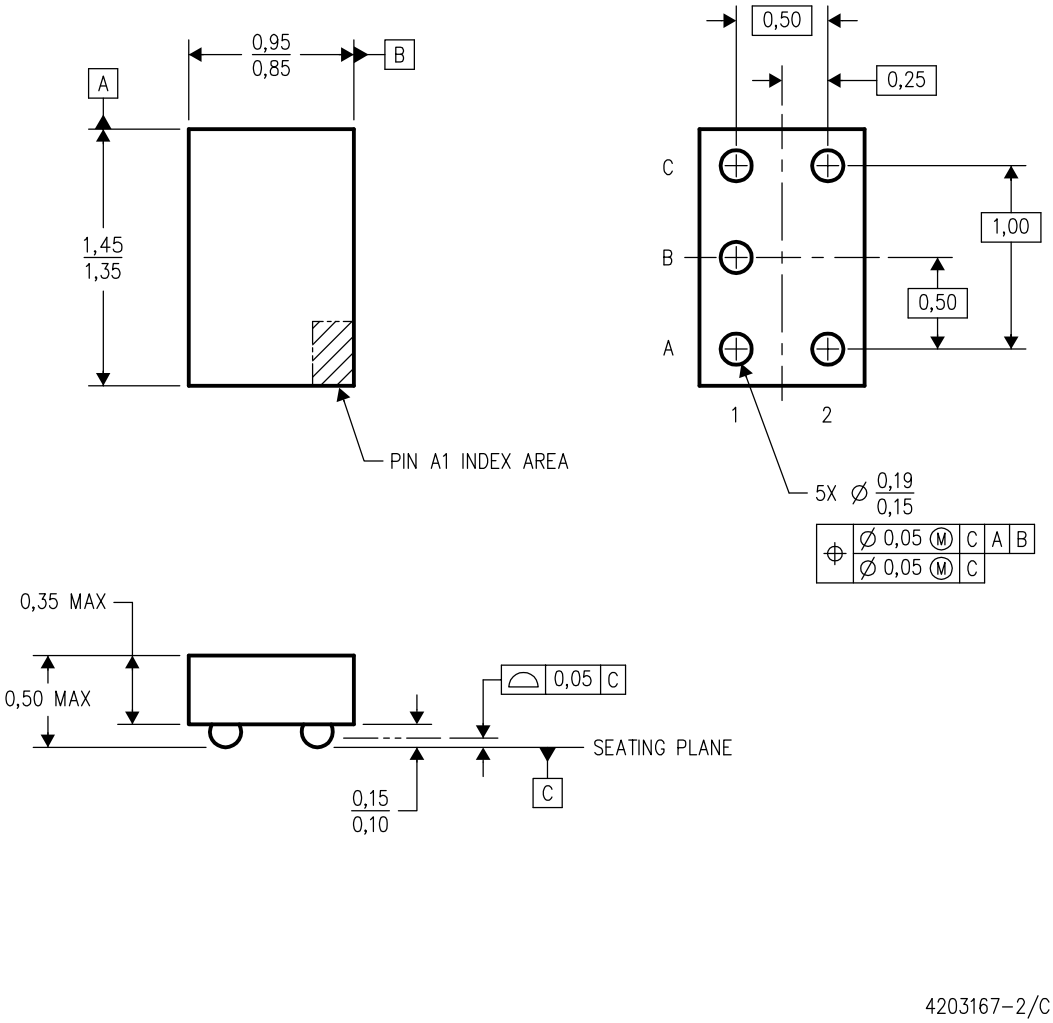
4093553–2/E 10/2005

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC package registration is pending.

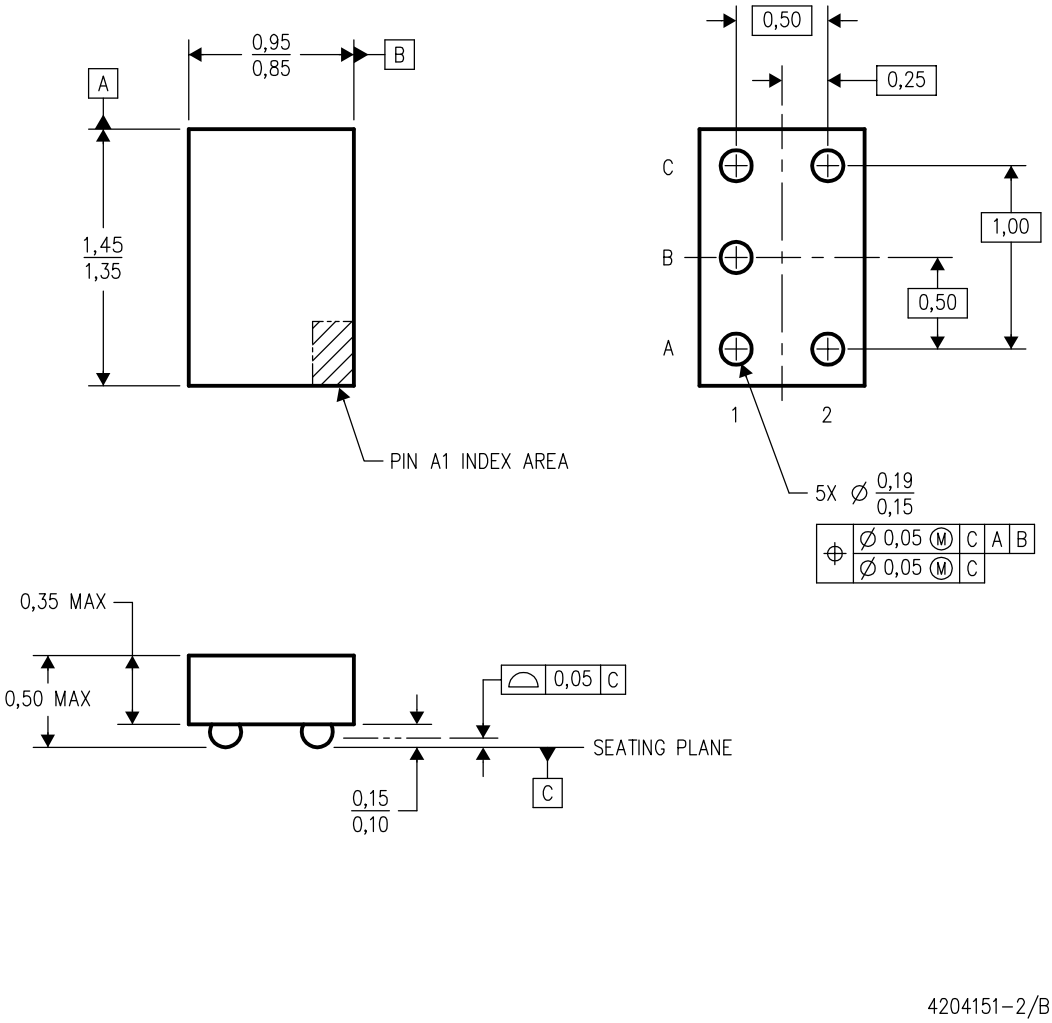
YEA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is tin–lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead–free.

NanoStar is a trademark of Texas Instruments.

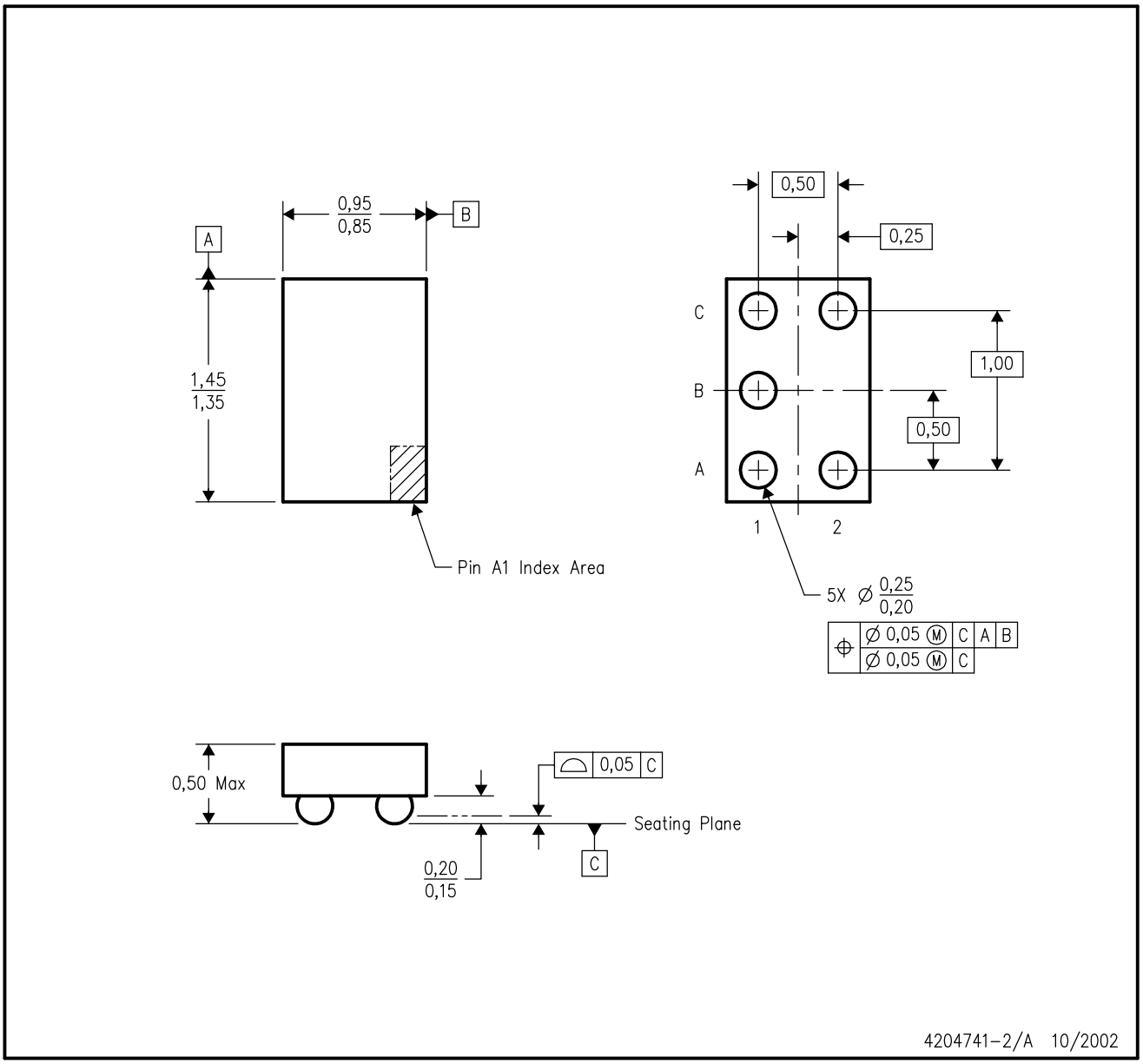
YZA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is lead–free. Refer to the 5 YEA package (drawing 4203167) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

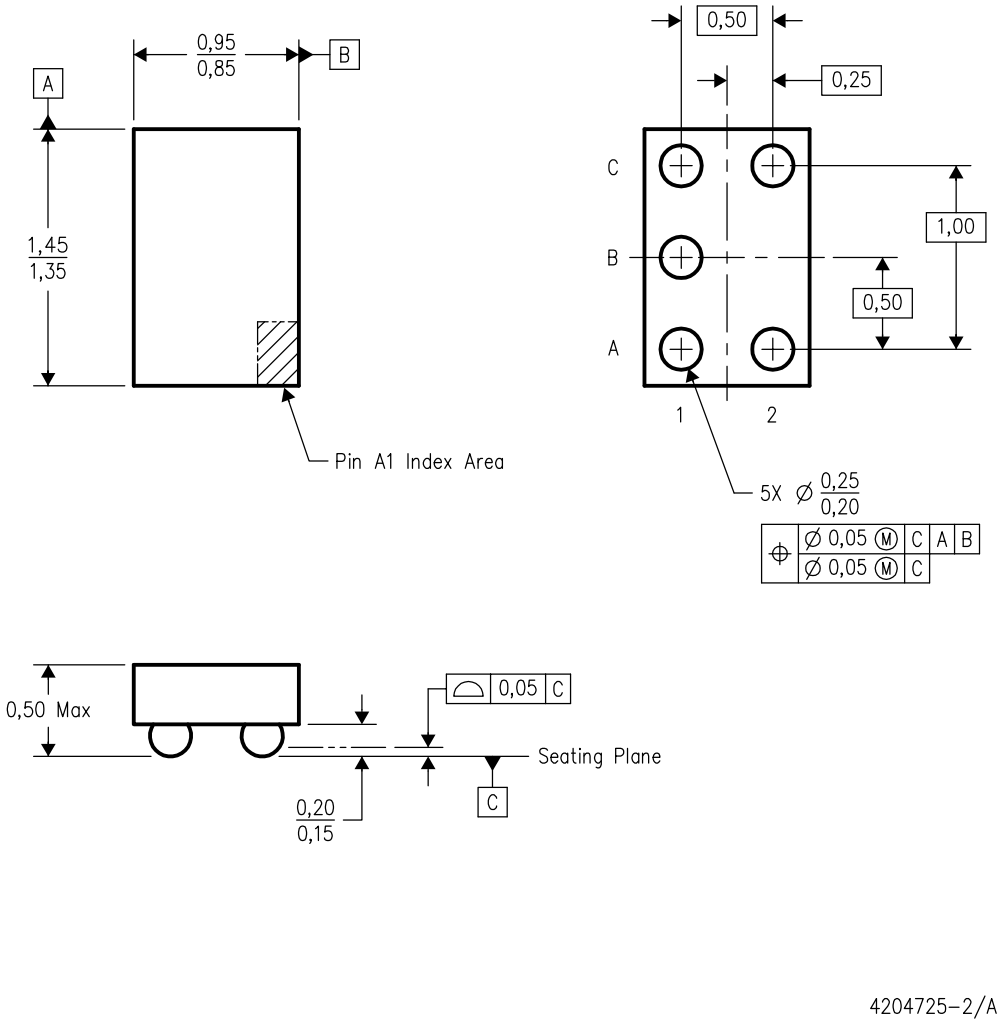
YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 5 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead–free.

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SN74LVC1G32, Status: ACTIVE

Single 2-Input Positive-OR Gate

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Features | Samples | Technical Documents
Quality & Pb-Free Data | Pricing/Packaging | Applications Notes
Related Products | Inventory | Simulation Models
Tools & Software | Symbols/Footprints | Reference Designs

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- KnowledgeBase
- Contact Technical Supp
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomencla

Datasheet

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	LVC1G32-1.8	LVC1G32-2.5	LVC1G32-3.3	LVC1G32-5.0
Voltage Node(V)	1.8	2.5	3.3	5
Performance			Optimized	
Vcc min(V)	1.65	1.65	1.65	1.65
Vcc max(V)	5.5	5.5	5.5	5.5
IOH(mA)	-4	-8	-24	-32
IOL(mA)	4	8	24	32
tpd max(ns)	8	5.5	4.4	4
ICC(uA)	10	10	10	10
Input Level	1.8V CMOS	2.5V CMOS	LV TTL	CMOS
Output Level	1.8V CMOS	2.5V CMOS	LV TTL	CMOS
No. of Gates	1	1	1	1
	Samples	Samples	Samples	Samples
	Inventory Not Available	Inventory Not Available	Inventory Not Available	Inventory Not Available

Product Information

Features

Save this to your personal library

Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
Supports 5-V V_{CC} Operation
Inputs Accept Voltages to 5.5 V
Max t_{pd} of 3.6 ns at 3.3 V
Low Power Consumption, 10-µA Max I_{CC}
±24-mA Output Drive at 3.3 V
I_{off} Supports Partial-Power-Down Mode Operation
Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
ESD Protection Exceeds JESD 22
- 2000-V Human-Body Model (A114-A)
  200-V Machine Model (A115-A)
- 1000-V Charged-Device Model (C101)

NanoStar and NanoFree are trademarks of Texas Instruments.

Description

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G32 performs the Boolean function Y = A + B or Y = (A\ • B\)\ in positive logic.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the

outputs, preventing damaging current backflow through the device when it is powered down.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price ($US) | QTY	Industry Standard (TI Pkg) | Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LVC1G32DBVR	ACTIVE	-40 to 85	0.13 | 1KU	SOT-23 (DBV) | 5	View	3000		Request Free Samples
SN74LVC1G32DBVRE4	ACTIVE	-40 to 85	0.12 | 1KU	SOT-23 (DBV) | 5	View	3000		Purchase Samples
SN74LVC1G32DBVRG4	ACTIVE	-40 to 85	0.13 | 1KU	SOT-23 (DBV) | 5	View	3000		Purchase Samples
SN74LVC1G32DBVT	ACTIVE	-40 to 85	0.46 | 1KU	SOT-23 (DBV) | 5	View	250		Purchase Samples
SN74LVC1G32DBVTE4	ACTIVE	-40 to 85	0.46 | 1KU	SOT-23 (DBV) | 5	View	250		Purchase Samples
SN74LVC1G32DCKR	ACTIVE	-40 to 85	0.13 | 1KU	SC70 (DCK) | 5	View	3000		Request Free Samples
SN74LVC1G32DCKRE4	ACTIVE	-40 to 85	0.13 | 1KU	SC70 (DCK) | 5	View	3000		Request Free Samples
SN74LVC1G32DCKRG4	ACTIVE	-40 to 85	0.15 | 1KU	SC70 (DCK) | 5	View	3000		Purchase Samples
SN74LVC1G32DCKT	ACTIVE	-40 to 85	0.46 | 1KU	SC70 (DCK) | 5	View	250		Purchase Samples
SN74LVC1G32DCKTE4	ACTIVE	-40 to 85	0.46 | 1KU	SC70 (DCK) | 5	View	250		Purchase Samples
SN74LVC1G32DRLR	ACTIVE	-40 to 85	0.26 | 1KU	SOP (DRL) | 5		4000		Request Free Samples
SN74LVC1G32DRLRG4	ACTIVE	-40 to 85	0.26 | 1KU	SOP (DRL) | 5		4000		Request Free Samples
SN74LVC1G32YEAR	ACTIVE	-40 to 85	0.23 | 1KU	WCSP (YEA) | 5		3000		Purchase Samples
SN74LVC1G32YEPR	ACTIVE	-40 to 85	0.23 | 1KU	WCSP (YEP) | 5		3000		Purchase Samples
SN74LVC1G32YZAR	ACTIVE	-40 to 85	0.23 | 1KU	WCSP (YZA) | 5		3000		Request Free Samples
SN74LVC1G32YZPR	ACTIVE	-40 to 85	0.23 | 1KU	WCSP (YZP) | 5		3000		Request Free Samples

Inventory

	TI Inventory Status			Reported Distributor Inventory			
SN74LVC1G32DBVR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k | 4 Jan	6 Weeks	Americas	DigiKey	>1k	
				Europe	Avnet-SILICA	175	
SN74LVC1G32DBVRE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k | 12 Dec	6 Weeks	None Reported View Distributors			
SN74LVC1G32DBVRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	>10k*	>10k | 9 Jan	6 Weeks	None Reported View Distributors			
SN74LVC1G32DBVT	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			

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Choose a Region

	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	3250*	>10k | 12 Dec	6 Weeks	Americas	Newark InOne	637	
SN74LVC1G32DBVTE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	3250*	>10k | 12 Dec	6 Weeks	None Reported View Distributors			
SN74LVC1G32DCKR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	6000 | 16 Jan	8 Weeks	Americas	Avnet	>1k	
		>10k | 24 Jan			Newark InOne	>1k	
				Asia	P&S	589	
				Europe	Arrow Northern Europe	>1k	
SN74LVC1G32DCKRE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	6000 | 16 Jan	8 Weeks	None Reported View Distributors			
		>10k | 24 Jan					
SN74LVC1G32DCKRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 12 Dec	6 Weeks	None Reported View Distributors			
SN74LVC1G32DCKT	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	1500*	>10k | 7 Feb	6 Weeks	Americas	Arrow	683	
				Asia	P&S	240	
				Europe	Avnet-SILICA	250	
SN74LVC1G32DCKTE4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	1500*	>10k | 7 Feb	6 Weeks	None Reported View Distributors			
SN74LVC1G32DRLR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 12 Dec	4 Weeks	Americas	DigiKey	>1k	
SN74LVC1G32DRLRG4	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 12 Dec	4 Weeks	None Reported View Distributors			
SN74LVC1G32YEAR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 12 Dec	6 Weeks	None Reported View Distributors			
SN74LVC1G32YEPR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 31 Jan	9 Weeks	None Reported View Distributors			

SN74LVC1G32YZAR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k | 20 Feb	10 Weeks	Americas	DigiKey	>1k	
SN74LVC1G32YZPR	As of 9:07 AM GMT, 29 Nov 2005			As of 9:07 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2997 | 14 Feb	10 Weeks	Americas	DigiKey	973	
		>10k | 20 Feb					

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Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
SN74LVC1G32DBVR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DBVRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DBVRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DBVT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DBVTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DCKR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DCKRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DCKRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DCKT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DCKTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DRLR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32DRLRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC1G32YEAR	TBD	SNPB	Level-1-260C-UNLIM	View	View
SN74LVC1G32YEPR	TBD	SNPB	Level-1-260C-UNLIM	View	View
SN74LVC1G32YZAR	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM	View	View
SN74LVC1G32YZPR	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

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Simulation Models

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