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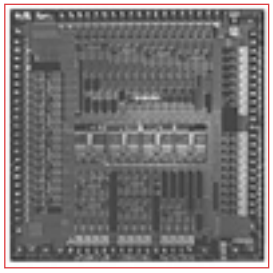
BCM8212 PRODUCT Brief



TRANSCEIVER WITH INTERNAL LOOP TIMING AND PHASE DETECTOR

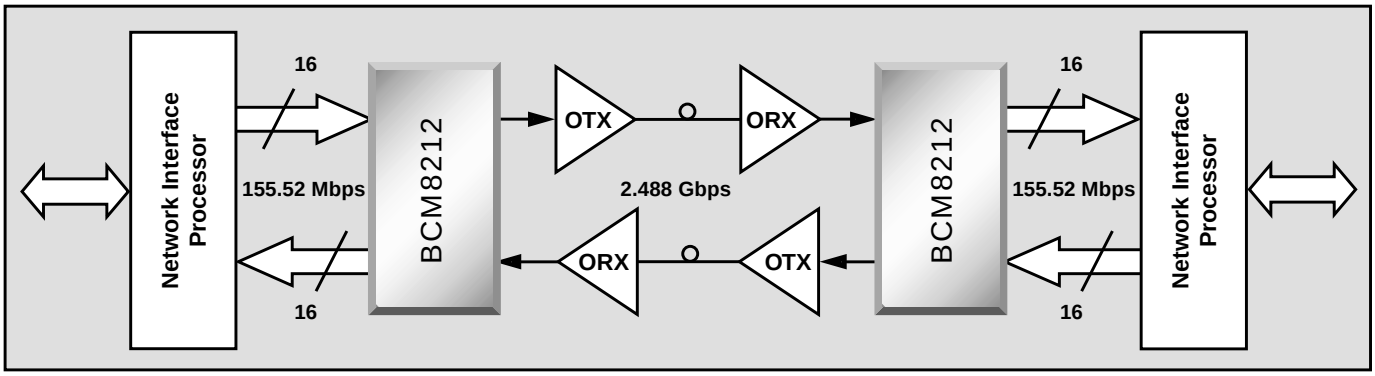
BCM8212 FEATURES

- **2.488-Gbps SONET/SDH transceiver with dual differential serial I/O**
- **Fully integrated CDR, MUX, DEMUX, and CMU with 16-bit, 155.52-MHz LVPECL interface**
- **On-chip, PLL-based clock generator**
- **Internal phase detector and charge pump for cleanup PLL**
- **Line and system loopback modes**
- **Loss-of-signal output (LOSB) and input (LOSIB)**
- **TX and RX lock detect**
- **Elastic buffering with FIFO overflow alarm**
- **Selectable 77.76/155.52-MHz reference clock**
- **Selectable RX clock and RX data squelch on LOS**
- **Selectable loop timing mode**
- **Dual 2.5V/3.3V supplies**
- **Power dissipation: 1.2W typical**
- **Selectable divide-by-32 or divide-by-16 receiver/ transmitter low-speed parallel output clock**
- **Standard CMOS fabrication process**
- **23 × 23 mm, 208-pin BGA package**

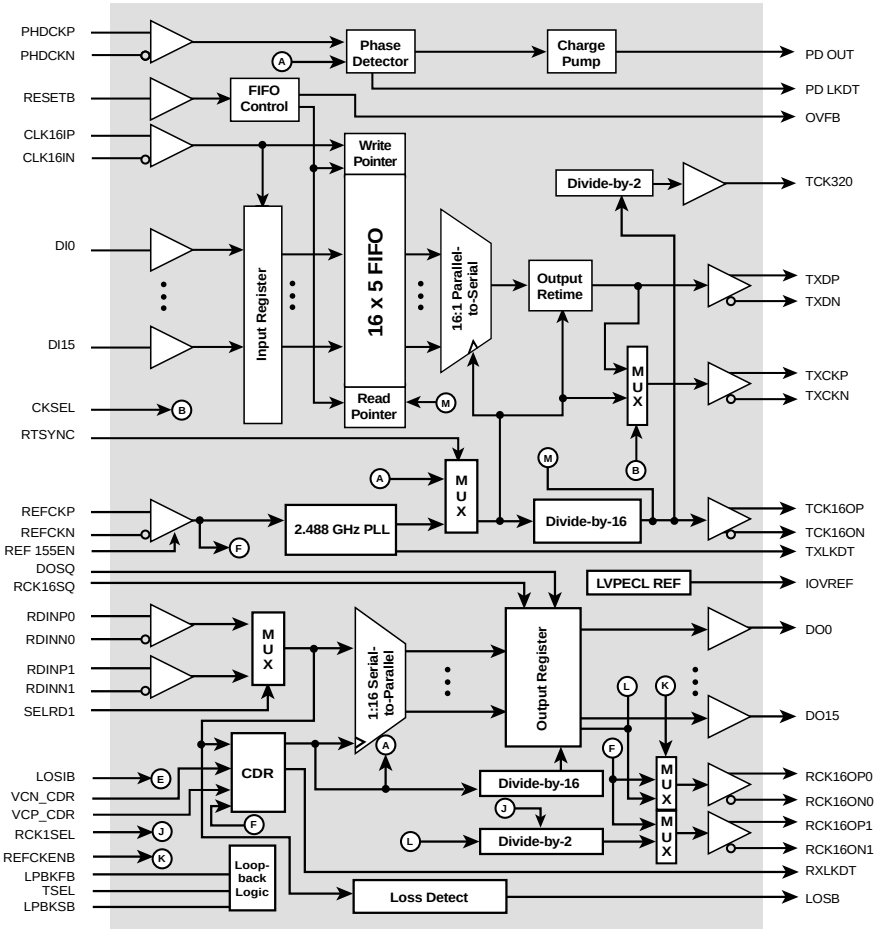
SUMMARY OF BENEFITS

- **Low power consumption eliminates external heat sinks, fans for system airflow, and expensive high current power supplies.**
- **Supports SONET dual-fiber ring architecture.**
- **High integration reduces design cycle and time to market.**
- **Provides increased port density per board and system.**
- **Features low jitter: 3 mUI_{RMS} typical.**
- **CMOS-based device uses the most effective silicon economy of scale.**
- **Exceeds SONET jitter requirements, which allows the use of low-cost optics.**
- **Target applications:**
  - OC-48/STM-16 transmission equipment
  - SONET/SDH optical modules
  - ADD/DROP multiplexers
  - Digital cross-connects
  - ATM switch backbone
  - SONET/SDH test equipment
  - Terabit and edge routers

Application Block Diagram



Block Diagram



The **BCM8212** SONET/SDH transceiver is a fully integrated serialization/deserialization SONET OC-48 (2.488 Gbps) interface device with an integrated Clock Multiplication Unit (CMU) and an integrated Clock and Data Recovery (CDR) circuit. On-chip clock synthesis is performed by the high-frequency and low-jitter, phase-locked loop on the **BCM8212** transceiver chip, allowing the use of a slower 77.76/155.52-MHz external transmit clock reference.

Dual RX and TX 2.488 Gbps interfaces support dual-fiber ring architectures. Clock recovery is performed on the device by synchronizing its on-chip VCO directly to the incoming data stream. The low-jitter, LVPECL interface guarantees compliance with the bit error rate requirements of the Telcordia GR-253-CORE, ANSI, and ITU-T standards. The **BCM8212** is packaged in a 23 x 23 x 1.53 mm, 208-pin BGA.

The **BCM8212** operates in a 2.5/3.3V configuration. The core and CML I/Os operate at 2.5V. The LVPECL I/Os operate at 3.3V.

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