

OMNIFET: fully autoprotected Power MOSFET

Datasheet - production data



- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET
- Standard TO-220 package
- Compliant with 2002/95/EC European directive

Description

The VNP35N07-E, VNB35N07-E and VNV35N07-E are monolithic devices made using STMicroelectronics VIPower® technology, intended for replacement of standard Power MOSFETs in DC to 50 KHz applications.

Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Features

Type	V _{clamp}	R _{DS(on)}	I _{lim}
VNP35N07-E	70 V	0.028 Ω	35 A
VNB35N07-E	70 V	0.028 Ω	35 A
VNV35N07-E	70 V	0.028 Ω	35 A

- Automotive qualified
- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
TO-220	VNP35N07-E	VNP35N07TR-E
D ² PAK	VNB35N07-E	VNB35N07TR-E
PowerSO-10	VNV35N07-E	VNV35N07TR-E

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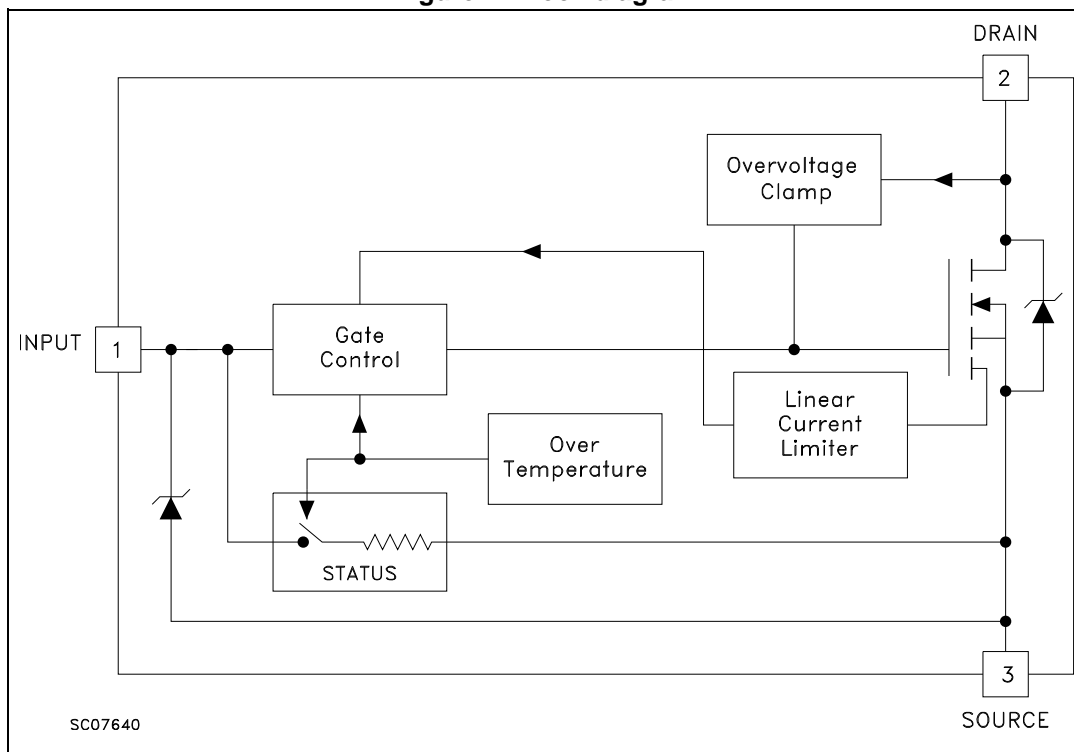
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1 Block diagram

Figure 1. Block diagram



1. PowerSO-10 pin configuration: INPUT = 6, 7, 8, 9, 10; SOURCE = 1, 2, 4, 5; DRAIN = TAB.

2 Electrical specification

2.1 Absolute maximum rating

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK PowerSO-10	TO-220	
V _{DS}	Drain-source voltage (V _{in} = 0)	Internally clamped		V
V _{in}	Input voltage	18		V
I _D	Drain current	Internally limited		A
I _R	Reverse DC output current	-50		A
V _{esd}	Electrostatic Discharge (C = 100 pF; R = 1.5 KΩ)	2000		V
P _{tot}	Total dissipation at T _C = 25°C	125	40	W
T _J	Operating junction temperature	Internally limited		°C
T _C	Case operating temperature	Internally limited		°C
T _{stg}	Storage temperature	-55 to 150		°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		PowerSO-10	D ² PAK	TO-220	
R _{thj-case}	Thermal Resistance Junction-case (max)	1	1	3.12	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient (max)	50	62.5	62.5	°C/W

2.3 Electrical characteristics

$T_{\text{case}} = 25^{\circ}\text{C}$ unless otherwise specified.

Table 4. Off

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain-source clamp voltage	$I_{\text{D}} = 200 \text{ mA}; V_{\text{in}} = 0 \text{ V}$	60	70	80	V
V_{CLTH}	Drain-source clamp threshold voltage	$I_{\text{D}} = 2 \text{ mA}; V_{\text{in}} = 0 \text{ V}$	55			V
V_{INCL}	Input-source reverse clamp voltage	$I_{\text{in}} = -1 \text{ mA}$	-1		-0.3	V
I_{DSS}	Zero input voltage drain current ($V_{\text{in}} = 0 \text{ V}$)	$V_{\text{DS}} = 13 \text{ V}; V_{\text{in}} = 0 \text{ V}$			50	mA
		$V_{\text{DS}} = 25 \text{ V}; V_{\text{in}} = 0 \text{ V}$			200	μA
I_{ISS}	Supply current from input pin	$V_{\text{DS}} = 0 \text{ V}; V_{\text{in}} = 10 \text{ V}$		250	500	μA

Table 5. On

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{\text{IN(th)}}^{(1)}$	Input threshold voltage	$V_{\text{DS}} = V_{\text{in}}; I_{\text{D+}}, I_{\text{in}} = 1 \text{ mA}$	0.8	—	3	V
$R_{\text{DS(on)}}^{(1)}$	Static drain-source on resistance	$V_{\text{in}} = 10 \text{ V}; I_{\text{D}} = 18 \text{ A}$		—	0.028	Ω
		$V_{\text{in}} = 5 \text{ V}; I_{\text{D}} = 18 \text{ A}$		—	0.035	Ω

1. Pulsed: Pulse duration = 300 ms, duty cycle 1.5%.

Table 6. Dynamic

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$g_{\text{fs}}^{(1)}$	Forward transconductance	$V_{\text{DS}} = 13 \text{ V}; I_{\text{D}} = 18 \text{ A}$	20	25		S
C_{OSS}	Output capacitance	$V_{\text{DS}} = 13 \text{ V}; f = 1 \text{ MHz}; V_{\text{in}} = 0 \text{ V}$		980	1400	pF

1. Pulsed: Pulse duration = 300 ms, duty cycle 1.5%.

Table 7. Switching

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{\text{d(on)}}^{(1)}$	Turn-on delay time	$V_{\text{DD}} = 28 \text{ V}; I_{\text{d}} = 18 \text{ A};$ $V_{\text{gen}} = 10 \text{ V}; R_{\text{gen}} = 10 \Omega$ (see Figure 2)	—	100	200	ns
$t_{\text{r}}^{(1)}$	Rise time		—	350	600	ns
$t_{\text{d(off)}}^{(1)}$	Turn-off delay time		—	650	1000	ns
$t_{\text{f}}^{(1)}$	Fall time		—	200	350	ns
$t_{\text{d(on)}}^{(1)}$	Turn-on delay time	$V_{\text{DD}} = 28 \text{ V}; I_{\text{d}} = 18 \text{ A};$ $V_{\text{gen}} = 10 \text{ V}; R_{\text{gen}} = 1000 \Omega$ (see Figure 2)	—	500	800	μs
$t_{\text{r}}^{(1)}$	Rise time		—	2.7	4.2	μs
$t_{\text{d(off)}}^{(1)}$	Turn-off delay time		—	10	16	μs
$t_{\text{f}}^{(1)}$	Fall time		—	4.3	6.5	μs

Table 7. Switching (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$(di/dt)_{on}^{(1)}$	Turn-on current slope	$V_{DD} = 28\text{ V}; I_D = 18\text{ A}; V_{in} = 10\text{ V}; R_{gen} = 10\ \Omega$	—	60		A/ μs
$Q_i^{(1)}$	Total input charge	$V_{DD} = 12\text{ V}; I_D = 18\text{ A}; V_{in} = 10\text{ V}$	—	100		nC

1. Parameters guaranteed by design/characterization.

Table 8. Source drain diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 18\text{ A}; V_{in} = 0\text{ V}$	—		1.6	V
$t_{rr}^{(2)}$	Reverse recovery time	$I_{SD} = 18\text{ A}; di/dt = 100\text{ A}/\mu\text{s}; V_{DD} = 30\text{ V}; T_J = 25\text{ }^\circ\text{C}$ (see Figure 5)	—	250		ns
$Q_{rr}^{(2)}$	Reverse recovery charge		—	1		μC
$I_{RRM}^{(2)}$	Reverse recovery current		—	8		A

1. Pulsed: Pulse duration = 300 ms, duty cycle 1.5%.

2. Parameters guaranteed by design/characterization.

Table 9. Protection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain current limit	$V_{IN} = 10\text{ V}; V_{DS} = 13\text{ V}$	25	35	45	A
		$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$	25	35	45	A
$t_{dlim}^{(1)}$	Step response current limit	$V_{in} = 10\text{ V}$		35	60	μs
		$V_{in} = 5\text{ V}$		70	140	μs
$T_{jsh}^{(1)}$	Overtemperature shutdown		150			$^\circ\text{C}$
$T_{jrs}^{(1)}$	Overtemperature reset		135			$^\circ\text{C}$
$I_{gf}^{(1)}$	Fault sink current	$V_{IN} = 10\text{ V}; V_{DS} = 13\text{ V}$		50		mA
		$V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$		20		mA
$E_{as}^{(1)}$	Single pulse avalanche energy	Starting $T_J = 25\text{ }^\circ\text{C}; V_{DD} = 20\text{ V}; V_{in} = 10\text{ V}; R_{gen} = 1\text{ K}\Omega; L = 10\text{ mH}$	2.5			J

1. Parameters guaranteed by design/characterization.

Figure 2. Switching times test circuits for resistive load



Figure 3. Input charge test circuit



Figure 4. Unclamped inductive load test circuits



Figure 5. Test circuit for inductive load switching & diode recovery times

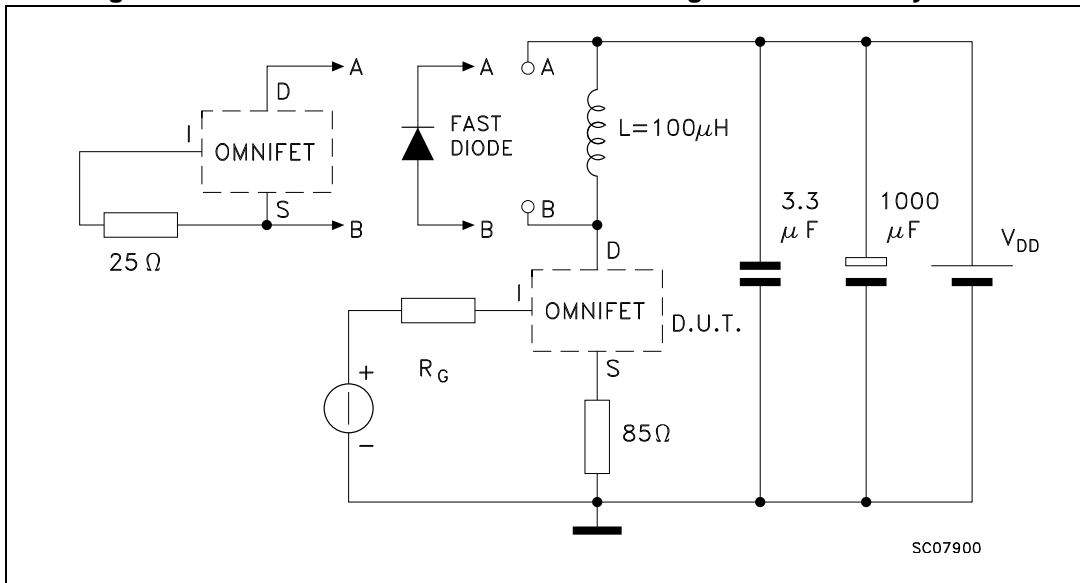


Figure 6. Waveforms



Figure 7. Unclamped inductive waveforms



Figure 8. Thermal impedance for TO-220



Figure 9. Derating curve

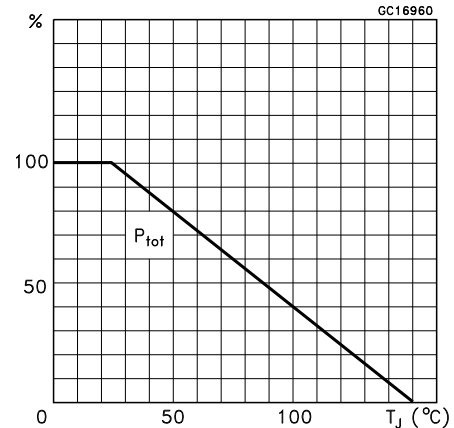


Figure 10. Static drain-source on resistance



Figure 11. Static drain-source on resistance vs input voltage

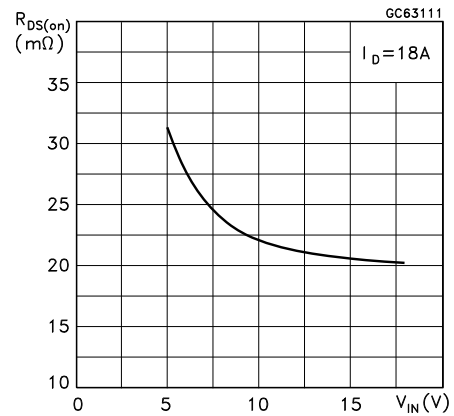


Figure 12. Output characteristics



Figure 13. Transconductance

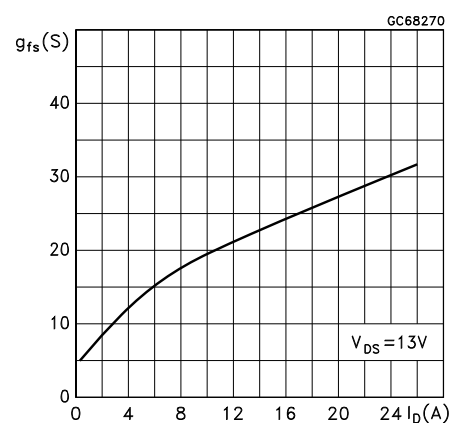


Figure 14. Static drain-source on resistance



Figure 15. Input charge vs input voltage



Figure 16. Normalized on resistance vs temperature (part 1)



Figure 17. Normalized on resistance vs temperature (part 2)



Figure 18. Normalized input threshold voltage vs temperature



Figure 19. Capacitance variations



Figure 20. Turn-on current slope (part 1)

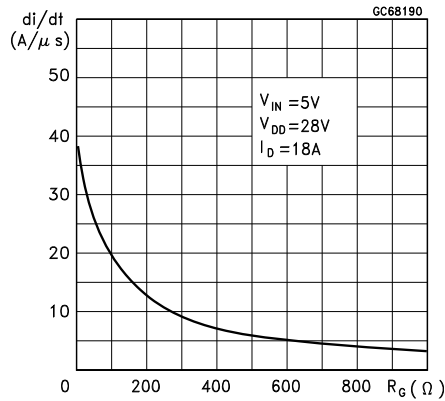


Figure 21. Turn-on current slope (part 2)

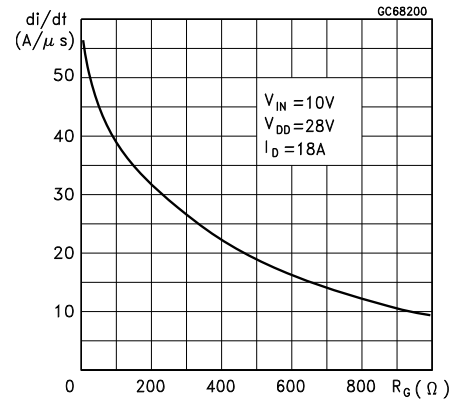


Figure 22. Turn-off drain-source voltage slope (part 1)

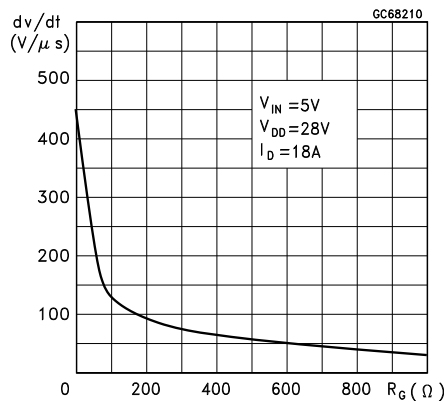


Figure 23. Turn-off drain-source voltage slope (part 2)

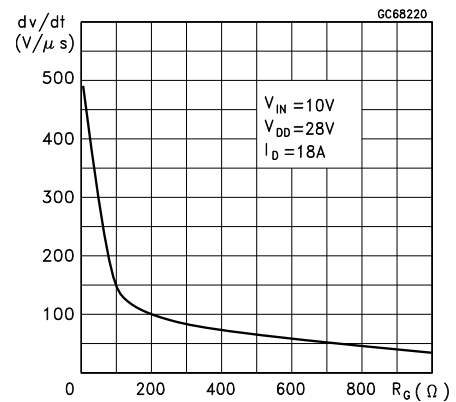


Figure 24. Switching time resistive load (part 1)

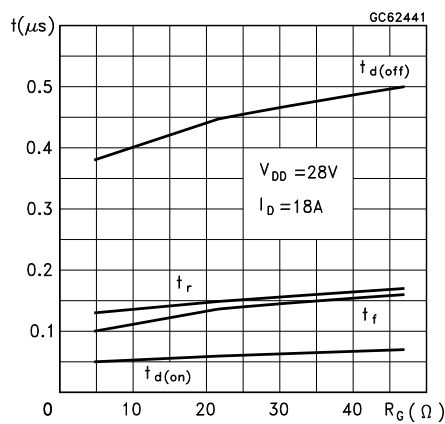


Figure 25. Switching time resistive load (part 2)

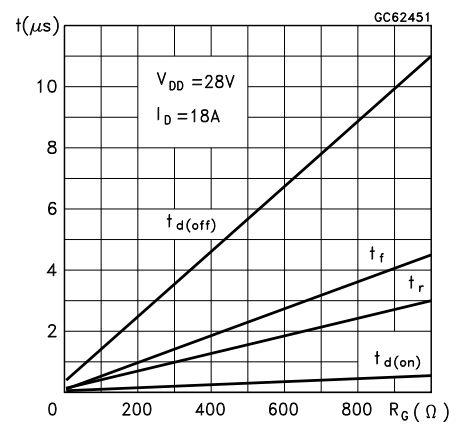


Figure 26. Current limit vs junction temperature

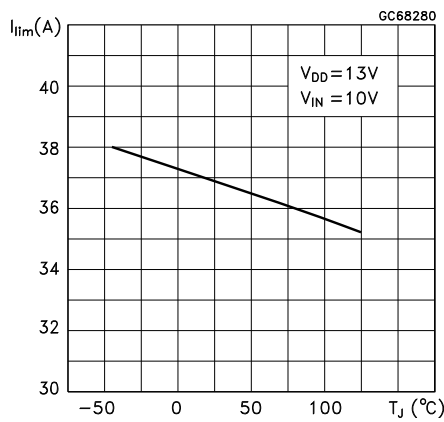


Figure 27. Source drain diode forward characteristics



Figure 28. Switching time resistive load

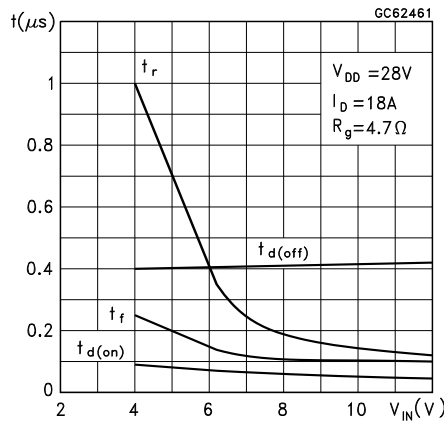


Figure 29. Step response current Limit

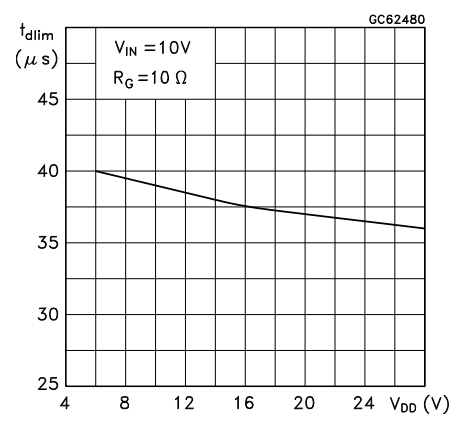
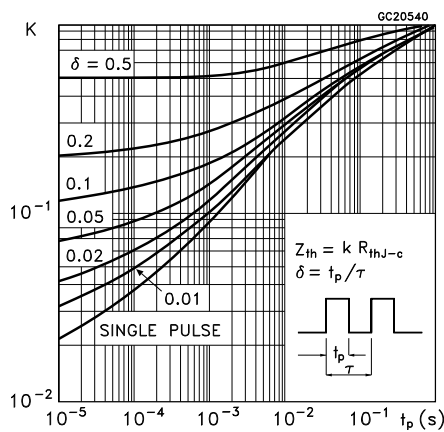


Figure 30. Thermal impedance for D²PAK/ PowerSO-10



3 Protection features

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{ISS}) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

- **Overvoltage Clamp Protection:** internally set at 70V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **Linear Current Limiter Circuit:** limits the drain current I_d to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .
- **Overtemperature and Short Circuit Protection:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150°C. The device is automatically restarted when the chip temperature falls below 135°C.
- **Status Feedback:** in the case of an overtemperature fault condition, a Status Feedback is provided through the input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω .

The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this devices are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

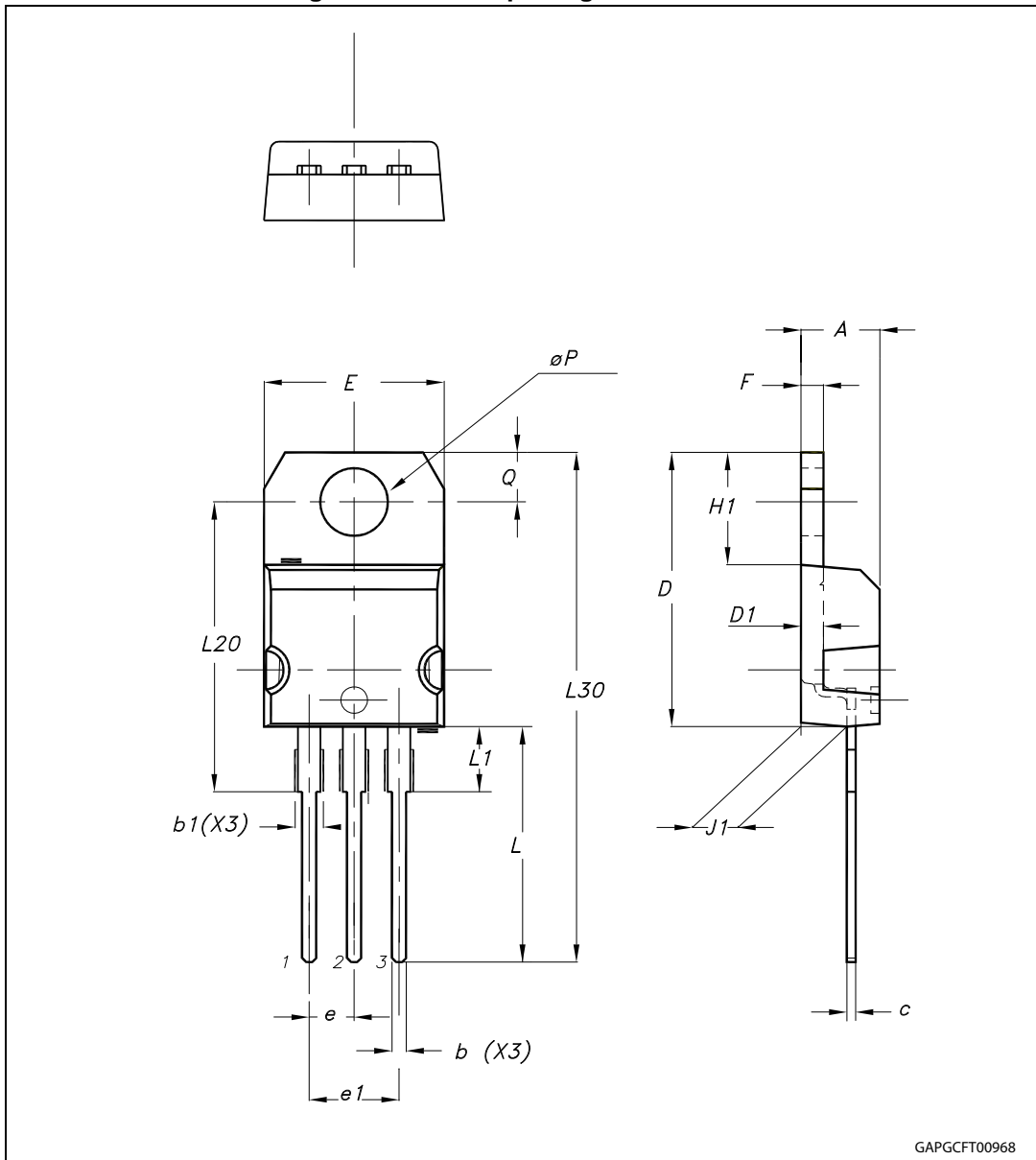
ECOPACK[®] is an ST trademark.

4.1 TO-220 package information

Table 10. TO-220 mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95
Package weight	1.9Gr. (Typ.)		

Figure 31. TO-220 package dimensions



4.2 D²PAK package information

Table 11. D²PAK mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 32. D²PAK package dimensions



4.3 PowerSO-10 mechanical data

Table 12. PowerSO-10 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1 ⁽¹⁾	7.40		7.60
E	13.80		14.40
E1 ⁽¹⁾	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°

1. Resin protrusion not included (max value: 0.20 mm per side)

Figure 33. PowerSO-10 package dimensions



5 Revision history

Table 13. Document revision history

Date	Revision	Changes
09-Jan-2014	1	Initial release.
07-May-2014	2	Added D ² PAK package and related details. <i>Table 2: Absolute maximum ratings:</i> – P _{tot} : updated value <i>Table 3: Thermal data:</i> – R _{thj-case} : updated value
02-Feb-2015	3	Added PowerSO-10 package and related details. Updated <i>Chapter 4: Package information</i>

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