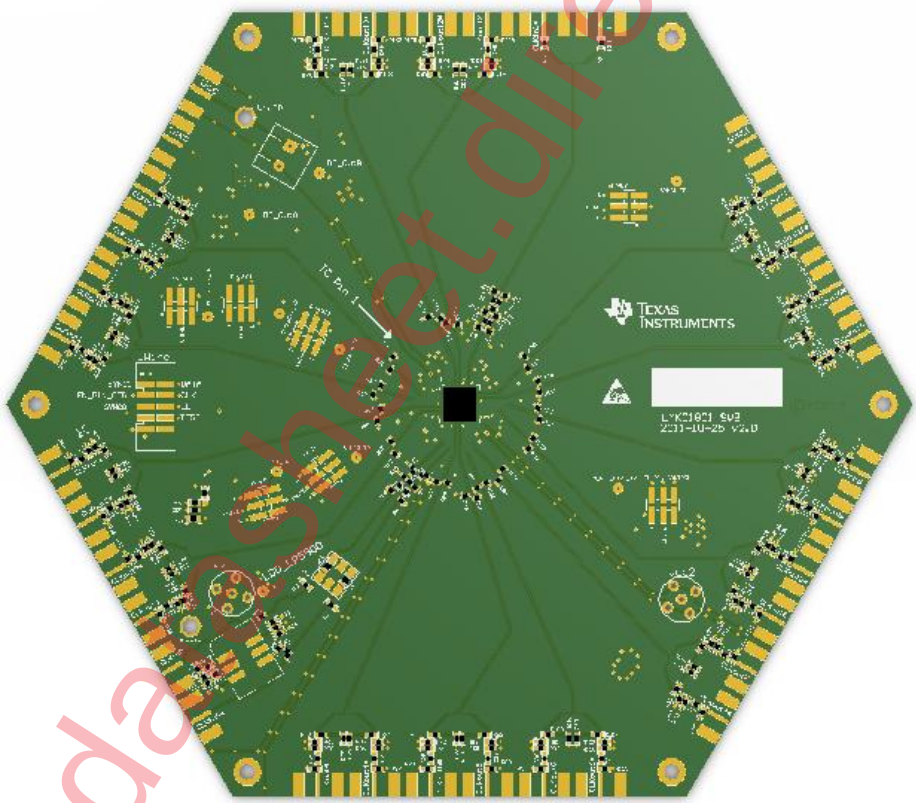
LMK01801
Dual Clock Divider Buffer
Evaluation Board Operating Instructions

7 December 2011



LMK01801 EVAL

Texas Instruments, Inc.

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General Description

The LMK01801 Evaluation Board simplifies evaluation of the LMK01801 Dual Clock Buffer Divider. Configuring and controlling the board is accomplished using Texas Instrument's *CodeLoader* software, which can be downloaded from: http://www.ti.com/tool/codeloader. The LMK01801 can also be configured to operate in a pin control mode via headers on the PCB.

Block Diagram

The block diagram in Figure 1 illustrates the functional architecture of the LMK01801 clock divider buffer. The LMK01801 is a very low noise solution for clocking systems that require distribution and frequency division of precision clocks. The LMK01801 features extremely low residual noise, frequency division, digital and analog delay adjustments, and fourteen (14) programmable differential outputs: LVPECL, LVDS and LVCMOS (2 outputs per differential output). The LMK01801 features two independent inputs that can be driven differentially or in single-ended mode. The first input drives output Bank A consisting of eight (8) outputs. The second input drives output Bank B consisting of six (6) outputs.

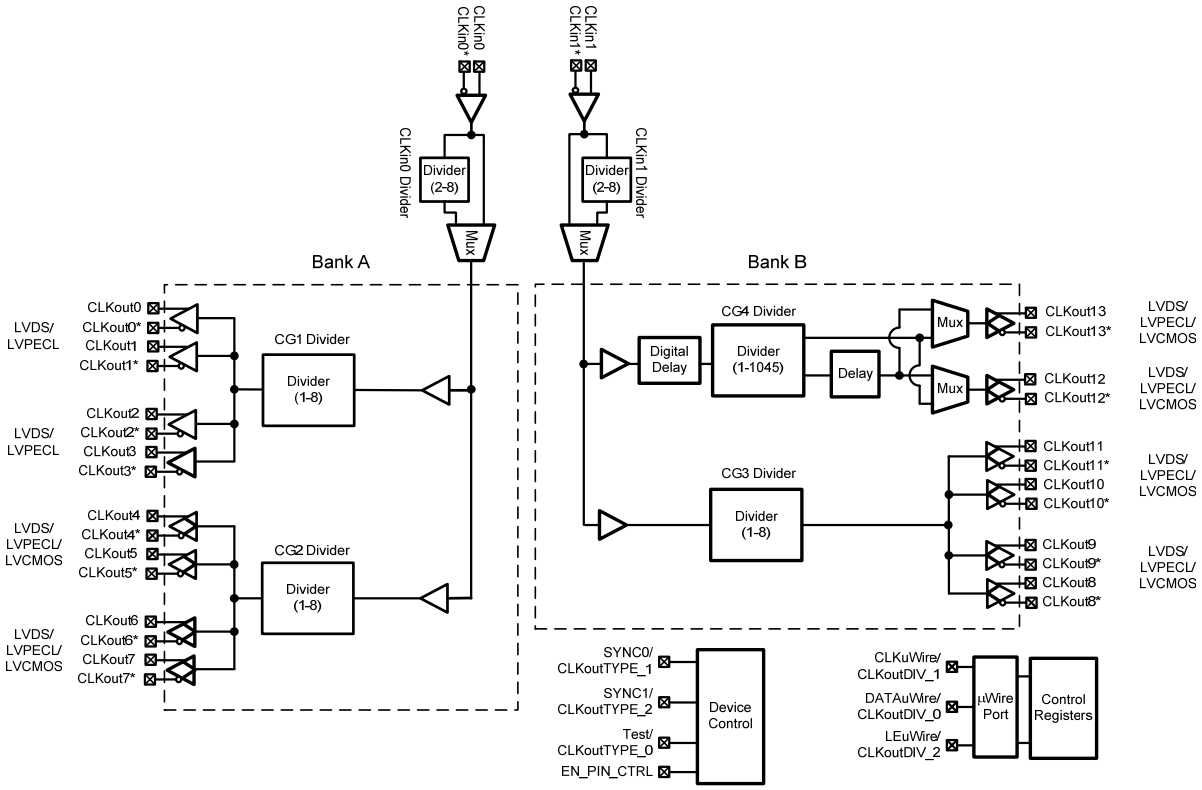


Figure 1 - LMK01801 Block Diagram

Evaluation Board Kit Contents

The evaluation board kit contains…

- An LMK01801 Evaluation board.
- LMK01801 Family quick start guide.
    - Evaluation board instructions are downloadable from the product folder on Texas Instument's website, www.ti.com/.
- CodeLoader uWire cable (LPT --> uWire).
- A USB interface board can be purchased separately under NSID USB2UWIRE_IFACE.

The *CodeLoader* software will run on a Windows 2000 or Windows XP PC. The *CodeLoader* software is used to program the internal registers of the LMK01801 device through a MICROWIRE™ interface.

Clock output configuration:

Clock	Output Type	Output Connector Installed
0	LVPECL	Yes
1	LVPECL	No
2	LVPECL	Yes
3	LVPECL	No
4	LVPECL	Yes
5	LVPECL	No
6	LVPECL	Yes
7	LVPECL	No
8	LVPECL	Yes
9	LVPECL	Yes
10	LVPECL	Yes
11	LVPECL	Yes
12	LVPECL	Yes
13	LVPECL	Yes

Quick Start – Code Loader Mode

1. Connect a voltage of 3.3 volts to either the Vcc SMA connector or the alternate terminal block.
2. Connect a reference clock from a signal generator or other source. Exact frequency depends on programming.
3. Connect the uWire header to a computer parallel port with the CodeLoader cable. A USB communication option is available, search at www.ti.com/ for: USB2UWIRE-IFACE.
4. Install jumpers on TYPE0, TYPE1, TYPE2, DivVal0, DivVal1, DivVal2 in the middle 'uWire' (pins 3,5) position but NOT on EN_PIN_CTRL.
5. Program the device with CodeLoader. Ctrl-L must be pressed at least once to load all registers once after CodeLoader is started or after restoring a Mode. CodeLoader is available for download at www.ti.com/tool/codeloader.
6. Measurements may be made at any clock output if enabled by programming.

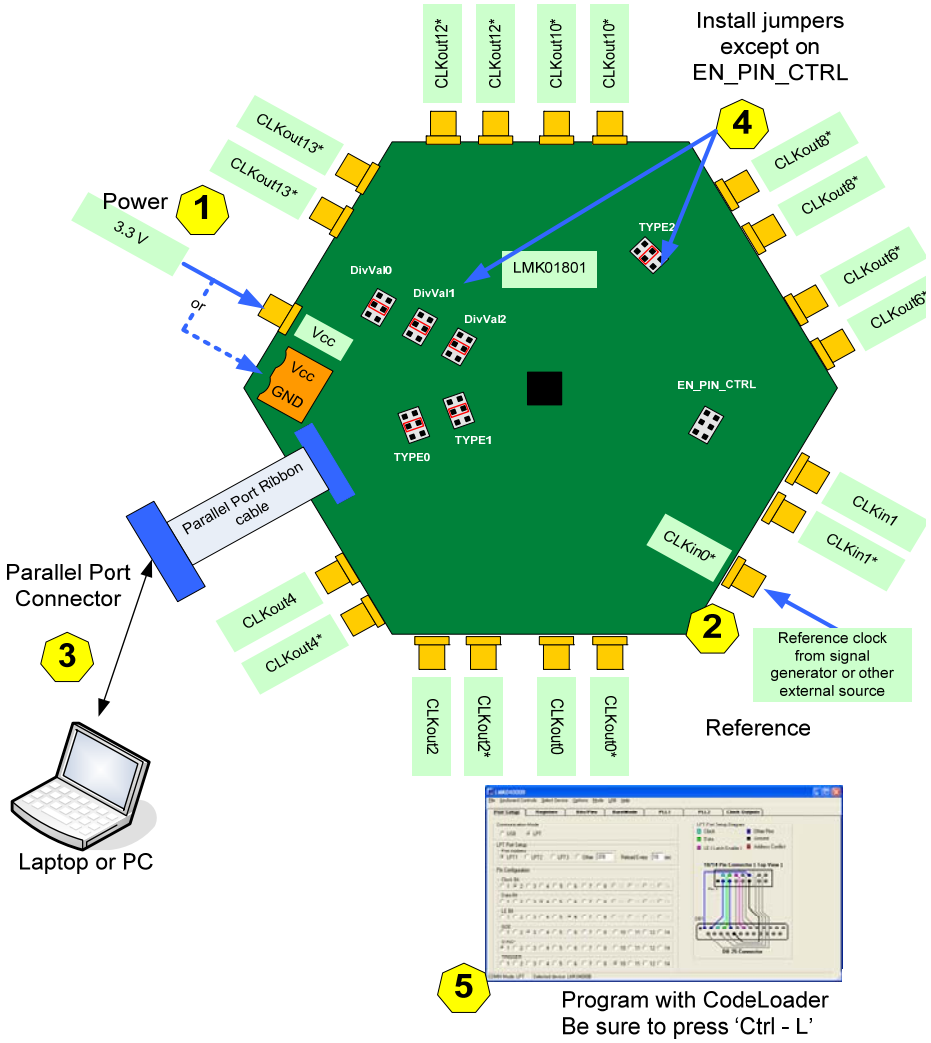


Figure 2 - Quick Start Diagram

Quick Start – Pin Control Mode

1. Connect a voltage of 3.3 volts to either the Vcc SMA connector or the alternate connector.
2. Connect a reference clock from a signal generator or other source. Exact frequency depends on programming.
3. Install a jumper on EN_PIN_CTRL header in either the High or Low position.
4. Install other jumpers on Type0, Type1, Type2, DivVal0, DivVal1, and DivVal2 headers based on the configurations shown in Table 1 and Table 2.

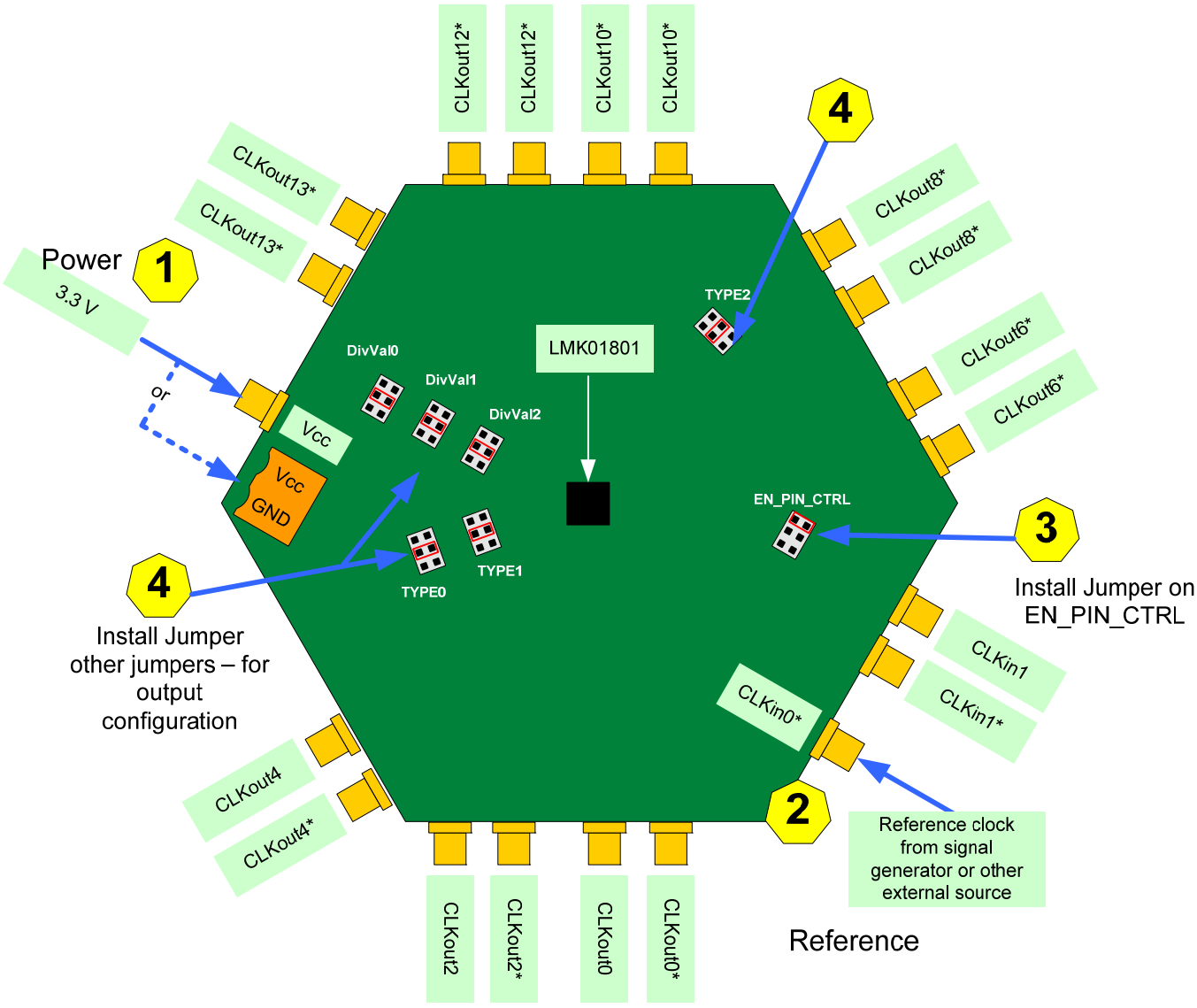


Figure 3 - Pin Control Mode Quick Start Diagram

Pin Control Modes

For the following tables, Low is defined as installing a jumper between pins 5 and 6 on the desired header. A HIGH is defined as installing a jumper between pins 1 and 2 on the desired header.

If EN_PIN_CTRL = LOW (jumper installed between header positions 5 and 6) then the following table describes possible output configurations:

Header	Output Groups	Header = Low	Header = Middle	Header = High
Type0	CLKout0 – CLKout3	LVDS	Powerdown	LVPECL
Type1	CLKout4 – CLKout7	LVDS	LVCMOS (Norm/Inv)	LVPECL
Type2	CLKout8 – CLKout13	LVDS	LVCMOS (Norm/Inv)	LVPECL
DivVal0	CLKout0-3 Divider	÷1	÷4	÷2
DivVal1	CLKout4-7 Divider	÷1	÷4	÷2
DivVal2	CLKout8-11 Divider	÷1	÷4	÷2
	CLKout12-13 Divider	÷8	÷512	÷16

Table 1 - EN_PIN_CTRL = LOW Configuration

If EN_PIN_CTRL = HIGH (jumper installed between header positions 1 and 2) then the following table describes possible output configurations:

Header	Output Groups	Header = Low	Header = Middle	Header = High
Type0	CLKout0 – CLKout3	LVDS	LVPECL	LVPECL
	CLKout4 – CLKout7		LVCMOS (Norm/Inv)	
Type1	CLKout8 – CLKout11	LVDS	LVCMOS (Norm/Inv)	LVPECL
Type2	CLKout12-13	LVDS	LVCMOS (Norm/Inv)	LVPECL
DivVal0	CLKout0-7 Divider	÷1	÷4	÷2
DivVal1	CLKout8-11 Divider	÷1	÷4	÷2
DivVal2	CLKout12-13 Divider	÷4	÷512	÷16

Table 2 - EN_PIN_CTRL = HIGH Configuration

Using CodeLoader to Program the LMK01801

The purpose of this section is to walk the user through using CodeLoader to make some measurements with the LMK01801 device. For more information on CodeLoader refer to Appendix A: CodeLoader Usage or the CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader/.

Before proceeding, be sure to follow the Quick Start section above to ensure proper connections.

1. Start CodeLoader 4 Application

Click "Start" → "Programs" → "CodeLoader 4" → "CodeLoader 4"

The CodeLoader 4 program is installed by default to the CodeLoader 4 application group.

2. Select Device

Click "Select Device" → "Clock Conditioners" → "LMK01801A1"

Once started CodeLoader 4 will load the last used device. To load a new device click "Select Device" from the menu bar, then select the subgroup and finally device to load. For this example, the LMK01800A1 is chosen.
Selecting the device does cause the device to be programmed. However, it is advisable to do CTRL-L to ensure programming.

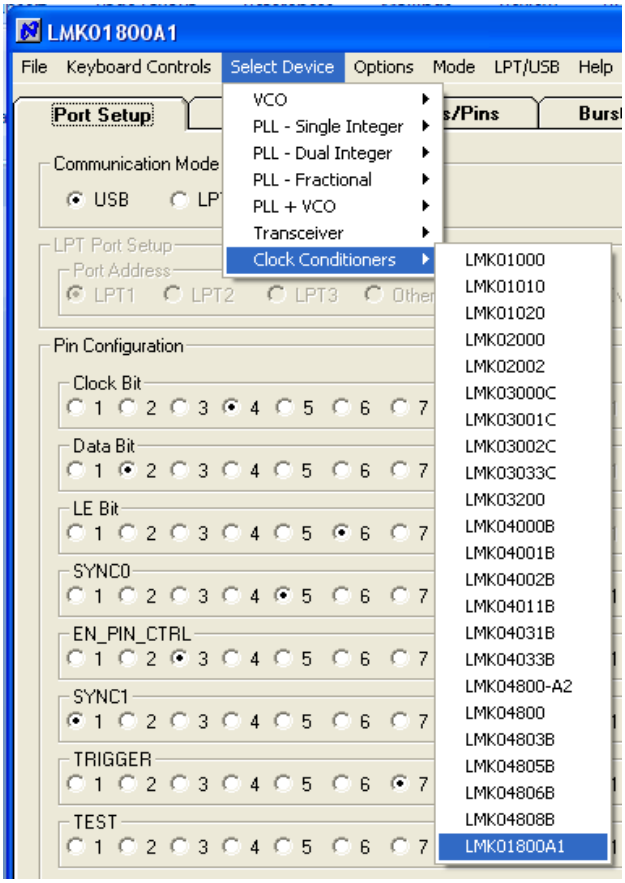


Figure 4 – Selecting the LMK01801

3. Program/Load Device

Press “Ctrl – L”

Assuming the Port Settings are correct, it is now possible to click “Keyboard Controls” → “Load Device” from the menu to program the device to the current state of the newly loaded LMK01801 file. Ctrl-L is the accelerator assigned to the Load Device option and is very convenient.

Figure 5 - Loading the Device

Once the device has been loaded, by default CodeLoader will automatically program changed registers, so it is not necessary to load the device again completely. It is possible to disable this functionality by ensuring there is no checkmark by the “Options” → “AutoReload with Changes.”

Since a default mode will be restored in the next step, this step isn’t really needed but included to emphasize the importance of pressing “Ctrl-L” to load the device at least once after starting CodeLoader, restoring a mode, or restoring a saved setup using the File menu.

See Appendix A: CodeLoader Usage or the CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader for more information on port setup. Appendix H: Troubleshooting Information contains information on troubleshooting communications.

4. Restoring a Default Mode

Click “Mode” → “122.88 MHz VCXO Default”; then
Press “Ctrl – L”

Figure 6 – Setting the 122.88 MHz VCXO Default mode

For the purposes of this walkthrough a default mode will be loaded to ensure a common starting point. This is important because when CodeLoader is closed, it remembers the last settings used for a particular device. By loading the default mode a common starting point is ensured.

Loading a mode does not automatically program the device so it is necessary to press “Ctrl – L” again to program the device.

5. Enable Clock Outputs

To measure phase noise at the clock outputs,

1. Click on the “Bank A” tab,
2. Enable an output,
3. Then set the
    a. CLKout Type,
    b. divide value

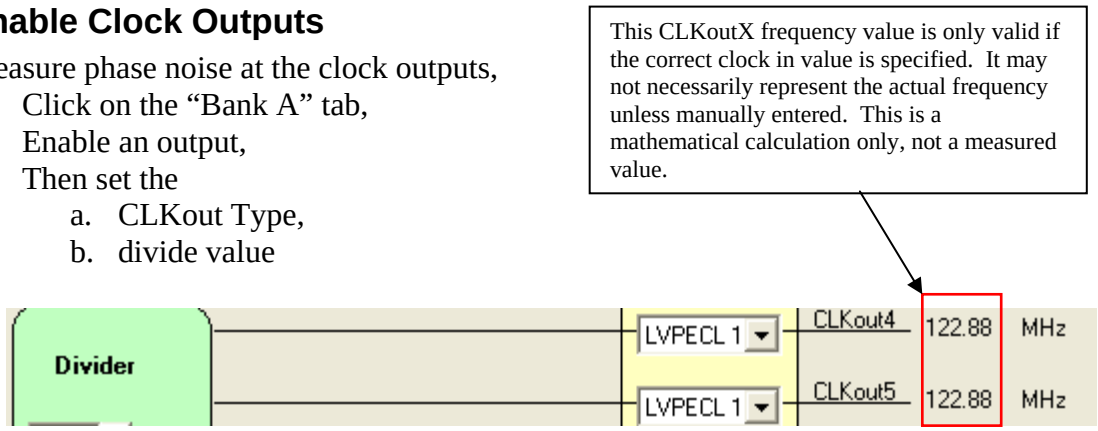
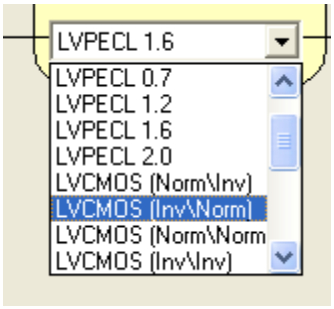


Figure 7 - Setting Divide, CLKout_TYPE, Enabled for CLKout1 on "Clock Outputs" tab.

4. Connect the clock output SMAs to a spectrum analyzer or signal source analyzer.
    a. For LVDS, a balun is recommended such as the ADT2-1T (for frequency range of 0.4 MHz to 450 MHz).
    b. For LVPECL,
        i. A balun can be used, or
        ii. One side of the LVPECL signal can be terminated with a 50 ohm load and the other side can be run to the test equipment single ended.
    c. For LVCMOS,
        i. One side of the LVCMOS signal can be terminated with a 50 ohm load and the other side can be run to the test equipment single ended.
5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.



See Appendix B: Typical Phase Noise Performance Plots for phase noise plots of the clock outputs.

Evaluation Board Inputs/Outputs

The following table contains descriptions of the various inputs and outputs for the evaluation board.

Table 3. LMK01801 Evaluation Board I/O

Connector Name	Input/Output	Description
CLKout0 / CLKout0*, CLKout2 / CLKout2*, CLKout4 / CLKout4*, CLKout6 / CLKout6*, CLKout8 / CLKout8*, CLKout9/ CLKout9*, CLKout10 / CLKout10*, CLKout11/ CLKout11*, CLKout12 / CLKout12*, CLKout13 / CLKout13*	Output	Populated connectors. Differential clock output pairs. All outputs are configured in LVPECL mode. On the evaluation board, all clock outputs are AC-coupled to allow safe testing with RF test equipment. • All LVPECL/2VPECL clock outputs are terminated to GND with a 240 ohm resistor, one on each output pin of the pair.
Vcc	Input	Populated connector. DC power supply for the PCB. Removing R1, R2, or R3 allow for splitting the power to various devices on the board. Note: The LMK01801 Family contains internal voltage regulators for the VCO, PLL and related circuitry. The clock outputs do not have an internal regulator. A clean power supply is required for best performance.
Vcc2	Input	Unpopulated connector. Vcc input to power the output planes separately from the Aux Plane. Refer to schematics for more information.

Connector Name	Input/Output	Description
CLKin0/CLKin0*, CLKin1/CLKin1*	Input	Populated connectors. The default board configuration is setup for a single-ended reference source at CLKin0* (CLKin0 pin is AC-coupled to ground). If a DC-coupled clock is used to drive either of the inputs, the high voltage level must be at least 2 volts and the low voltage no greater than 0.4 volts.
uWire	Input/Output	Populated connector. 10-pin header programming interface for the board. Of Most important are the CLKuWire, DATAuWire, and LEuWire programming lines from this header. Each of these signals, TEST, and SYNC0, and SYNC1 can be monitored through test points on the board.
SYNC0, SYNC1	Input	Unpopulated connector. Access to SYNC0 or SYNC1 of device.

Recommended Test Equipment

Power Supply

The Power Supply should be a low noise power supply.

Phase Noise / Spectrum Analyzer

For measuring phase noise an Agilent E5052A Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052A is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Appendix A: CodeLoader Usage

CodeLoader is used to program the evaluation board with either an LPT port using the included CodeLoader cable or with a USB port using the optional USB <--> uWire cable available from http://www.ti.com/. The part number is USB2UWIRE-IFACE.

Port Setup Tab

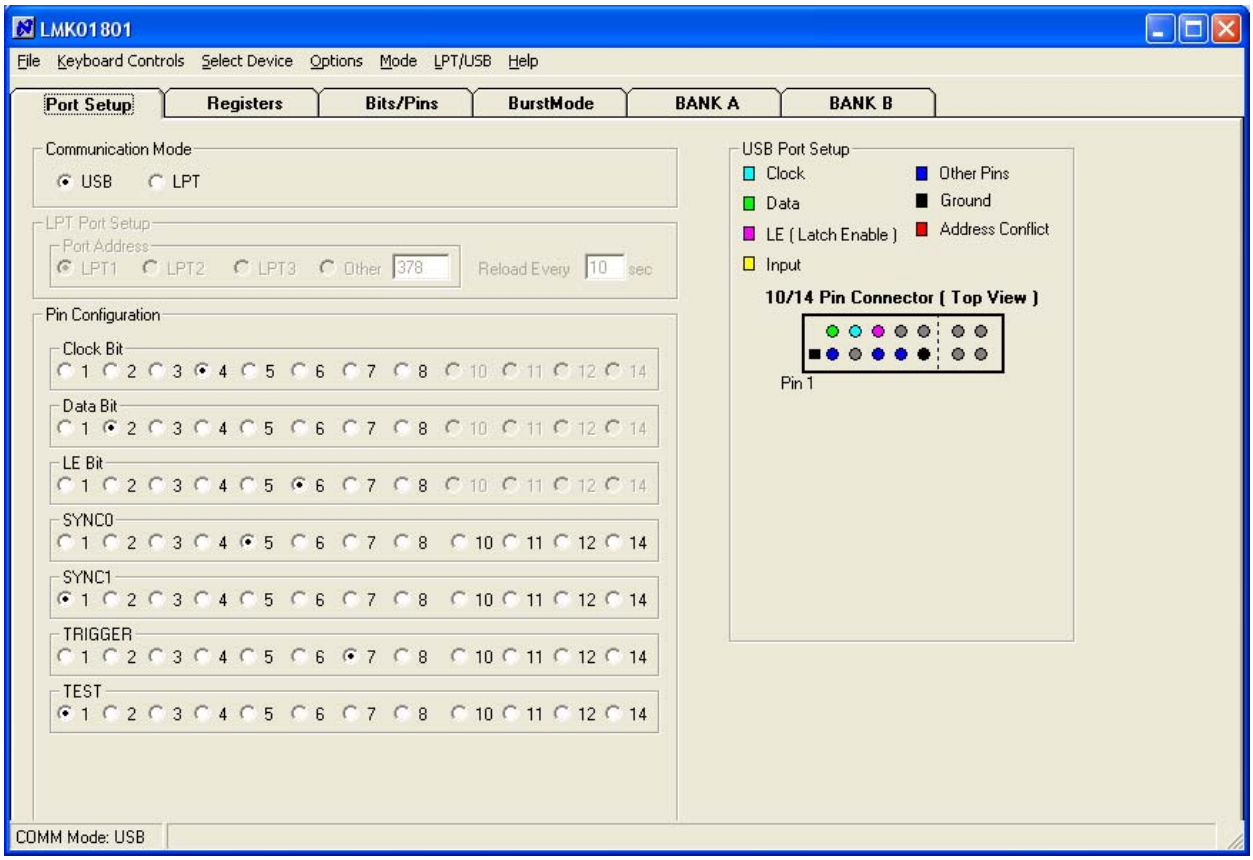


Figure 9 - Port Setup tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered.

The Pin Configuration field is hardware dependent and normally SHOULD NOT be changed by the user. Figure 9 shows the default settings.

Clock Outputs Tab

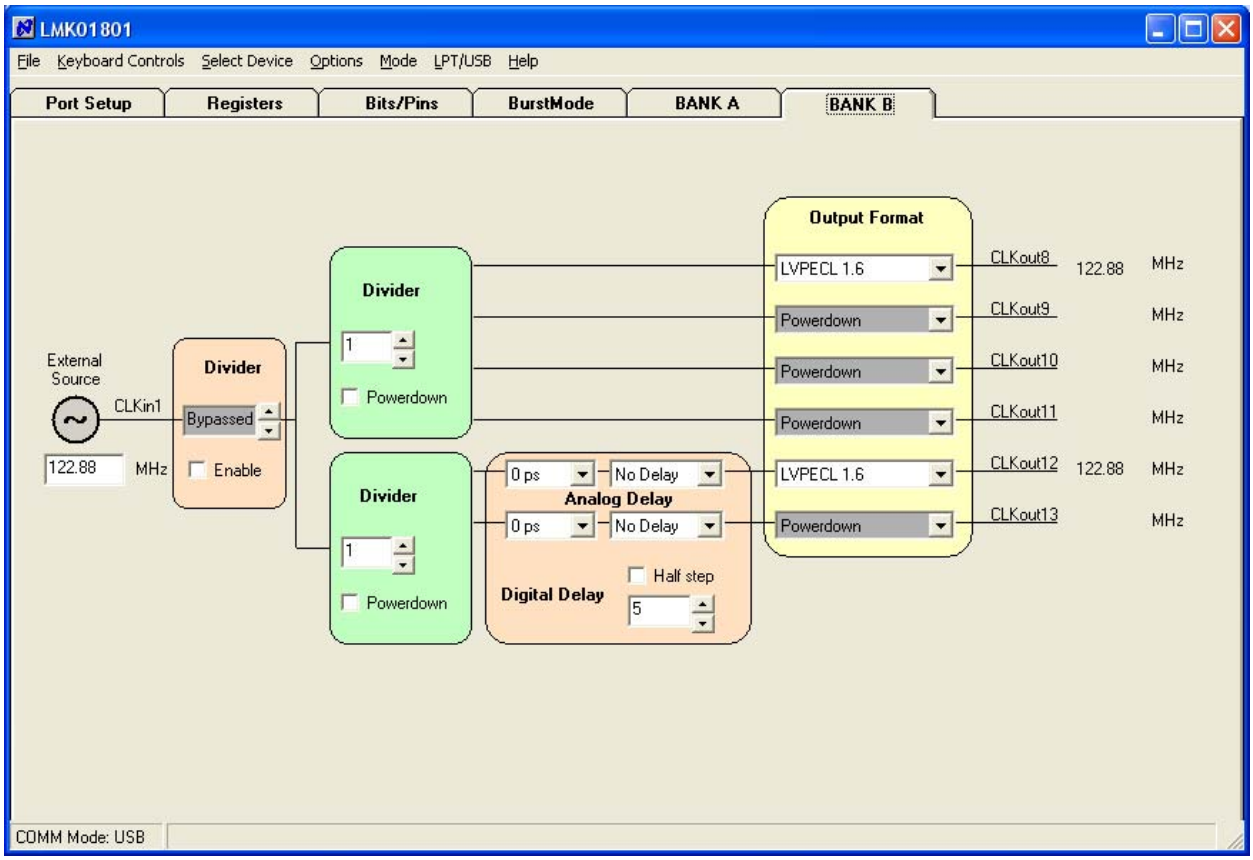


Figure 10 - Clock Outputs tab

The clock outputs tab allows the user to Enable/Disable individual clock outputs, select the clock mode (Bypass/Divided/Delayed/Divided & Delayed – for outputs 12 and 13), set the clock output delay value (if delay is enabled for outputs 12 and 13 only), and the clock output divider value (2, 4, 6, …, 510 for clock outputs 12 and 13 or 1-8 for clock outputs 0 - 11).

Bits/Pins Tab

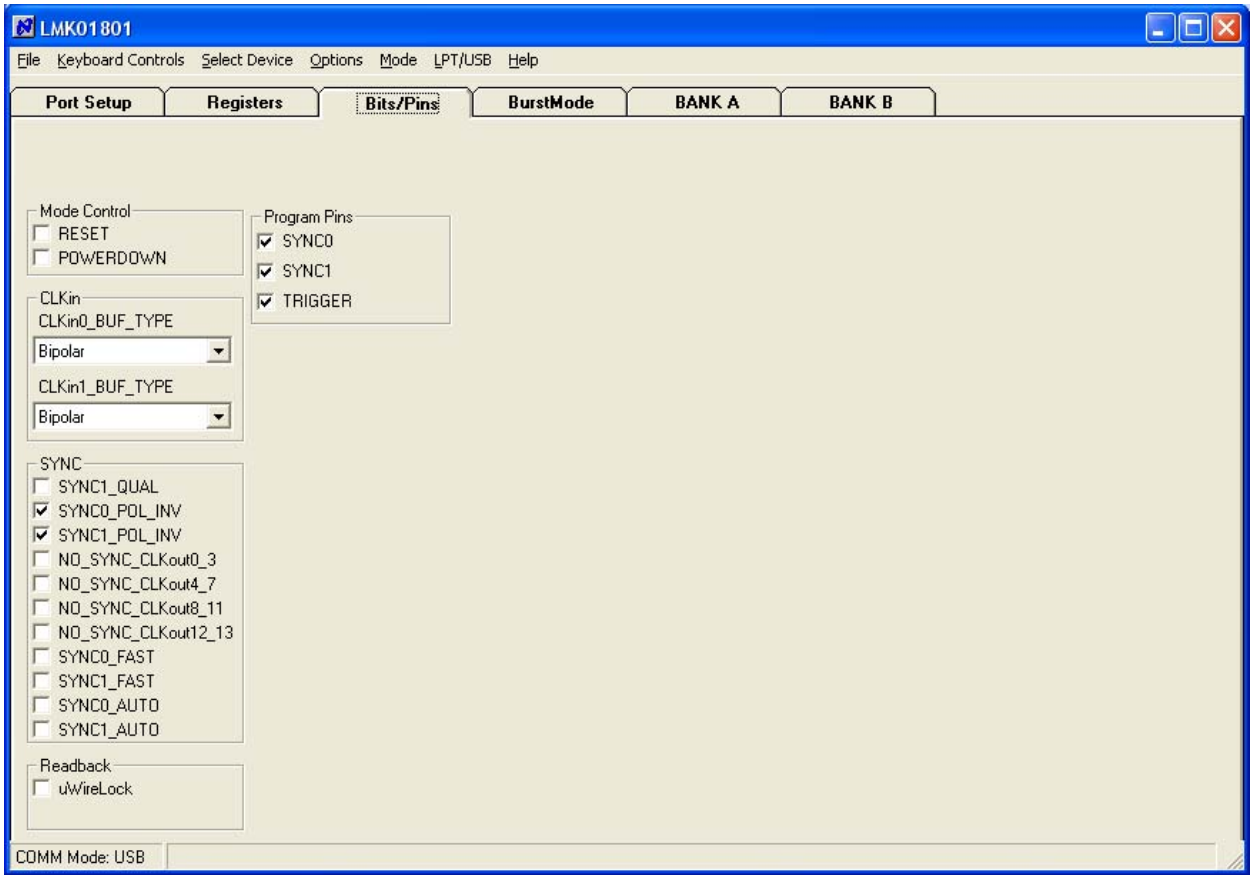


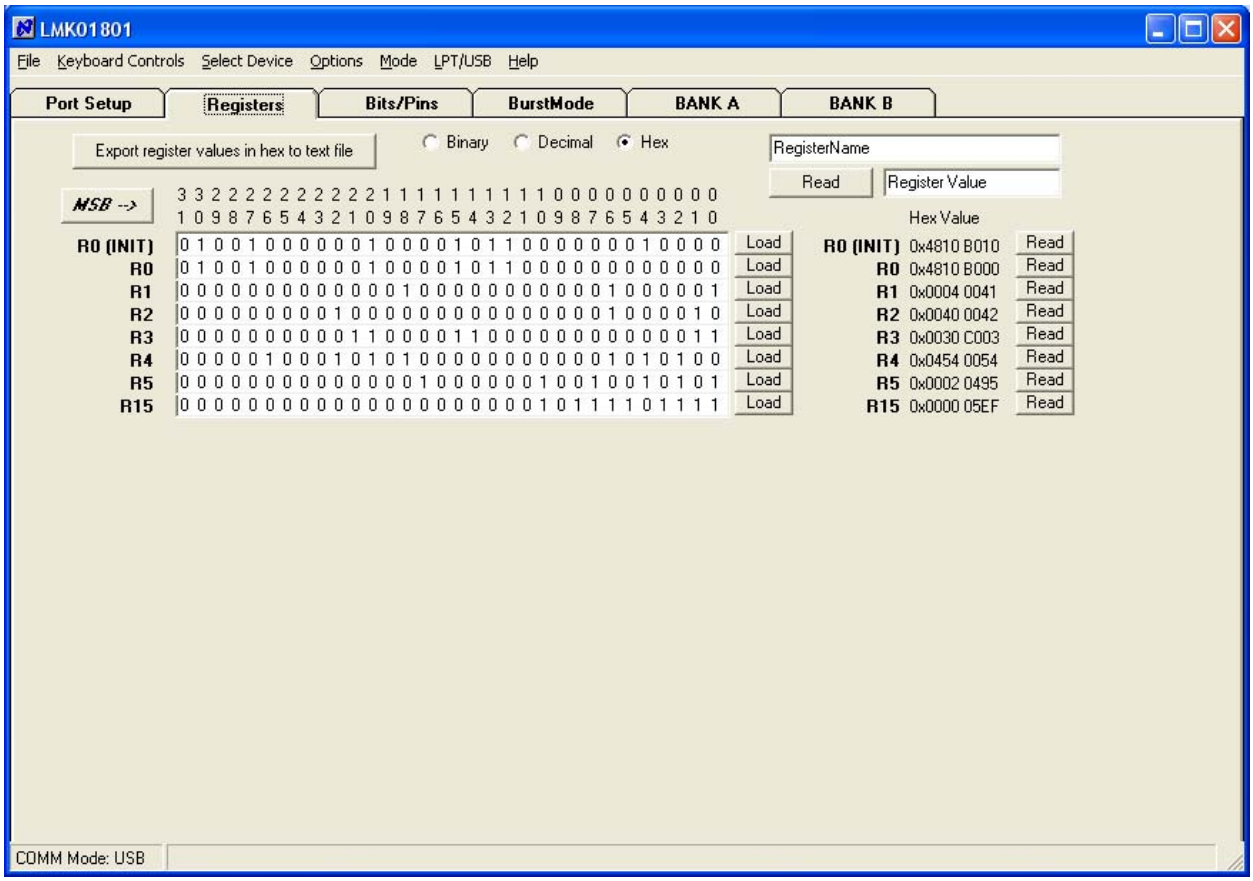
Figure 11 - Bits/Pins tab.

The Bits/Pins tab allows the user to program bits directly. Many of which are not available on other tabs. Refer to the datasheet for more detailed information. The bits available are:

- Common Box
  - RESET - Set the reset bit. This will reset the device. In a normal application it is not necessary to program this bit clear since it is auto-clearing. However in the CodeLoader software, RESET must be clicked again (cleared) to not cause a reset every time R7 is programmed.
  - POWERDOWN - Place the device in powerdown mode.

- Program Pins Box – These pins only have effect if the PWB headers are in the uWire position (3-5). See Figure 2 - Quick Start Diagram for the correct configuration.
  - EN_PIN_CTRL – Sets the control of the output via uWire or pins
  - SYNC0 – Set high or low voltage on SYNC0 pin. Checked is high voltage.
  - TRIGGER – Set high or low voltage on pin 10 of uWire header.

Registers Tab



The registers tab shows the value of each register. This is convenient for programming the device to the desired settings, then recording the hex values for programming in your own application. The “Export register values in hex to text file” button will allow these register values to be saved to a text file.

By clicking in the “bit field” it is possible to manually change the value of registers by typing ‘1’ and ‘0.’

Appendix B: Typical Phase Noise Performance Plots

Clock Outputs

The LMK01801 Family features LVDS, LVPECL, 2VPECL, and LVCMOS types of outputs. Include are the phase noise plots for the following outputs.

Device	CLKoutX	Output Divide	Output Type
LMK01801A1	8	1	LVPECL
LMK01801A1	8	4	LVPECL
LMK01801A1	8	1	2VPECL
LMK01801A1	8	4	2VPECL
LMK01801A1	4	1	LVDS
LMK01801A1	4	4	LVDS
LMK01801A1	4	1	LVCMOS(Norm/Inv)
LMK01801A1	4	4	LVCMOS(Norm/Inv)

Table 4 - Phase Noise Output Test Configuration

Clock Output Measurement Technique

The measurement technique for each output type varies.

LVPECL/2VPECL – Measured by using an Minicircuits ADT2-1T balun on the input and on the output.
LVCMOS and LVDS – Measured by using an Minicircuits ADT2-1T balun on the output and single ended input.

Parameter	Test Case 1	Test Case 2	Test Case 3	Test Case 4
Input Source	Wenzel XTAL	Wenzel XTAL	SMHU	Rohde&Schwarz SMHU
Input Frequency	100 MHz	100 MHz	983.04 MHz	983.04 MHz
Input Power	0 dBm	0 dBm	0 dBm	0 dBm
Output Divider	1	4	1	4
Figure	Figure 12	Figure 13	Figure 14	Figure 15

Table 5 - LMK01801 test conditions

LMK01801 Phase Noise, CLKin = 100 MHz, Output Divider = 1

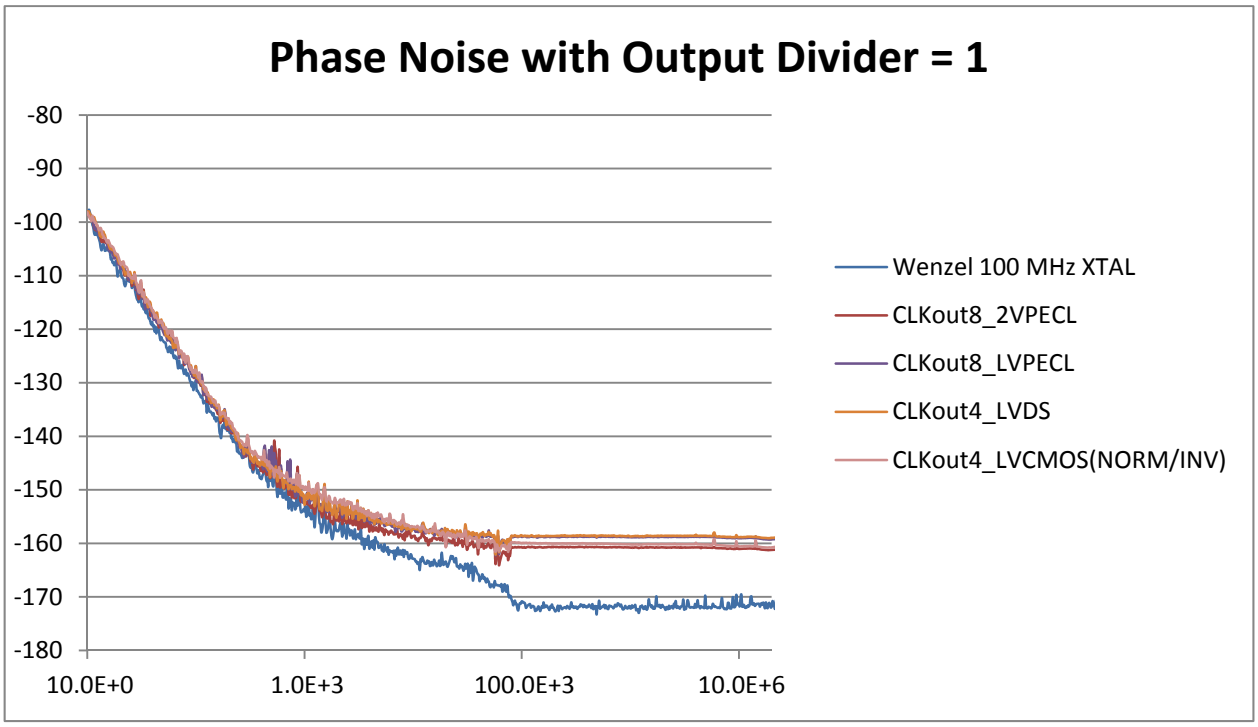


Figure 12 - LMK01801 Phase Noise @ 100 MHz with Output Divider = 1

LMK01801 Phase Noise, CLKin = 100 MHz, Output Divider = 4

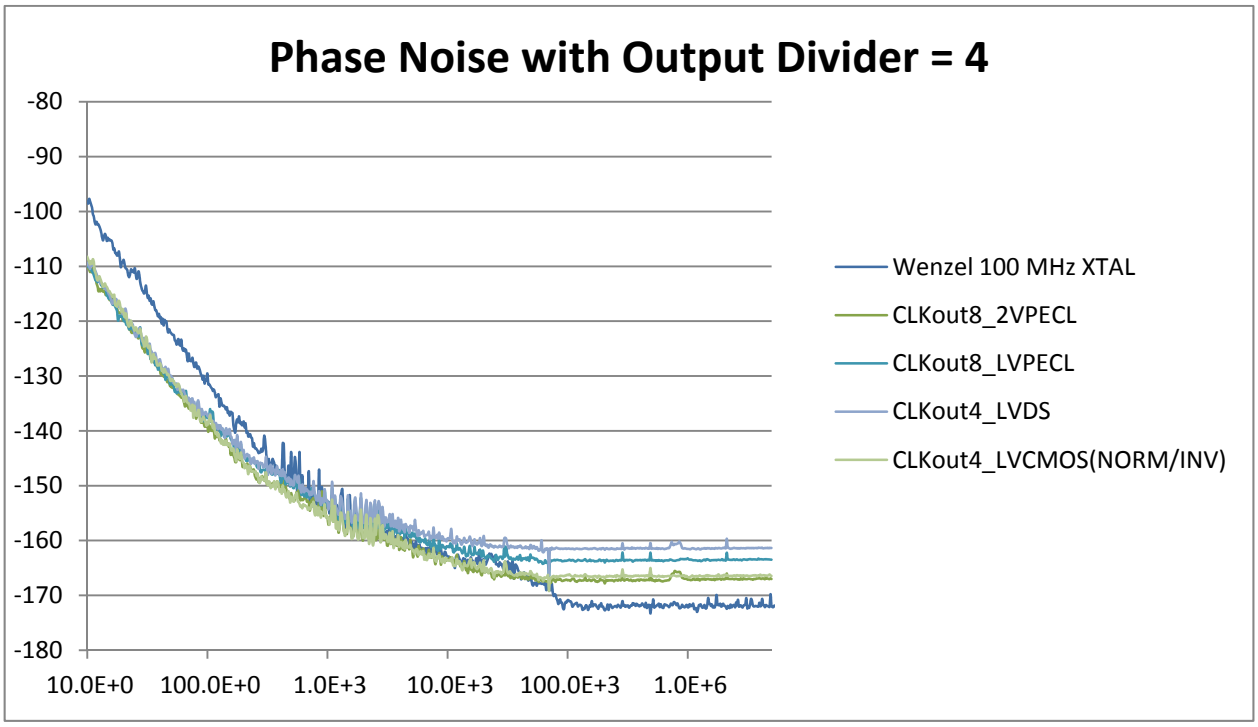


Figure 13 - LMK01801 Phase Noise @ 100 MHz with Output Divider = 4

LMK01801 Phase Noise, CLKin = 983.04 MHz, Output Divider = 1

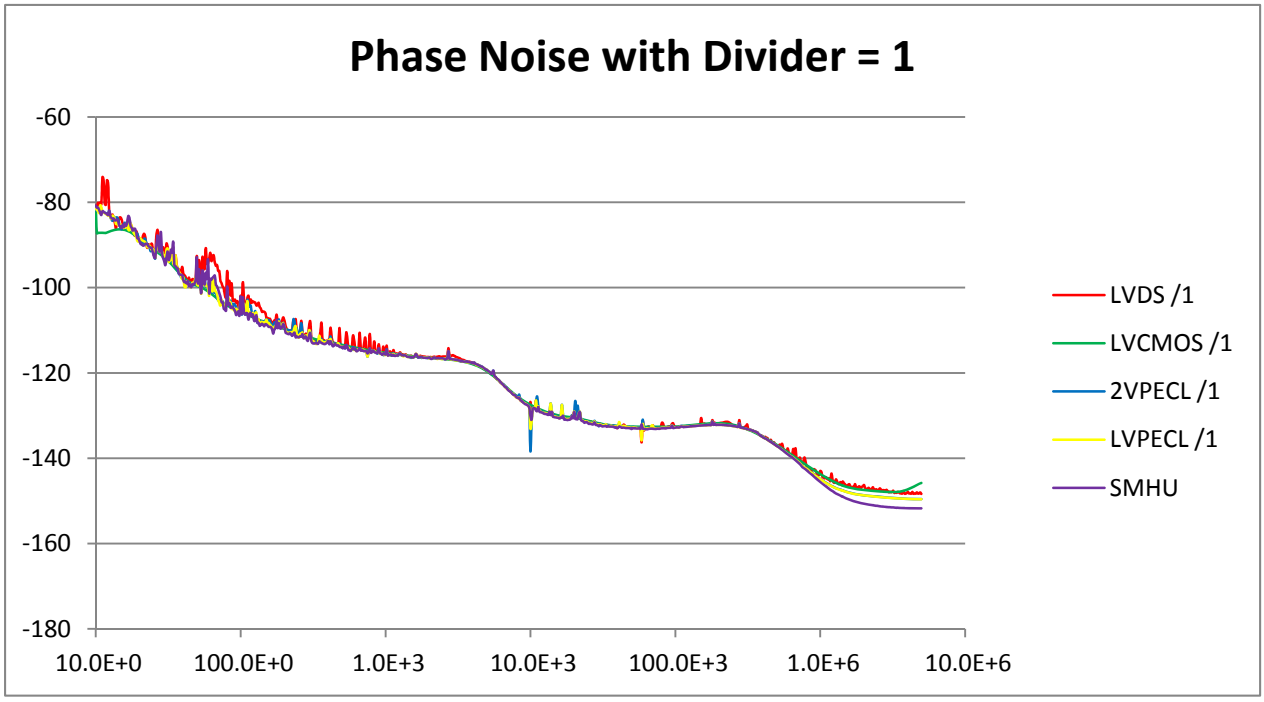


Figure 14 - LMK01801 Phase Noise @ 983.04 MHz with Output Divider = 1

LMK01801 Phase Noise, CLKin = 983.04 MHz, Output Divider = 4

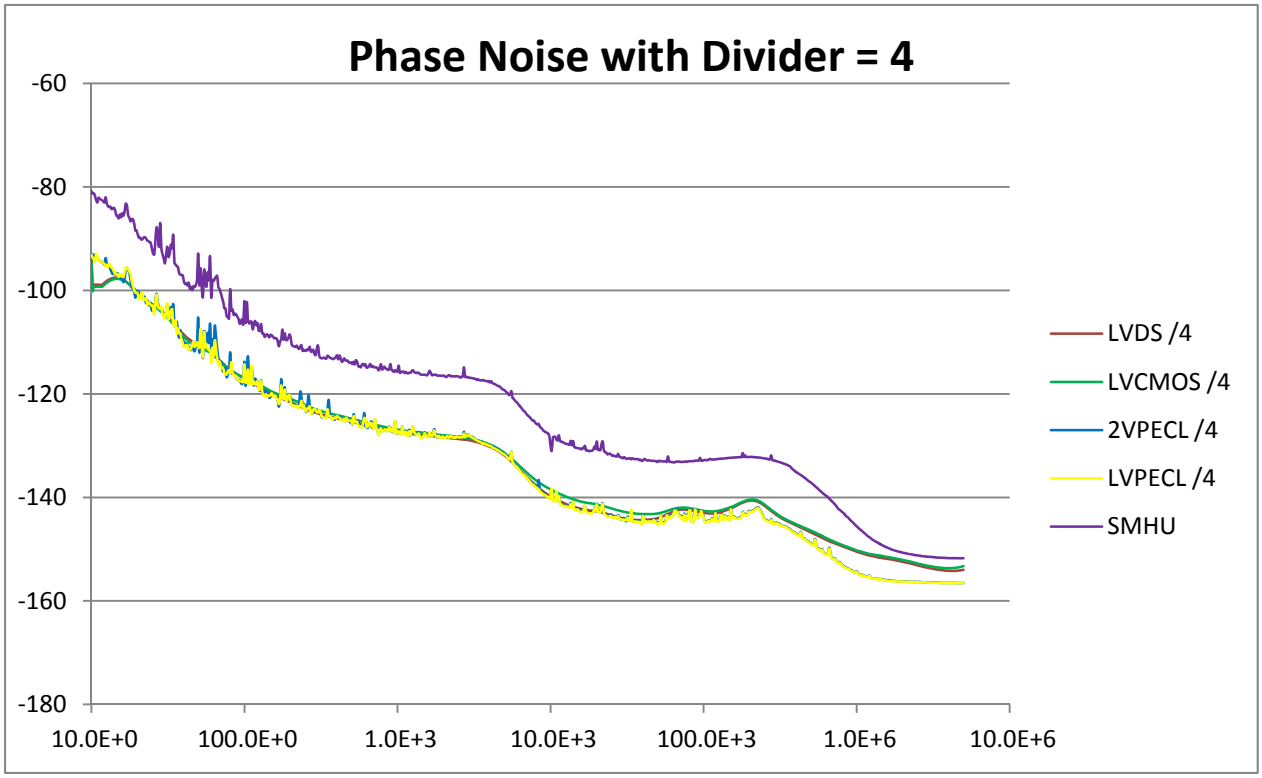


Figure 15 - LMK01801 Phase Noise @ 983.04 MHz with Output Divider = 4

Phase Noise Measurement

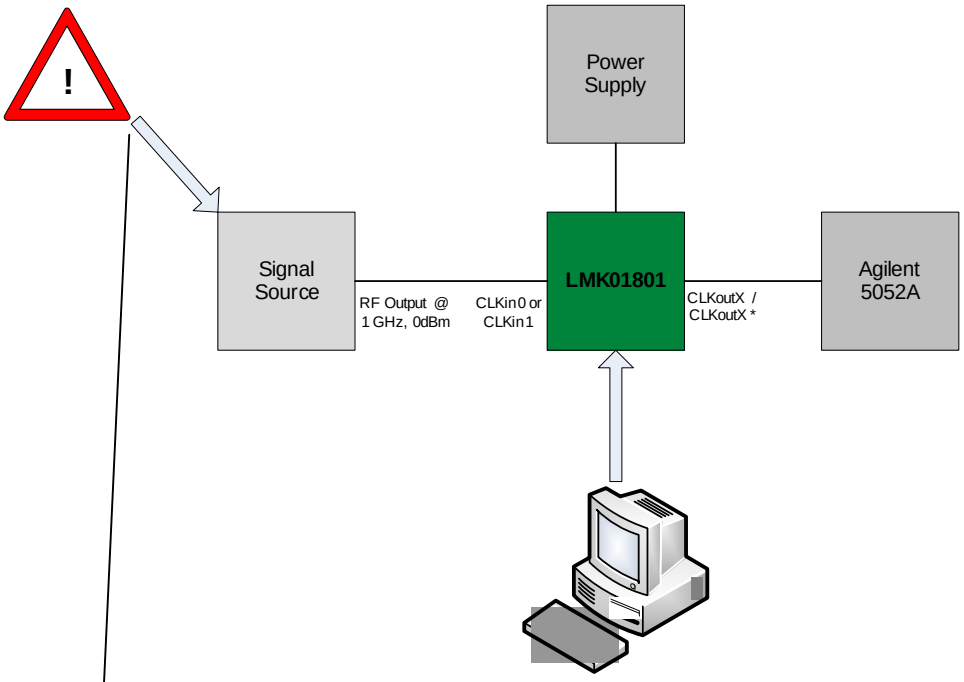


Figure 16 - Phase Noise Measurement Set-Up

The phase noise of the signal source will impact the measured phase noise of the LMK01801.

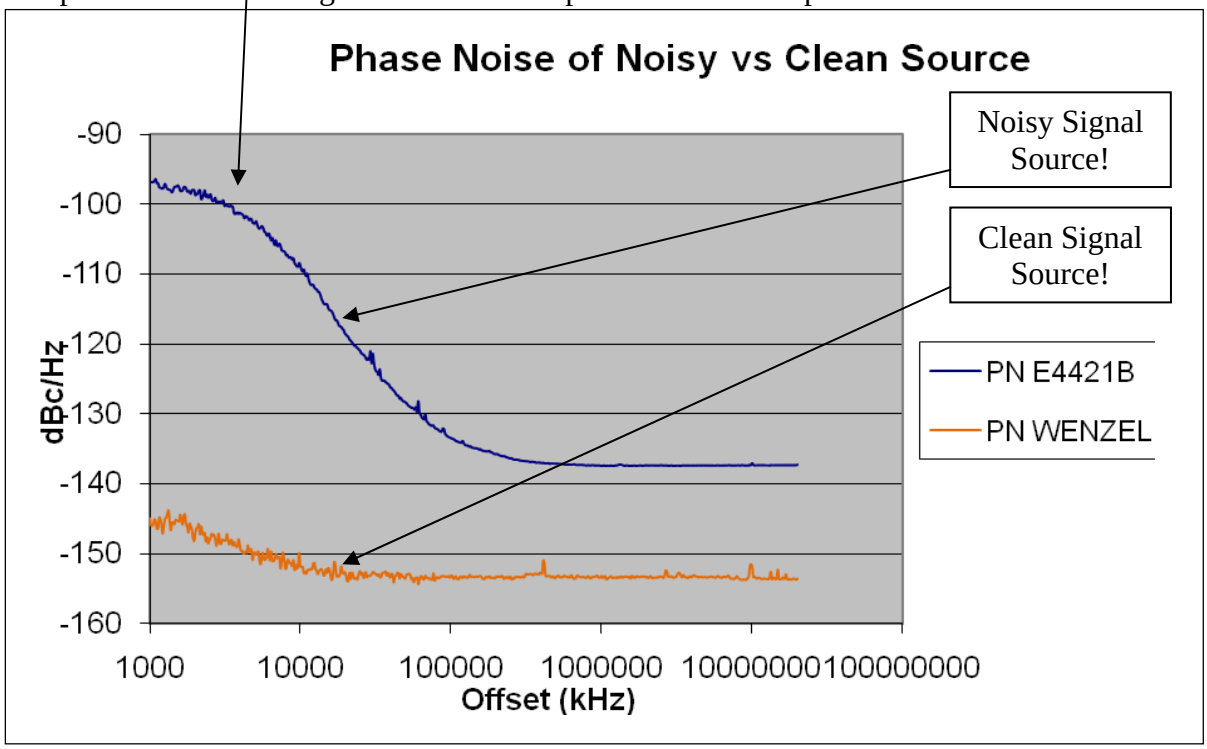


Figure 17 - Noisy vs. Clean Phase Noise

LMK01801 Sample Output Waveforms

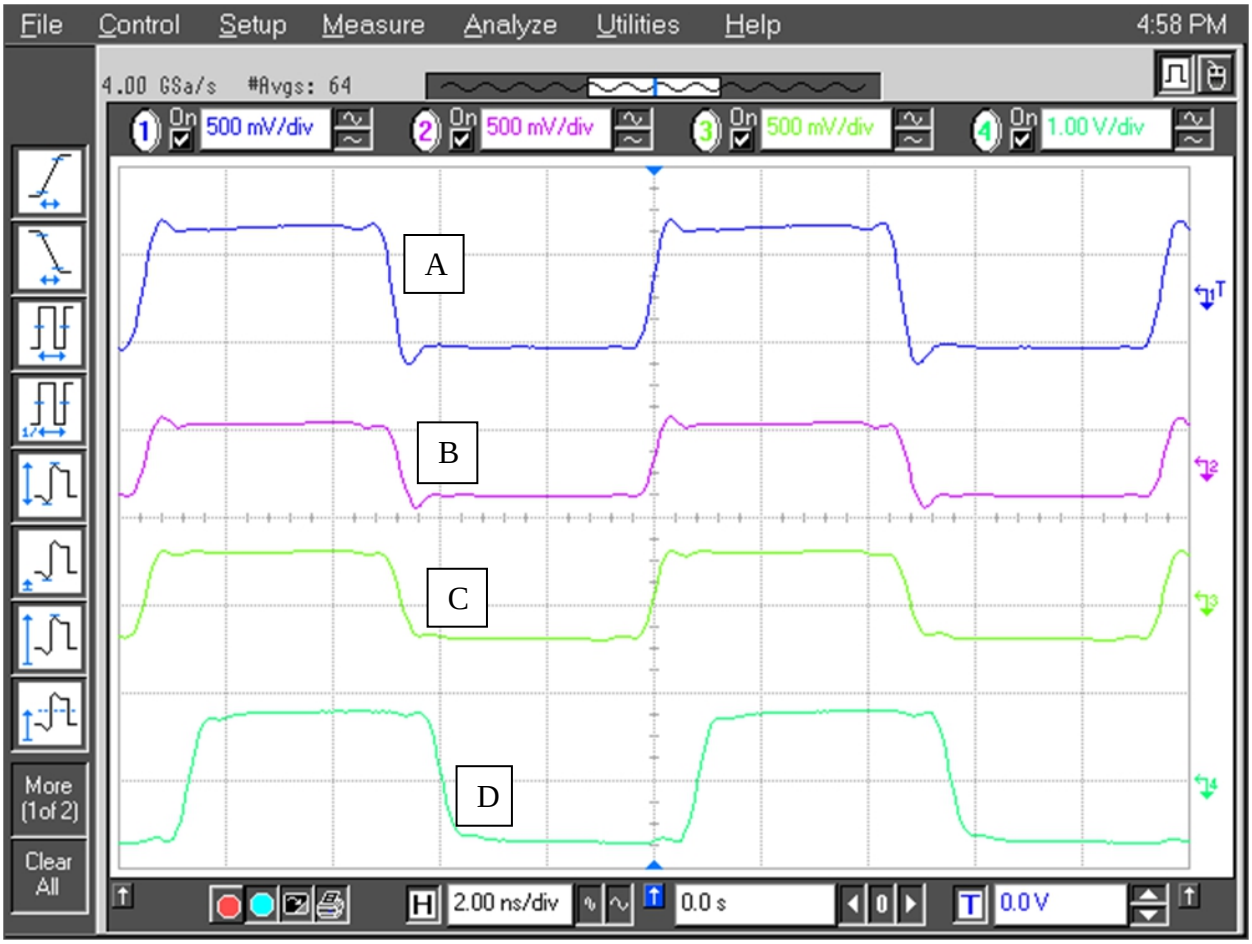


Figure 18 - LMK01801 Sample Clock Output Waveforms

The output waveforms shown in Figure 18 were taken at a clock in frequency of 122.88 MHz, AC coupled. These measurements follow the V_{ID} voltage convention – See Appendix G: Differential Voltage Measurement Terminology for more information.

The output modes are as follows:

Trace	Clock Output	Output Type
A	CLKout0	2VPECL
B	CLKout1	PECL (Low Power)
C	CLKout4	LVDS
D	CLKout5	LVCMOS (Normal/Invert)

LMK01801 Analog Delay Sample Data

The sample analog delay data was taken at a clock in frequency of 122.88 MHz, output format of 2VPECL. Notice in Figure 19 that with analog delay enabled there is approximately 460 ps of delay. Then in Figure 20 we added 100 ps of delay and the resulting delay is approximately 550 ps.

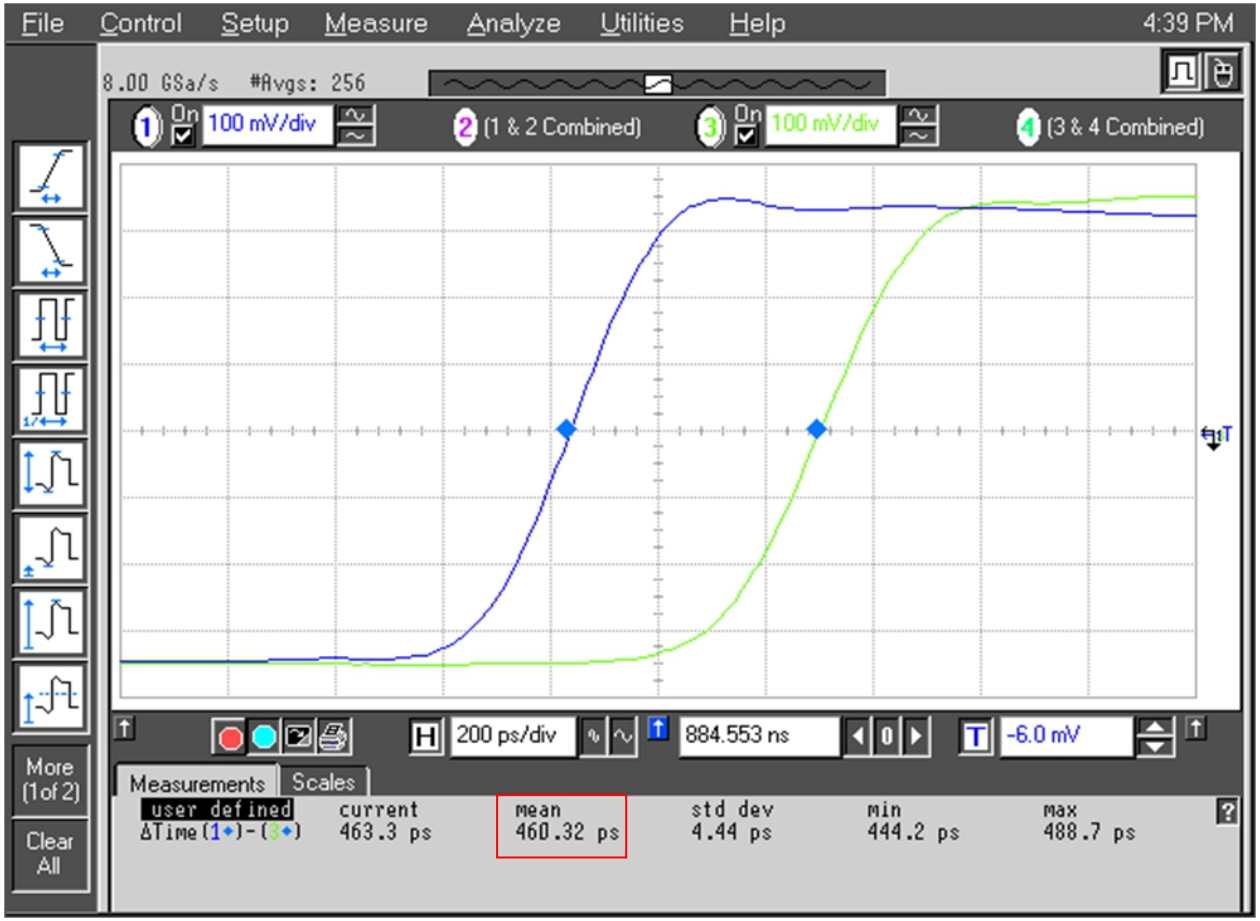


Figure 19 - CLKout12 and CLKout13 No Analog Delay

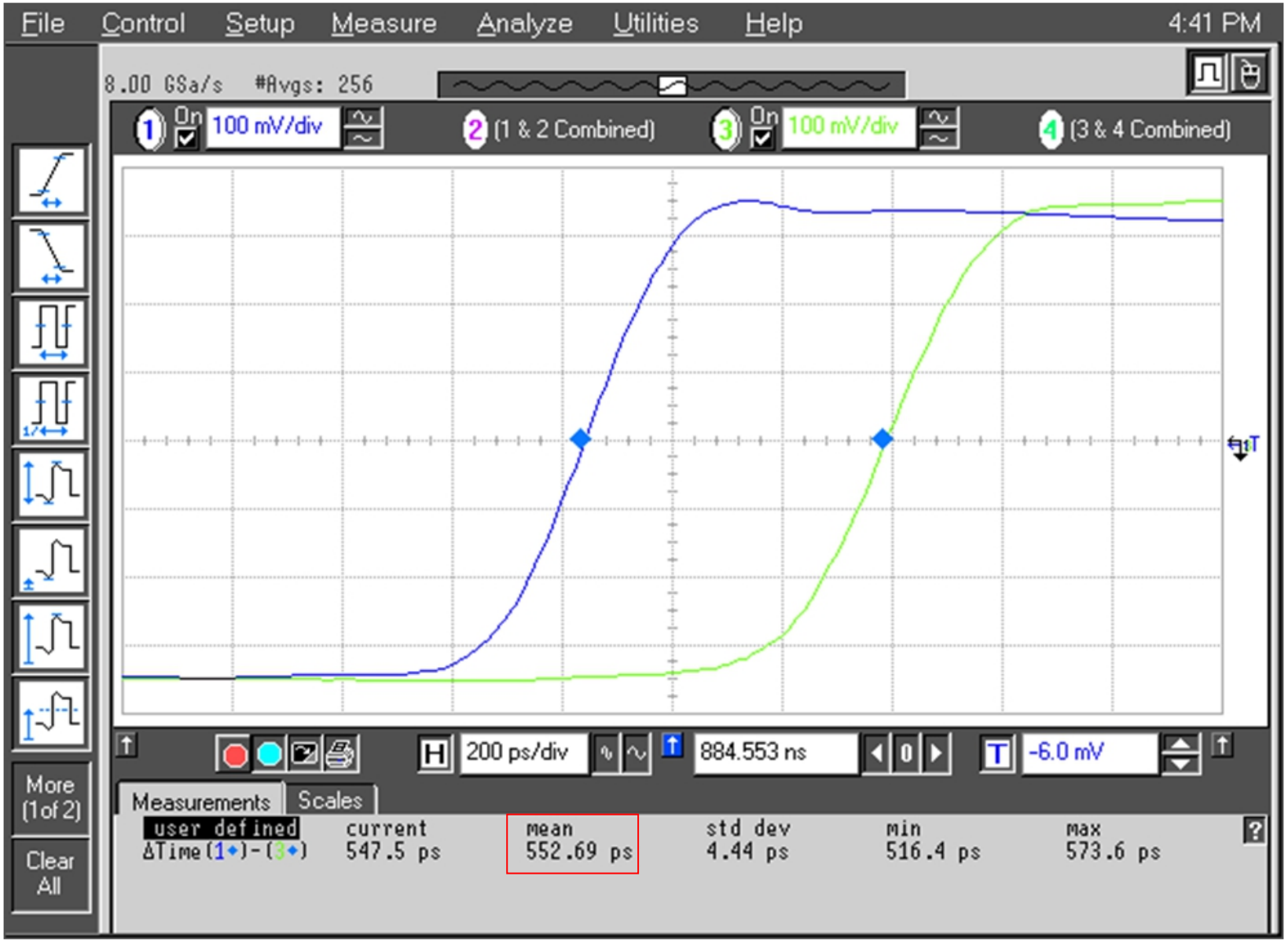
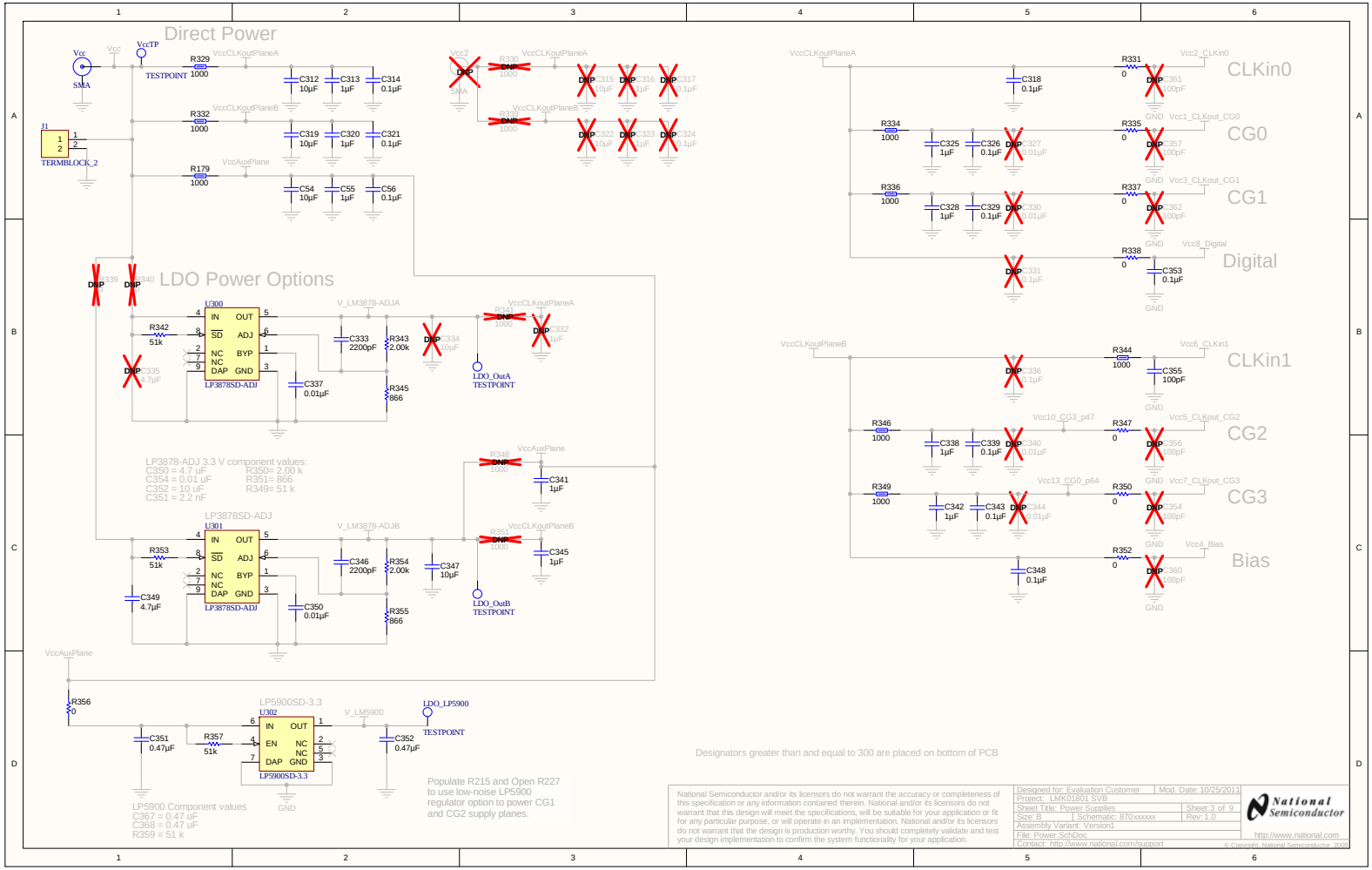


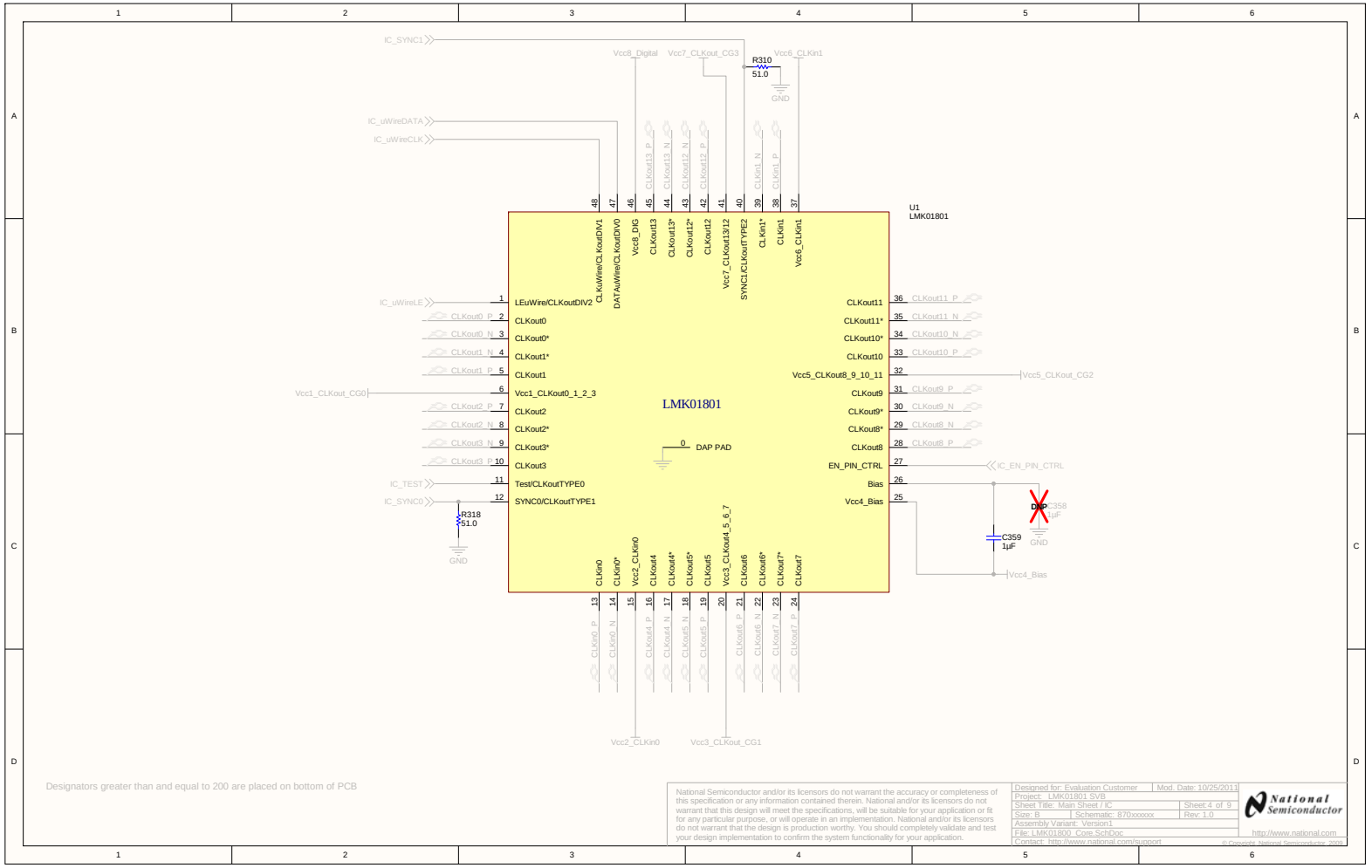
Figure 20 - CLKout12 with 100 pSec of delay relative to CLKout13

Appendix C: Schematics

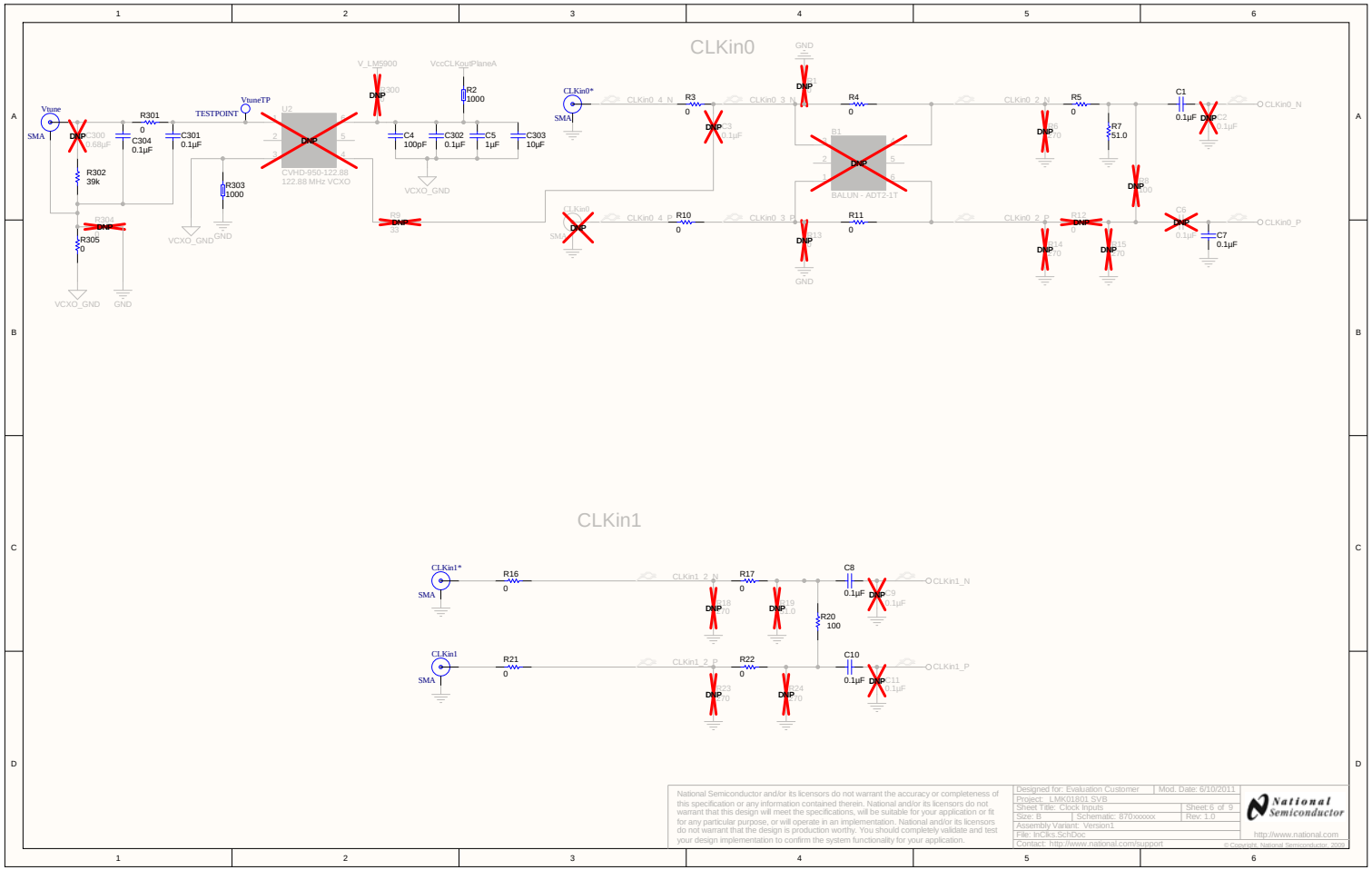
Power



Main


U1
LMK01801
LMK01801
LEuWire/CLKoutDIV2
CLKout0
CLKout0*
CLKout1*
CLKout1
Vcc1_CLKout0_1_2_3
CLKout2
CLKout2*
CLKout3*
CLKout3
Test/CLKoutTYPE0
SYNC0/CLKoutTYPE1
CLKout11
CLKout11*
CLKout10*
CLKout10
Vcc5_CLKout8_9_10_11
CLKout9
CLKout9*
CLKout8*
CLKout8
EN_PIN_CTRL
Bias
Vcc4_Bias
DAP PAD
R310
51.0
R318
51.0
C358
1µF
C359
1µF
Designators greater than and equal to 200 are placed on bottom of PCB

Inputs


CLKin0
CLKin1
Vtune
SMA
TESTPOINT
VtuneTP
CVHD-950-122.88
122.88 MHz VCXO
BALUN - ADT2-1T
VCXO_GND
GND
CLKin0*
CLKin1*
CLKin0_N
CLKin0_P
CLKin1_N
CLKin1_P
DNP
National Semiconductor and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. National and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. National and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
Designed for: Evaluation Customer
Mod. Date: 6/10/2011
Project: LMK01801 SVB
Sheet Title: Clock Inputs
Sheet 6 of 9
Size: B
Schematic: 870xxxxxx
Rev: 1.0
Assembly Variant: Version1
File: InClks.SchDoc
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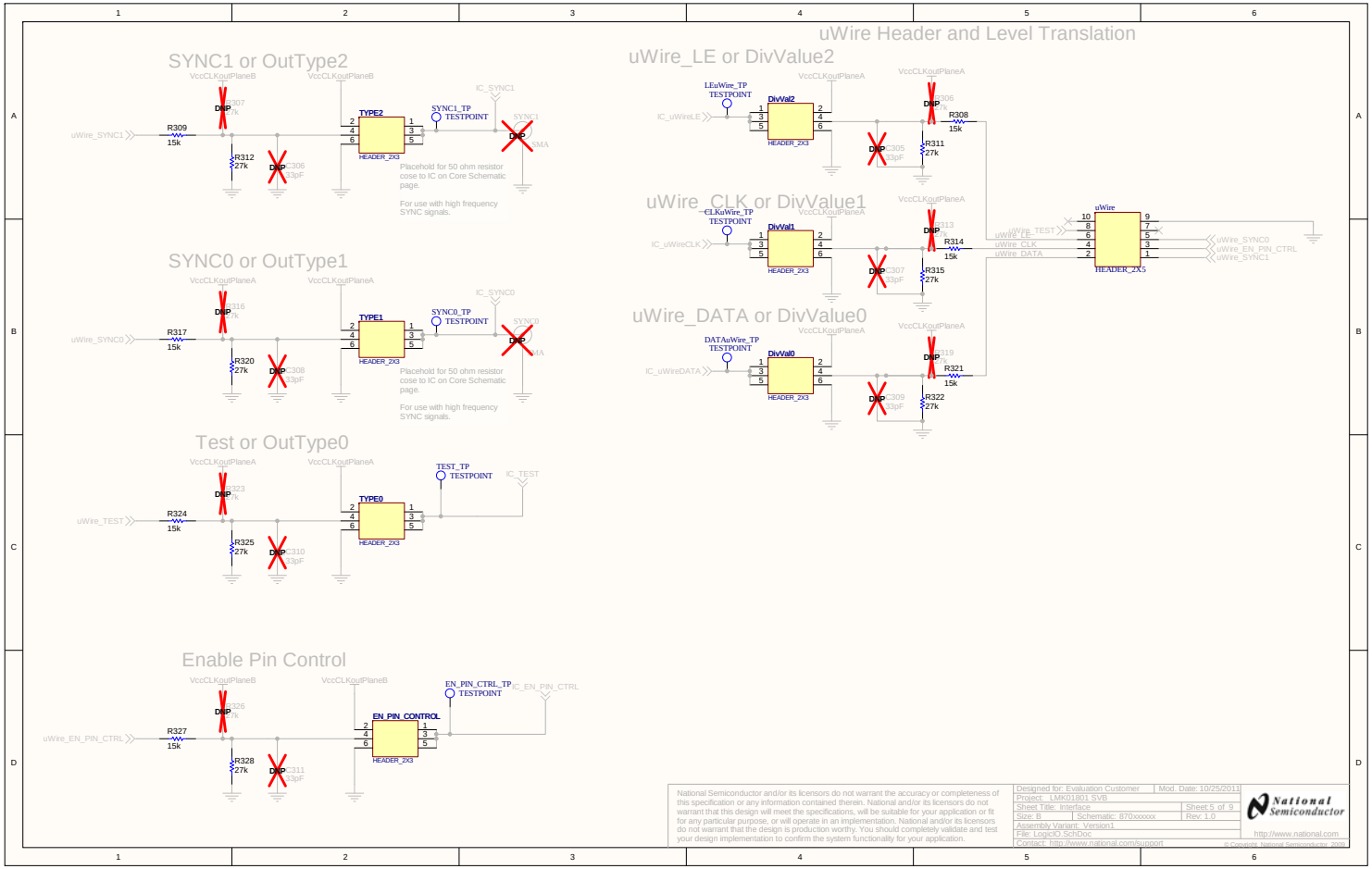
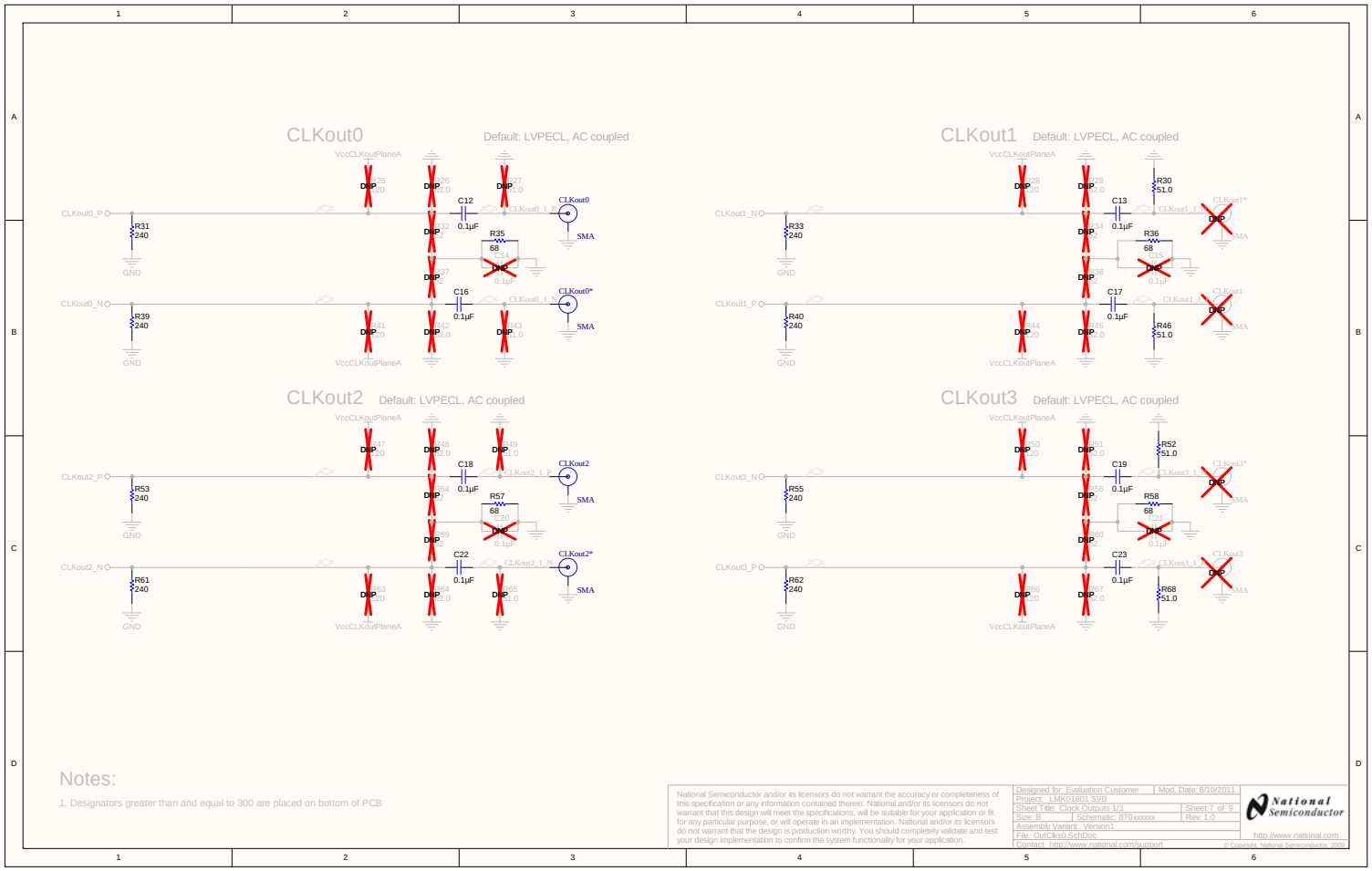
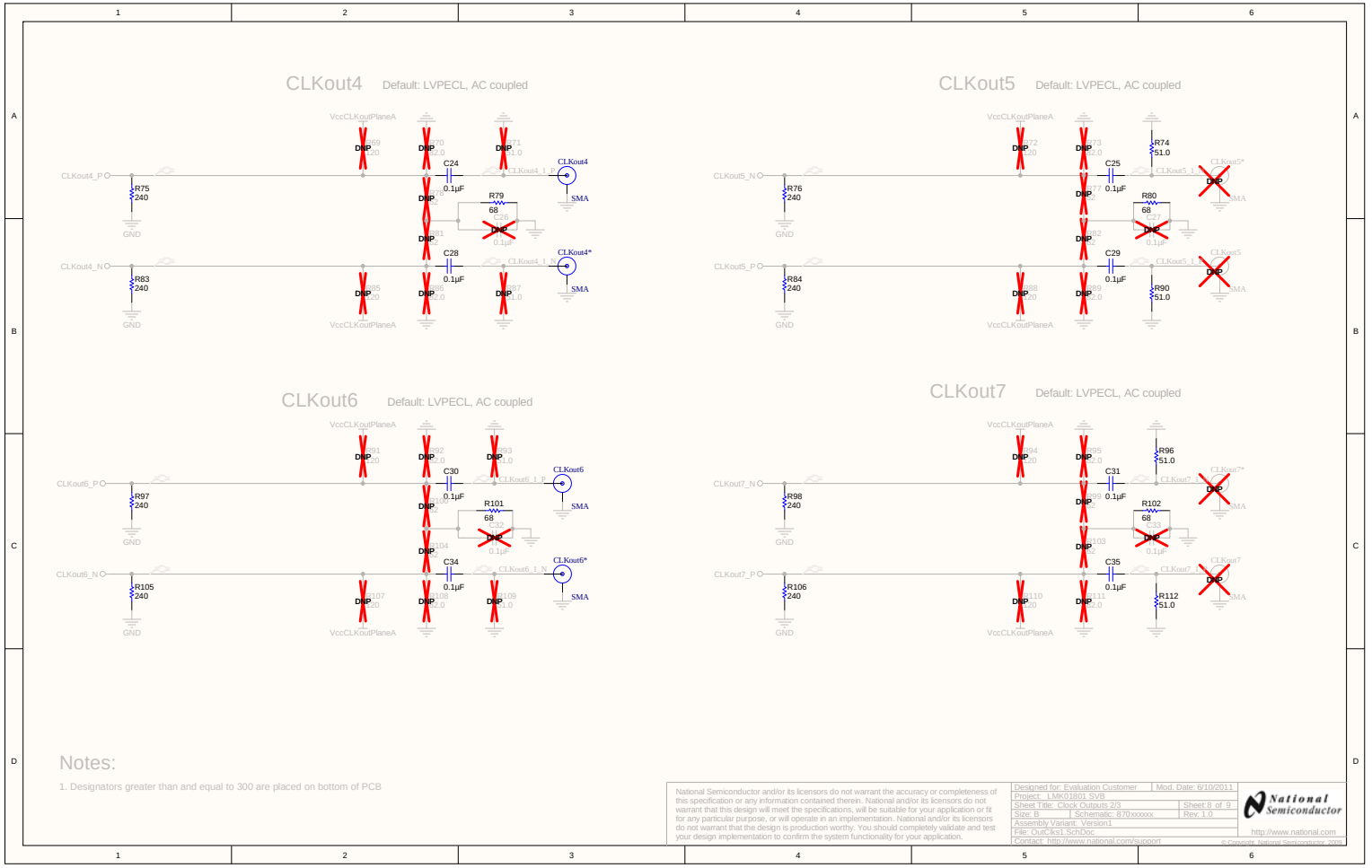
Inputs Page 2



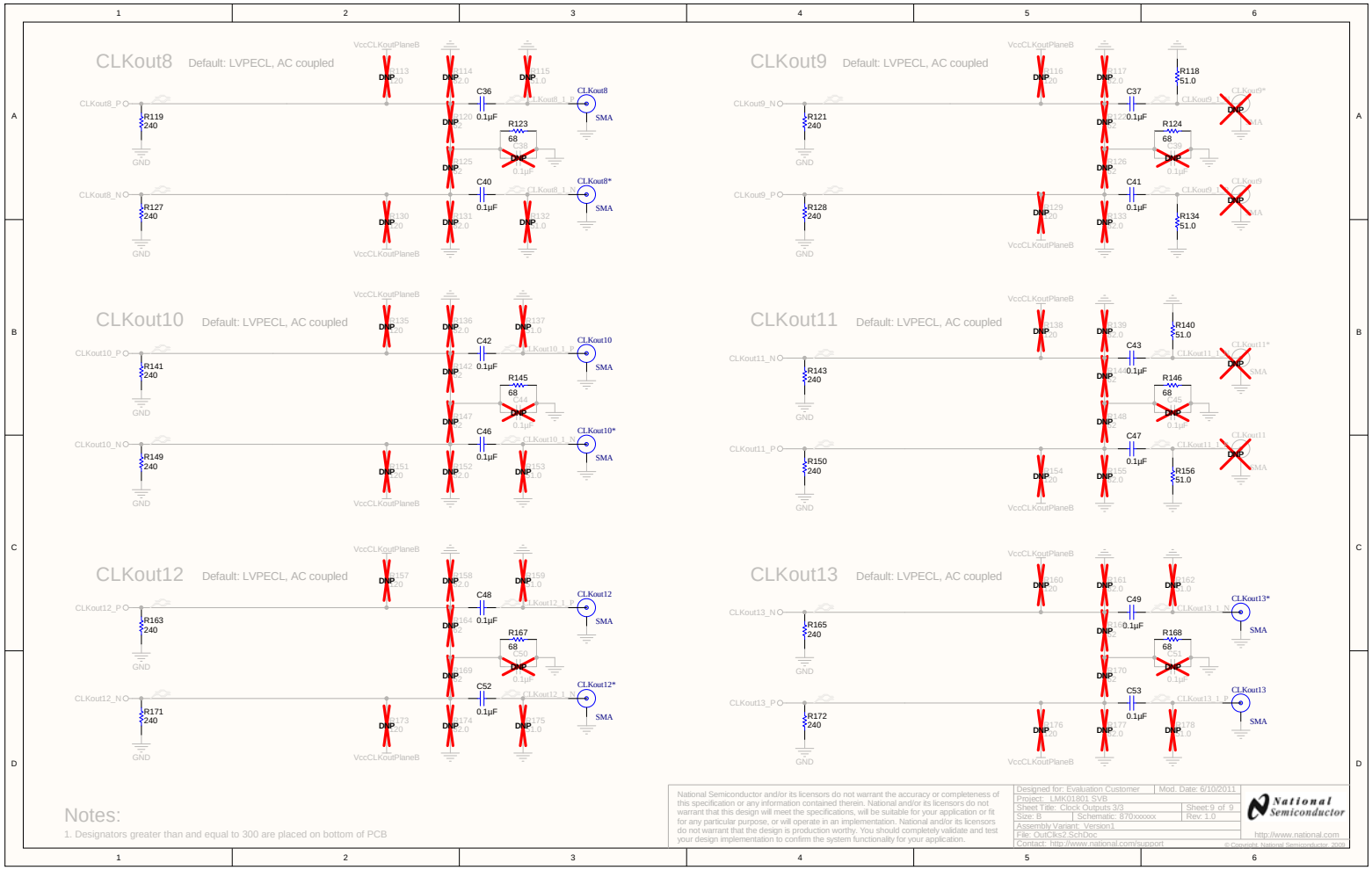
Clock Outputs Page 1



Clock Outputs Page 2



Clock Outputs Page 3



Appendix D: Bill of Materials

Common Bill of Materials for Evaluation Boards

Item	Designator	Description	RoHS	Manufacturer	PartNumber	Quantity
CAPACITORS						
1	C1, C7, C8, C10, C12, C13, C16, C17, C18, C19, C22, C23, C24, C25, C28, C29, C30, C31, C35, C36, C37, C40, C41, C42, C43, C46, C47, C48, C49, C52, C53, C56, C301, C302, C304, C314, C321	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	Y	Kemet	C0603C104J3RACTU	37
2	C4	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	Y	Kemet	C0603C101J5GACTU	1
3	C5, C55, C313, C320, C359	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	Y	Kemet	C0603C105K8PACTU	5
4	C34, C326, C329, C339, C343	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	Y	Kemet	C0603C104K3RACTU	5
5	C54, C303, C312, C319	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	Y	Kemet	C0805C106K8PACTU	4
6	C300	CAP, CERM, 0.68uF, 10V, +80/20%, Y5V, 0603	Y	Kemet	C0603C684Z8VACTU	1
7	C318, C331, C336, C348	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	Y	TDK	C1608X7R1C104K	4
8	C332, C341, C345	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	Y	TDK	C1608X7R1C105K	3
9	C333, C346	CAP, CERM, 2200pF, 100V, +/-5%, X7R, 0603	Y	AVX	06031C222JAT2A	2
10	C334, C347	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0805	Y	Kemet	C0805C106M8PACTU	2
11	C335, C349	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	Y	Kemet	C0603C475K8PACTU	2
12	C337, C350	CAP, CERM, 0.01uF, 25V, +/-5%, C0G/NP0, 0603	Y	TDK	C1608C0G1E103J	2
13	C340, C344	CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603	Y	Kemet	C0603C103K1RACTU	2
14	C351, C352	CAP, CERM, 0.47uF, 25V, +/-10%, X7R, 0603	Y	MuRata	GRM188R71E474KA12D	2

Item	Designator	Description	RoHS	Manufacturer	PartNumber	Quantity
CONNECTORS						
15	CLKin0*, CLKin1, CLKin1*, CLKout0, CLKout0*, CLKout2, CLKout2*, CLKout4, CLKout4*, CLKout6, CLKout6*, CLKout8, CLKout8*, CLKout10, CLKout10*, CLKout12, CLKout12*, Vcc, Vtune	Connector, SMT, End launch SMA 50 Ohm	Y	Emerson Network Power	142-0701-851	19
18	J1	CONN TERM BLK PCB 5.08MM 2POS OR	Y	Weidmuller	1594540000	1
RESISTORS						
19	R2, R179, R303, R329, R332	FB, 1000 ohm, 600 mA, 0603	Y	Murata	BLM18HE102SN1D	5
20	R3, R5, R10, R16, R17, R21, R22, R301, R305, R334, R336, R346, R349, R356	RES, 0 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW06030000Z0EA	14
21	R4, R11	RES, 0 ohm, 5%, 0.125W, 0805	Y	Vishay-Dale	CRCW08050000Z0EA	2
22	R7, R30, R46, R52, R68, R74, R90, R96, R112, R118, R134, R140, R156, R159, R175, R310, R318	RES, 51.0 ohm, 1%, 0.1W, 0603	Y	Yageo America	RC0603FR-0751RL	17
23	R20	RES, 100 ohm, 1%, 0.1W, 0603	Y	Yageo America	RC0603FR-07100RL	1
24	R31, R33, R39, R40, R53, R55, R61, R62, R75, R76, R83, R84, R97, R98, R105, R106, R119, R121, R127, R128, R141, R143, R149, R150, R163, R165, R171, R172	RES, 240 ohm, 1%, 0.1W, 0603	Y	Yageo America	RC0603FR-07240RL	28

25	R35, R36, R57, R58, R79, R80, R101, R102, R123, R124, R145, R146, R167, R168	RES, 68 ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060368R0JNEA	14
26	R302	RES, 39k ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060339K0JNEA	1
27	R306, R307, R311, R312, R313, R315, R316, R319, R320, R322, R323, R325, R326, R328	RES, 27k ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060327K0JNEA	14
28	R308, R309, R314, R317, R321, R324, R327	RES, 1.0k ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW06031K00JNEA	7
29	R331, R335, R337, R338, R344, R347, R350, R352	FB, 120 ohm, 500 mA, 0603	Y	Murata	BLM18AG121SN1D	8
30	R342, R353, R357	RES, 51k ohm, 5%, 0.1W, 0603	Y	Vishay-Dale	CRCW060351K0JNEA	3
31	R343, R354	RES, 2.00k ohm, 1%, 0.1W, 0603	Y	Vishay-Dale	CRCW06032K00FKEA	2
32	R345, R355	RES, 866 ohm, 1%, 0.1W, 0603	Y	Vishay-Dale	CRCW0603866RFKEA	2
INTEGRATED CIRCUITS						
34	U1	LMK01801				1
35	U300, U301	Micropower 800mA Low Noise 'Ceramic Stable' Adjustable Voltage Regulator for 1V to 5V Applications	Y	Texas Instruments	LP3878SD-ADJ	2
36	U302	Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor	Y	Texas Instruments	LP5900SD-3.3	1
37	uWire	Low Profile Vertical Header 2x5 0.100"	Y	FCI	52601-G10-8LF	1

Appendix E: Balun Information

Typical Balun Frequency Response

The following figure illustrates the typical frequency response of the Mini-circuit's ADT2-1T balun.

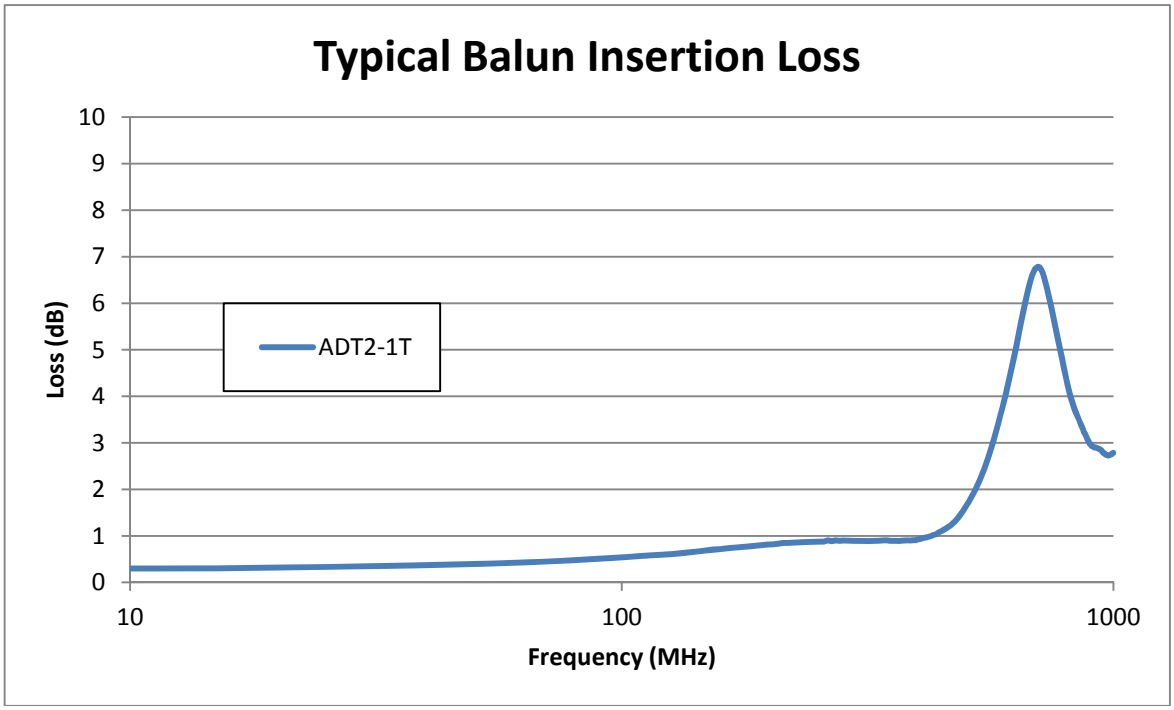


Figure 21 - Typical Balun Frequency Response

Appendix F: Properly Configuring LPT Port

When trying to solve any communications issue, it is convenient to program the POWERDOWN bit to confirm high/low current draw of the evaluation board or the PLL_MUX between "Logic Low" and "Logic High" LD output to confirm successful communications.

LPT Driver Loading

The parallel port must be configured for proper operation. To confirm that the LPT port driver is successfully loading click "LPT/USB" → "Check LPT Port." If the driver properly loads then the following message is displayed:

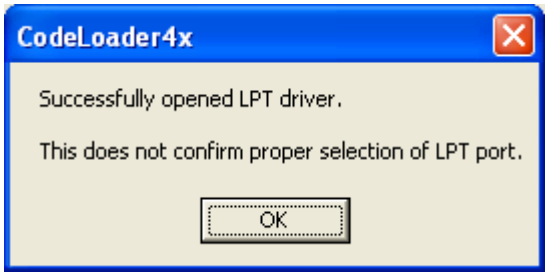


Figure 22 - Successfully Opened LPT Driver

Successful loading of LPT driver does not mean LPT communications in CodeLoader are setup properly. The proper LPT port must be selected and the LPT port must not be in an improper mode.

The PC must be rebooted after install for LPT support to work properly.

Correct LPT Port/Address

To determine the correct LPT port in Windows, open the device manager (On Windows XP, Start → Settings → Control Panel → System → Hardware Tab → Device Manager) and check the LPT port under the Ports (COM & LPT) node of the tree. It can be helpful to confirm that the LPT port is mapped to the expected port address, for instance to confirm that LPT1 is really mapped to address 0x378. This can be checked by viewing the properties of the LPT1 port and viewing resources tab to verify that the I/O Range starts at 0x378. CodeLoader expects the a traditional port mapping:

Port	Address
LPT1	0x378
LPT2	0x278
LPT3	0x3BC

If a non-standard address is used, use the "Other" port address in CodeLoader and type in the port address in hexadecimal. It is possible to change the port address in the computer's BIOS settings. The port address is set in CodeLoader at the Port Setup tab as shown in Figure 23.

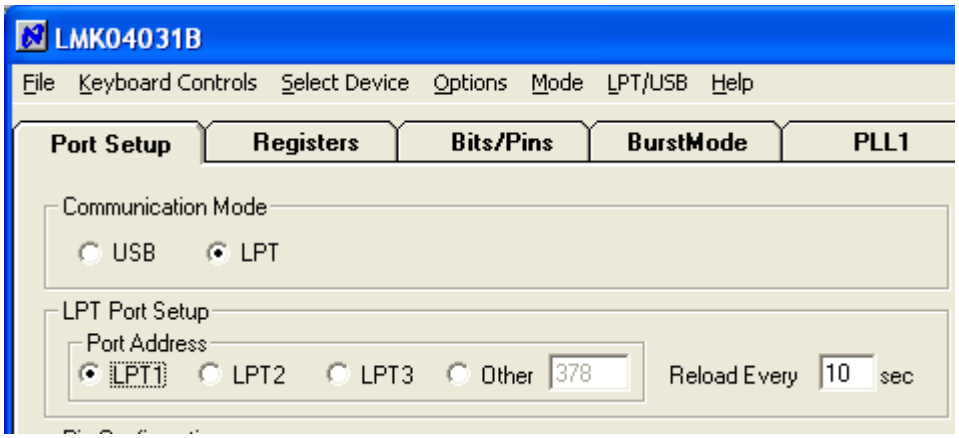


Figure 23 - Selecting the LPT Port

Correct LPT Mode

If communications are not working, then it is possible the LPT port mode is set improperly. It is recommended to use the simple, Output-only mode of the LPT port. This can be set in the BIOS of the computer. Common terms for this desired parallel port mode are “Normal,” “Output,” or “AT.” It is possible to enter BIOS setup during the initial boot up sequence of the computer.

Appendix G: Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading datasheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references; otherwise this value can be calculated as twice the value of V_{OD} as described in the first section

Figure 24 illustrates the two different definitions side-by-side for inputs and Figure 25 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the non-inverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined in volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

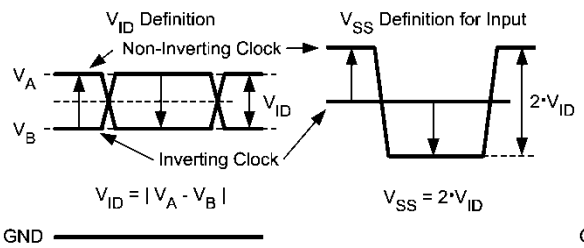


Figure 24 - Two Different Definitions for Differential Output Signals

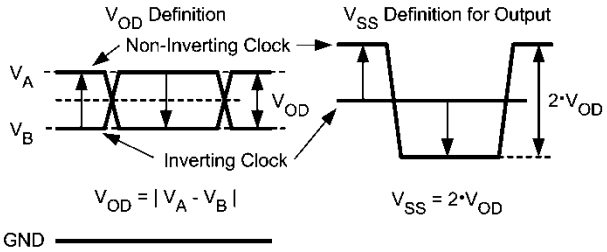


Figure 25 - Two Different Definitions for Differential Input Signals

Appendix H: Troubleshooting Information

If the evaluation board is not behaving as expected, the most likely issues are…

1) Board communication issue
2) Incorrect Programming of the device
3) Setup Error

Refer to this checklist for a practical guide on identifying/exposing possible issues.

Confirm Communications

Refer to Appendix F: Properly Configuring LPT Port to trouble shoot this item.

Remember to load device with Ctrl-L!

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