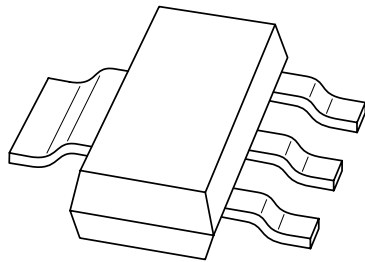


# DATA SHEET



Datasheet.Directory

**PBSS5540Z**

40 V low  $V_{CEsat}$  PNP transistor

Product data sheet  
Supersedes data of 2001 Jan 26

2001 Sep 21

# 40 V low $V_{CEsat}$ PNP transistor

# PBSS5540Z

### FEATURES

- Low collector-emitter saturation voltage
- High current capability
- Improved device reliability due to reduced heat generation.

### APPLICATIONS

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Heavy duty battery powered equipment (motor and lamp drivers)
- MOSFET driver applications.

### DESCRIPTION

PNP low  $V_{CEsat}$  transistor in a SOT223 plastic package.  
NPN complement: PBSS4540Z.

### MARKING

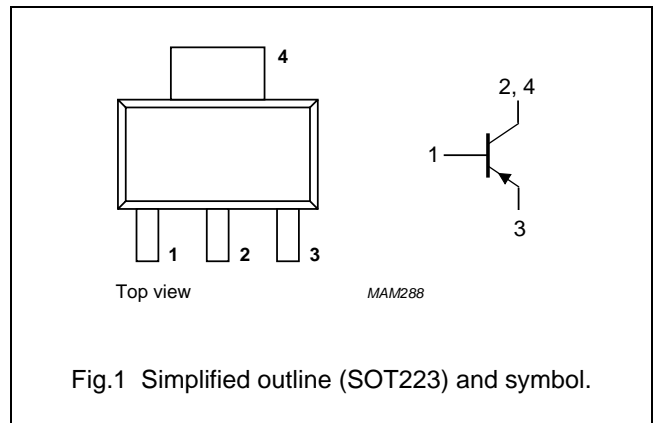
TYPE NUMBER	MARKING CODE
PBSS5540Z	PB5540

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX	UNIT
$V_{CEO}$	emitter-collector voltage	-40	V
$I_C$	collector current (DC)	-5	A
$I_{CM}$	peak collector current	-10	A
$R_{CEsat}$	equivalent on-resistance	<80	m $\Omega$

### PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter
4	collector



40 V low  $V_{CEsat}$  PNP transistor

PBSS5540Z

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–40	V
$V_{CEO}$	collector-emitter voltage	open base	–	–40	V
$V_{EBO}$	emitter-base voltage	open collector	–	–6	V
$I_C$	collector current (DC)		–	–5	A
$I_{CM}$	peak collector current		–	–10	A
$I_{BM}$	peak base current		–	–2	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	1.35	W
		$T_{amb} \leq 25\text{ °C}$ ; note 2	–	2	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>.
2. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 6 cm<sup>2</sup>. For other mounting conditions, see “*Thermal considerations for SOT223 in the General Part of associated Handbook*”.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	92	K/W

**Note**

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>.

40 V low  $V_{CEsat}$  PNP transistor

PBSS5540Z

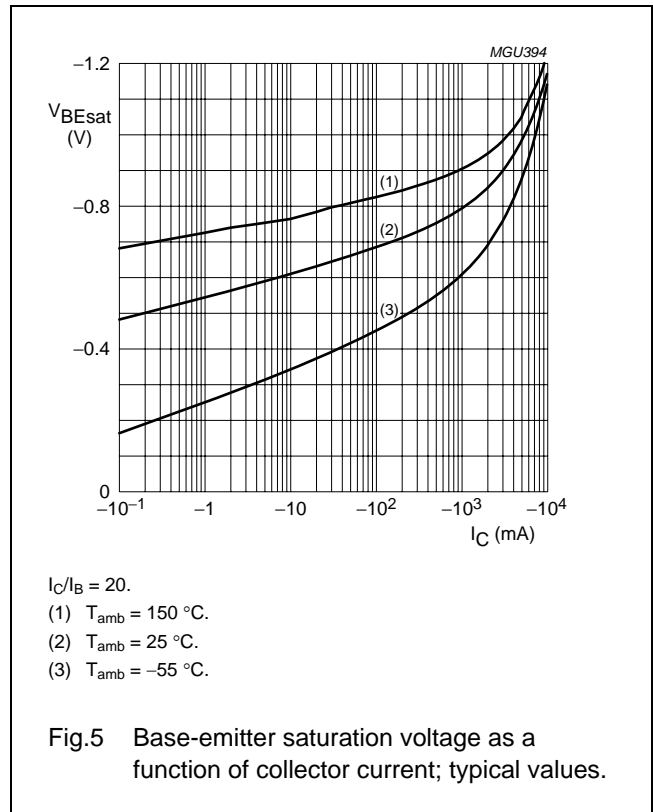
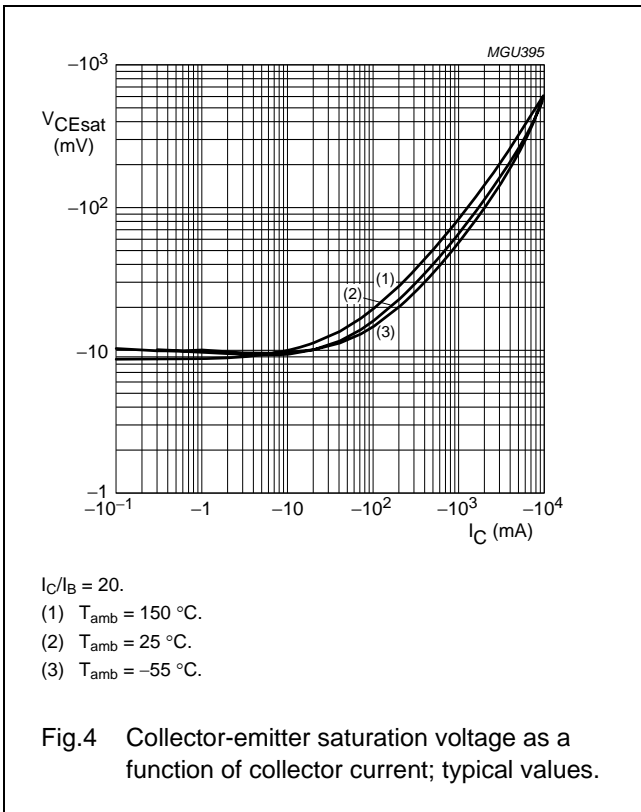
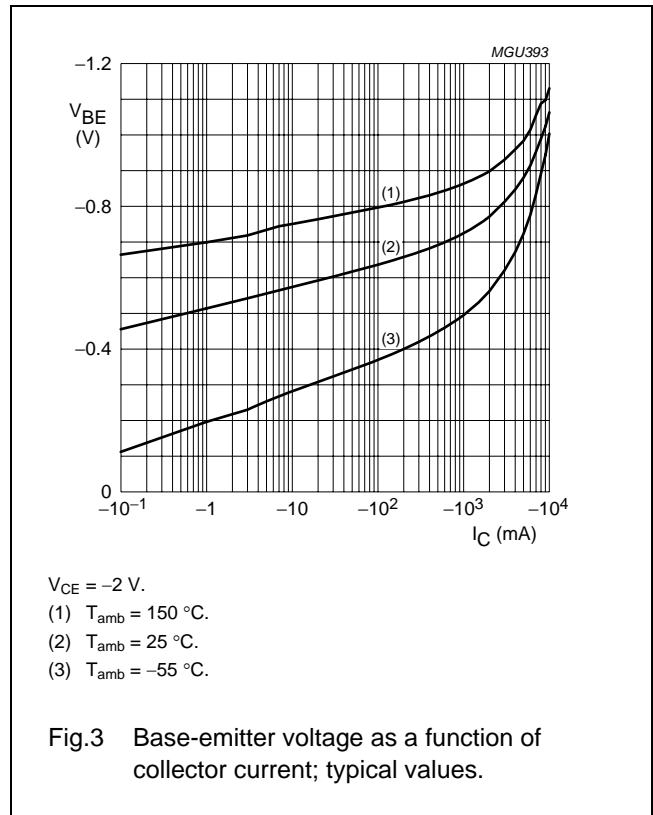
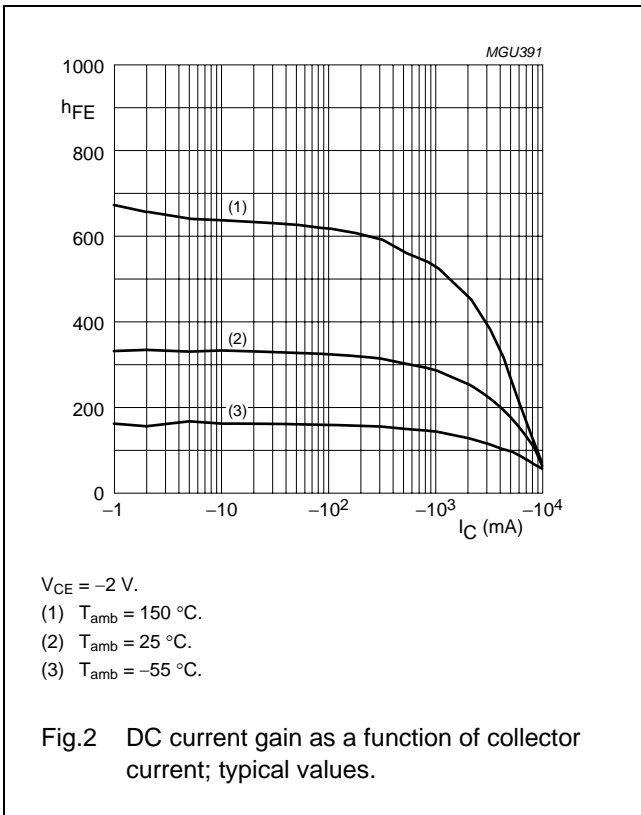
**CHARACTERISTICS** $T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0$	–	–	–100	nA
		$V_{CB} = -30\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	–	–50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0$	–	–	–100	nA
$h_{FE}$	DC current gain	$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	250	350	–	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; \text{note 1}$	200	300	–	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}; \text{note 1}$	150	250	–	
		$V_{CE} = -2\text{ V}; I_C = -5\text{ A}; \text{note 1}$	50	150	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -5\text{ mA}$	–	–80	–120	mV
		$I_C = -1\text{ A}; I_B = -10\text{ mA}$	–	–120	–170	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–110	–160	mV
$R_{CEsat}$	equivalent on-resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	<55	<80	$\text{m}\Omega$
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -5\text{ A}; I_B = -500\text{ mA}$	–	–250	–375	mV
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -5\text{ A}; I_B = -500\text{ mA}$	–	–	–1.3	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	–	–0.8	–1.25	V
$f_T$	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	60	120	–	MHz
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	90	105	pF

**Note**1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}$ ;  $\delta \leq 0.02$ .

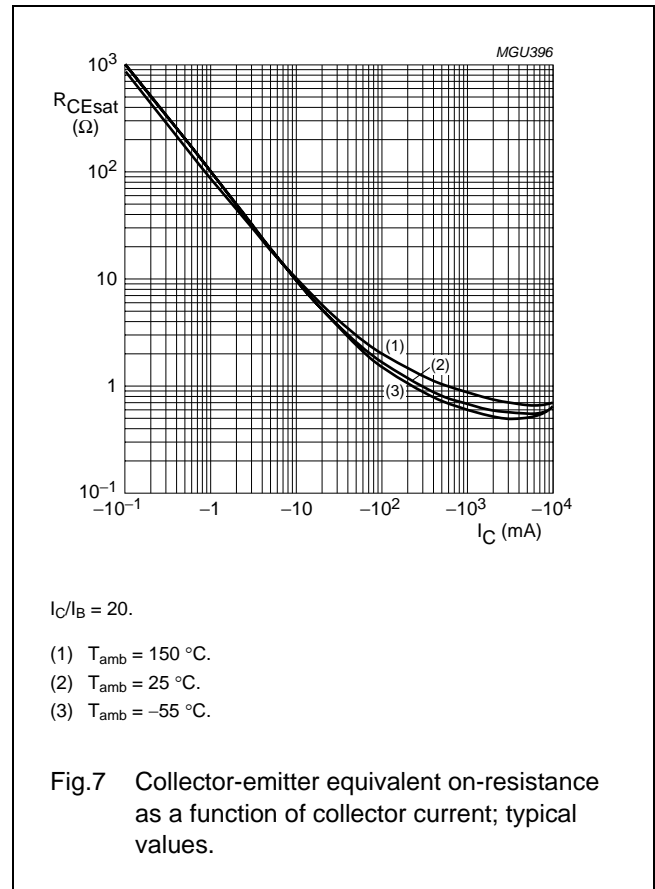
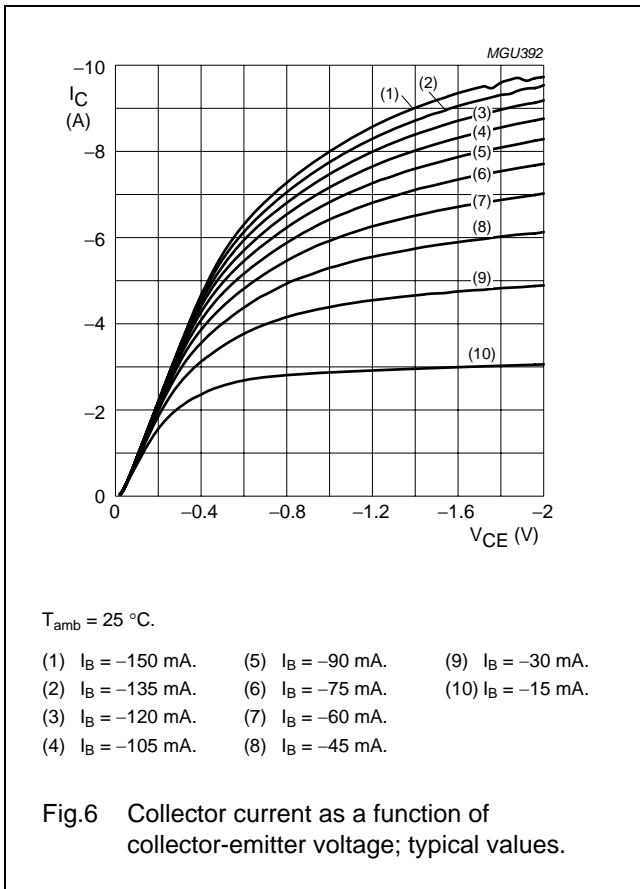
40 V low  $V_{CEsat}$  PNP transistor

PBSS5540Z



40 V low  $V_{CEsat}$  PNP transistor

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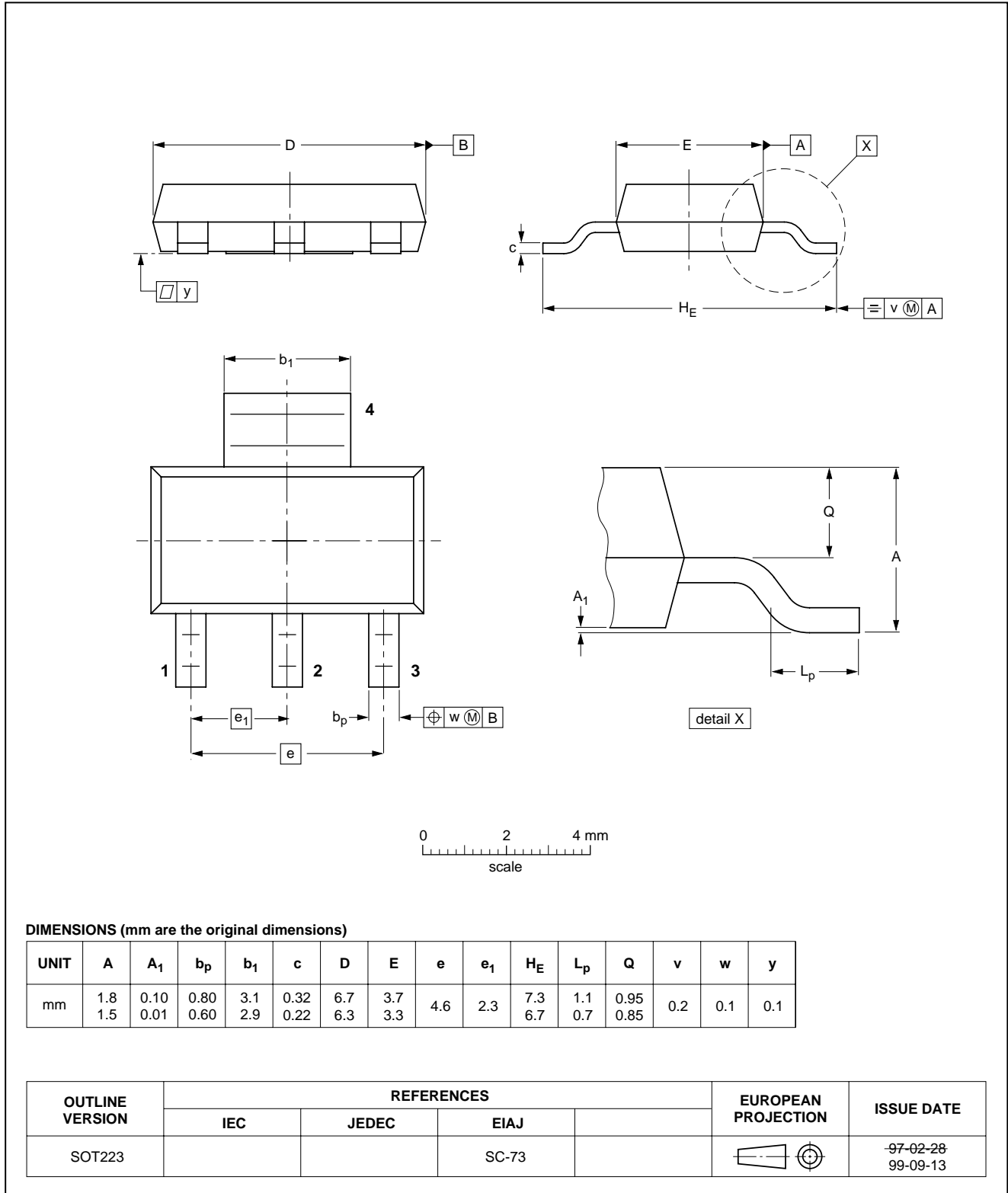
40 V low  $V_{CEsat}$  PNP transistor

PBSS5540Z

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



40 V low  $V_{CEsat}$  PNP transistor

PBSS5540Z

**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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