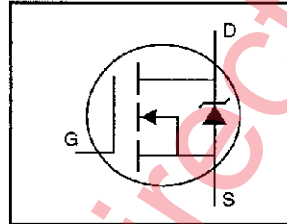


IRF830SPbF

HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free

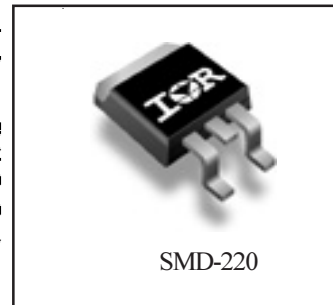


$V_{DSS} = 500V$
 $R_{DS(on)} = 1.5\Omega$
 $I_D = 4.5A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	4.5	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	2.9	
I_{DM}	Pulsed Drain Current ①	18	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	74	
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	3.1	W/°C
	Linear Derating Factor	0.59	
	Linear Derating Factor (PCB Mount)**	0.025	
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	280	mJ
I_{AR}	Avalanche Current ①	4.5	A
E_{AR}	Repetitive Avalanche Energy ①	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.7	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

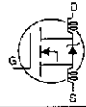
** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

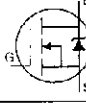
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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.61	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V _{GS} =10V, I _D =2.7A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	2.5	—	—	S	V _{DS} =50V, I _D =2.7A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} =500V, V _{GS} =0V
		—	—	250		V _{DS} =400V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} =-20V
Q _g	Total Gate Charge	—	—	38	nC	I _D =3.1A
Q _{gs}	Gate-to-Source Charge	—	—	5.0		V _{DS} =400V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	22		V _{GS} =10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	8.2	—	ns	V _{DD} =250V
t _r	Rise Time	—	16	—		I _D =3.1A
t _{d(off)}	Turn-Off Delay Time	—	42	—		R _G =12Ω
t _f	Fall Time	—	16	—		R _D =79Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	610	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	160	—		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	68	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	4.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	18		
V _{SD}	Diode Forward Voltage	—	—	1.6	V	T _J =25°C, I _S =4.5A, V _{GS} =0V ③
t _{rr}	Reverse Recovery Time	—	320	640	ns	T _J =25°C, I _F =3.1A
Q _{rr}	Reverse Recovery Charge	—	1.0	2.0	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=50V, starting T_J=25°C, L=24mH
R_G=25Ω, I_{AS}=4.5A (See Figure 12)
- ③ I_{SD}≤4.5A, di/dt≤75A/μs, V_{DD}≤V_{(BR)DSS},
T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

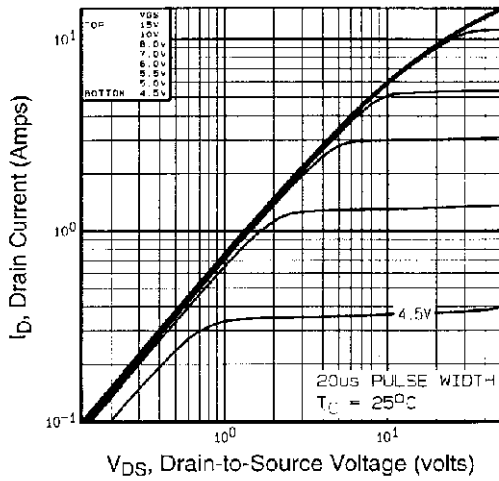


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

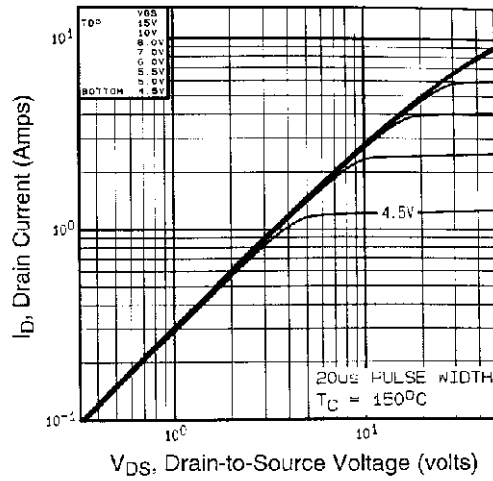


Fig 2. Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

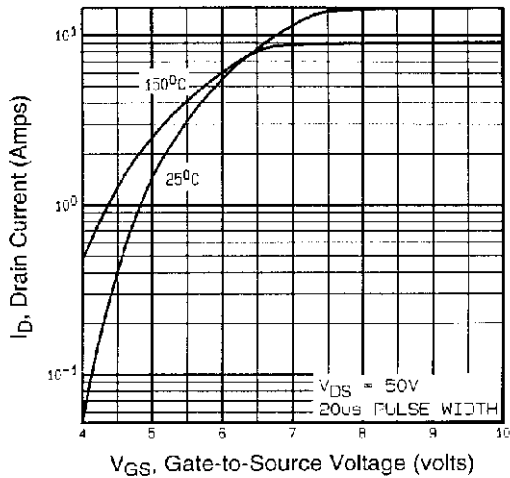


Fig 3. Typical Transfer Characteristics

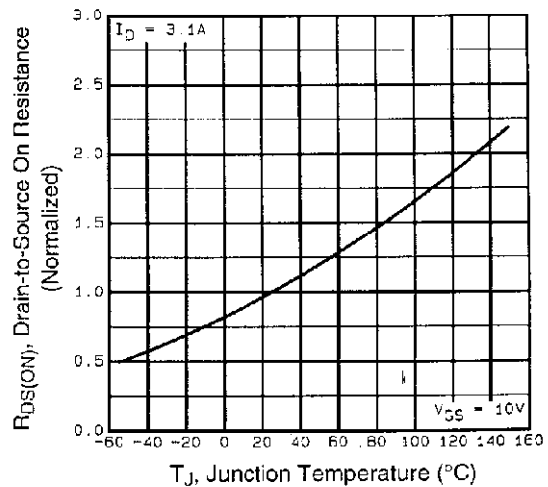


Fig 4. Normalized On-Resistance
 Vs. Temperature

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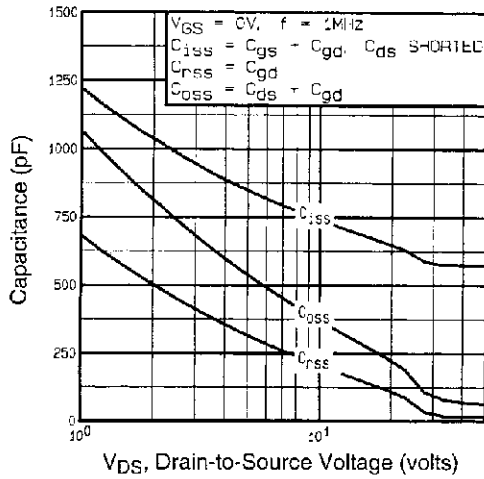


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

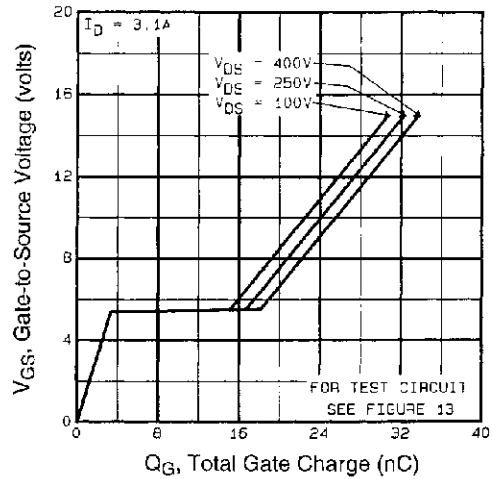


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

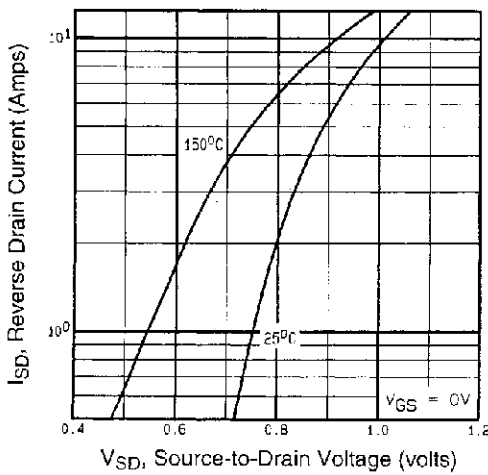


Fig 7. Typical Source-Drain Diode Forward Voltage

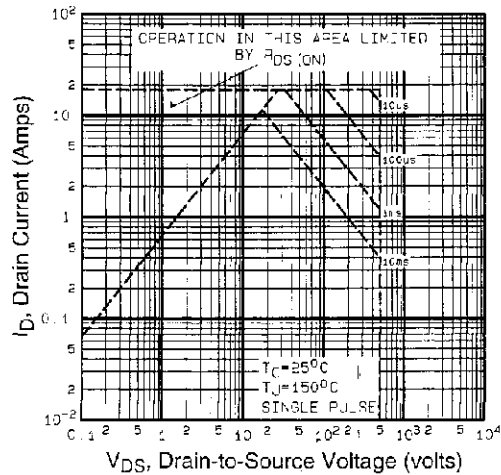


Fig 8. Maximum Safe Operating Area

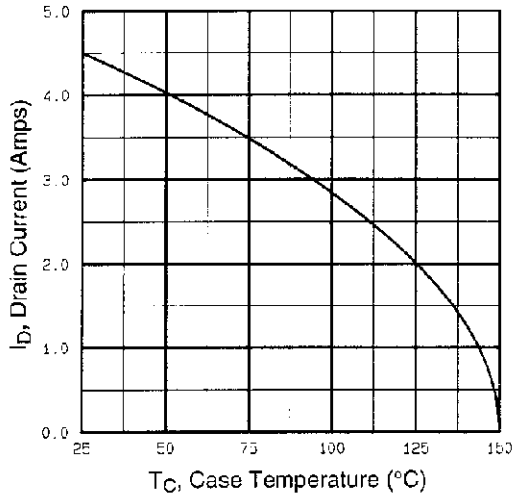


Fig 9. Maximum Drain Current Vs. Case Temperature

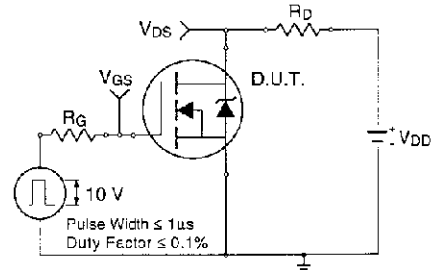


Fig 10a. Switching Time Test Circuit

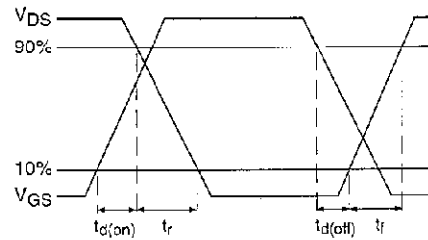


Fig 10b. Switching Time Waveforms

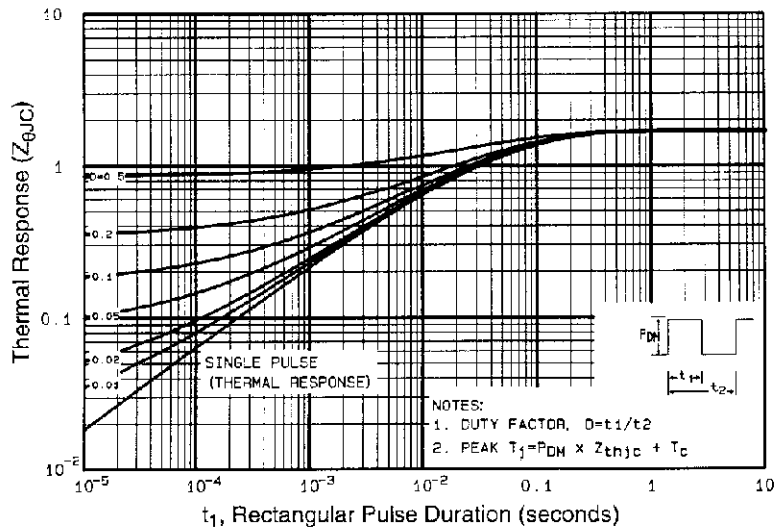


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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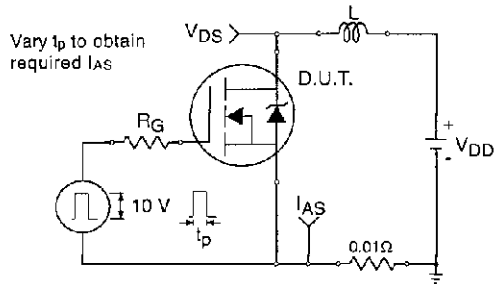


Fig 12a. Unclamped Inductive Test Circuit

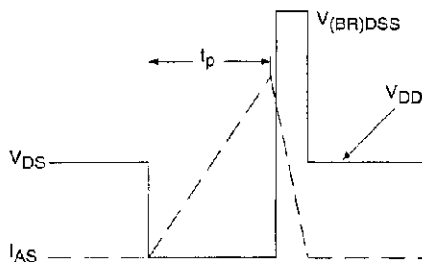


Fig 12b. Unclamped Inductive Waveforms

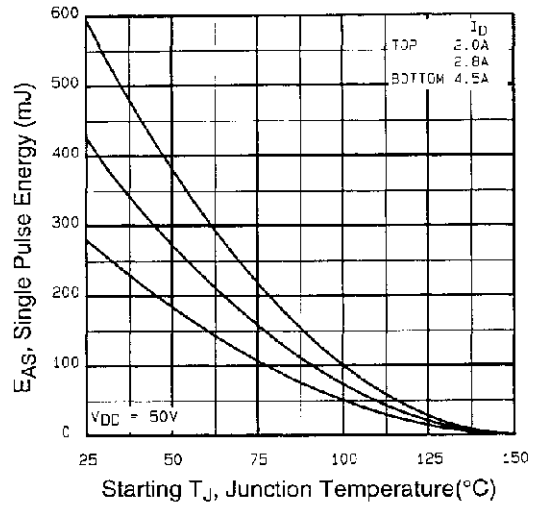


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

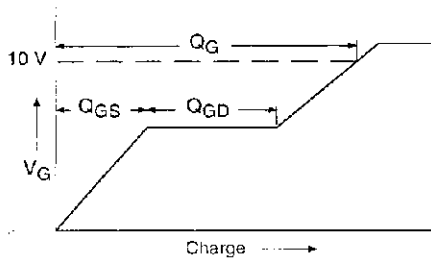


Fig 13a. Basic Gate Charge Waveform

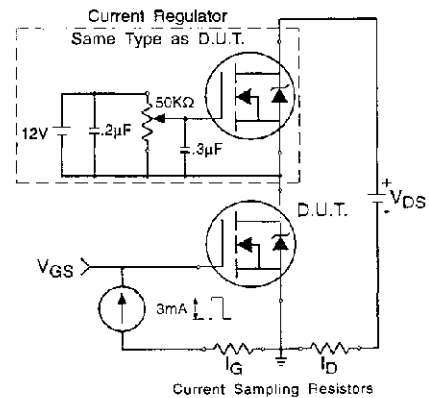
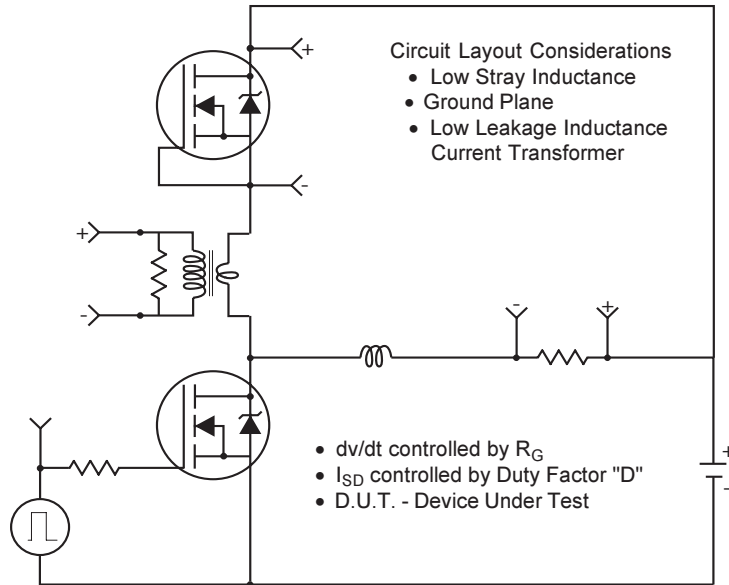


Fig 13b. Gate Charge Test Circuit

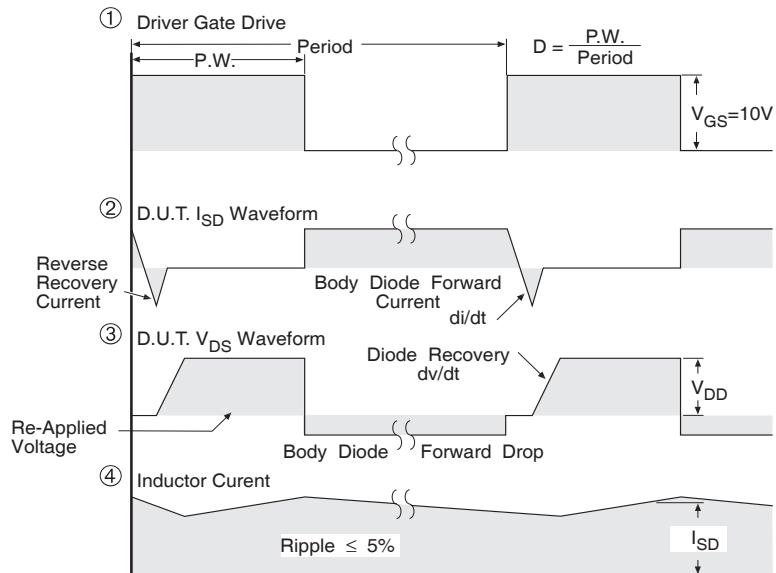
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Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

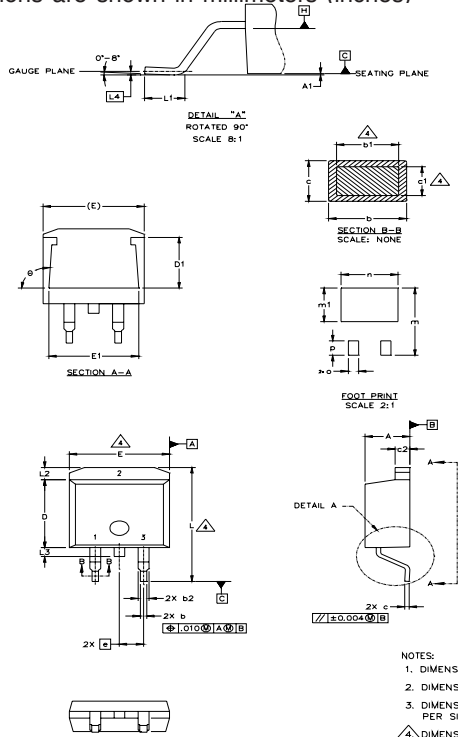
Fig. 14 For N and P Channel HEXFETS

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	3
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs - CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE +
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

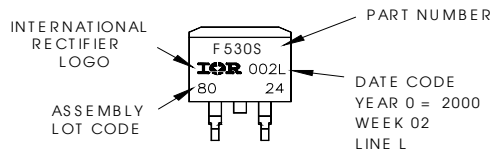
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

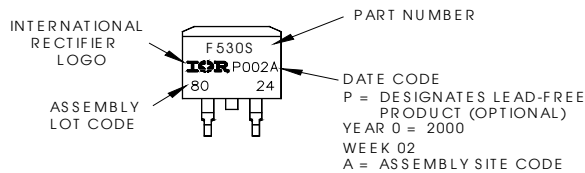
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

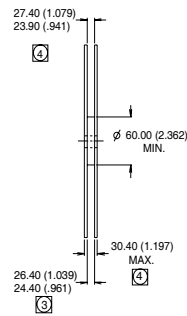
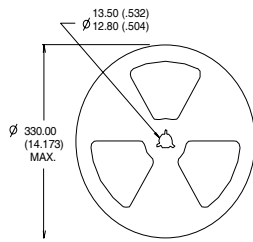
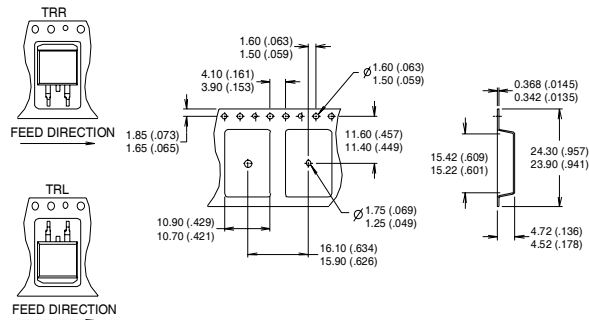
Note: "P" in assembly line
position indicates "Lead-Free"



OR



D²Pak Tape & Reel Information



- NOTES:
 1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.



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