LC²MOS 16-Bit Voltage Output DAC

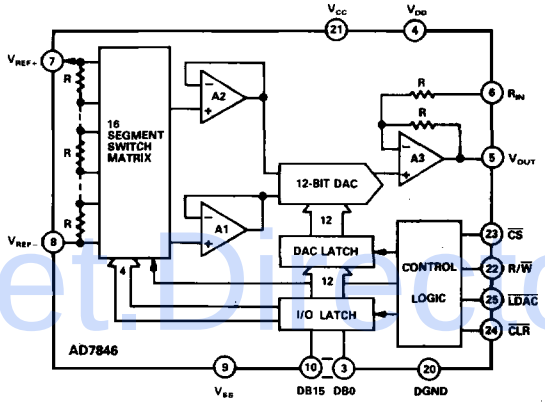
AD7846

3

FEATURES

16-Bit Monotonicity over Temperature
±2LSBs Integral Linearity Error
Microprocessor Compatible with Readback Capability
Unipolar or Bipolar Output
Multiplying Capability
Low Power (100mW typical)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7846 is a 16-bit DAC constructed with Analog Devices' LC²MOS process. It has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier. These can be configured to give a unipolar output range (0 to +5V, 0 to +10V) or bipolar output ranges (±5V, ±10V).

The DAC uses a segmented architecture. The 4MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

In addition to the excellent accuracy specifications, the AD7846 also offers a comprehensive microprocessor interface. There are 16 data I/O pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ allow writing to and reading from the I/O latch. This is the readback function which is useful in ATE applications. $\overline{LDAC}$ allows simultaneous updating of DACs in a multi-DAC system and the $\overline{CLR}$ line will reset the contents the DAC latch to 00 . . . 000 or 10 . . . 000 depending on the state of R/$\overline{W}$. This means that the DAC output can be reset to 0V in both the unipolar and bipolar configurations.

The AD7846 is available in 28-pin plastic, ceramic, LCCC and PLCC packages.

PRODUCT HIGHLIGHTS

1. 16-Bit Monotonicity
   The guaranteed 16-bit monotonicity over temperature makes the AD7846 ideal for closed-loop applications.
2. Readback
   The ability to read back the DAC register contents minimizes software routines when the AD7846 is used in ATE systems.
3. Power Dissipation
   Power dissipation of 100mW makes the AD7846 the lowest power, high accuracy DAC on the market.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7846—SPECIFICATIONS[1]

(V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V. V_{OUT} loaded with 2kΩ, 1000pF to 0V. V_{REF+} = +5V, R_{IN} connected to 0V. All specifications T_{MIN} to T_{MAX} unless otherwise stated.)

Parameter	J, A Versions	K, B Versions	S Version[2]	Units	Test Conditions/Comments
Resolution	16	16	16	Bits	
UNIPOLAR OUTPUT					V_{REF-}=0V, V_{OUT}=0V to +10V
Relative Accuracy @ 25°C	±12	±4	±12	LSB typ	1LSB=153μV
T_{min} to T_{max}	±16	±8	±16	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±12	±6	±12	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±16	±16	±24	LSB max	
Offset Error @ 25°C	±12	±6	±12	LSB typ	
T_{min} to T_{max}	±16	±16	±24	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-}=−5V, V_{OUT}=−10V to +10V
Relative Accuracy @ 25°C	±6	±2	±6	LSB typ	1LSB=305μV
T_{min} to T_{max}	±8	±4	±8	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ 25°C	±6	±4	±6	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±16	±16	±16	LSB max	
Offset Error @ 25°C	±6	±4	±6	LSB typ	V_{OUT} Load=10MΩ
T_{min} to T_{max}	±16	±12	±16	LSB max	
Bipolar Zero Error @ 25°C	±6	±4	±6	LSB typ	
T_{min} to T_{max}	±12	±8	±16	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	20	20	20	kΩ min	Resistance from V_{REF-} to V_{REF+}
	40	40	40	kΩ max	Typically 30kΩ
V_{REF+} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
V_{REF-} Range	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	V_{SS}+6 to V_{DD}−6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V_{SS}+4 to V_{DD}−3	V max	
Resistive Load	2	2	3	kΩ min	To 0V
Capacitive Load	1000	1000	1000	pF max	To 0V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	To 0V or Any Power Supply
DIGITAL INPUTS					
V_{IH} (Input High Voltage)	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK}=1.6mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE}=400μA
Floating State Leakage Current	±10	±10	±10	μA max	DB0-DB15=0 to V_{CC}
Floating State Output Capacitance[3]	10	10	10	pF max	
POWER REQUIREMENTS[4]					
V_{DD}	+11.4/+15.75	+11.4/+15.75	+11.4/+15.75	Vmin/Vmax	
V_{SS}	−11.4/−15.75	−11.4/−15.75	−11.4/−15.75	Vmin/Vmax	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	Vmin/Vmax	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded
I_{CC}	1	1	1	mA max	
Power Supply Sensitivity[5]	1.5	1.5	2	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES

[1]Temperature Ranges as follows: J, K Versions: 0 to +70°C; A, B Versions: −25°C to +85°C; S Version: −55°C to +125°C.

[2]Minimum load for S version is 3kΩ.

[3]Sample tested to ensure compliance.

[4]AD7846 is functional with power supplies of ±12V. See Typical Performance Curves.

[5]Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test. (V_{REF+} = +5V, V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V, R_{FB} connected to 0V.)

Parameter	T_A = 25°C	T_A = T_{min} to T_{max}	Units	Test Conditions/Comments
Output Settling Time	7	7	µs max	To 0.006% FSR. V_{OUT} loaded. V_{REF-} = 0V.
	9	9	µs max	To 0.003% FSR. V_{OUT} loaded. V_{REF-} = −5V.
Digital-to-Analog Glitch Impulse	400	400	nV-secs typ	DAC alternately loaded with 10 . . . 0000 and 01 . . . 1111. V_{OUT} unloaded.
AC Feedthrough	0.5	0.5	mV pk-pk typ	V_{REF-} = 0V, V_{REF+} = 1V rms, 10kHz sine wave. DAC loaded with all 0s.
Digital Feedthrough	10	10	nV-secs typ	DAC alternately loaded with all 1s and all 0s. $\overline{CS}$ High.
Output Noise Voltage Density (1kHz–100kHz)	50	50	nV/√Hz typ	Measured at V_{OUT}. DAC loaded with 0111011 . . . 11. V_{REF+} = V_{REF-} = 0V.

TIMING CHARACTERISTICS (V_{DD} = +14.25V to +15.75V, V_{SS} = −14.25V to −15.75V, V_{CC} = +4.75V to +5.25V.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C, T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Setup Time
t_2	150	160	190	ns min	$\overline{CS}$ Pulse Width (Write Cycle)
t_3	40	40	50	ns min	R/$\overline{W}$ to $\overline{CS}$ Hold Time
t_4	110	110	120	ns min	Data Setup Time
t_5	0	0	0	ns min	Data Hold Time
t_6	230	270	320	ns max	Data Access Time
t_7	10	10	10	ns min	Bus Relinquish Time
	80	90	90	ns max	
t_8	20	20	20	ns min	$\overline{CLR}$ Setup Time
t_9	150	150	150	ns min	$\overline{CLR}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CLR}$ Hold Time
t_{11}	80	100	100	ns min	$\overline{LDAC}$ Pulse Width
t_{12}	240	280	330	ns min	$\overline{CS}$ Pulse Width (Read Cycle)

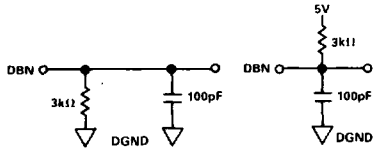
NOTES

[1]Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_R = t_F = 5 ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

[2]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

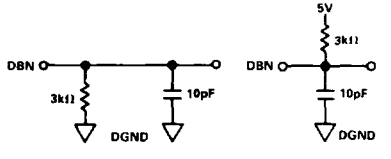
[3]t_7 is defined as the time required for an output to change 0.5V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.



a. High Z to V_{OH} b. High Z to V_{OL}

Figure 1. Load Circuits for Access Time (t_6)



a. V_{OH} to High Z b. V_{OL} to High Z

Figure 2. Load Circuits for Bus Relinquish Time (t_7)

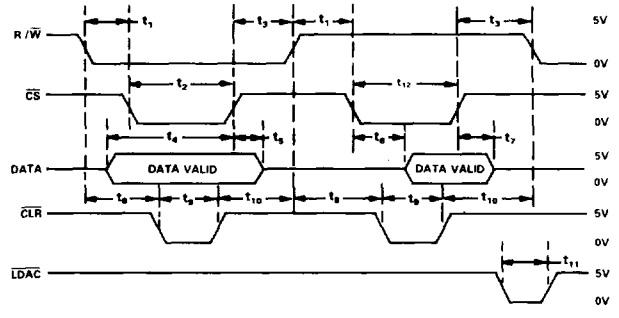
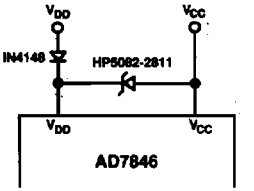


Figure 3. AD7846 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND . . . . . −0.3V or +17V
V_{CC} to DGND[2]
. . . . . −0.3V, V_{DD} +0.3V or +7V (Whichever Is Lower)
V_{SS} to DGND . . . . . +0.3V to −17V
V_{REF+} to DGND . . . . . ±25V
V_{REF-} to DGND . . . . . ±25V
V_{OUT} to DGND[3] . . . . . ±25V
R_{IN} to DGND . . . . . ±25V
Digital Input Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Digital Output Voltage to DGND . . . . . −0.3V to V_{CC} +0.3V
Power Dissipation (Any Package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C
Operating Temperature Range
J, K Versions . . . . . 0 to +70°C
A, B Versions . . . . . −25°C to +85°C
S Version . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.
[2]V_{CC} must not exceed V_{DD} by more than 0.3V. If it is possible for this to happen during power supply sequencing, the following diode protection scheme will ensure protection.



[3]V_{OUT} may be shorted to DGND, V_{DD}, V_{SS}, V_{CC} provided that the power dissipation of the package is not exceeded.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7846JN	0°C to +70°C	±16 LSB	N-28
AD7846KN	0°C to +70°C	±8 LSB	N-28
AD7846JP	0°C to +70°C	±16 LSB	P-28A
AD7846KP	0°C to +70°C	±8 LSB	P-28A
AD7846AQ	−25°C to +85°C	±16 LSB	Q-28
AD7846BQ	−25°C to +85°C	±8 LSB	Q-28
AD7846SQ/883B	−55°C to +125°C	±16 LSB	Q-28
AD7846SE/883B	−55°C to +125°C	±16 LSB	E-28A

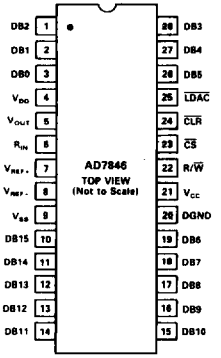
*Q = Ceramic DIP; E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

CAUTION

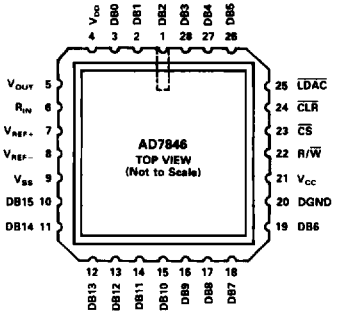
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP



LCCC



PLCC