

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.5A and 3.0A, 350V-400V

$r_{DS(on)} = 1.8 \Omega$ and 2.5Ω

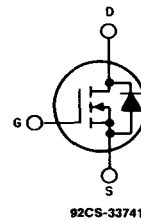
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRF720, IRF721, IRF722 and IRF723 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

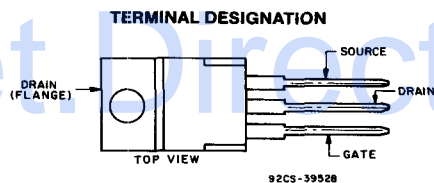
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM



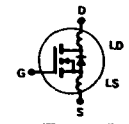
JEDEC TO-220AB

Absolute Maximum Ratings

Parameter	IRF720	IRF721	IRF722	IRF723	Units
V_{DS} Drain - Source Voltage ①	400	350	400	350	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ K}\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	3.0	3.0	2.5	2.5	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM} Pulsed Drain Current ②	12	12	10	10	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	40 (See Fig. 14)				W
Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
	12	12	10	10	
T_J Operating Junction and Storage Temperature Range	-55 to 150				°C
T_{stg} Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF720, IRF721, IRF722, IRF723


Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain-Source Breakdown Voltage	IRF720 IRF722	400	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	IRF721 IRF723	350	—	—	V		
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
I _{D(on)} On-State Drain Current ②	IRF720 IRF721	3.0	—	—	A	$V_{DS} \leq I_{D(on)} \times R_{DS(on) \text{ max.}}$, $V_{GS} = 10\text{V}$	
	IRF722 IRF723	2.5	—	—	A		
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF720 IRF721	—	1.5	1.8	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$	
	IRF722 IRF723	—	1.8	2.5	Ω		
g _{fs} Forward Transconductance ②	ALL	1.0	2.0	—	S/(V)	$V_{DS} \leq I_{D(on)} \times R_{DS(on) \text{ max.}}$, $I_D = 1.5\text{A}$	
C _{iss} Input Capacitance	ALL	—	450	—	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$	
C _{oss} Output Capacitance	ALL	—	100	—	pF	See Fig. 10	
C _{rss} Reverse Transfer Capacitance	ALL	—	20	—	pF		
t _{d(on)} Turn-On Delay Time	ALL	—	20	40	ns	$V_{DD} = 0.5 BV_{DSS}$, $I_D = 1.5\text{A}$, $Z_\theta = 500$ See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)	
t _r Rise Time	ALL	—	25	50	ns		
t _{d(off)} Turn-Off Delay Time	ALL	—	50	100	ns		
t _f Fall Time	ALL	—	25	50	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	12	15	nC	$V_{GS} = 10\text{V}$, $I_D = 4.0\text{A}$, $V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	6.0	9.0	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	6.0	9.0	nC		
L _D Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.	Modified MOSFET symbol showing the internal device inductances. 
		—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	
L _S Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	

Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	3.12	$^\circ\text{C}/\text{W}$	
R _{thCS} Case-to-Sink	ALL	—	1.0	—	$^\circ\text{C}/\text{W}$	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	80	$^\circ\text{C}/\text{W}$	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF720 IRF721	—	—	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF722 IRF723	—	—	2.5	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF720 IRF721	—	—	12	A	
	IRF722 IRF723	—	—	10	A	
V _{SD} Diode Forward Voltage ②	IRF720 IRF721	—	—	1.6	V	$T_C = 25^\circ\text{C}$, $I_S = 3.0\text{A}$, $V_{GS} = 0\text{V}$
	IRF722 IRF723	—	—	1.5	V	$T_C = 25^\circ\text{C}$, $I_S = 2.5\text{A}$, $V_{GS} = 0\text{V}$
t _{rr} Reverse Recovery Time	ALL	—	450	—	ns	$T_J = 150^\circ\text{C}$, $I_C = 3.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q _{RR} Reverse Recovered Charge	ALL	—	3.1	—	μC	$T_J = 150^\circ\text{C}$, $I_C = 3.0\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① $T_J = 25^\circ\text{C}$ to 150°C . ② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

IRF720, IRF721, IRF722, IRF723

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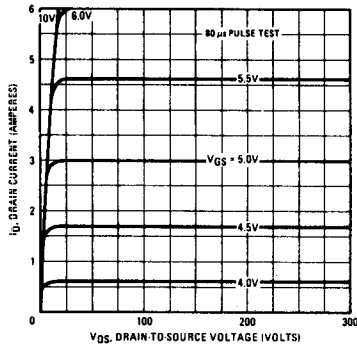


Fig. 1 - Typical Output Characteristics

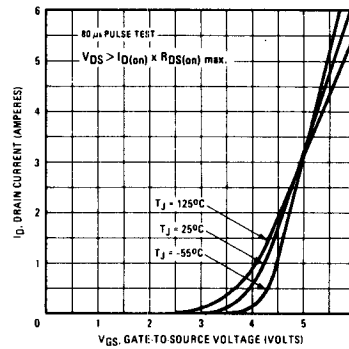


Fig. 2 - Typical Transfer Characteristics

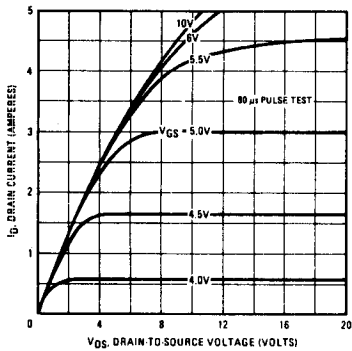


Fig. 3 - Typical Saturation Characteristics

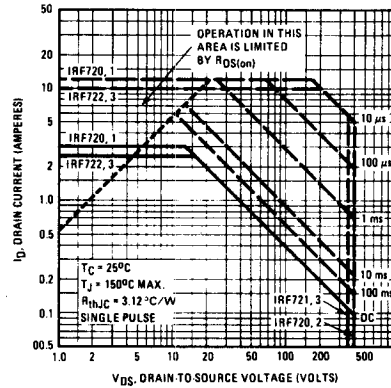


Fig. 4 - Maximum Safe Operating Area

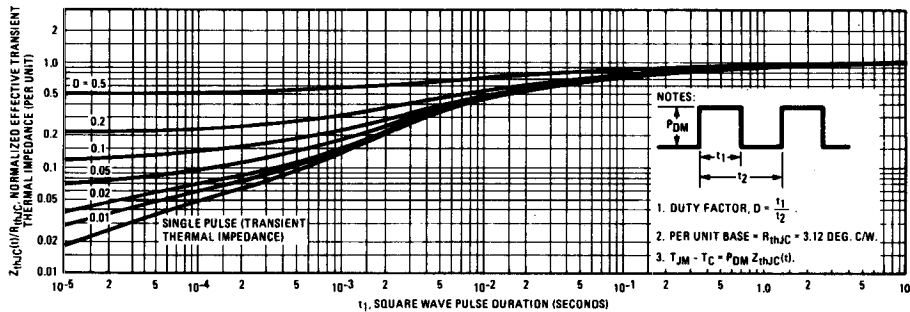


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF720, IRF721, IRF722, IRF723

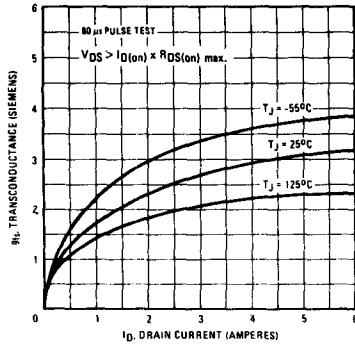


Fig. 6 - Typical Transconductance Vs. Drain Current

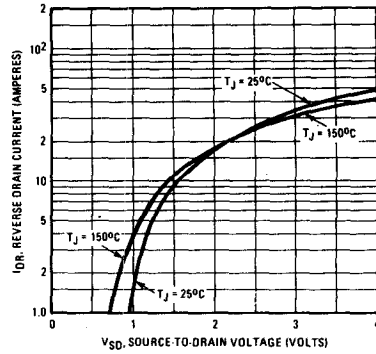


Fig. 7 - Typical Source-Drain Diode Forward Voltage

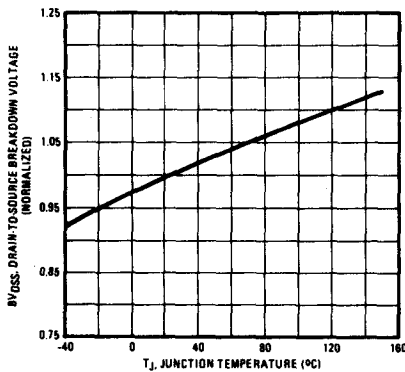


Fig. 8 - Breakdown Voltage Vs. Temperature

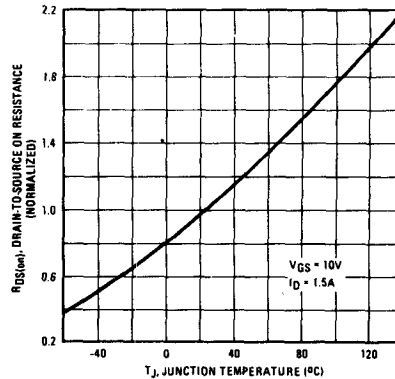


Fig. 9 - Normalized On-Resistance Vs. Temperature

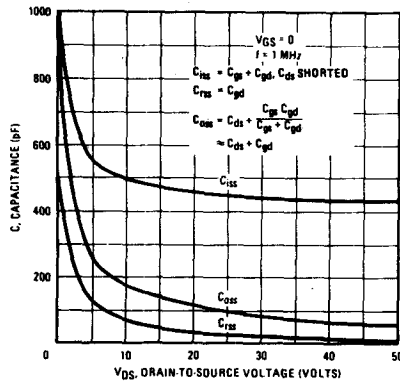


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

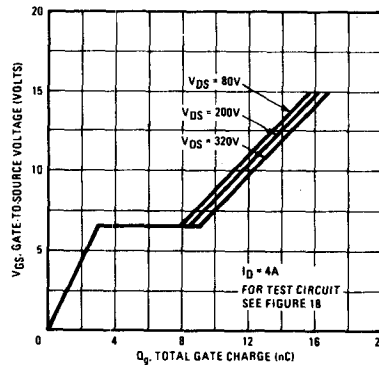


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRF720, IRF721, IRF722, IRF723

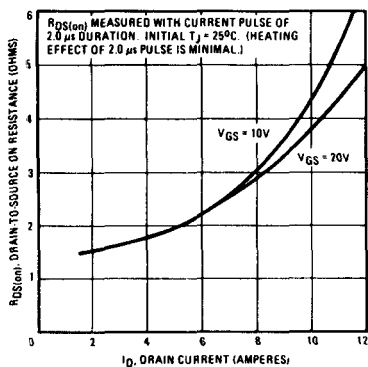


Fig. 12 - Typical On-Resistance Vs. Drain Current

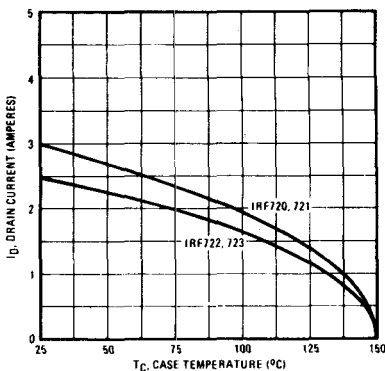


Fig. 13 - Maximum Drain Current Vs. Case Temperature

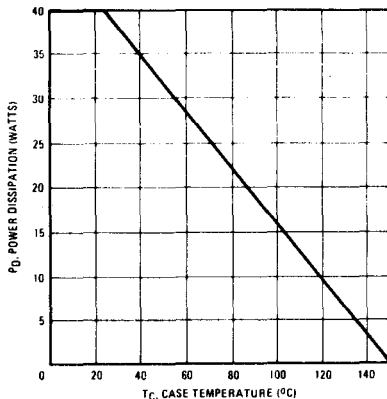


Fig. 14 - Power Vs. Temperature Derating Curve

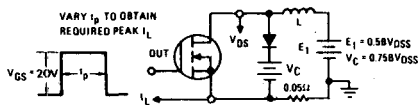


Fig. 15 - Clamped Inductive Test Circuit

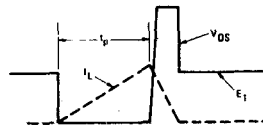


Fig. 16 - Clamped Inductive Waveforms

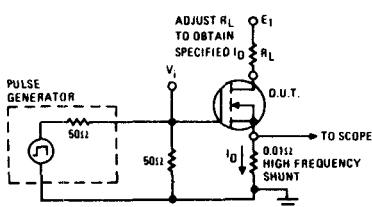


Fig. 17 - Switching Time Test Circuit

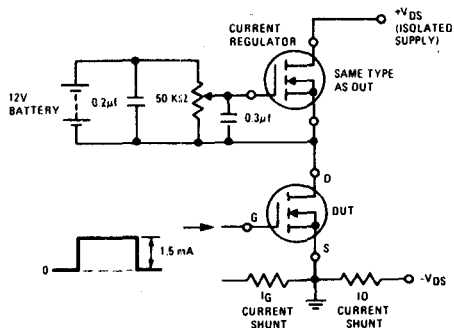


Fig. 18 - Gate Charge Test Circuit