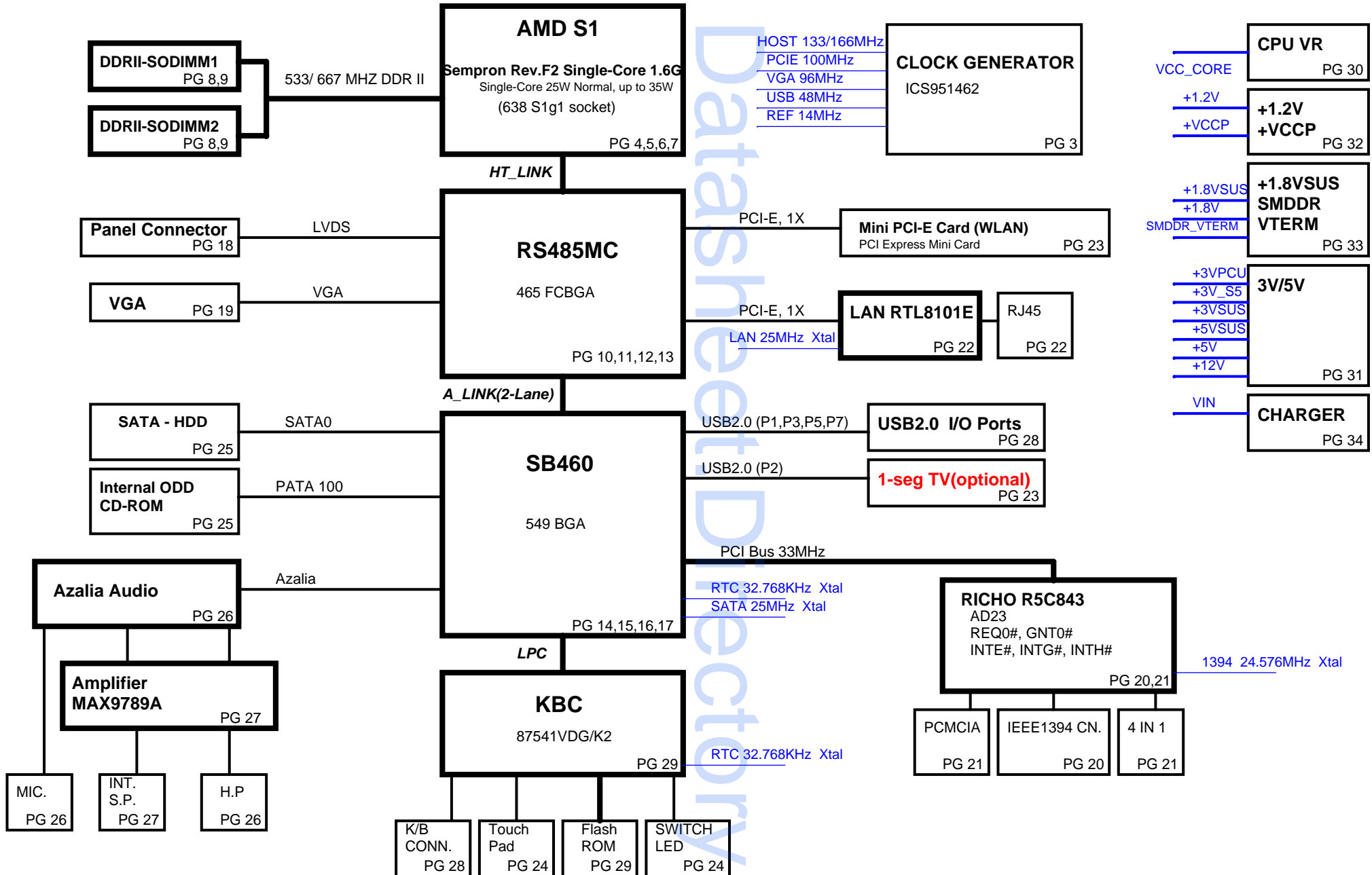


ES2 BLOCK DIAGRAM



Voltage Rails

Power	Voltage	ON S0-S2	ON S3	ON S4	ON S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3V	V	V	V	V	
RVCC3	3V	V	V	V		RVCC_ON
RVCC1.8	1.8V	V	V	V		RVCC_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON
VLDT_RUN	1.2V	V				VLDT_ON

PCB STACK UP

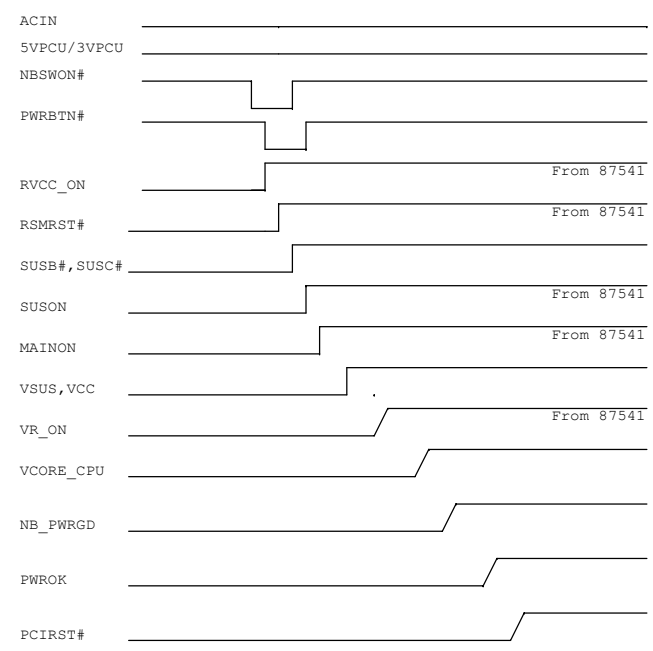
LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : VCC
 LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

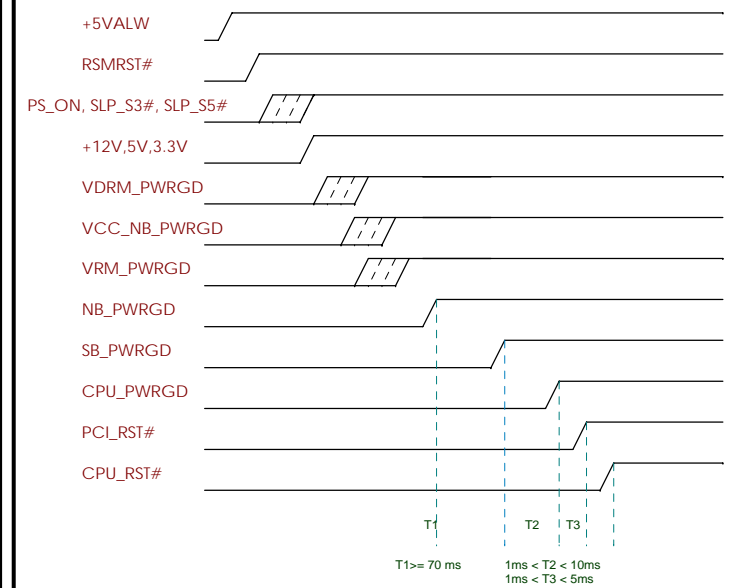
ES2 PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
R5C843	AD23	REQ0# / GNT0#	INT E/F/G

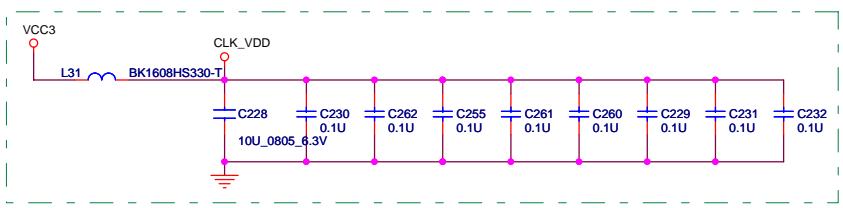
- Page 01: Block diagram
- Page 02: System information
- Page 03: Clock generator ICS951462
- Page 04: AMD S1 HT
- Page 05: AMD S1 DDR2
- Page 06: AMD S1 control&debug
- Page 07: AMD S1 power
- Page 08: DDR2 SODIMM X 2
- Page 09: DDR2 Termination
- Page 10: RS485M HT interface
- Page 11: RS485M PCIE interface
- Page 12: RS485M Sytem I/F & Clock Gen.
- Page 13: RS485M Power
- Page 14: SB460 PCIE/PCI/RTC/LPC/CPU/XTAL Interface
- Page 15: SB460 USB/ACPI/AZALIA/AC 97 Interface
- Page 16: SB460 SATA/PATA/HW Monitor/Power Interface
- Page 17: SB460 Straps
- Page 18: LCD PANEL
- Page 19: CRT
- Page 20: R5C843 PCI/1394 Interface
- Page 21: R5C843 PCMCIA/4 IN 1 Interface
- Page 22: PCI LAN RTL8101E/RJ45
- Page 23: FAN / MINI PCIE / 1-seg TV
- Page 24: LEDs / TP CONNECTOR
- Page 25: SATA HDD/PATA ODD Connector
- Page 26: CODEC ALC262 Mic/HP
- Page 27: Audio Amplifier MAX9789A
- Page 28: USB Connector/KeyBoard Connector
- Page 29: KBC PC87541/BIOS ROM
- Page 30: CPU CORE MAX8774
- Page 31: 3V/5V MAX8734
- Page 32: 1.2V SC470/1.5V/1.2V
- Page 33: 1.8V/0.9V TPS51116
- Page 34: Battery Charger MAX8724
- Page 35: Battery Connector

Power On Sequence

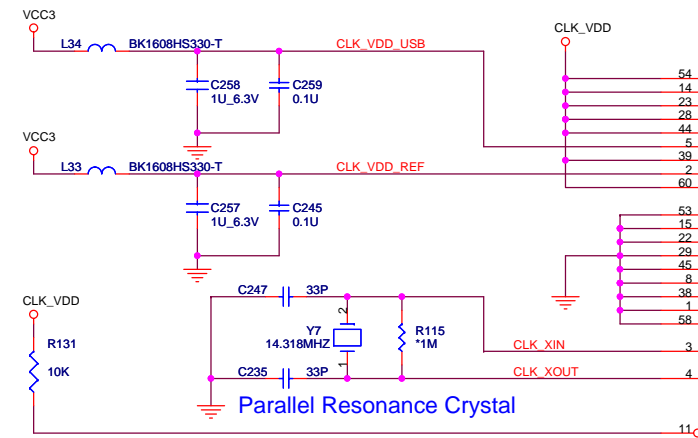
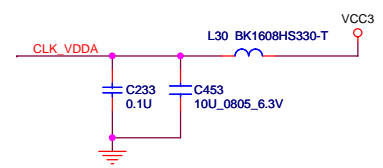


BONEFISH POWER UP SEQUENCE

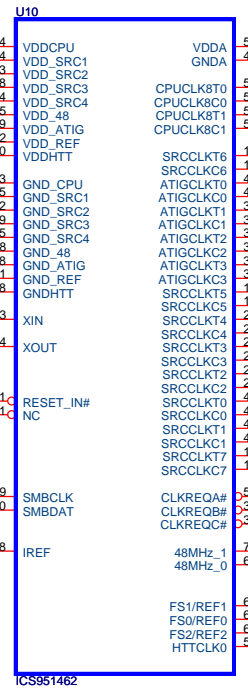
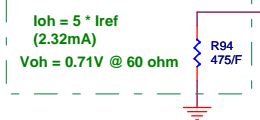
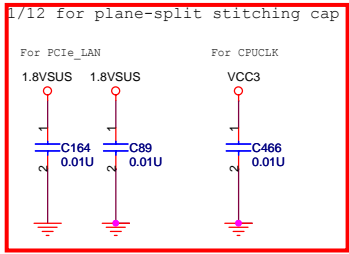




Put Decoupling Caps close to Clock Fen. power pin



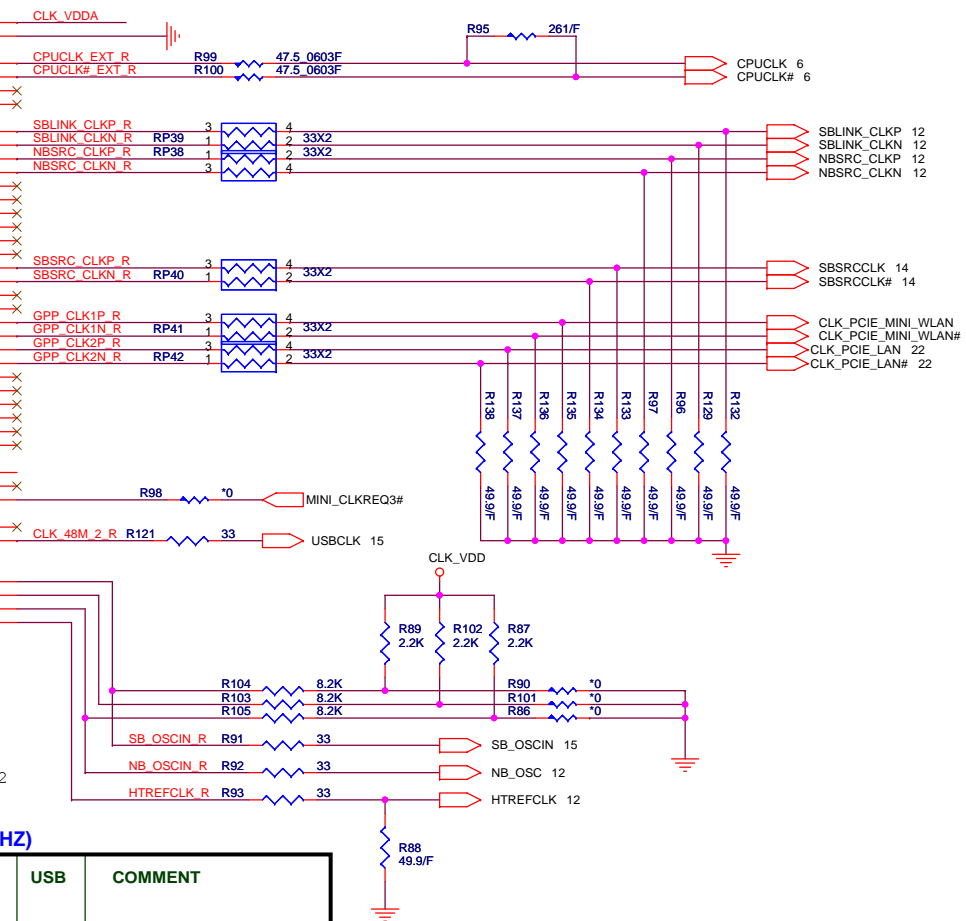
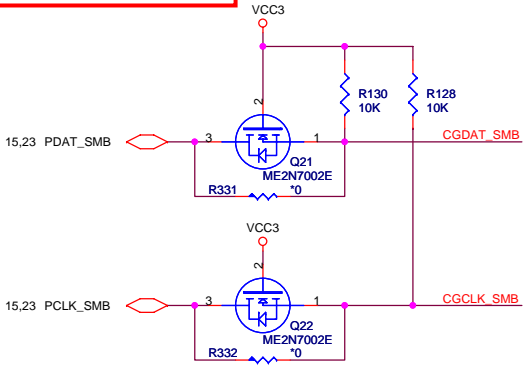
Parallel Resonance Crystal

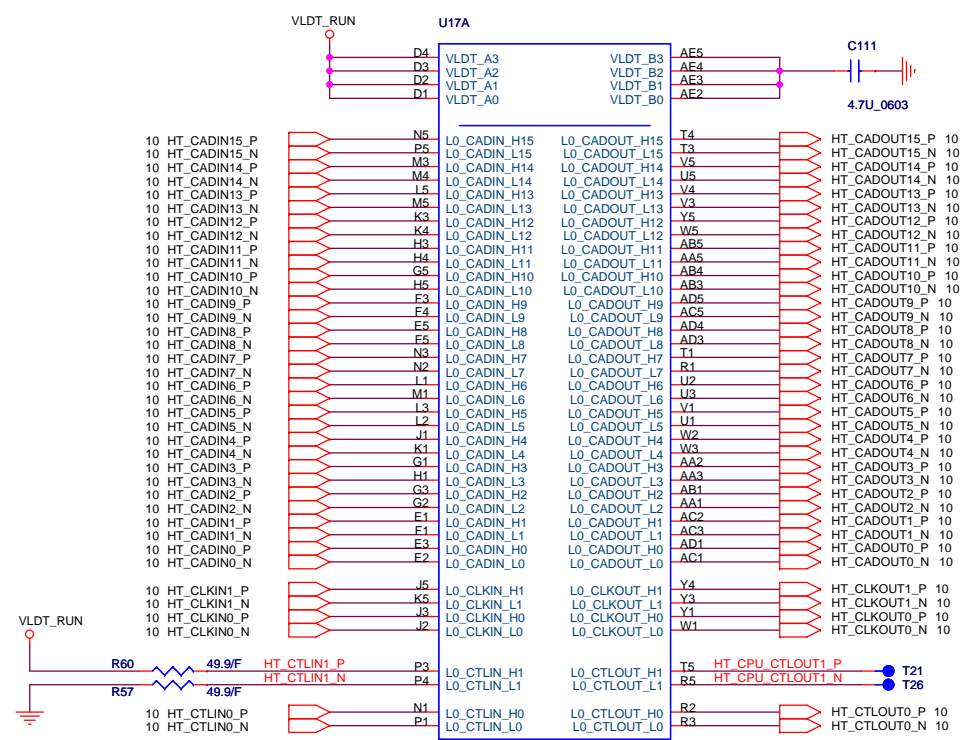


CLKREQA# CONTROL SRC5,6,7
 CLKREQB# CONTROL SRC2,3,4 ATIG3
 CLKREQC# CONTROL SRC0,1 ATIG0,1,2

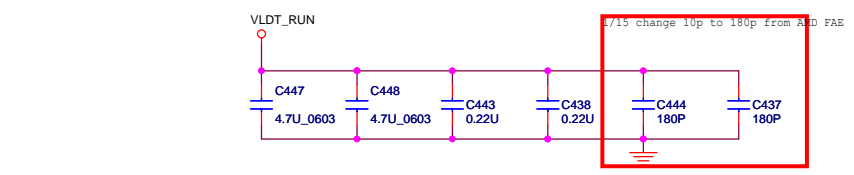
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

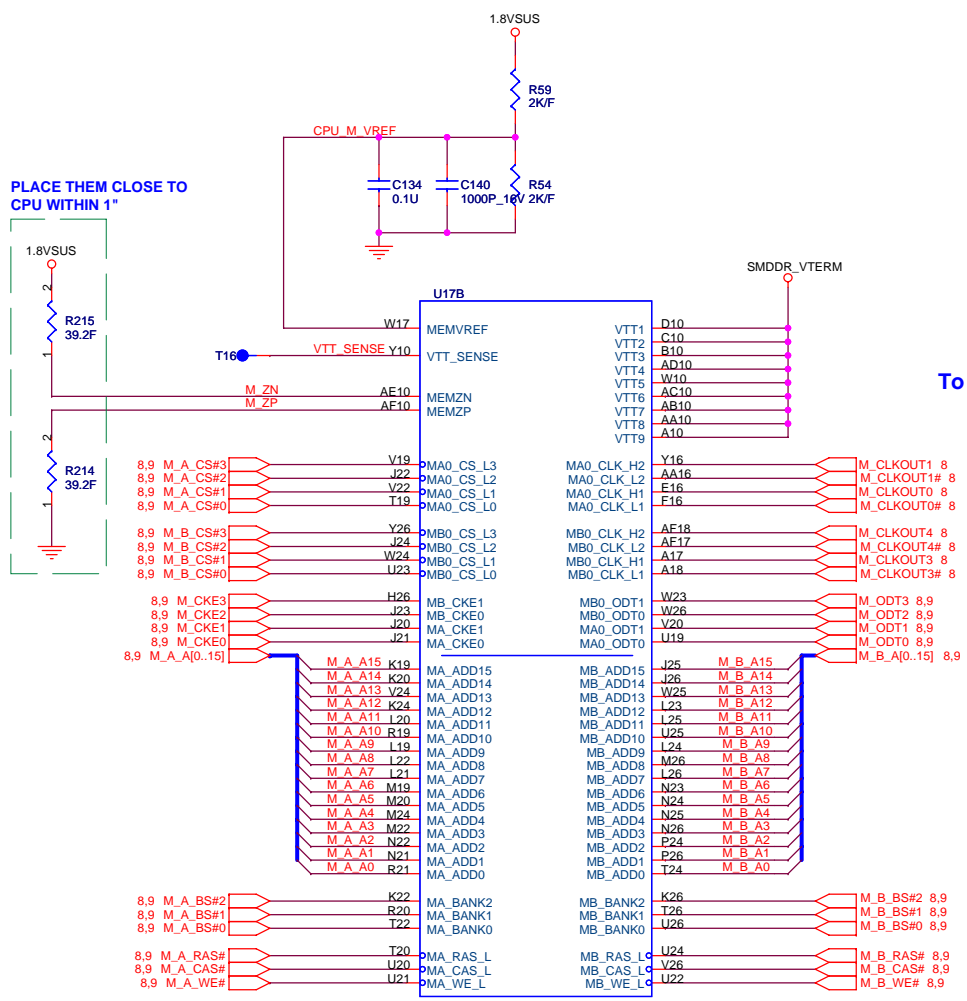




Athlon 64 S1 Processor Socket



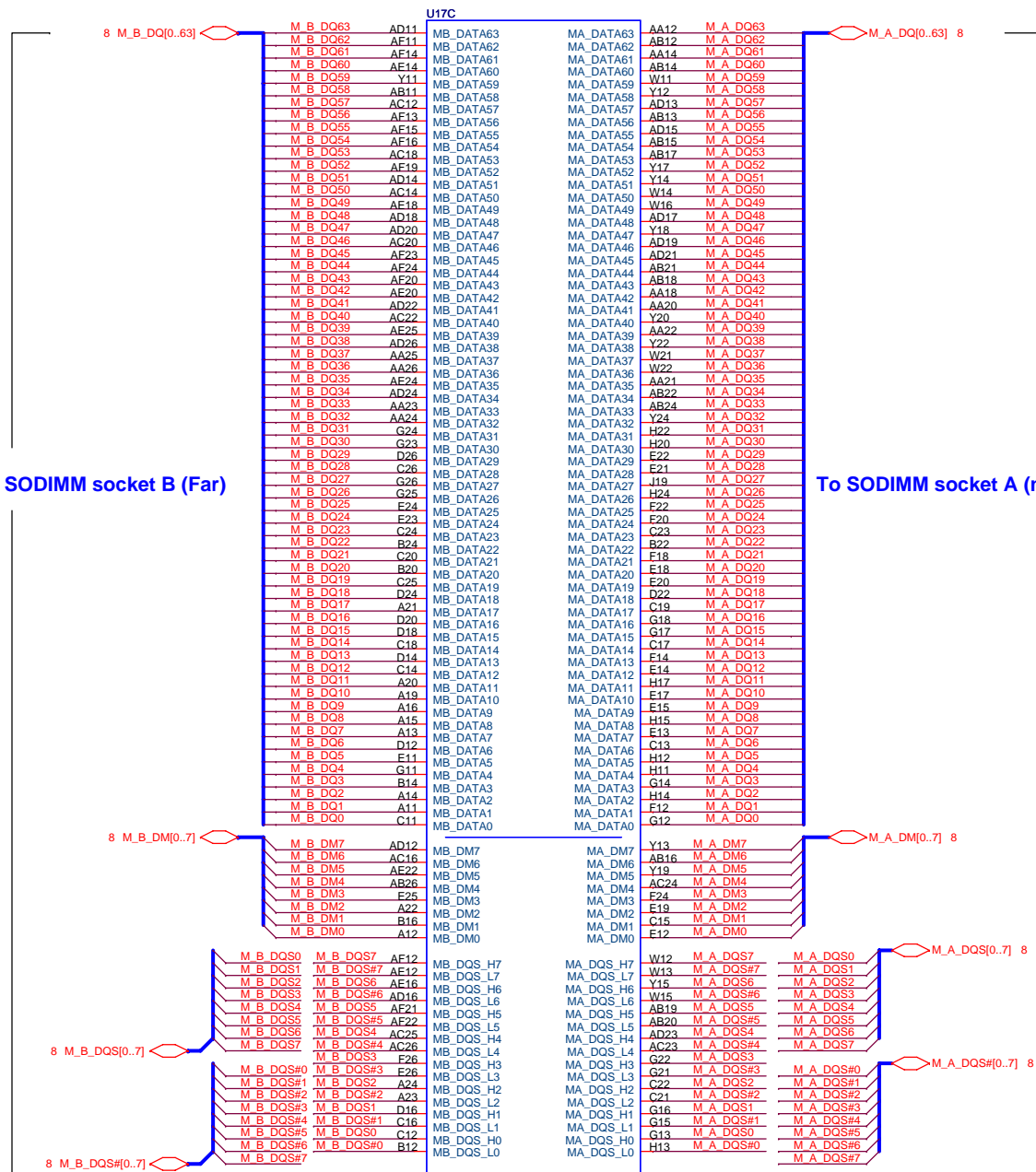
Processor DDR2 Memory Interface



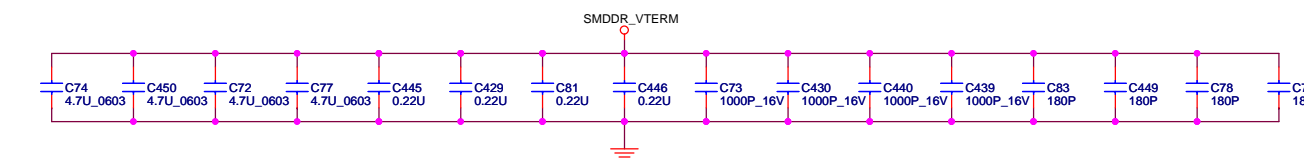
DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

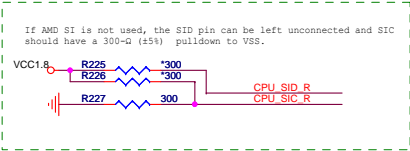
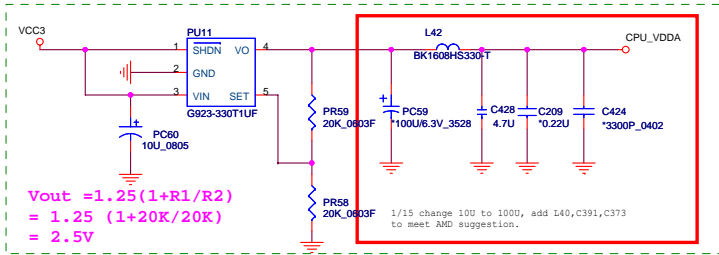
To SODIMM socket B (Far)

To SODIMM socket A (near)

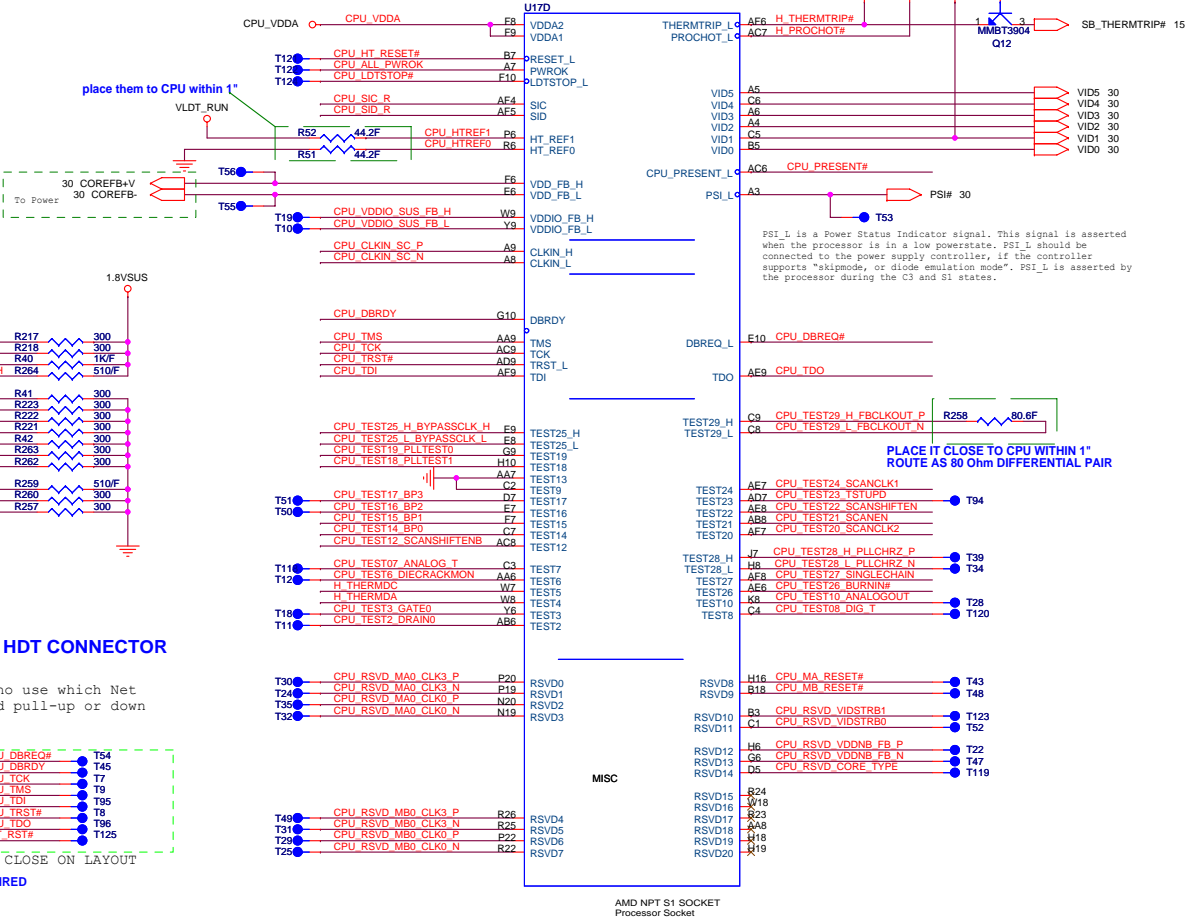
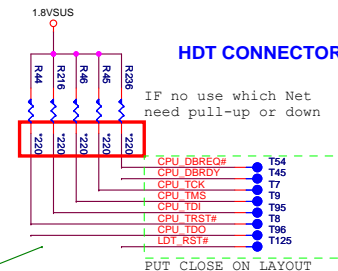
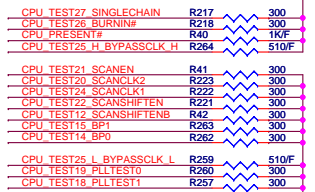
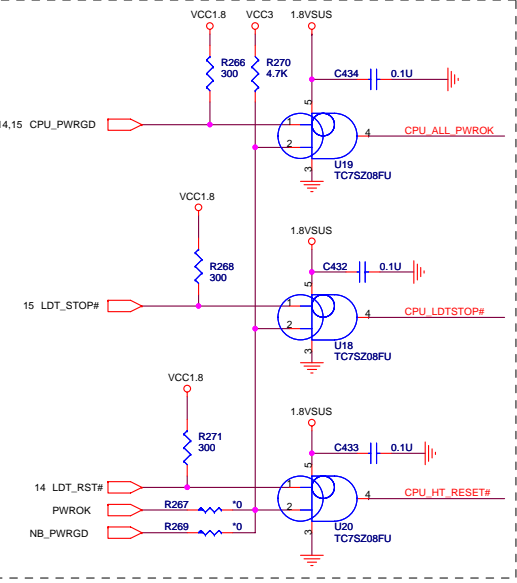
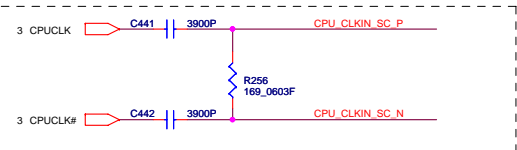


DDR: DATA
Athlon 64 S1
Processor Socket

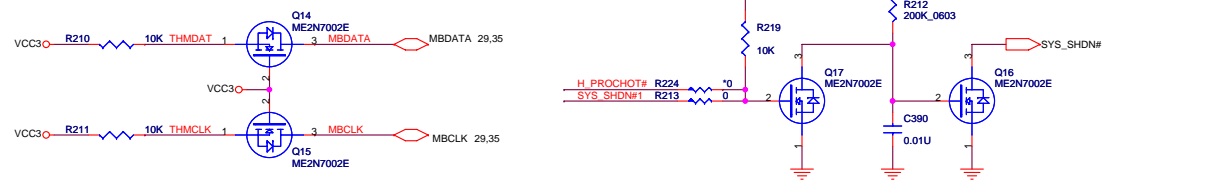
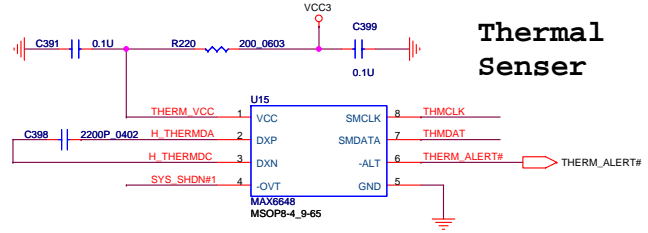


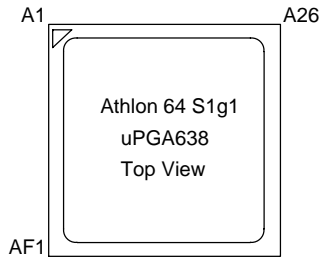
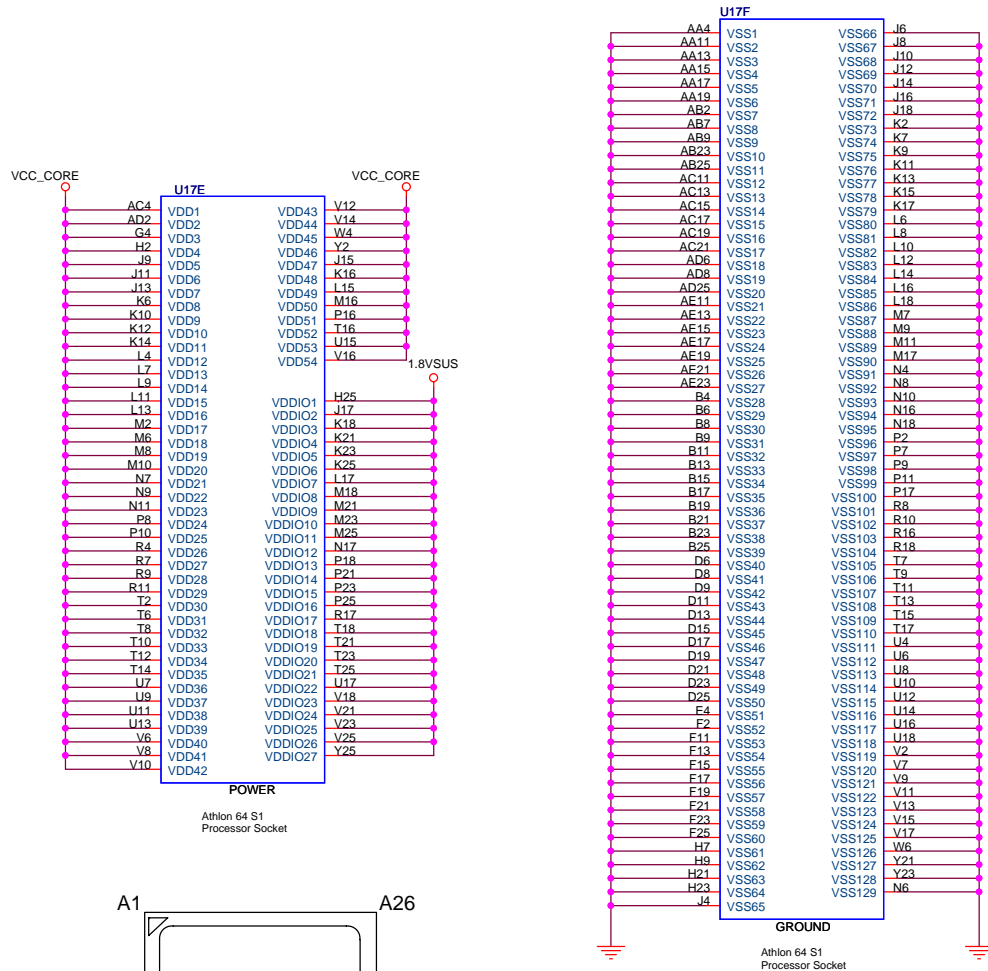


ATHLON Control and Debug



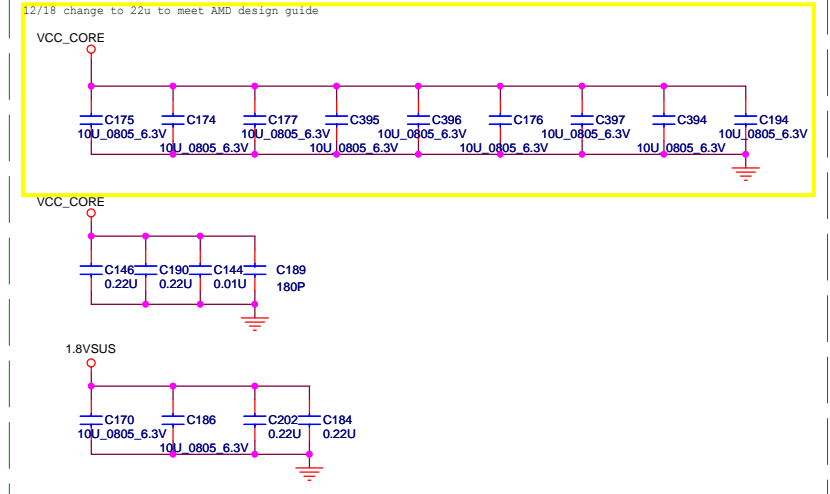
Thermal Sensor



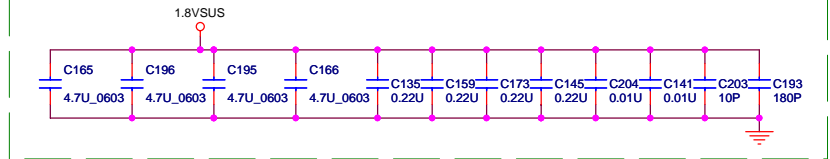


Turion64 X2 TL-50 Rev.F2 (TMDTL50HAX4CT) AJDTL50VG26
Sempron-64 Single core Rev.F2 (SMS3200HAX4CM) AJ03200VG11

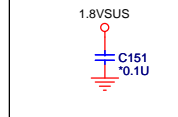
BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE

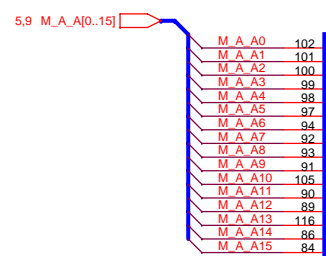


1/22 add 0.1u cap between DR2 and CPU for EMI

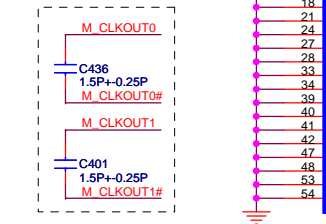
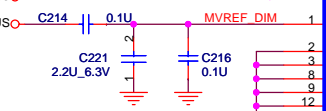
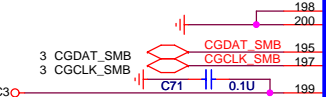
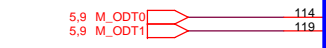
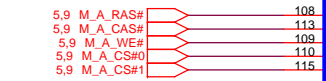
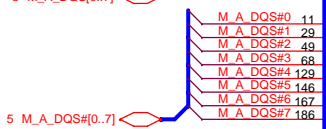
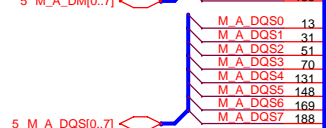
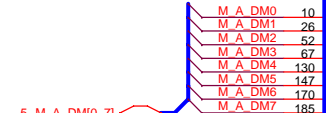


1.8VSUS

1.8VSUS

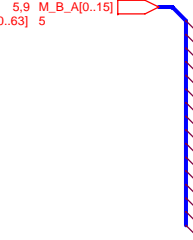


CN10
REVERSE

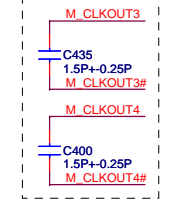
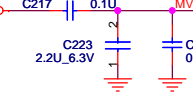
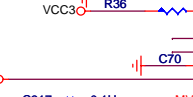
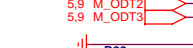
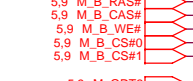
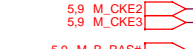
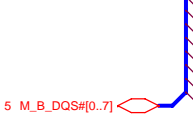
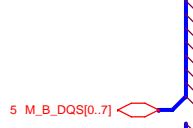
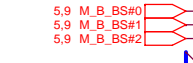


SO-DIMM
(H=5.2)

(H=5.2)

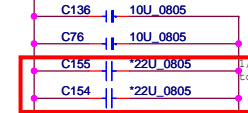
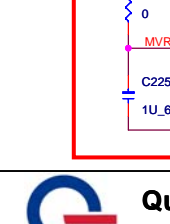
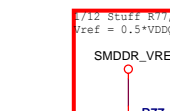
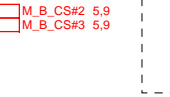
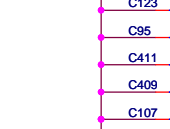
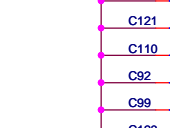
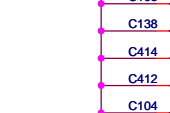
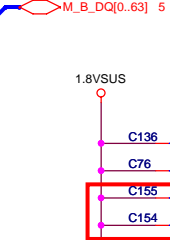
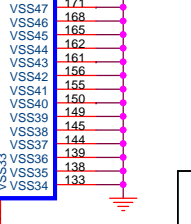
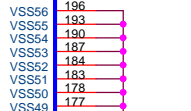
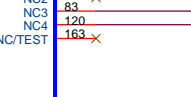
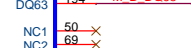
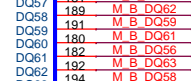
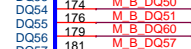
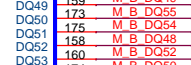
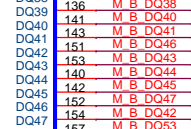
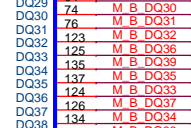
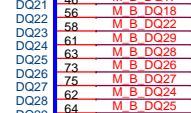
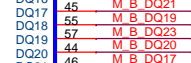
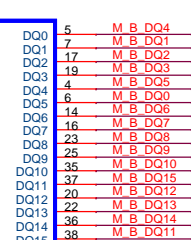
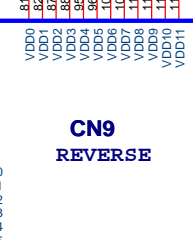


CN9
REVERSE

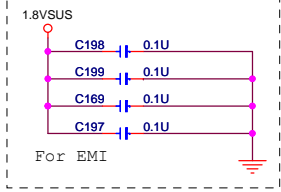
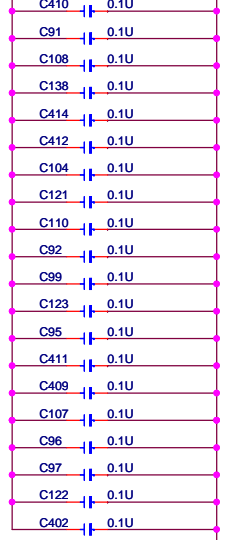


SO-DIMM
(H=9.2)

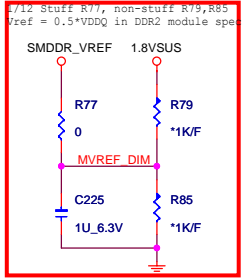
(H=9.2)



U15 change 10p to 22p to meet AMD suggestion



For EMI



7/12 Stuff R77, non-stuff R79,R85
Vref = 0.5*VDDQ in DDR2 module spec

DDR1I_SODIMM_R

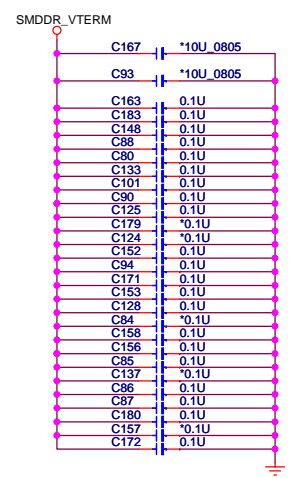
DDR1I_SODIMM_R

1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

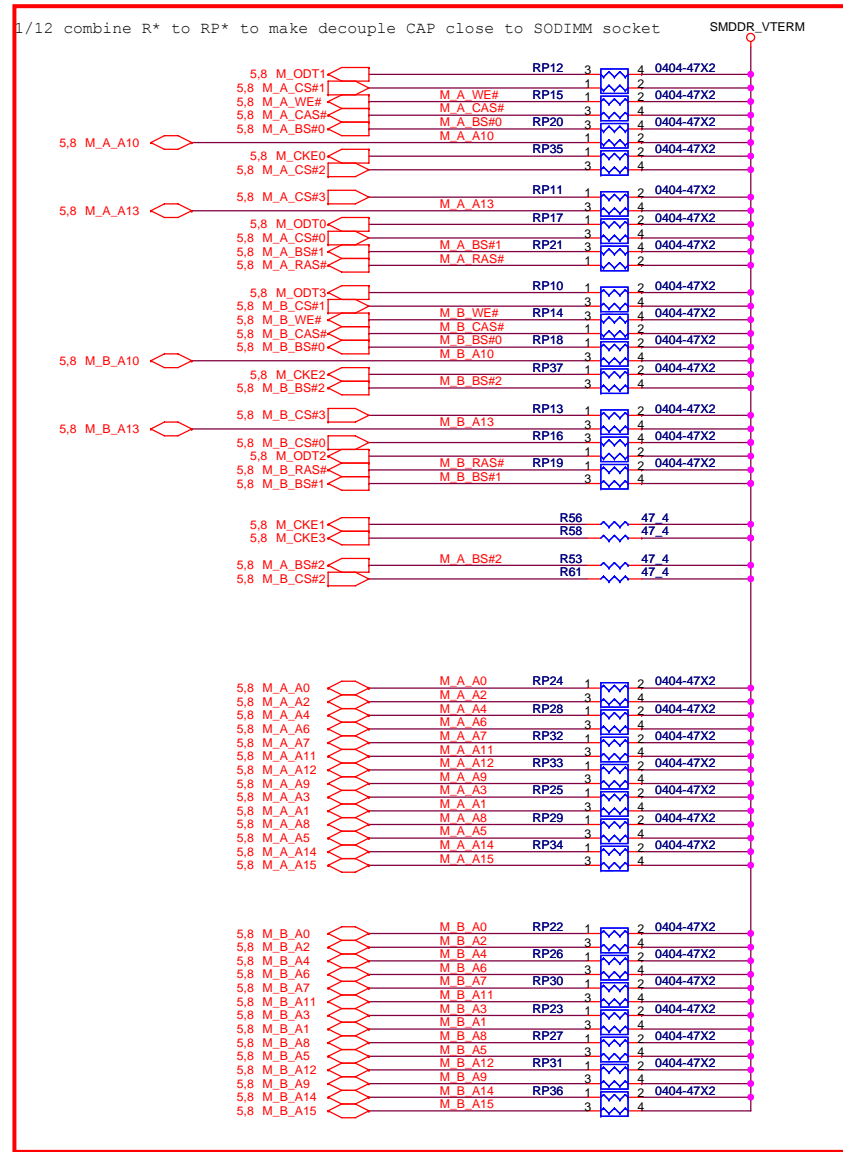
Quanta Computer Inc.
PROJECT : ES2

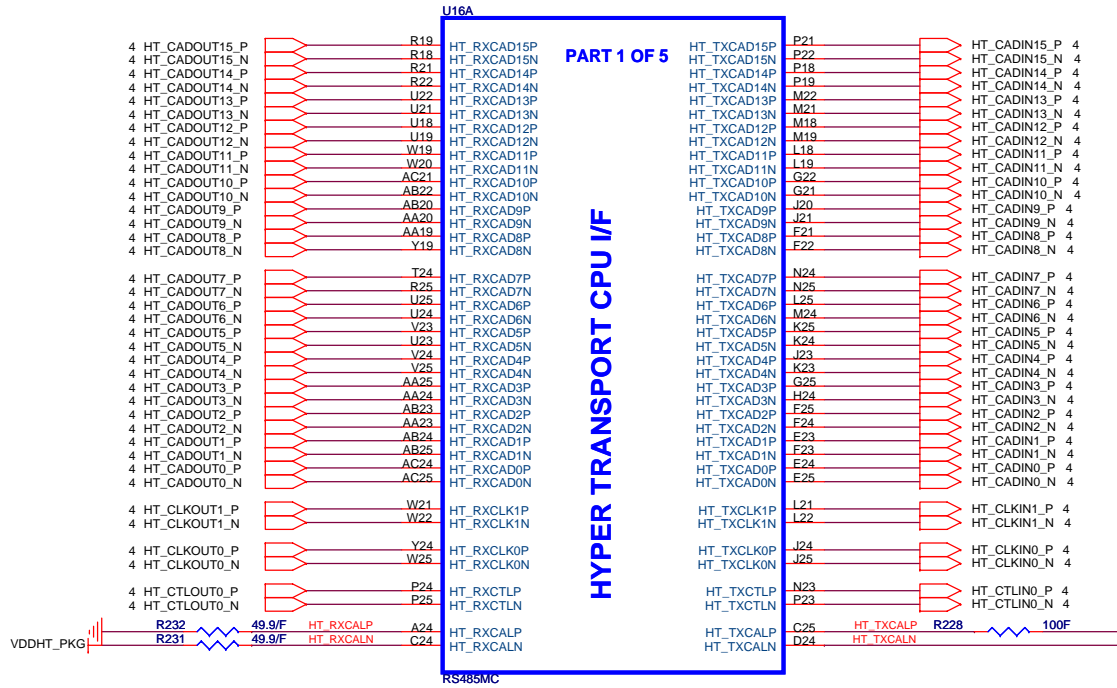
Size	Document Number	Rev D
	DDR1I SODIMMx2	
Date:	Thursday, May 24, 2007	Sheet 8 of 35

1/12 combine R* to RP* to make decouple CAP close to SODIMM socket SMDDR_VTERM

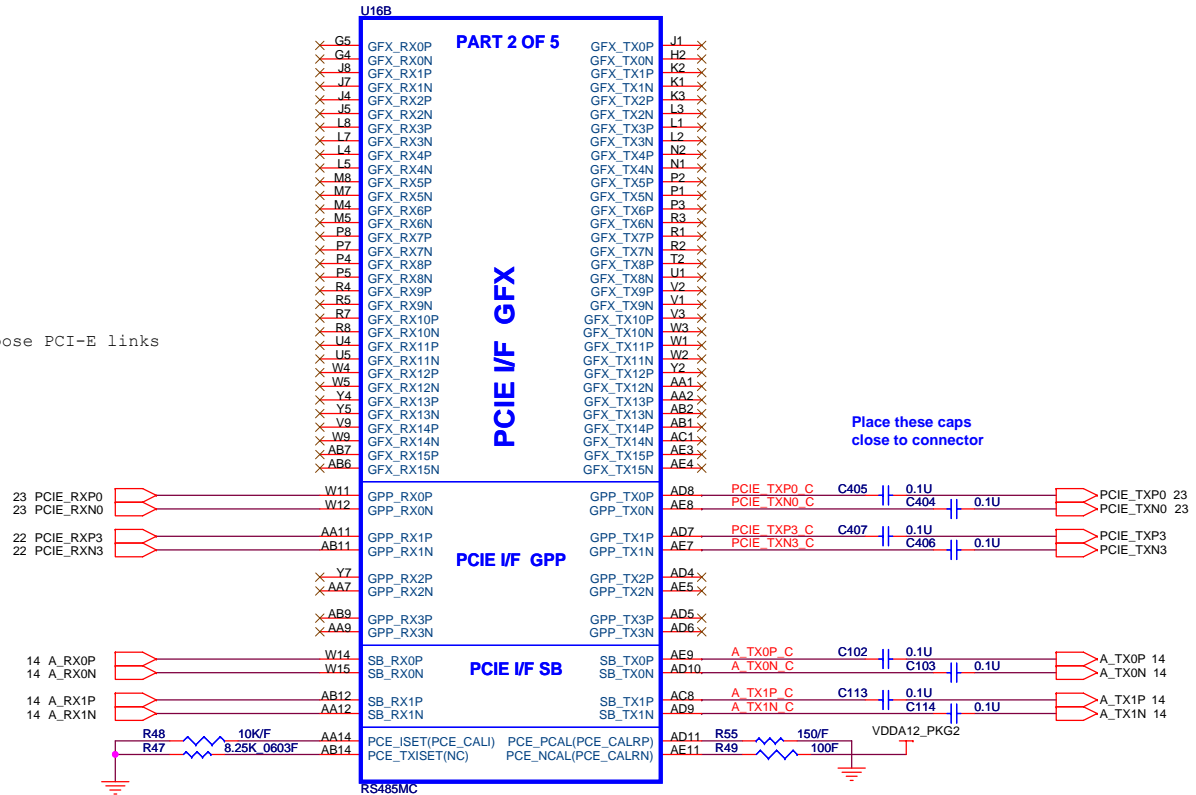


1/22 there is no layout space for decouple cap between 1.8VSUS and SMDDR_VTERM.



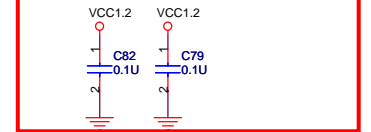


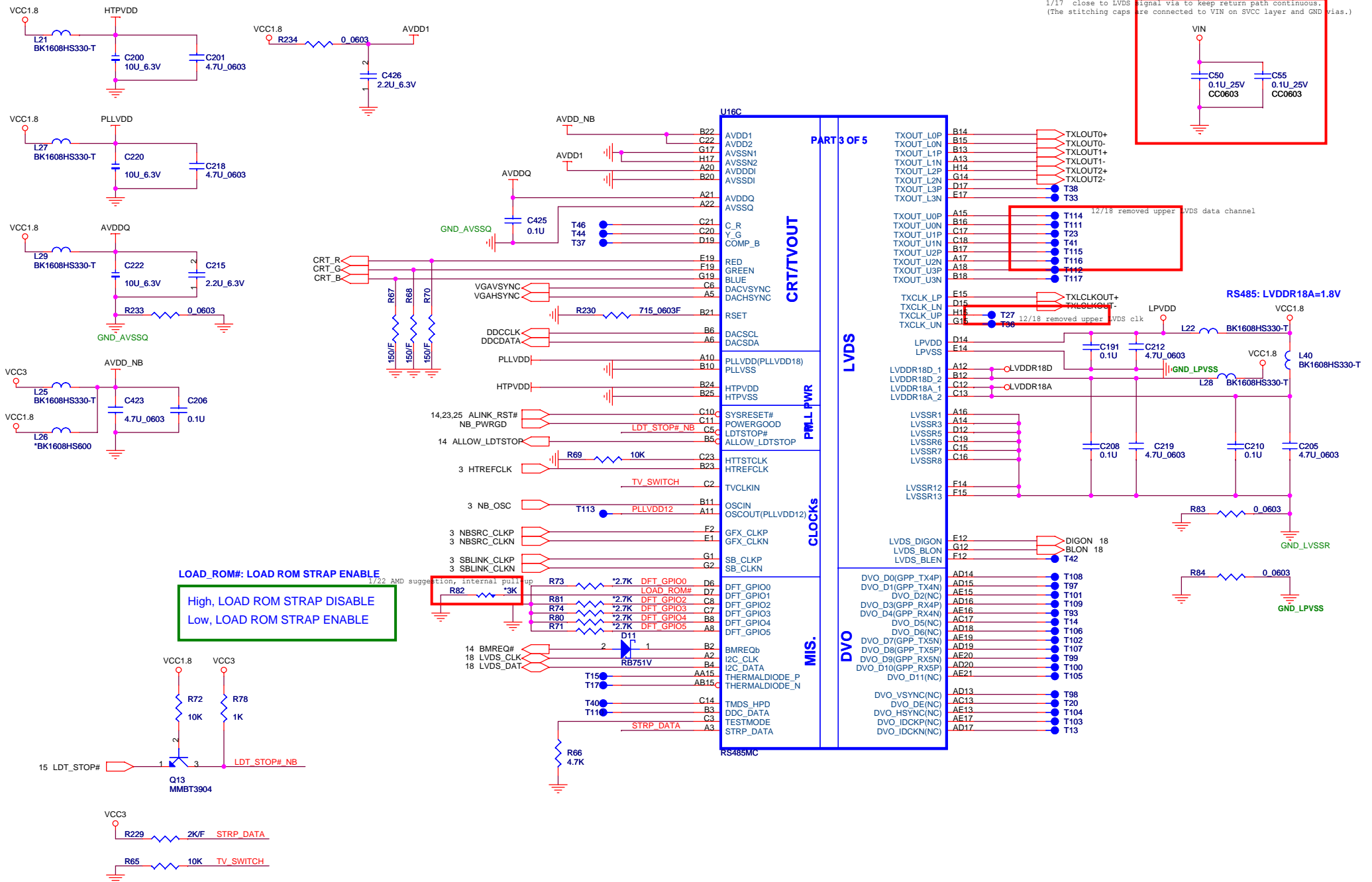
RS485MC only support two general purpose PCI-E links
 GPP_TX[0:1]P GPP_RX[0:1]P
 GPP_TX[0:1]N GPP_RX[0:1]N



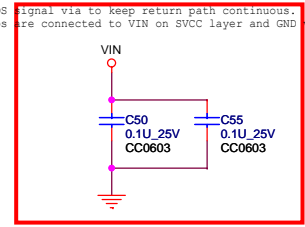
Place these caps close to connector

I/17 SI : PCIE_TXP3/N3, PCIE_RXP3/N3 change layer

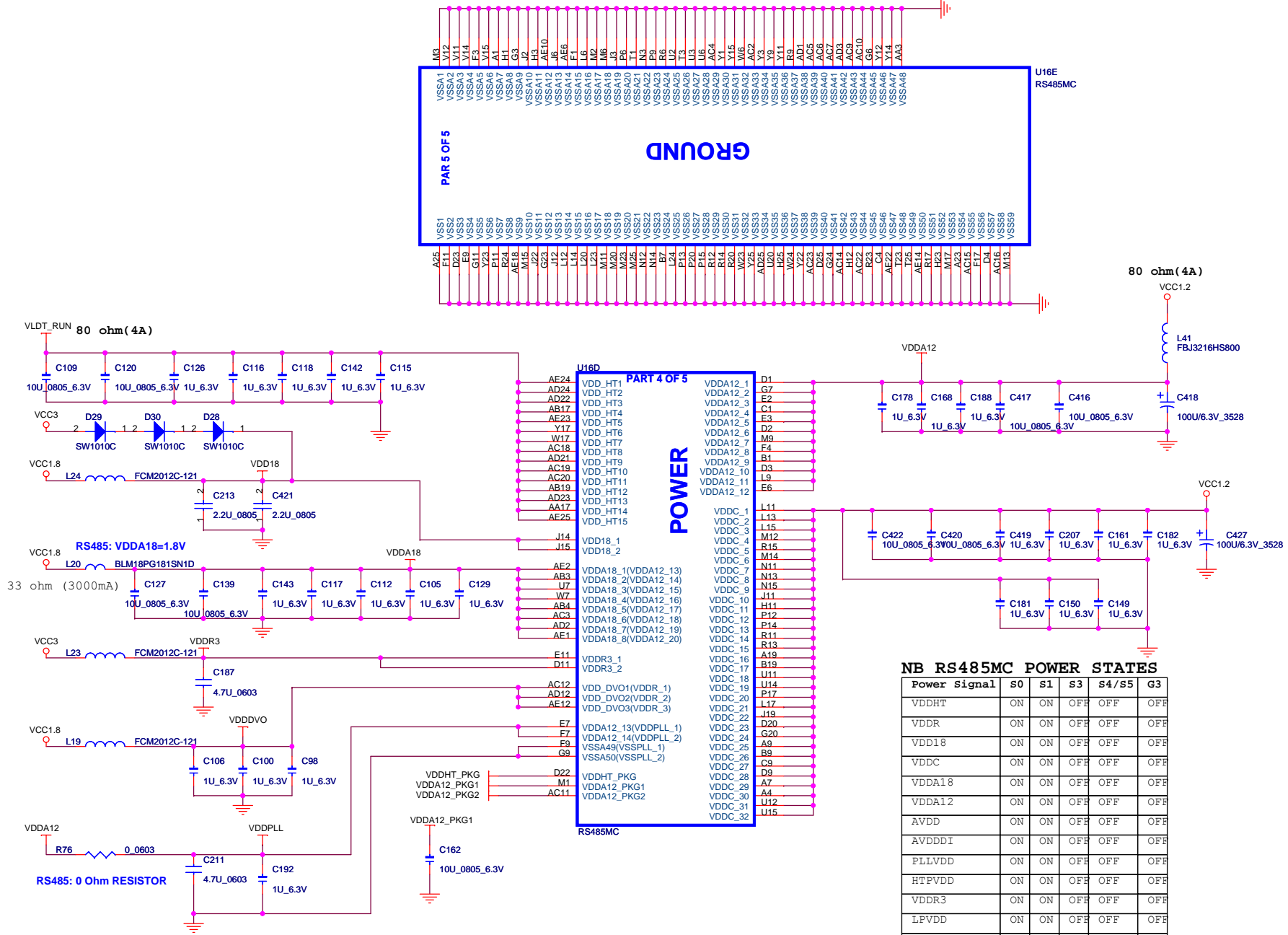




1/17 close to LVDS signal via to keep return path continuous. (The stitching caps are connected to VIN on SVCC layer and GND vias.)

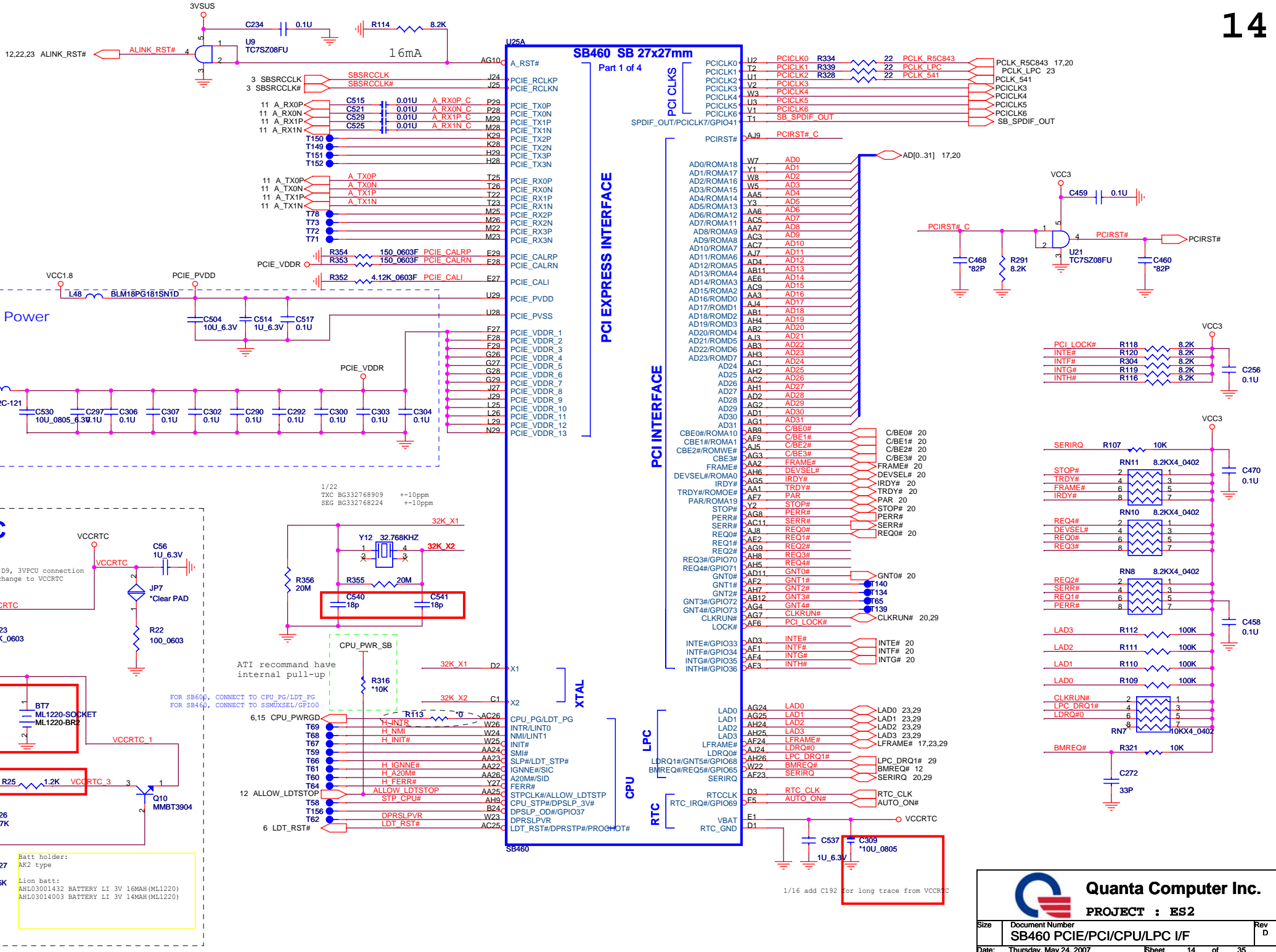


LOAD_ROM#: LOAD ROM STRAP ENABLE
 High, LOAD ROM STRAP DISABLE
 Low, LOAD ROM STRAP ENABLE

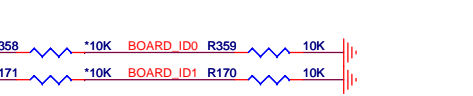
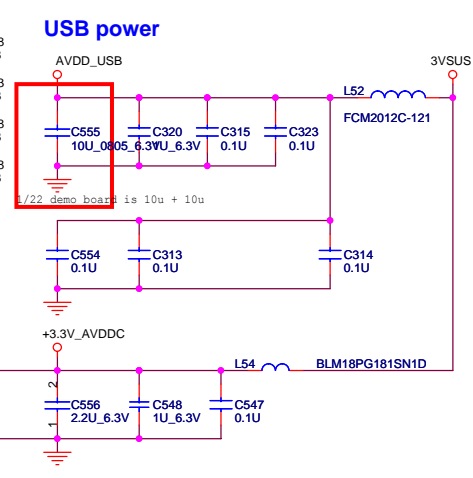
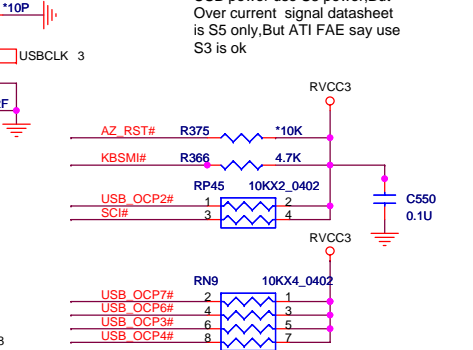
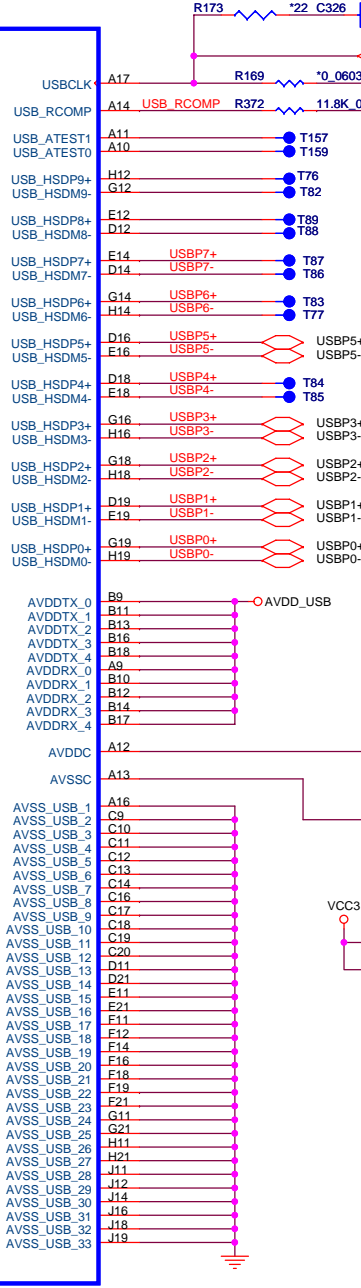
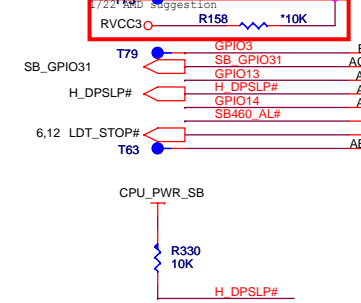
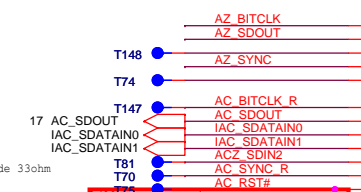
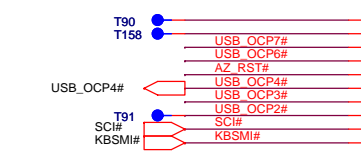
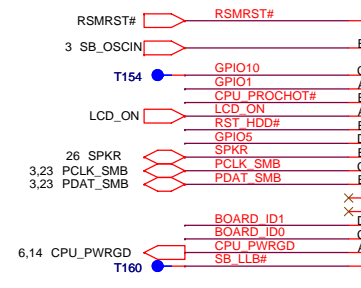
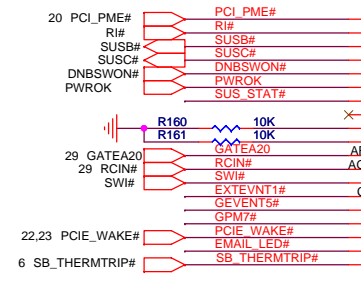
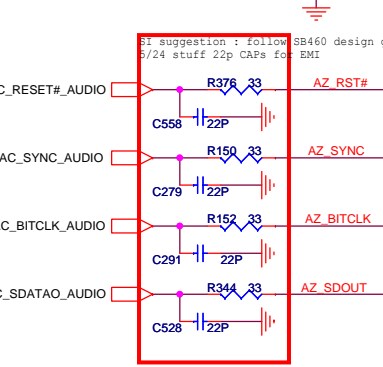
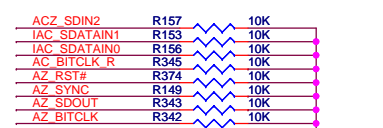
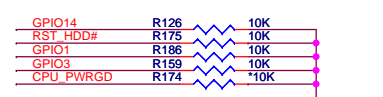
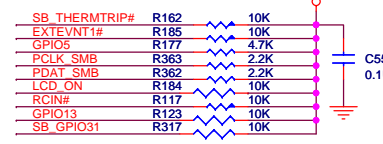
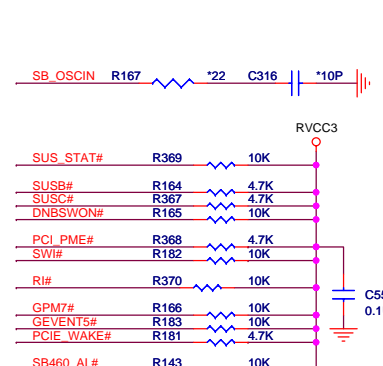
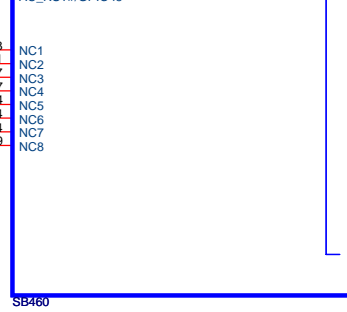
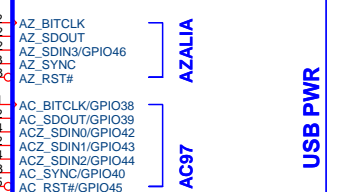
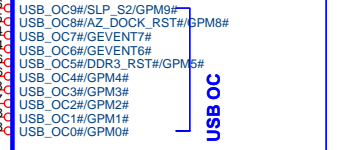
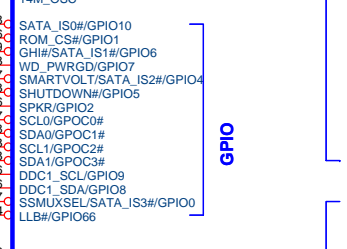
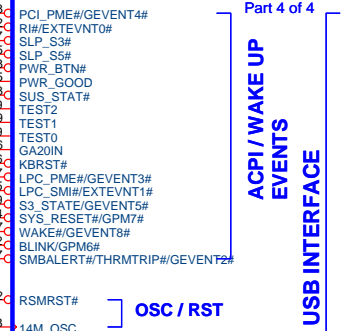


NB RS485MC POWER STATES

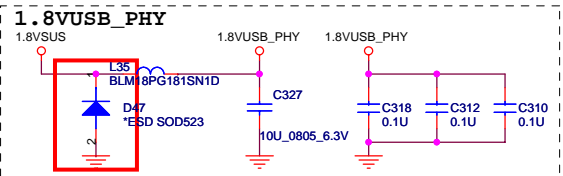
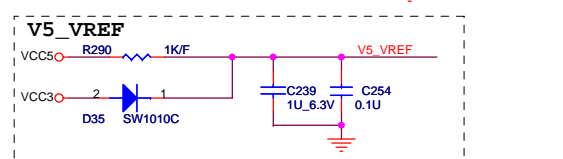
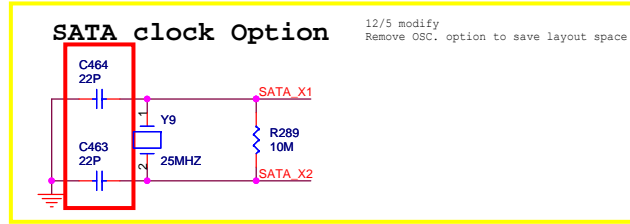
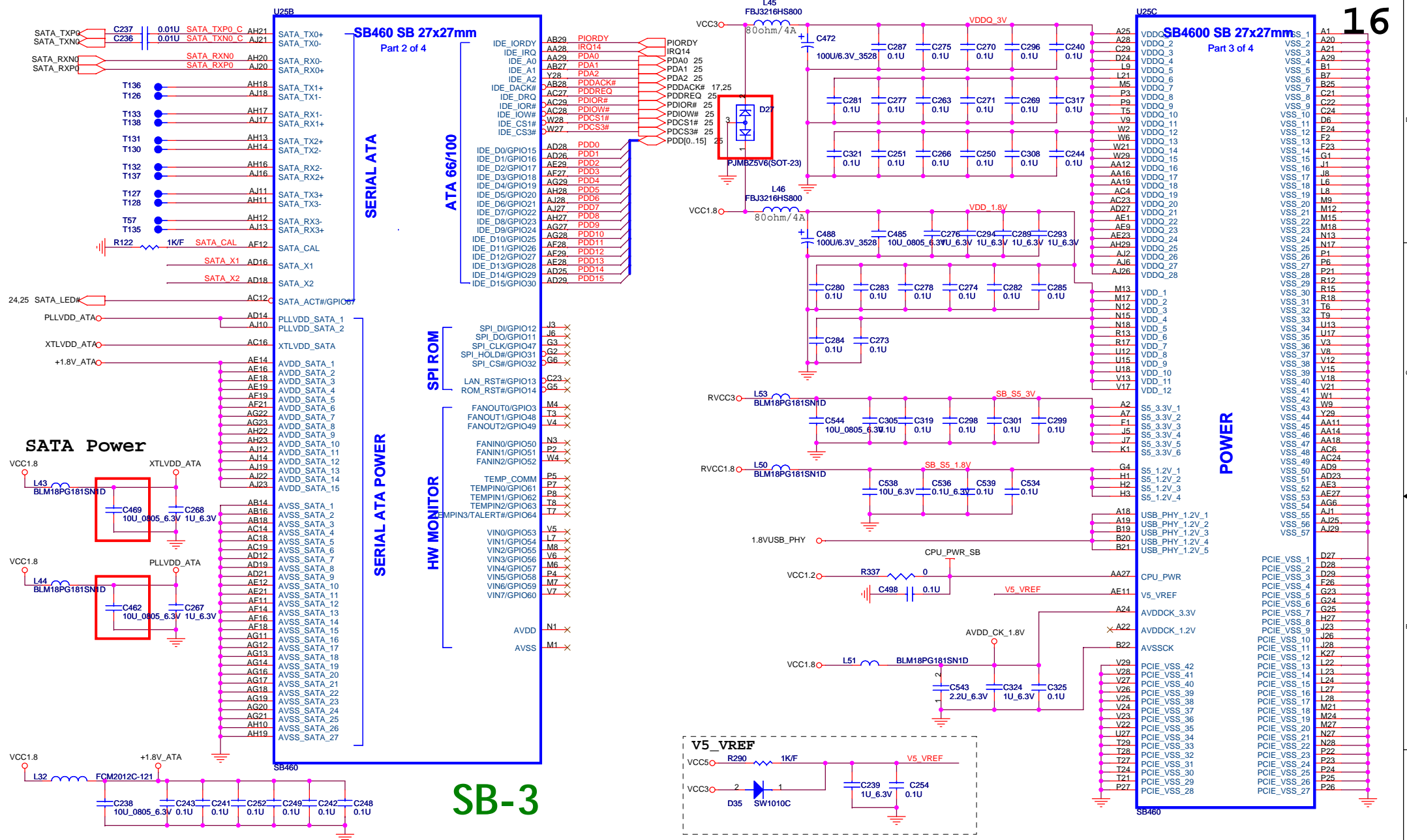
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



SB460 SB 27x27mm

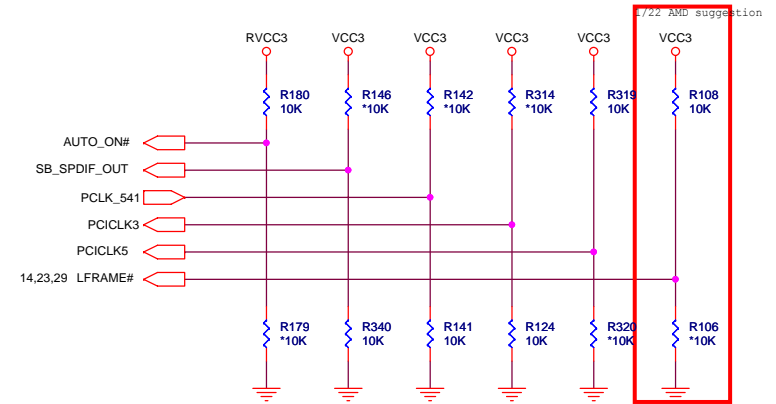
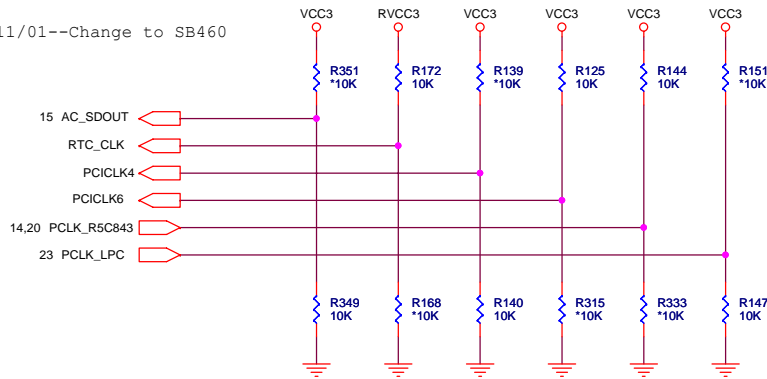


USB power use S3 power, But Over current signal datasheet is S5 only, But ATI FAE say use S3 is ok



REQUIRED STRAPS

Edison-11/01--Change to SB460

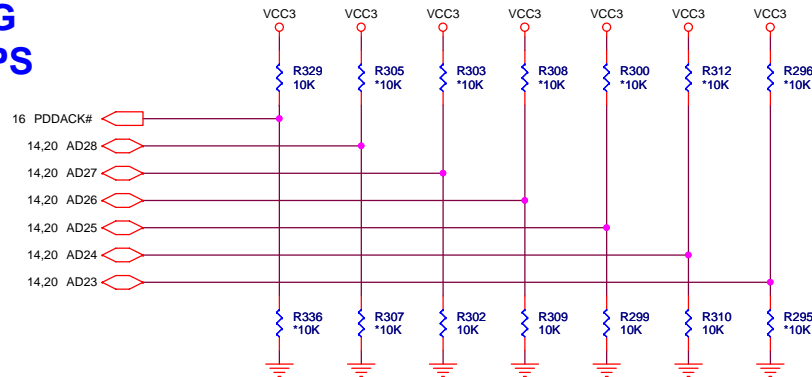


				PCLK_R5C843	PCLK_LPC
PULL HIGH	AC_SDOUT	RTC_CLK	PCICLK4	PCICLK6	PCI_CLK0
	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT


		AUTO_ON#	SB_SPDIF_OUT	PCLK_541	PCICLK3	PCICLK5	LFRAME#
PULL HIGH	ACPWON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#	
	MANUAL PWR ON	SIO 24MHz	XTAL MODE	USB PHY POWERDOWN DISABLE	PCIE_CM_SET LOW	ENABLE THERMTRIP#	
PULL LOW	AUTO PWR ON	SIO 48MHz	48MHZ OSC MODE	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	

BIOS ENABLE AFTER STARTUP

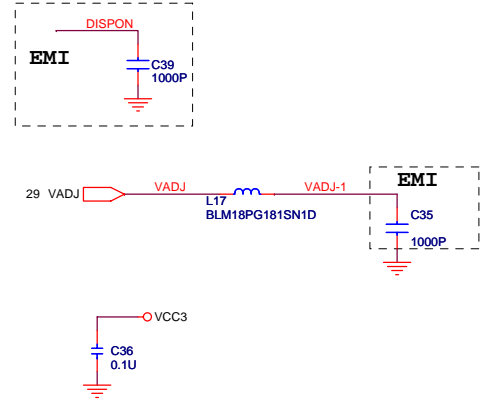
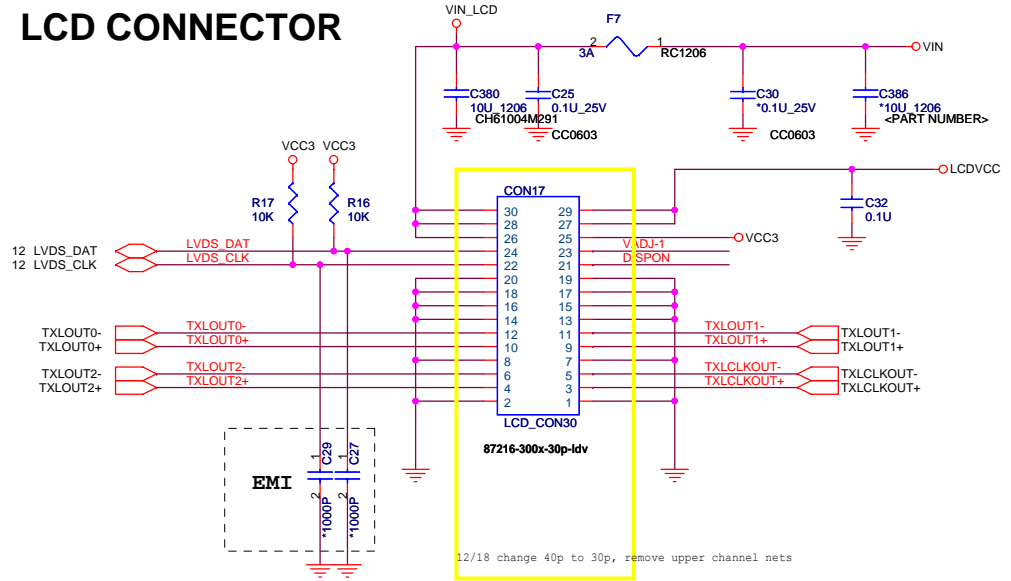
DEBUG STRAPS



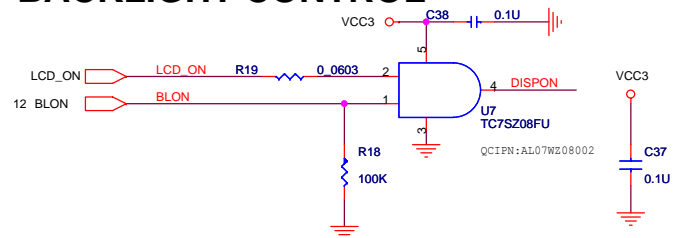
		PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	
	USE SHORT RESET		USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS		
	DEFAULT		DEFAULT	DEFAULT	DEFAULT	DEFAULT		


Quanta Computer Inc.
 PROJECT : ES2
 Size Document Number
SB460 STRAPS
 Date: Thursday, May 24, 2007 Sheet 17 of 35 Rev D

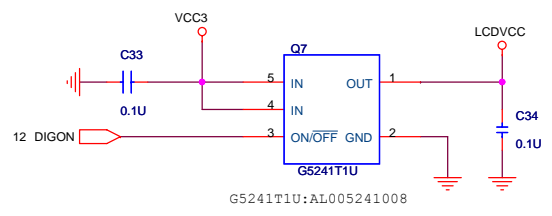
LCD CONNECTOR



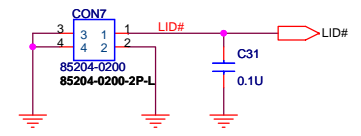
BACKLIGHT CONTROL



PANEL VCC CONTROL



LID

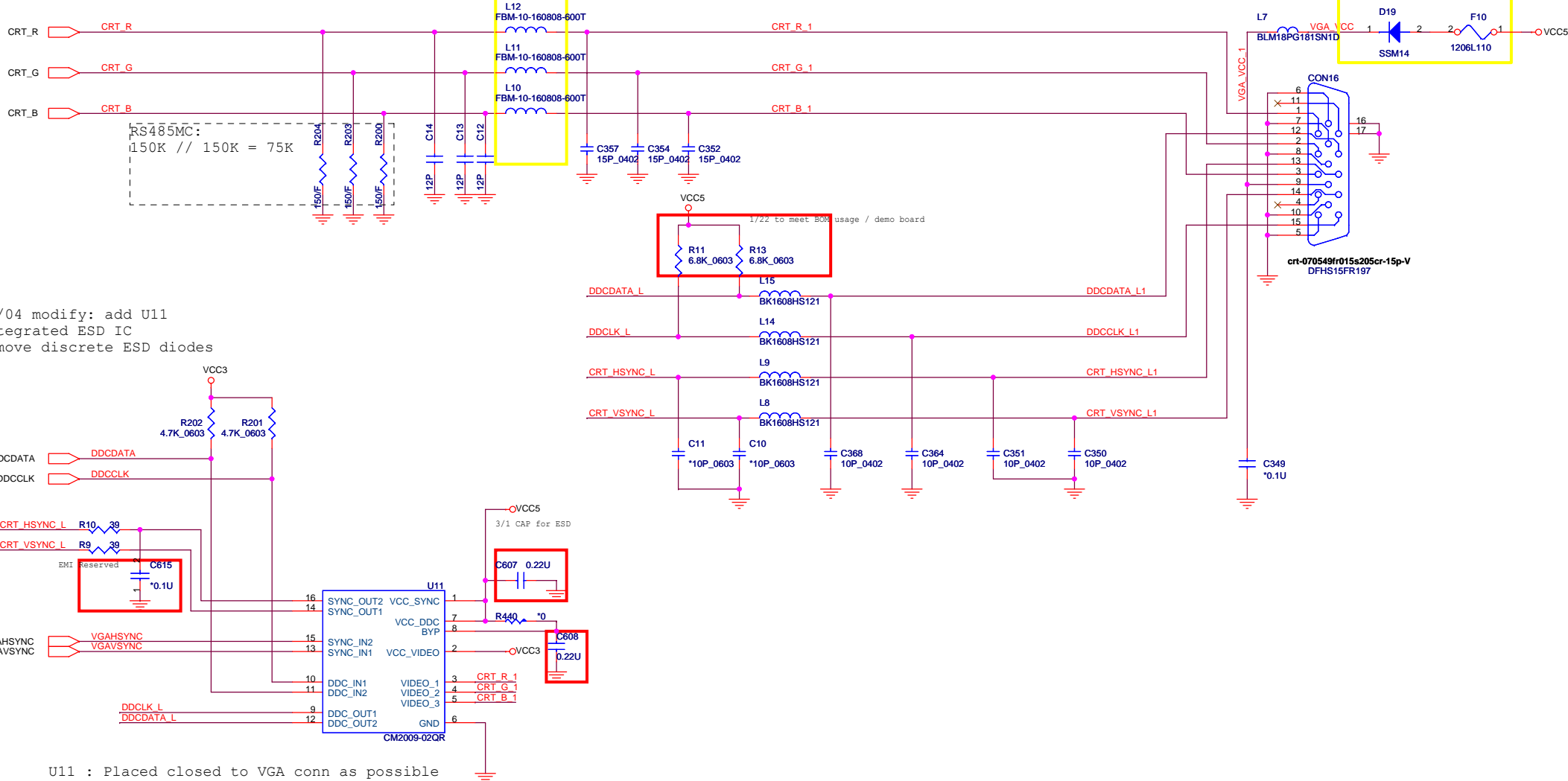


CRT

12/8 modify
 CX00070B08 MLB-160808-0070B-N3 OBS
 CX08B75001 TB160808B750 (75 Ohm BQ2A)
 CX80860001 KCE#FBM-10-160808-600T(60 ohm) - current use (PL1)

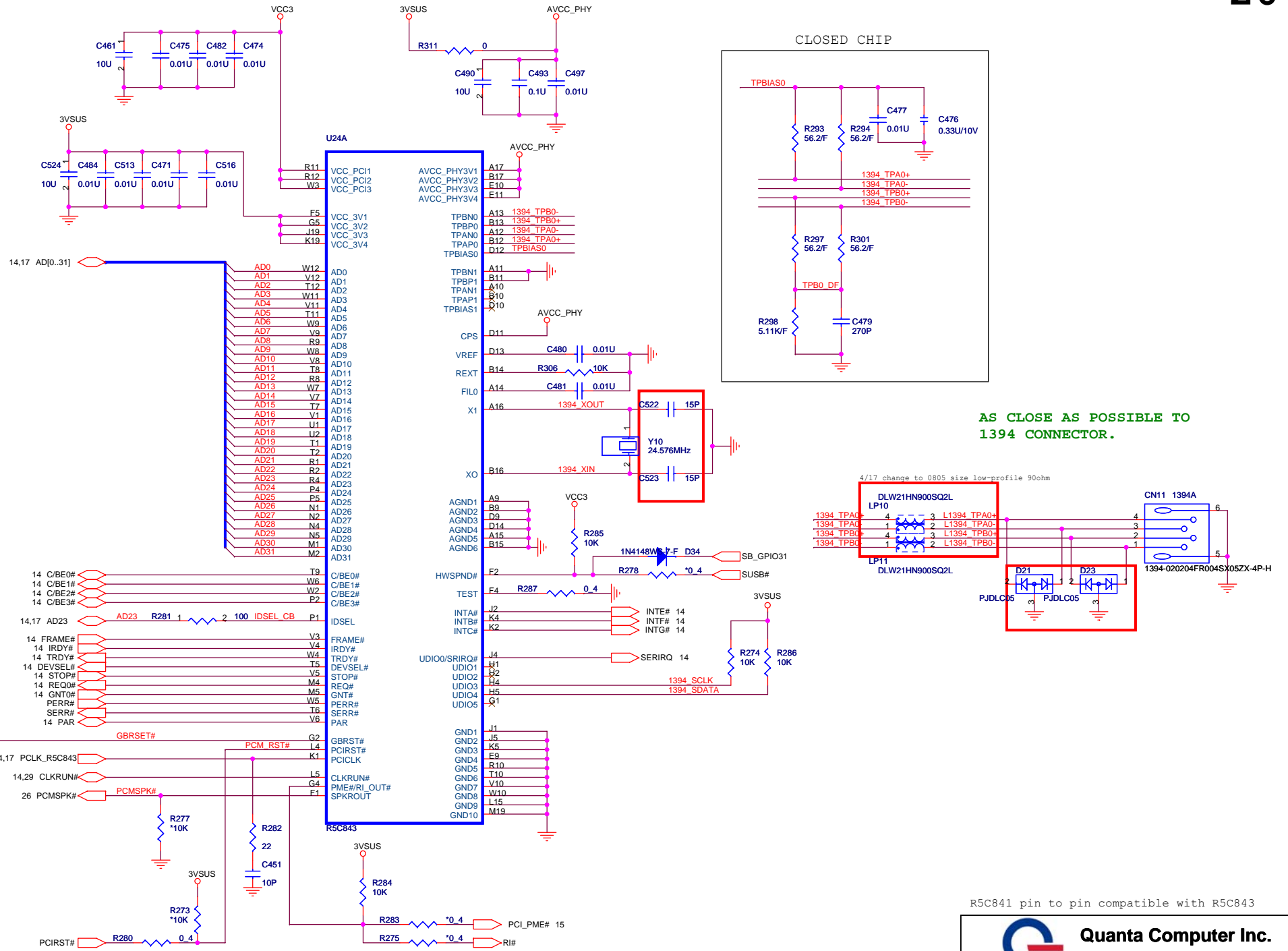
12/5 modify F10
 DK110TPU110 - SMD1812P110TF(KW3S) to
 DK200TFU101 (littlefuse)
 1812 to 1206

 D19
 KW3SBC1SS355Z051SS355 (80V,100MA) to
 PL1BC0SSM14Z30SSM14PT(40V,1A)



12/04 modify: add U11
 Integrated ESD IC
 Remove discrete ESD diodes

U11 : Placed closed to VGA conn as possible



AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

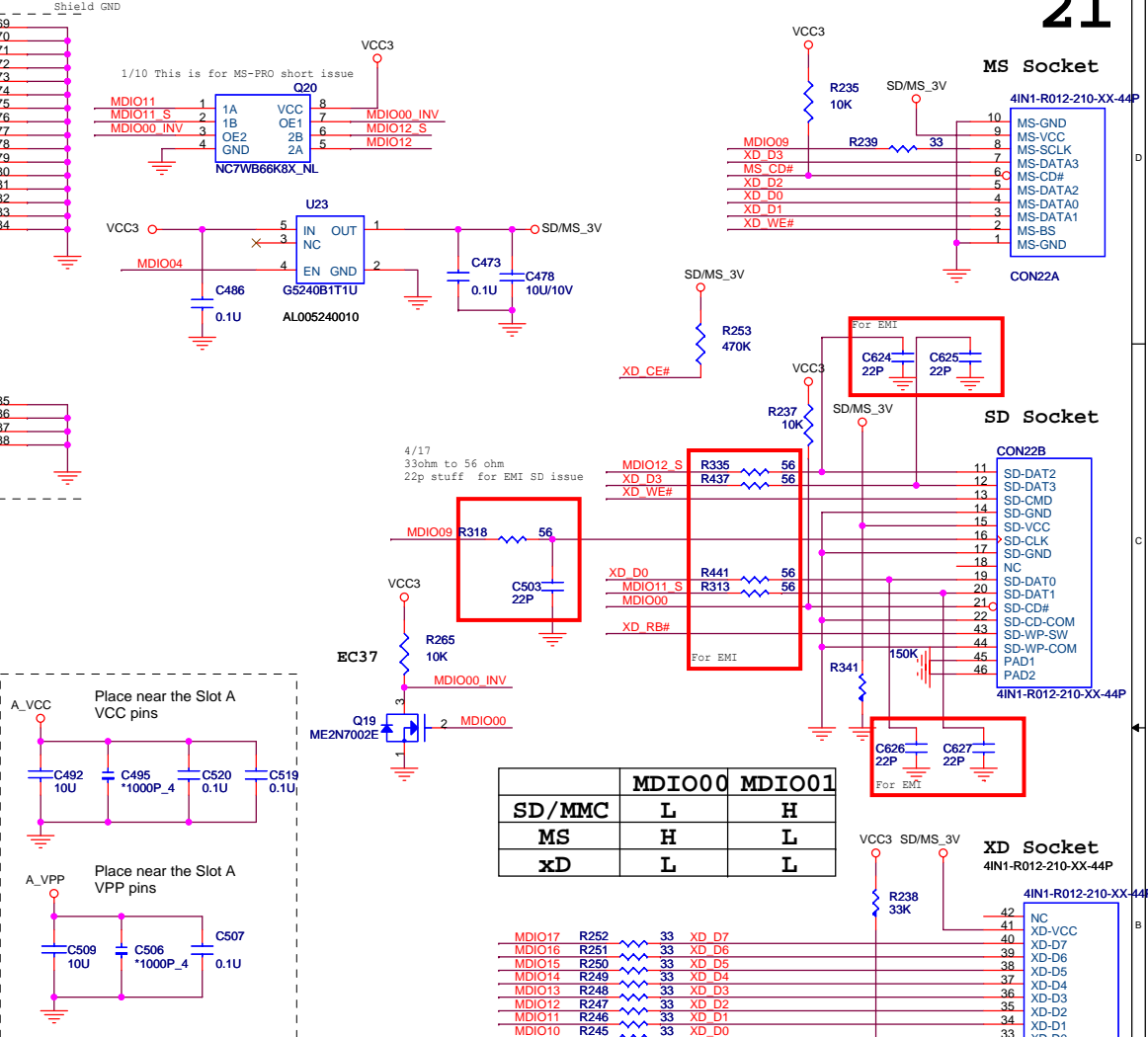
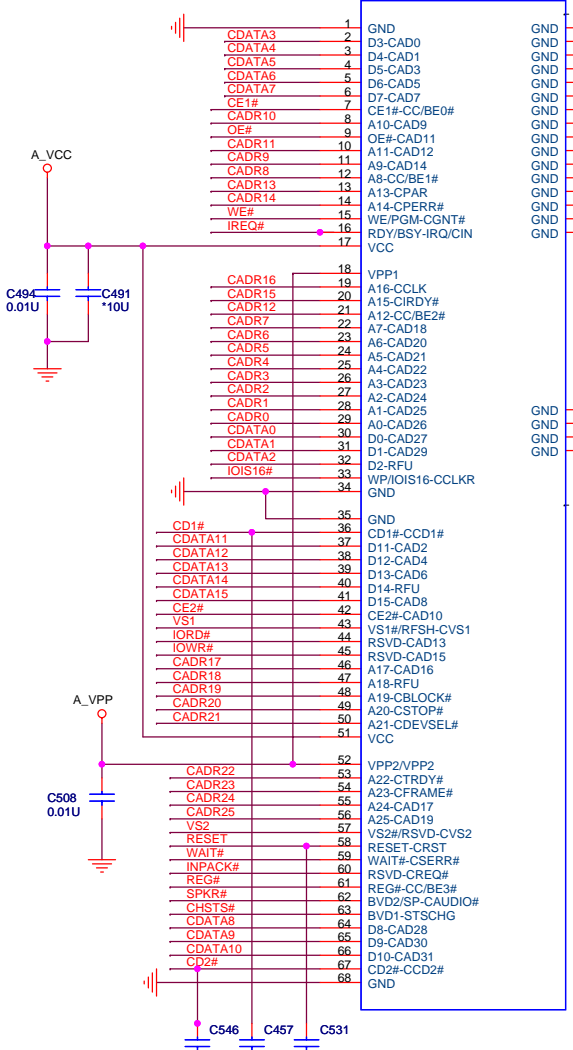
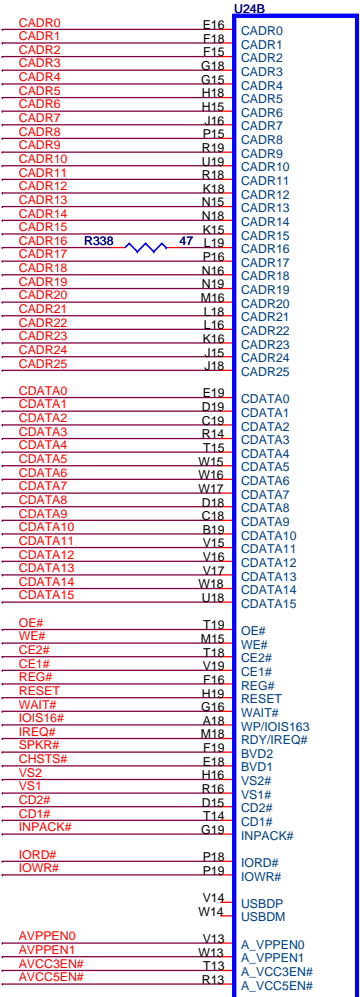
4/17 change to 0805 size low-profile 90ohm

R5C841 pin to pin compatible with R5C843

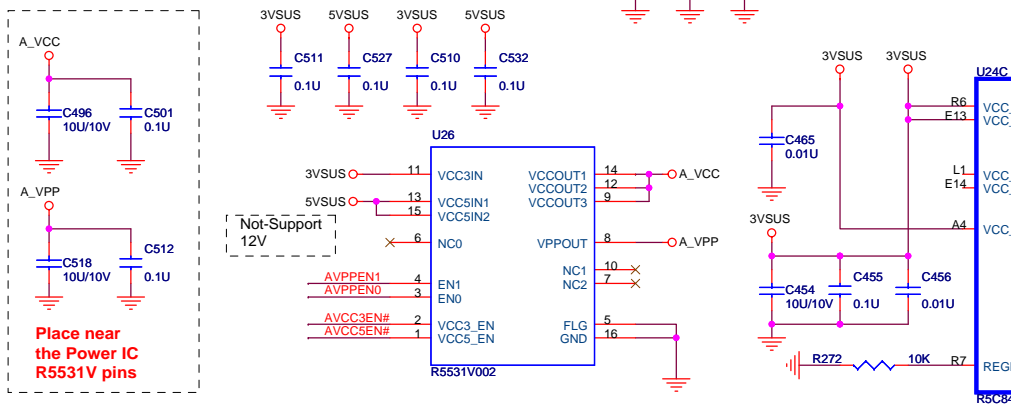
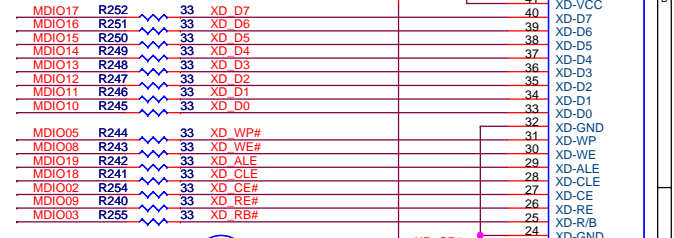
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	R5C843 PCI/1394	D
Date:	Thursday, May 24, 2007	Sheet 20 of 35

PCMCIA Conn.



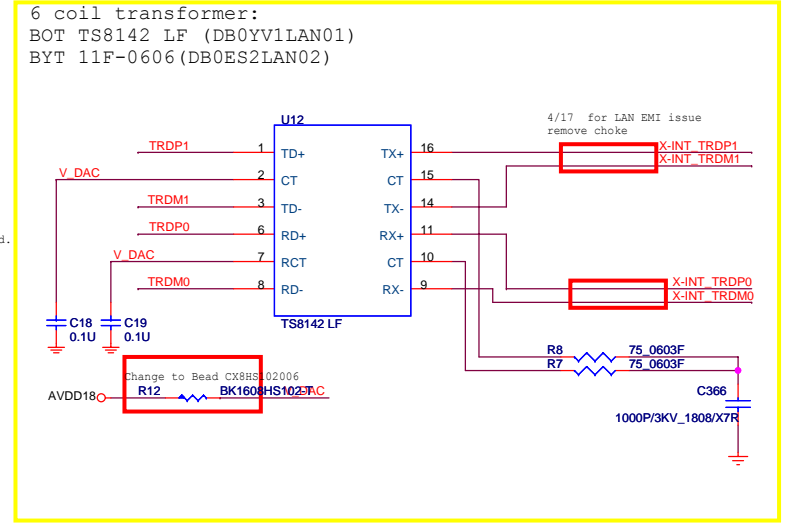
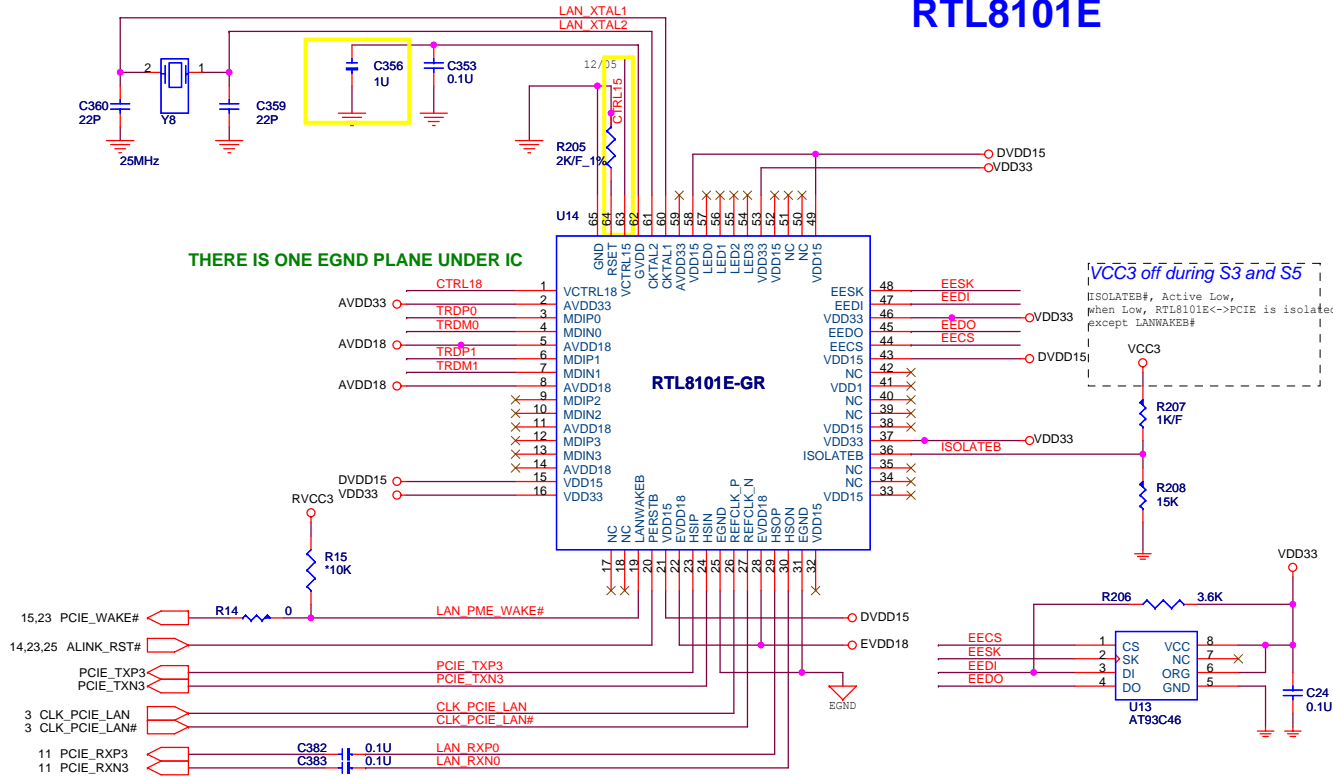
	MDIO00	MDIO01
SD/MMC	L	H
MS	H	L
xD	L	L



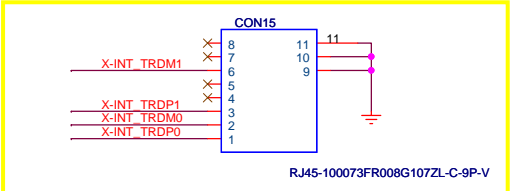
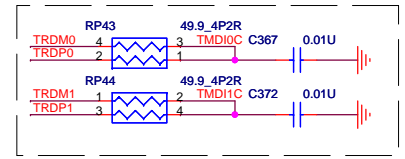
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	R5C843 PCMCIA/4 IN 1	D
Date:	Thursday, May 24, 2007	Sheet 21 of 35

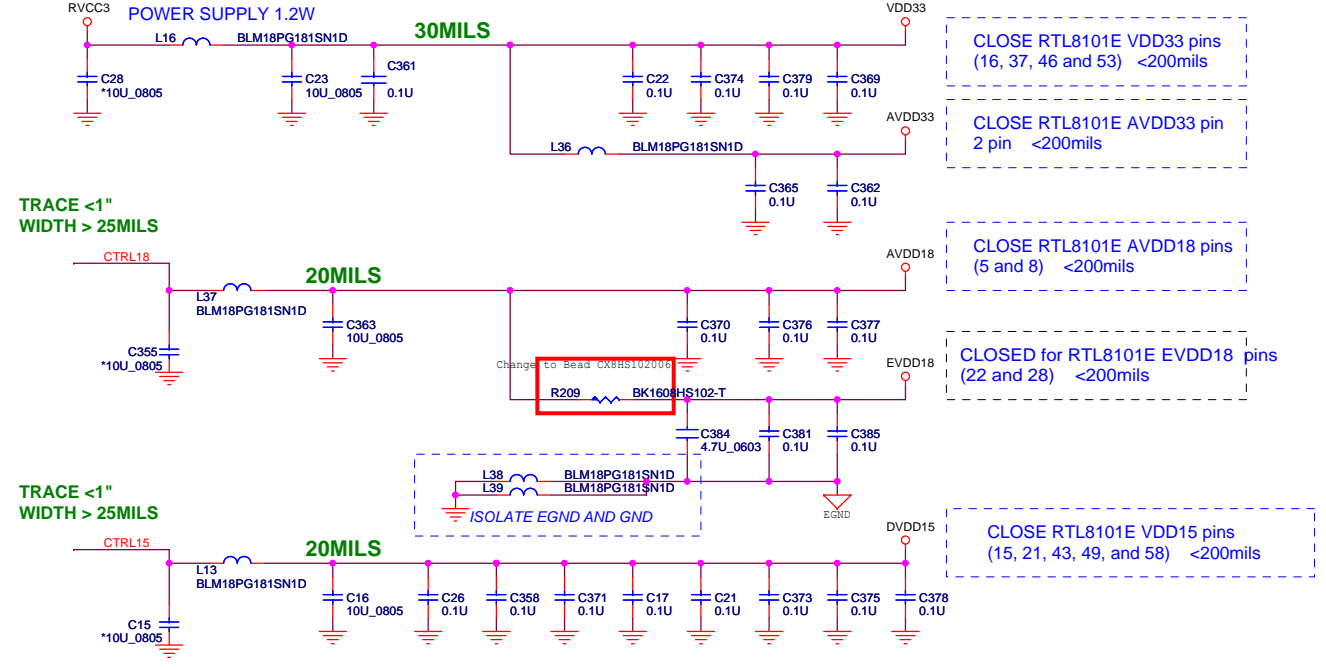
RTL8101E



These parts only for RTL8101E application



POWER SUPPLY



RTL8101E P/N:AL08101E005

RTL8101E is 10/100 Base, RTL8111B is Giga Base
RTL8101E and RTL8111B are pin to pin compatible

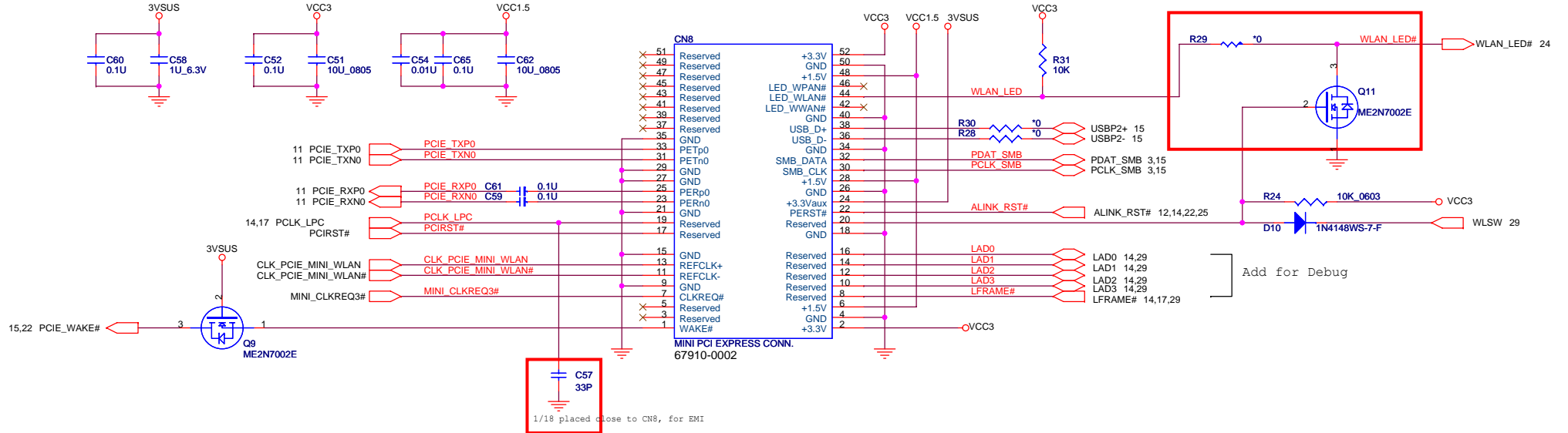
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev D
	LAN RTL8101E	
Date:	Thursday, May 24, 2007	Sheet 22 of 35

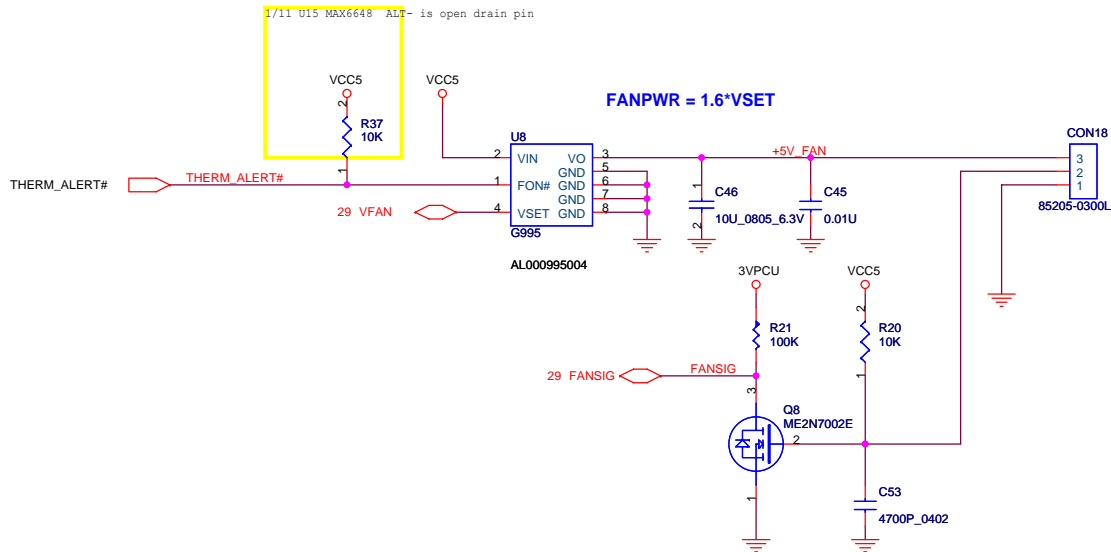
Mini PCI-E Card WLAN

4/17 CN8 change to 10.5mm high for TV function

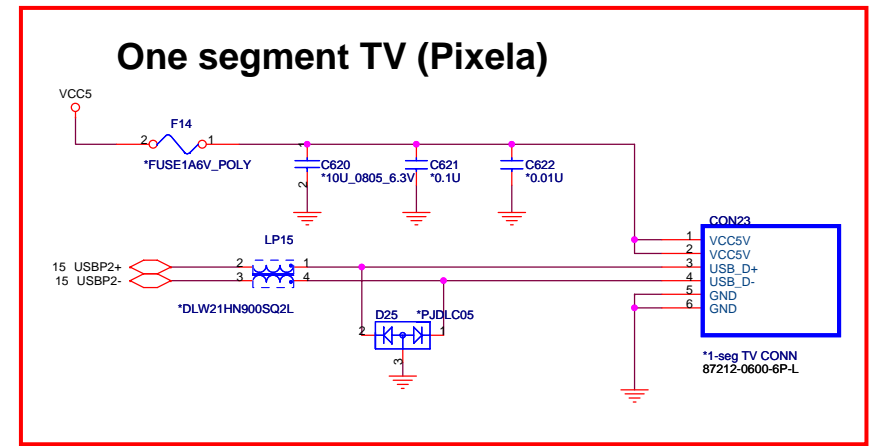
4/4 when working,
LED always ON: R29 nostuff, Q11 stuff
Normal pulse: R29 stuff, Q11 nostuff



FAN CONN

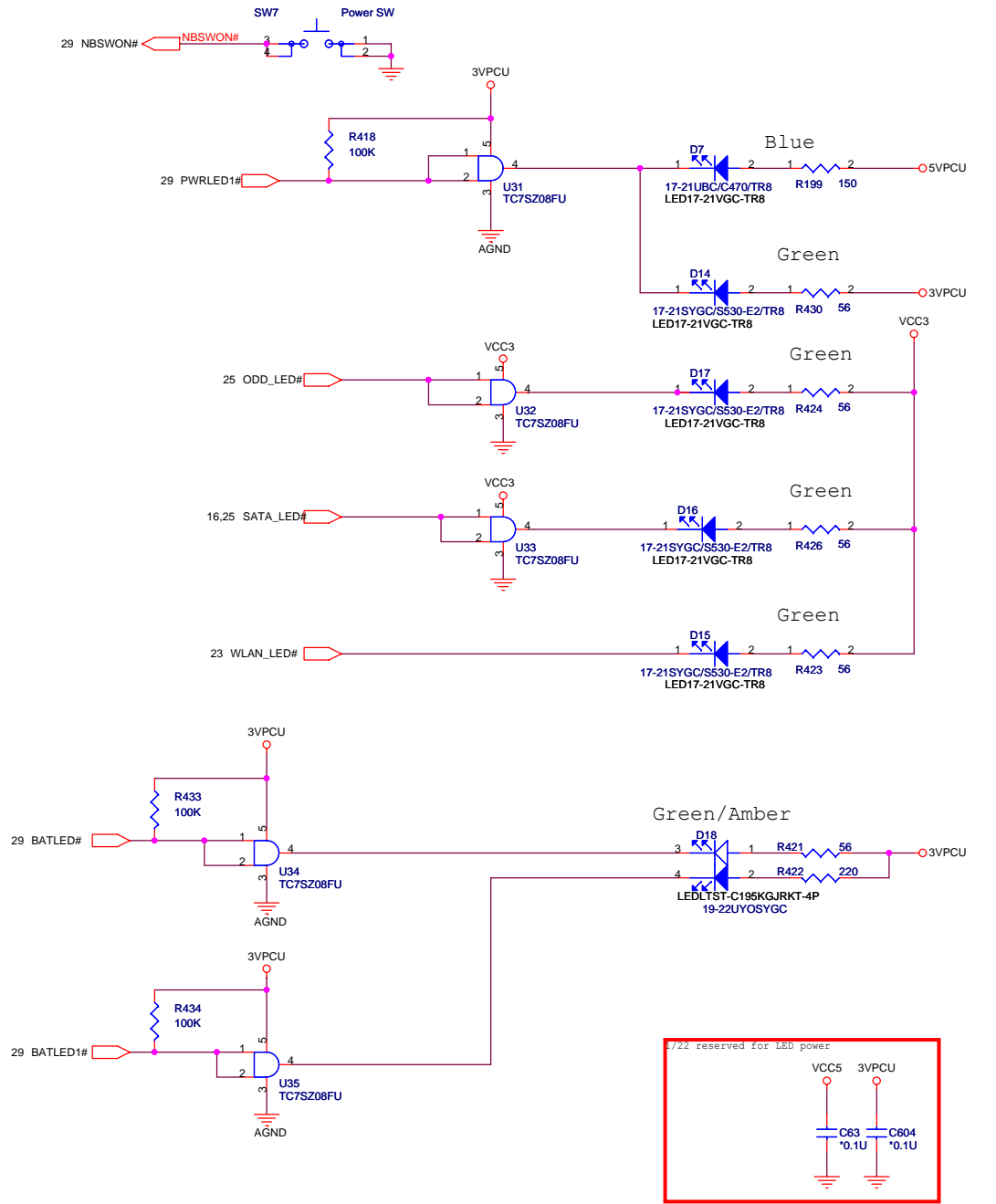
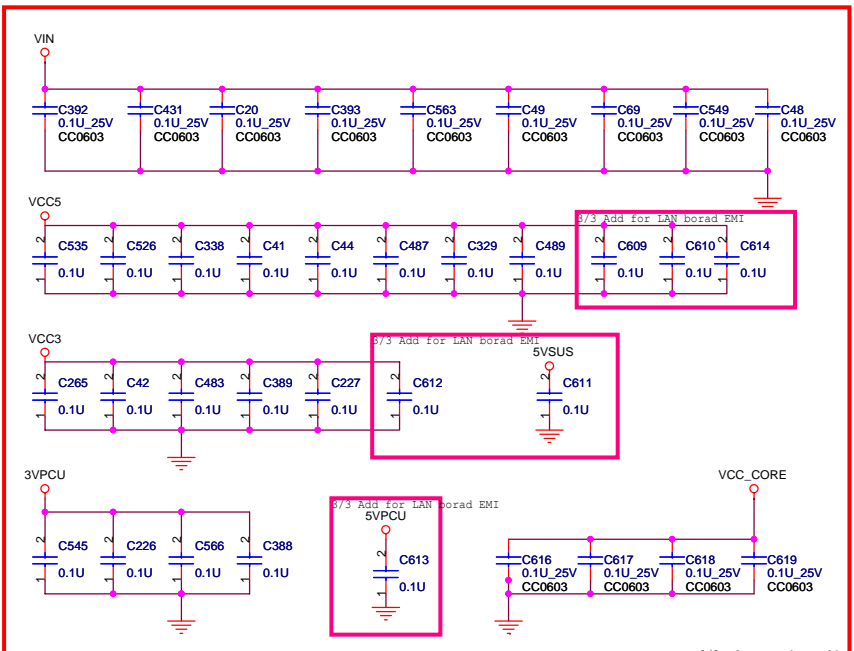
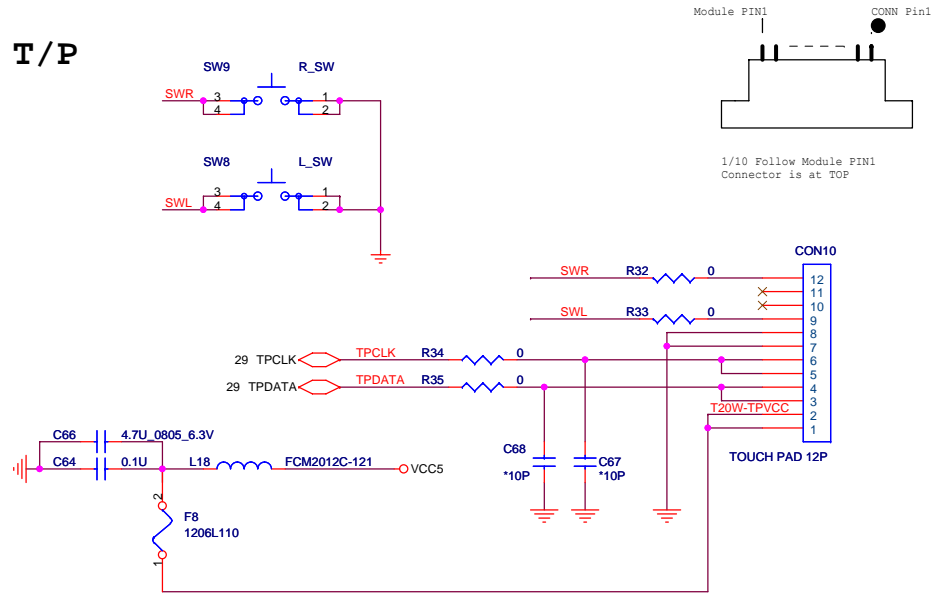


4/12 for IN1- BOT Layer change return path
placed it in the back of LP15 at TOP



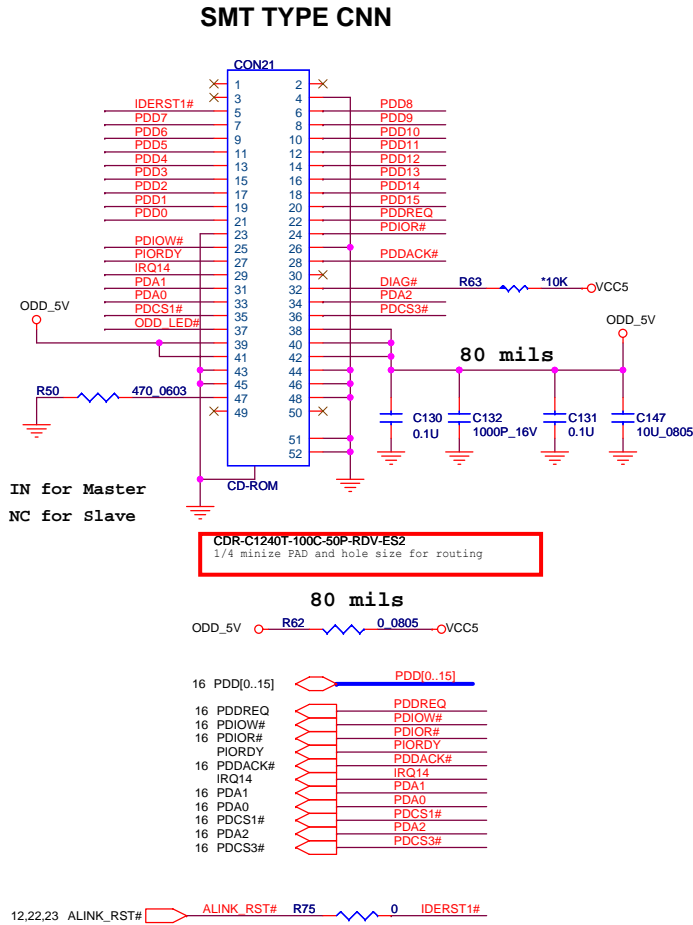
SYSTEM LEDs

T/P

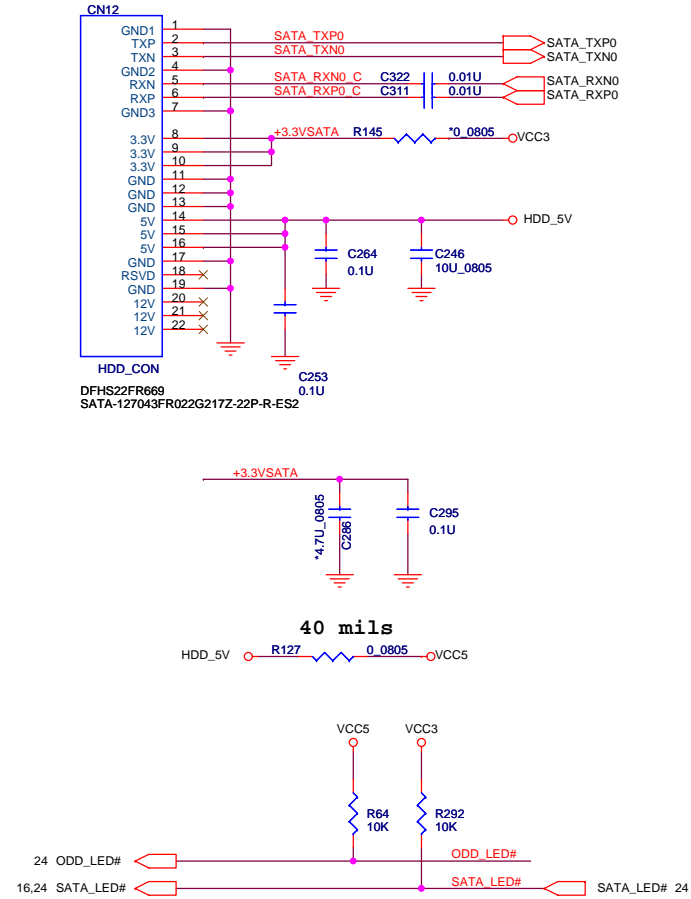


POWER LED	BATT LED	Wireless LED	HDD LED	ODD LED	POWER SWITCH
D14	D18	D15	D16	D17	D7

CD-ROM CONNECTOR

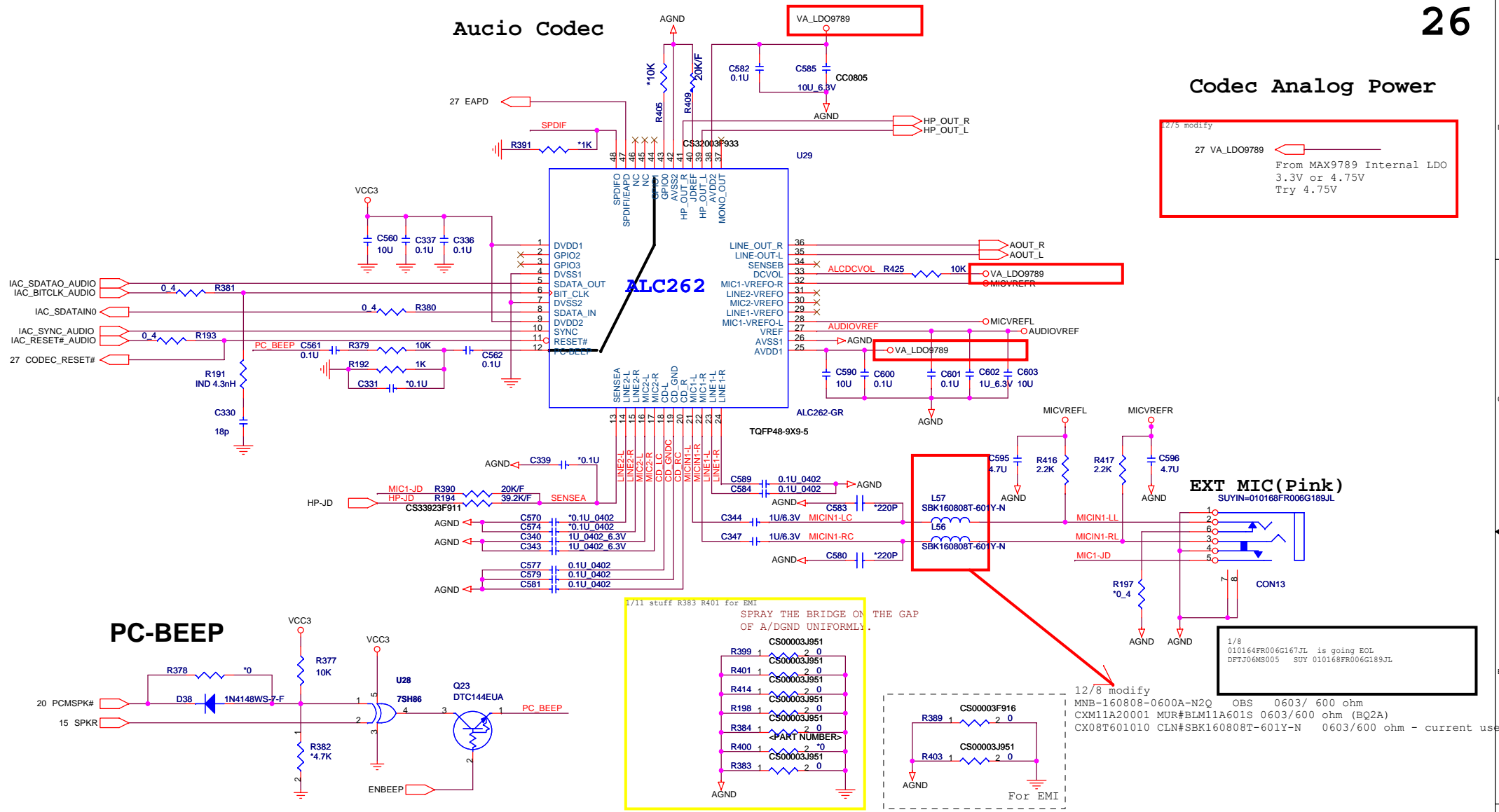


SATA HDD



Aucio Codec

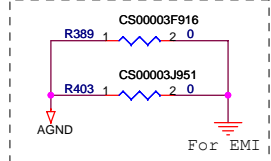
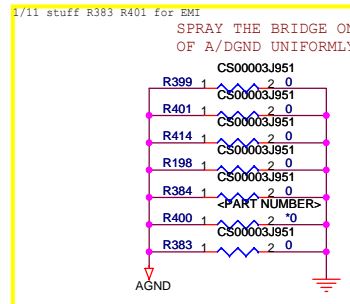
Codec Analog Power



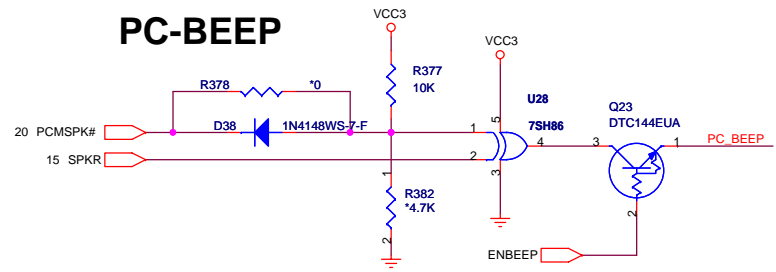
12/5 modify
 27 VA_LDO9789
 From MAX9789 Internal LDO
 3.3V or 4.75V
 Try 4.75V

EXT MIC (Pink)
 SUYIN=010168FR006G189JL

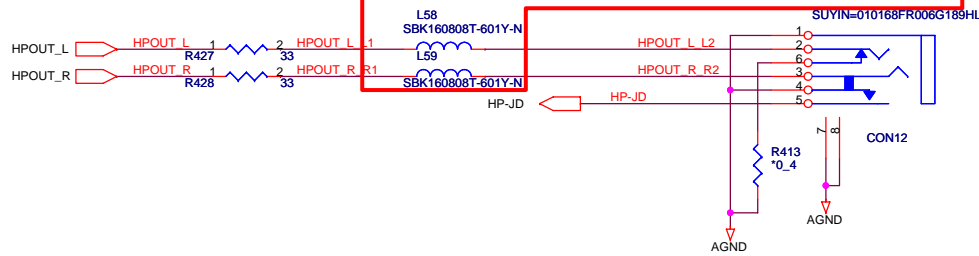
1/8
 010164FR006G167JL is going EOL
 DFTJ06MS005 SUY 010168FR006G189JL



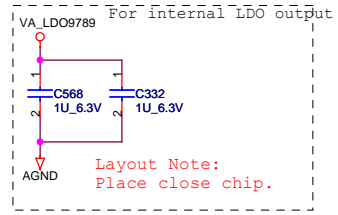
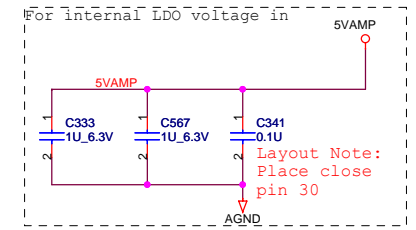
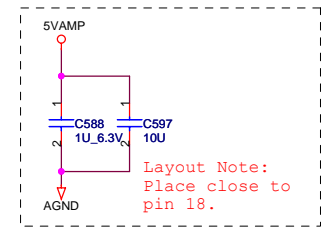
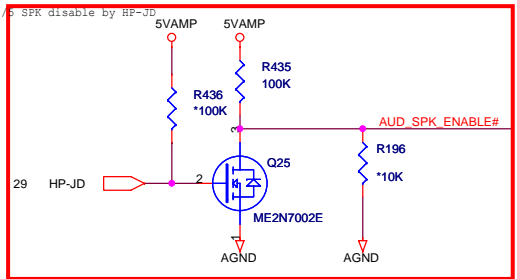
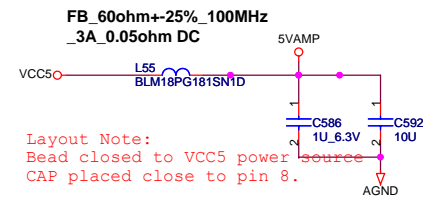
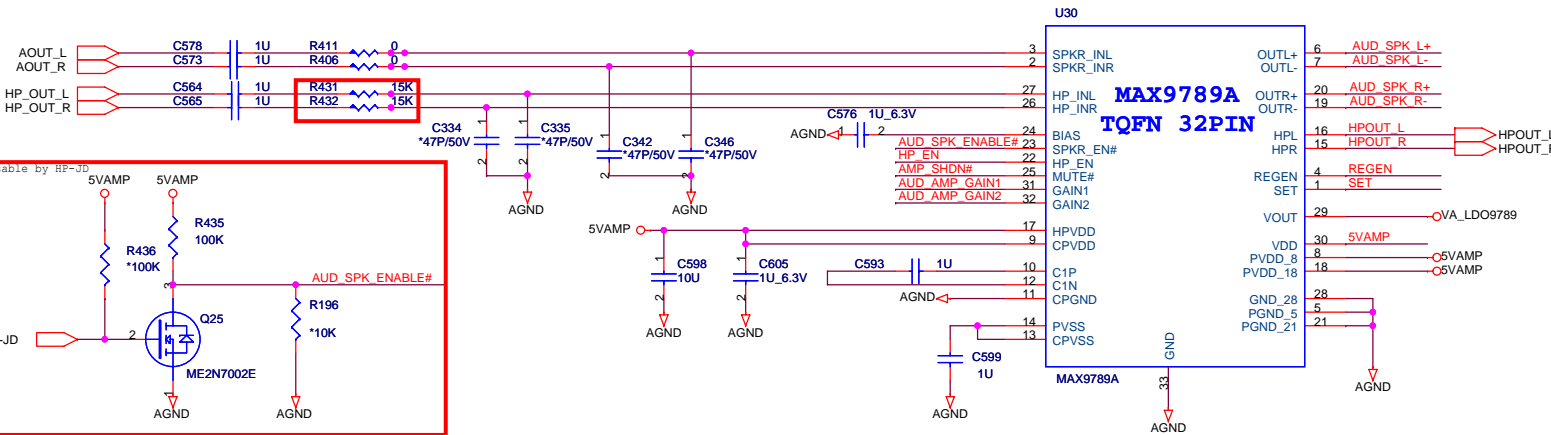
PC-BEEP



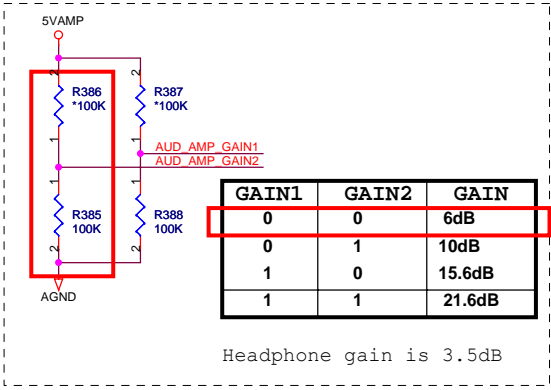
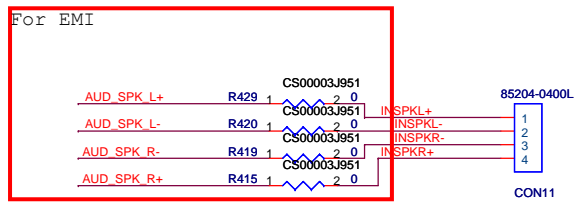
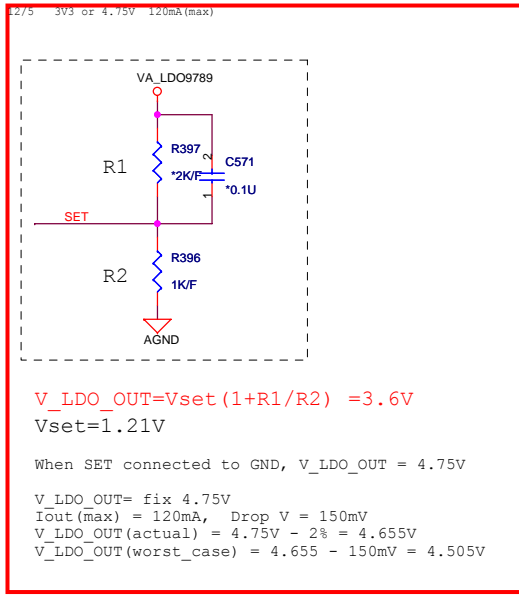
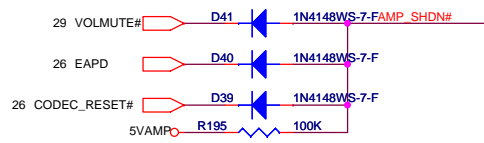
12/8 modify
 MNB-160808-0600A-N2Q OBS 0603/ 600 ohm
 CXM1A20001 MUR#BLM1A601S 0603/600 ohm (BQ2A)
 CX08T601010 CLN#SBK160808T-601Y-N 0603/600 ohm - current use



1/8
 010164FR006G167HL is going EOL
 DFTJ06MS004 SUY 010168FR006G189HL

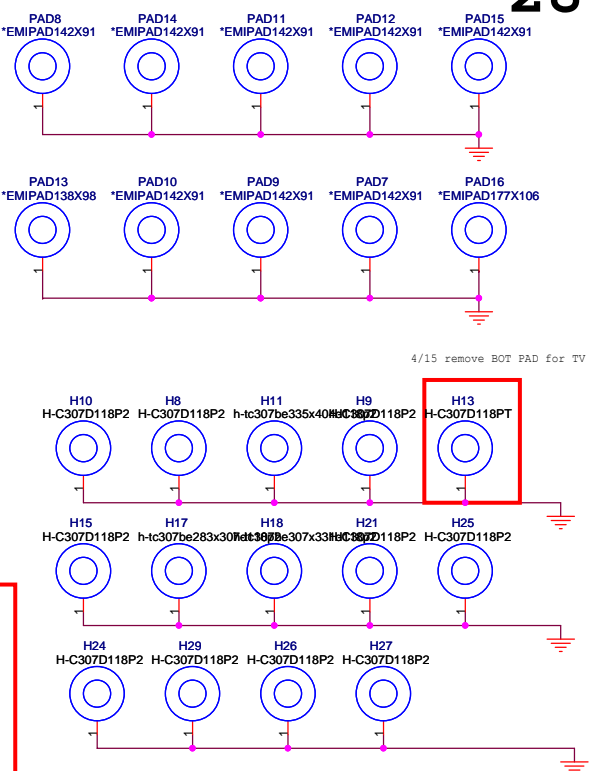
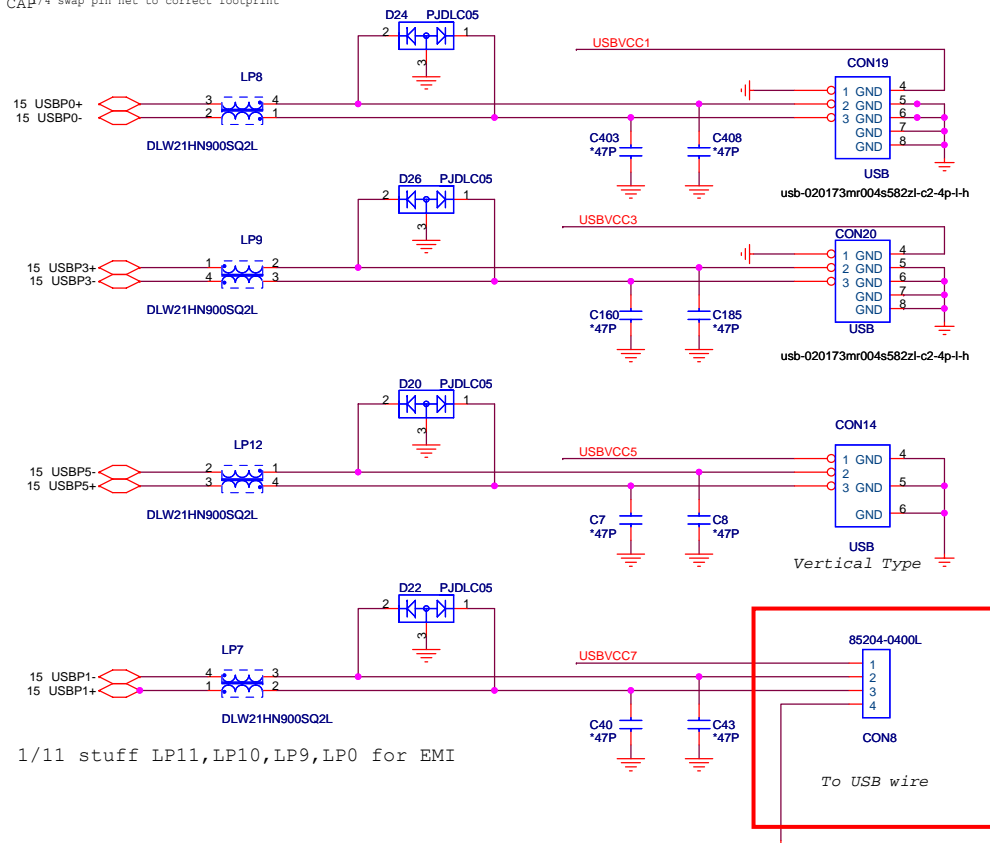
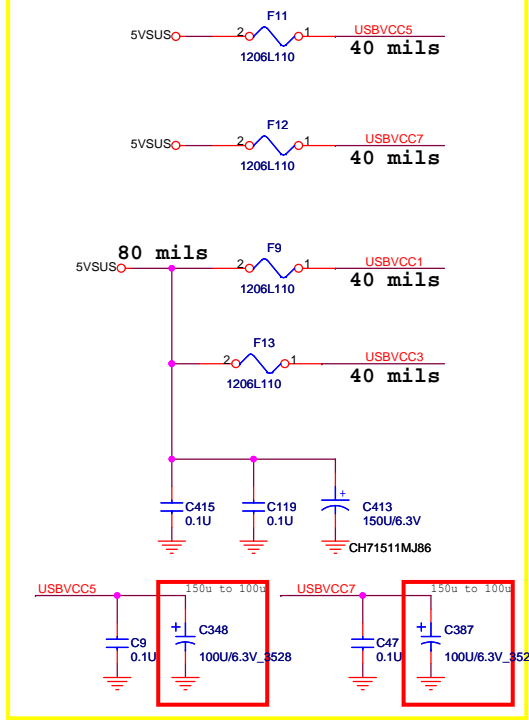


Head phone AMP always ON



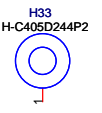
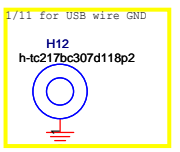
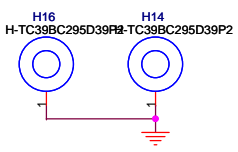
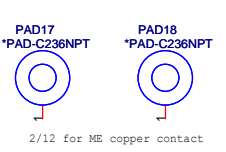
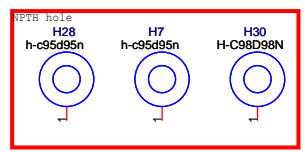
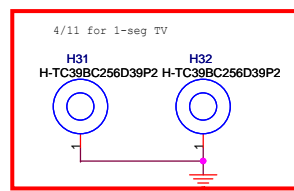
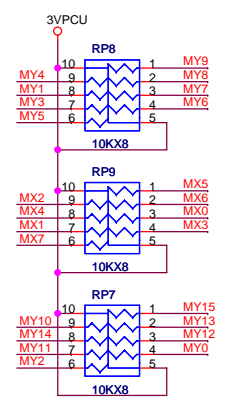
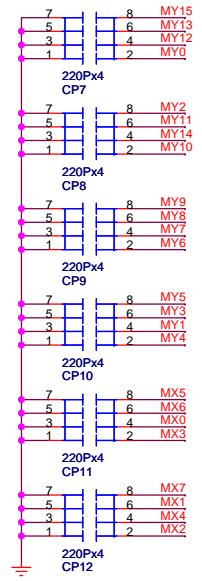
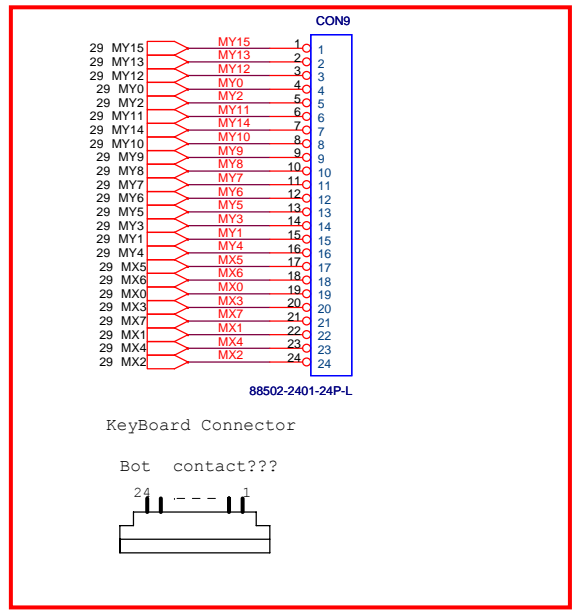
Enable Internal LDO

12/27 USBVCC3,5 and USBVCC5,7 swapped to use different CAP/4 swap pin net to correct footprint



1/11 stuff LP11,LP10,LP9,LP0 for EMI

Check Pin Define



Quanta Computer Inc.
PROJECT : ES2

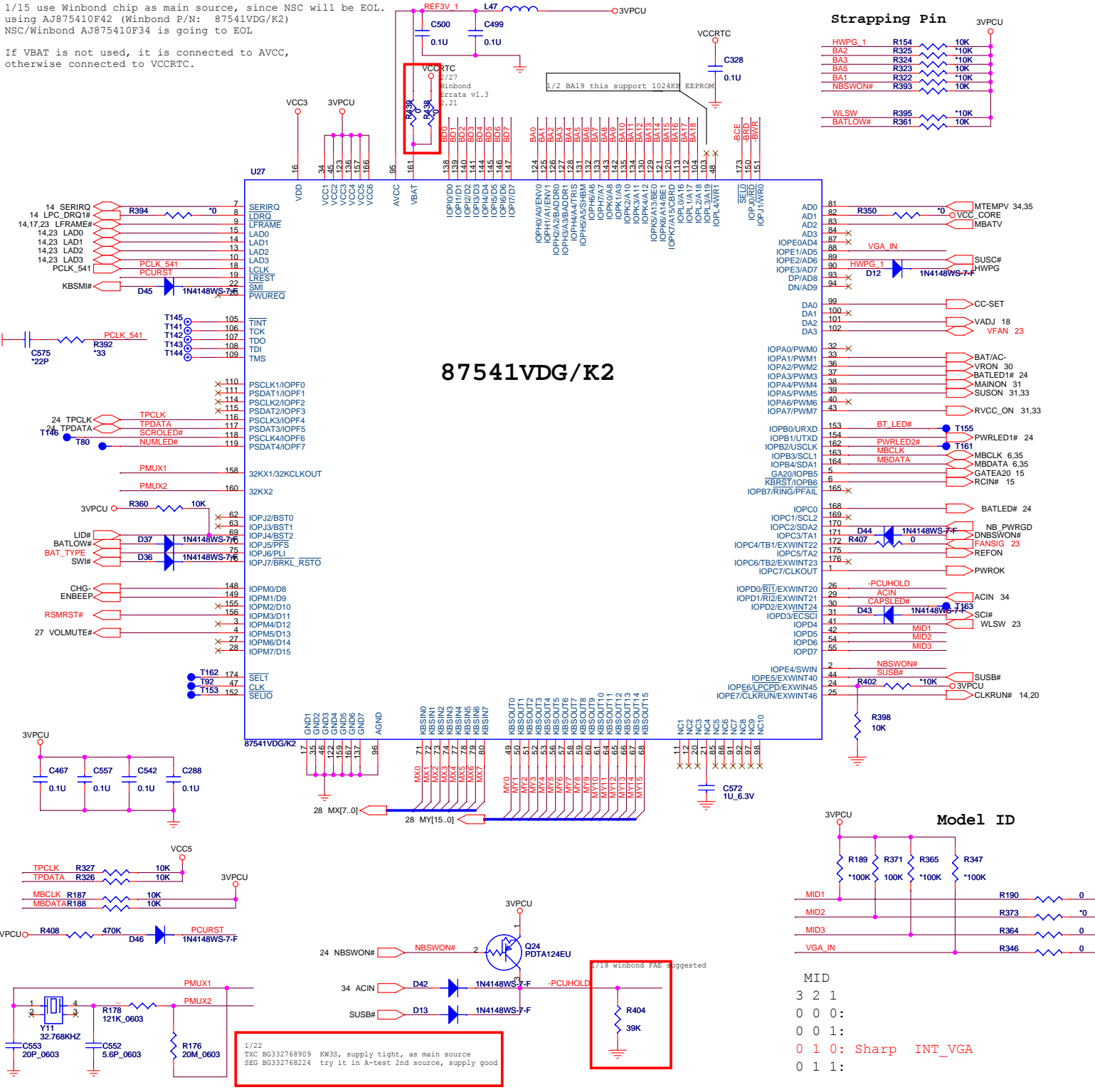
Size	Document Number	Rev
Date:	Thursday, May 24, 2007	A
KEYBOARD/USB/SCREW		Sheet 28 of 35

1/15 use Winbond chip as main source, since NSC will be EOL.
 using AJ875410F42 (Winbond P/N: 87541VDG/K2)
 NSC/Winbond AJ875410F34 is going to EOL

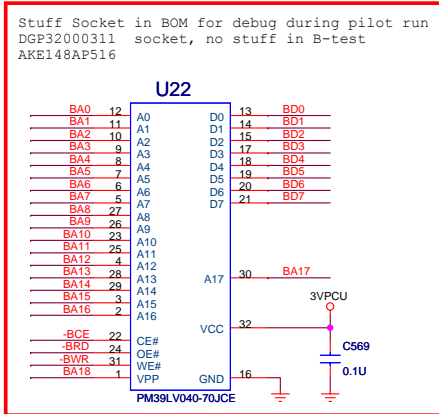
If VBAT is not used, it is connected to AVCC,
 otherwise connected to VCCRTC.

12/18 remove 1024K EEPROM
 to save space

1/18 winbond FAB suggested
 placed close to 87541 (



87541VDG/K2



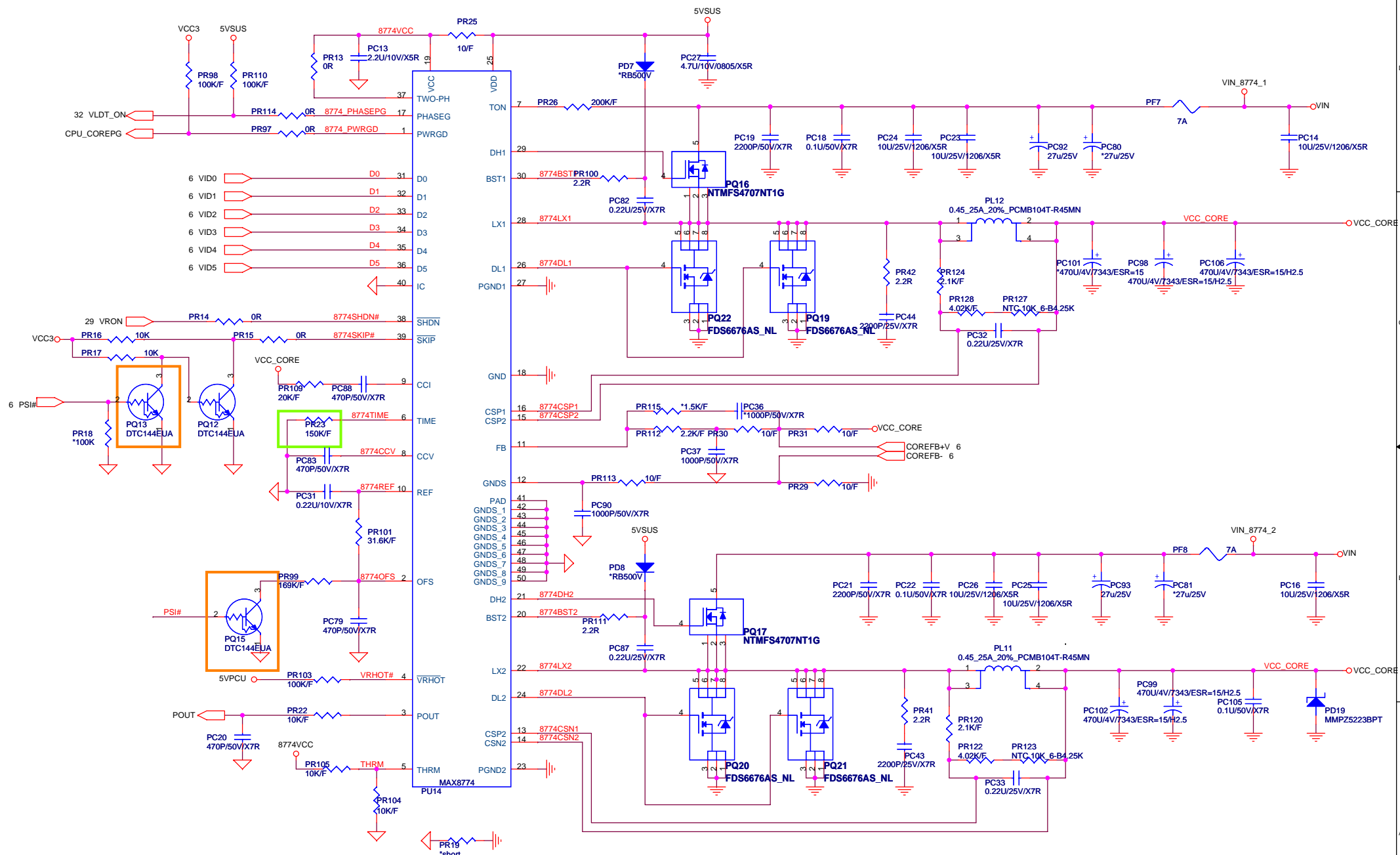
BADDR1=0	Index	I/O Address	Data
0 0	2E	2F	
0 1	4E	4F	
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)	=1
1 1		Reserved	

Environment	ENV0 (BA0)	ENV1 (BA1)	TRIS (BA4)
IRE	0	0	0
QBD	0	1	0
DEV	1	0	0
PROG	1	1	0

BA0 : ENV0
 BA1 : ENV1
 BA4 : TRIS (If =1 will tristate all I/O pins)
 BA5 : SHBM (If =1 Enable share host BIOS memory)

Quanta Computer Inc.
PROJECT : ES2

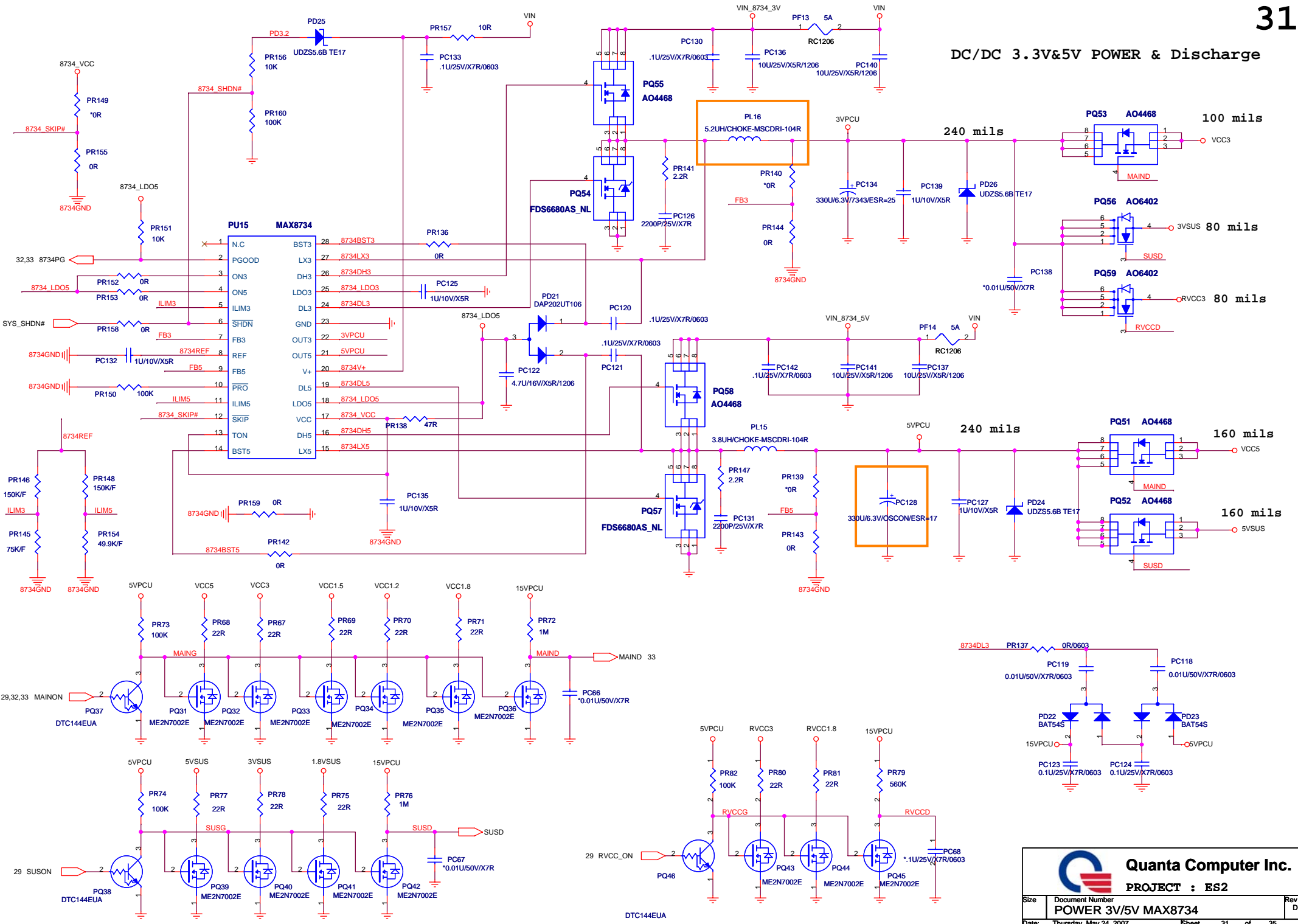
Size	Document Number	Rev
	EC PCU87541/FLASH ROM	D
Date:	Thursday, May 24, 2007	Sheet 29 of 35



Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev	D
	POWER CPU CORE MAX8774		
Date:	Thursday, May 24, 2007	Sheet	30 of 35

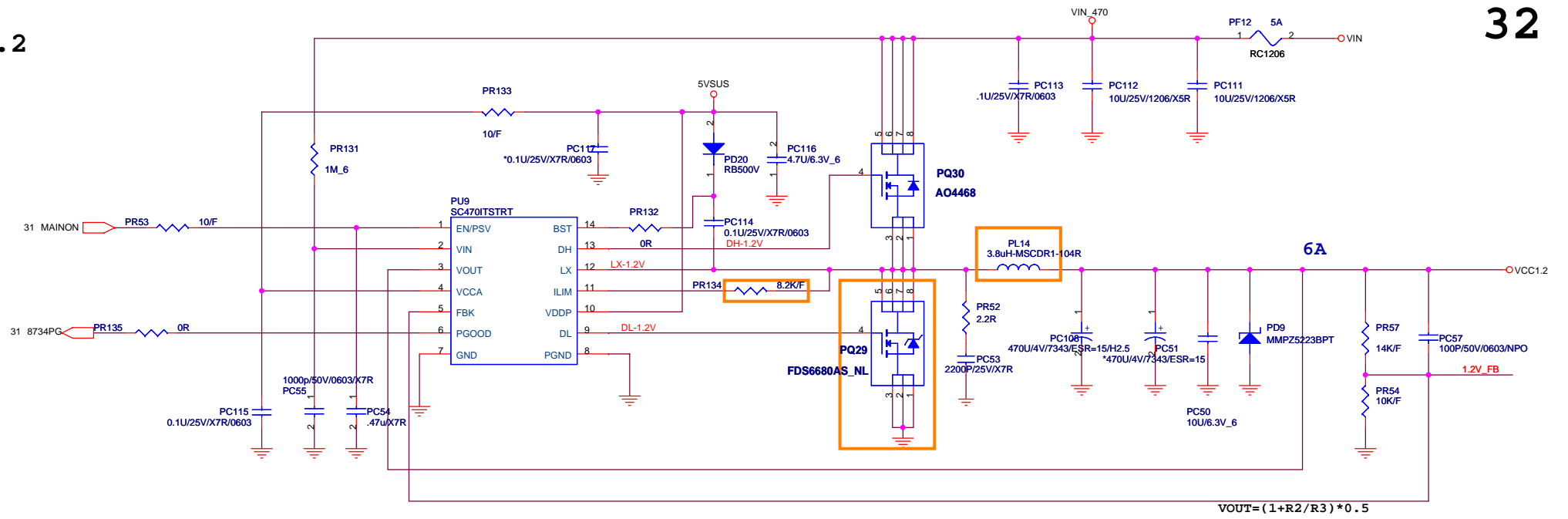
DC/DC 3.3V&5V POWER & Discharge



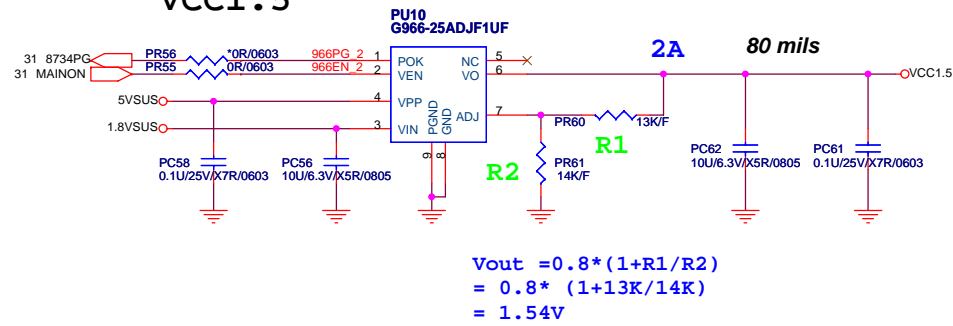
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	POWER 3V/5V MAX8734	D
Date:	Thursday, May 24, 2007	Sheet 31 of 35

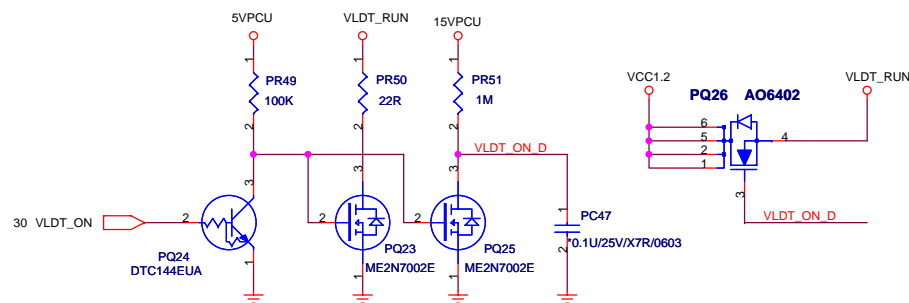
VCC1.2



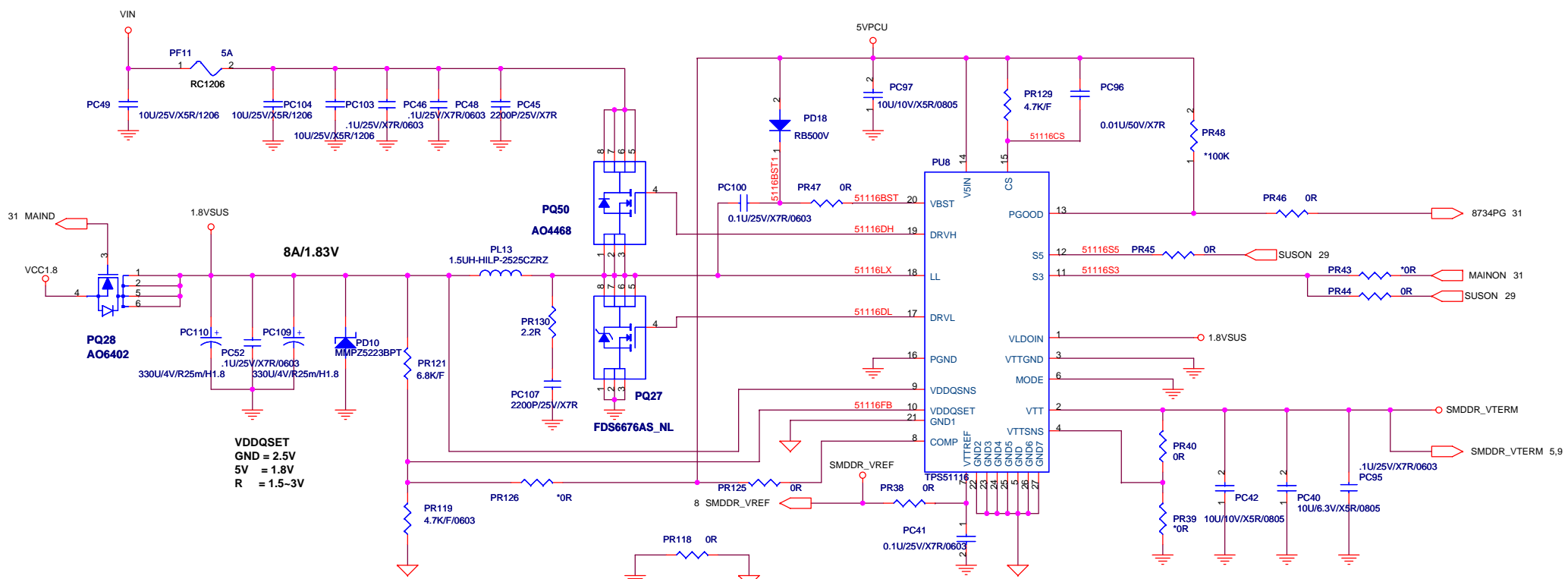
VCC1.5



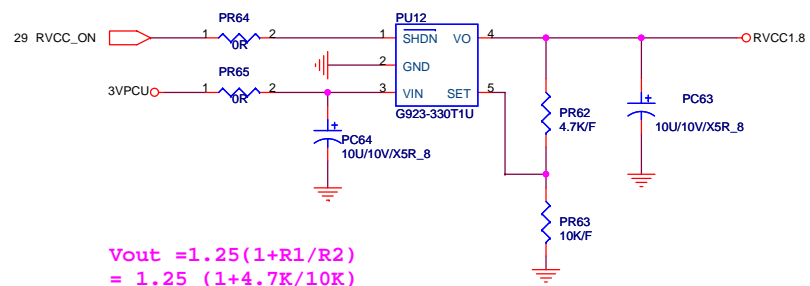
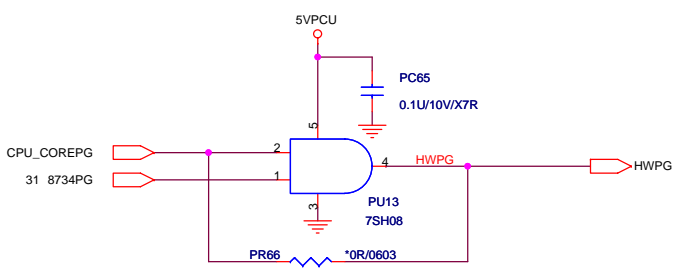
VLDT_RUN



1.8VSUS & VTERM(DDR2) & VCC1.8

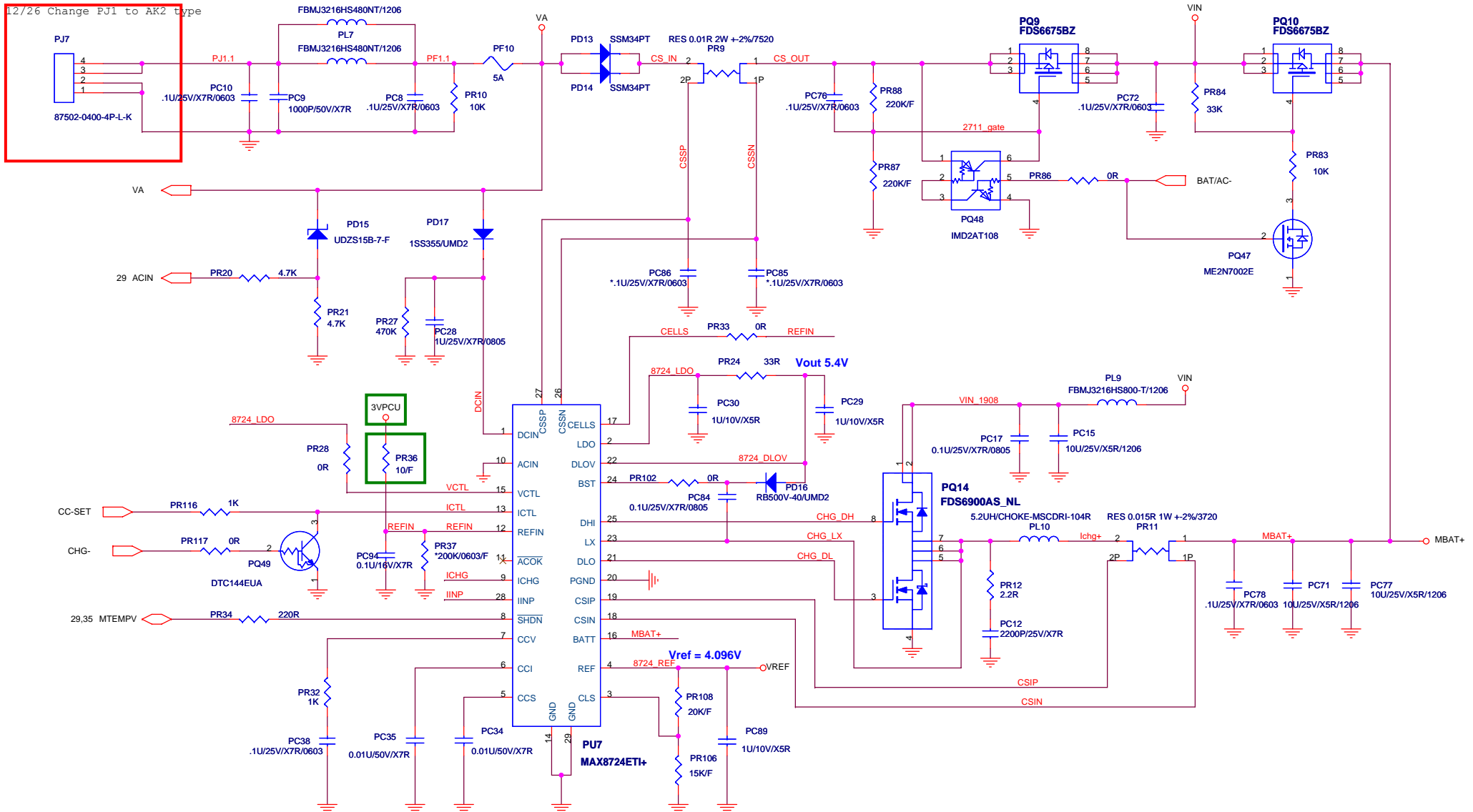


RVCC1.8



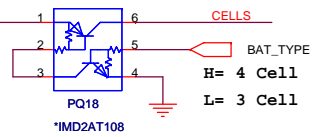
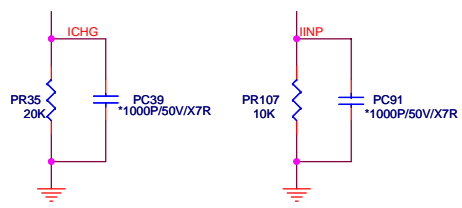
$$\begin{aligned}
 V_{out} &= 1.25(1+R1/R2) \\
 &= 1.25(1+4.7K/10K) \\
 &= 1.83V
 \end{aligned}$$


Battery Charger



$ILIM = [15 / (15 + 20)] * 75mV / 10mR = 3.21A. (65W)$

BATT-TYPE	
High	Low
Li-ion 4S2P	Li-ion 3S2P
Li-ion 4S1P	
Ni-MH 8S1P	

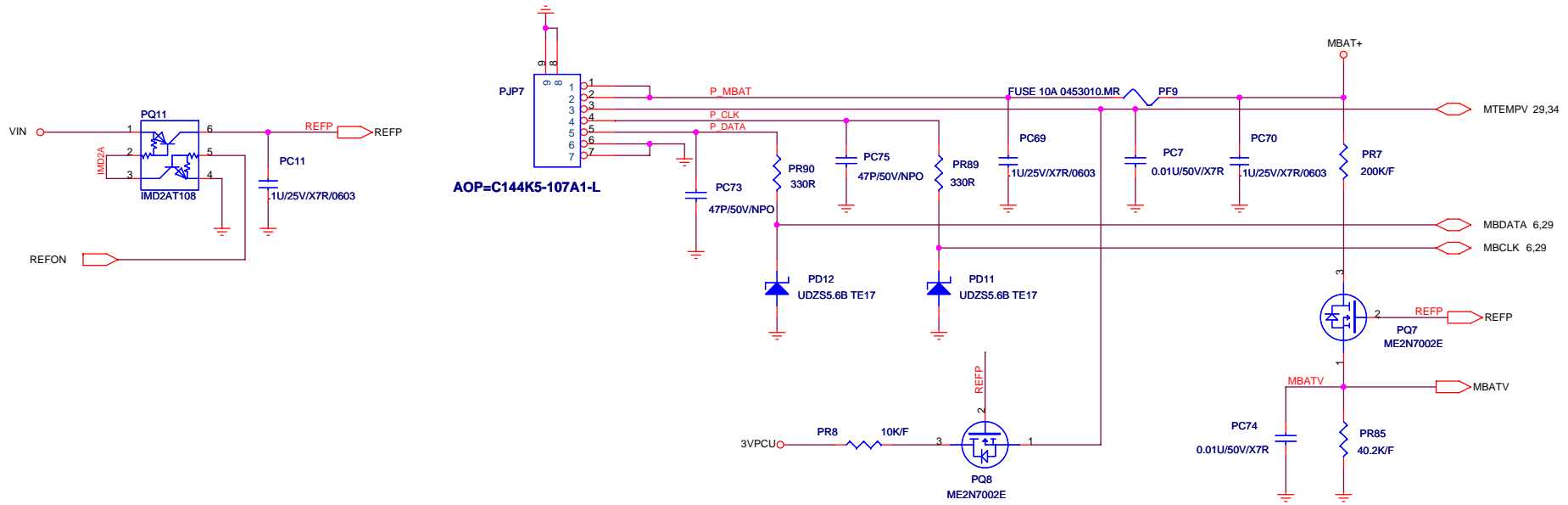




Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	BATTERY CHARGER MAX8724	D
Date:	Thursday, May 24, 2007	Sheet 34 of 35

Battery Connector



MTEMPV voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :

$$16.8V * 40.2 / (200 + 40.2) = 2.812V$$

$$12.0V * 40.2 / (200 + 40.2) = 2.008V$$

$$8.0V * 40.2 / (200 + 40.2) = 1.34V$$